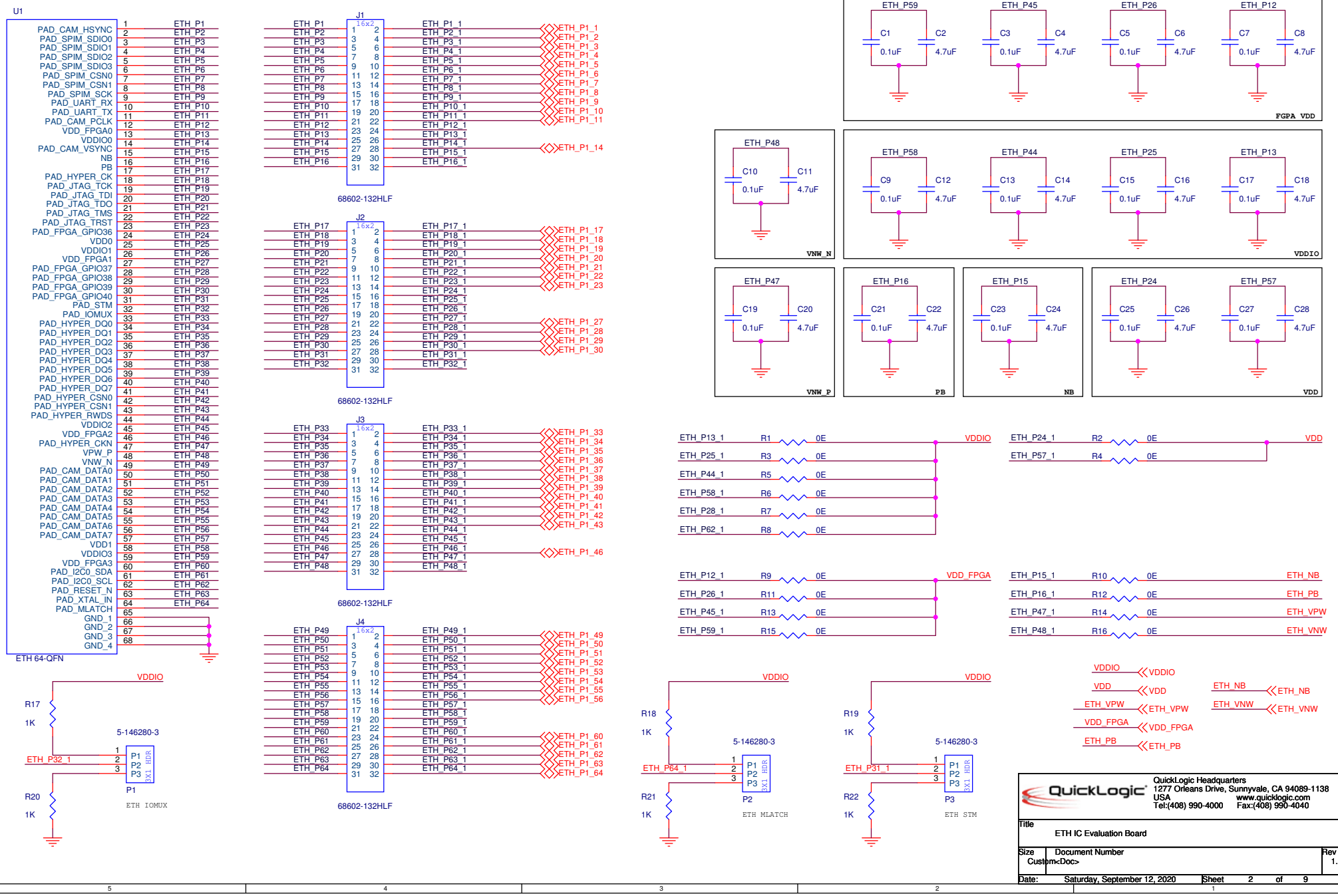
ETH IC Evaluation Board (Salinas)

Rev 1.1

QuickLogic Headquarters
1277 Orleans Drive, Sunnyvale, CA 94089-1138
USA www.quicklogic.com
Tel:(408) 990-4000 Fax:(408) 990-4040

Title: ETH IC Evaluation Board		
Size: B	Document Number: <Doc>	Rev: 1.1
Date: Saturday, September 12, 2020	Sheet 1 of 9	


U1
PAD_CAM_HSYNC
PAD_SPIM_SDIO0
PAD_SPIM_SDIO1
PAD_SPIM_SDIO2
PAD_SPIM_SDIO3
PAD_SPIM_CSN0
PAD_SPIM_CSN1
PAD_SPIM_SCK
PAD_UART_RX
PAD_UART_TX
PAD_CAM_PCLK
VDD_FPGA0
VDDIO0
PAD_CAM_VSYNC
NB
PB
PAD_HYPER_CK
PAD_JTAG_TCK
PAD_JTAG_TDI
PAD_JTAG_TDO
PAD_JTAG_TMS
PAD_JTAG_TRST
PAD_FPGA_GPIO36
VDD0
VDDIO1
VDD_FPGA1
PAD_FPGA_GPIO37
PAD_FPGA_GPIO38
PAD_FPGA_GPIO39
PAD_FPGA_GPIO40
PAD_STM
PAD_IOMUX
PAD_HYPER_DQ0
PAD_HYPER_DQ1
PAD_HYPER_DQ2
PAD_HYPER_DQ3
PAD_HYPER_DQ4
PAD_HYPER_DQ5
PAD_HYPER_DQ6
PAD_HYPER_DQ7
PAD_HYPER_CSN0
PAD_HYPER_CSN1
PAD_HYPER_RWDS
VDDIO2
VDD_FPGA2
PAD_HYPER_CKN
VPW_P
VNW_N
PAD_CAM_DATA0
PAD_CAM_DATA1
PAD_CAM_DATA2
PAD_CAM_DATA3
PAD_CAM_DATA4
PAD_CAM_DATA5
PAD_CAM_DATA6
PAD_CAM_DATA7
VDD1
VDDIO3
VDD_FPGA3
PAD_I2C0_SDA
PAD_I2C0_SCL
PAD_RESET_N
PAD_XTAL_IN
PAD_MLATCH
GND_1
GND_2
GND_3
GND_4
ETH 64-QFN
J1
J2
J3
J4
68602-132HLF
R17
1K
R20
1K
ETH_P32_1
5-146280-3
P1
ETH IOMUX
R18
R21
ETH_P64_1
P2
ETH MLATCH
R19
R22
ETH_P31_1
P3
ETH STM
VDDIO
C1
C2
C3
C4
C5
C6
C7
C8
0.1uF
4.7uF
FGPA VDD
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
VDDIO
VNW_N
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
VNW_P
PB
NB
VDD
R1
R2
R3
R4
R5
R6
R7
R8
0E
R9
R10
R11
R12
R13
R14
R15
R16
VDD_FPGA
ETH_NB
ETH_PB
ETH_VPW
ETH_VNW
QuickLogic
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USA
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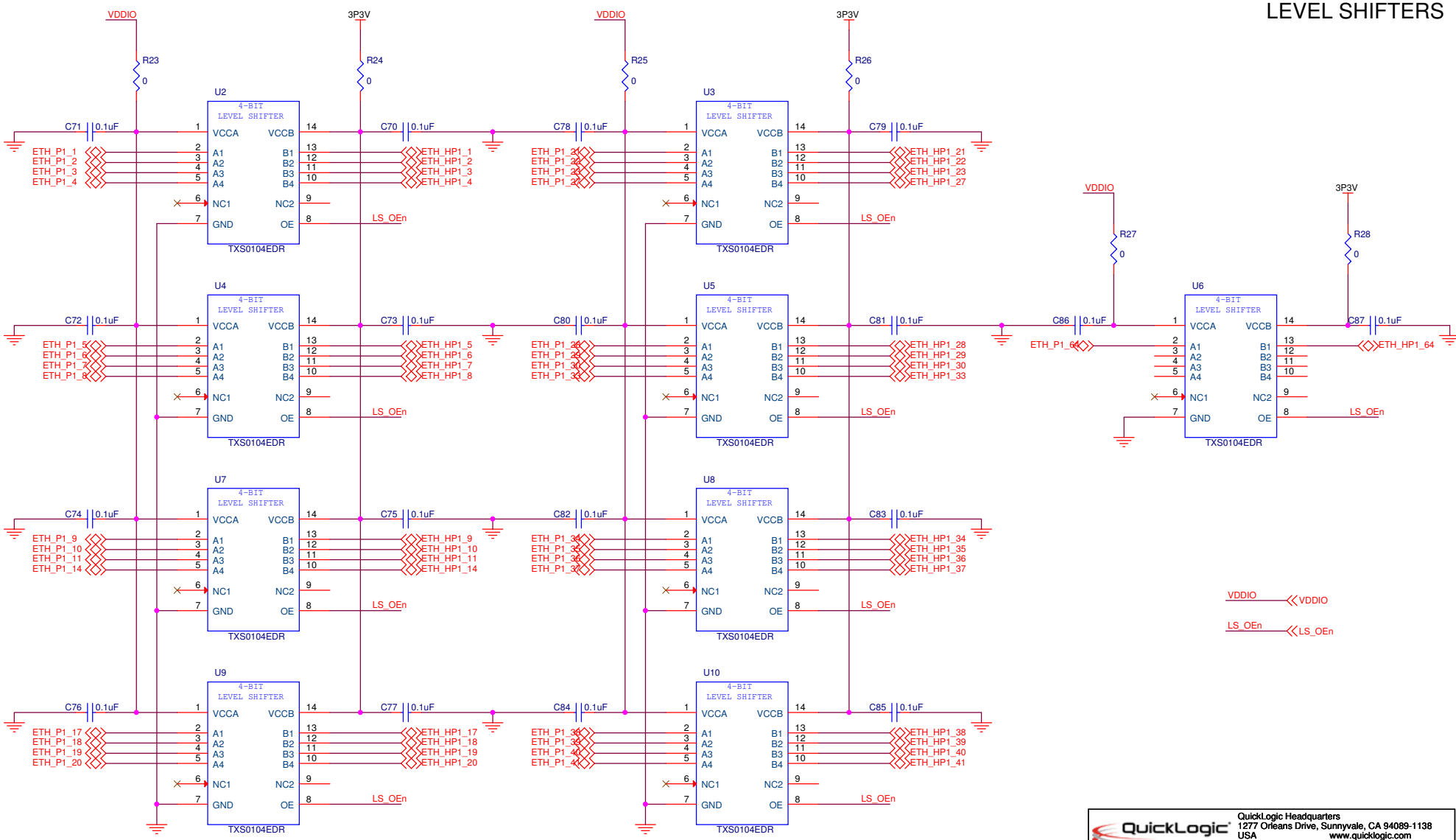
Title
ETH IC Evaluation Board
Size
Custom<Doc>
Document Number
Rev
1.1
Date:
Saturday, September 12, 2020
Sheet
2
of
9

LEVEL SHIFTERS



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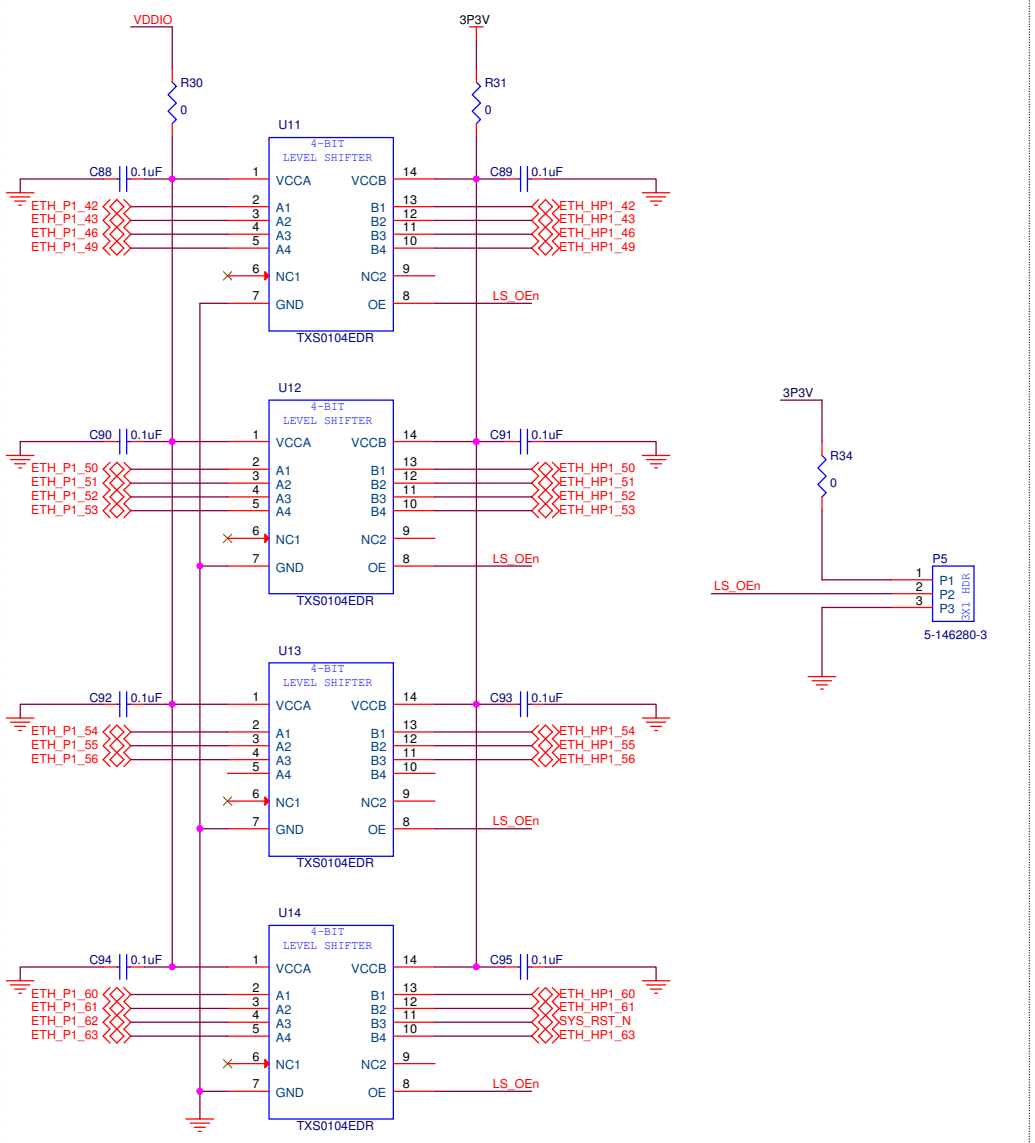
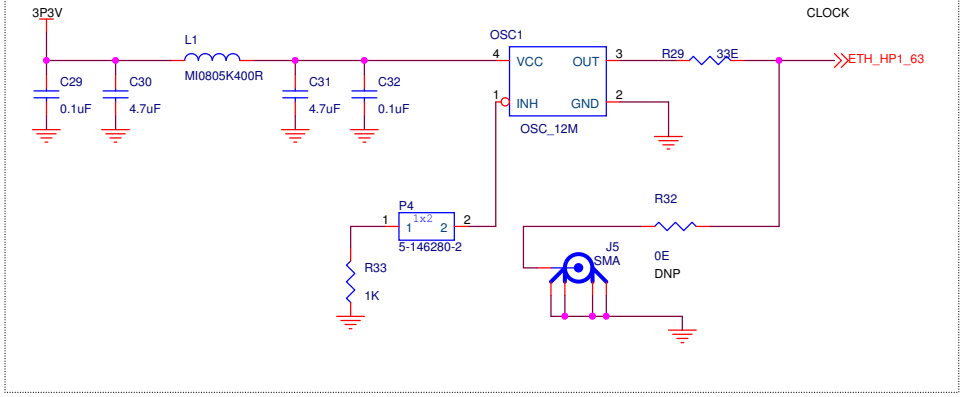
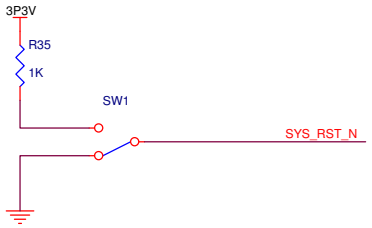
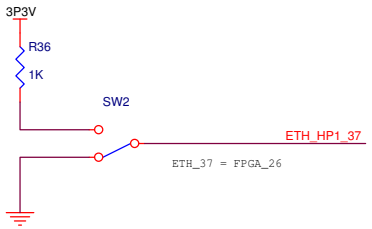
Date: Saturday, September 12, 2020	Sheet 3 of 9	

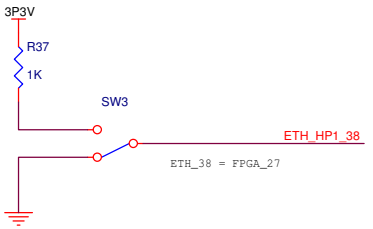


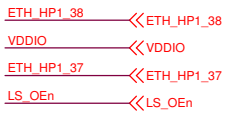
LEVEL SHIFTERS











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Title		
ETH Evaluation Board		
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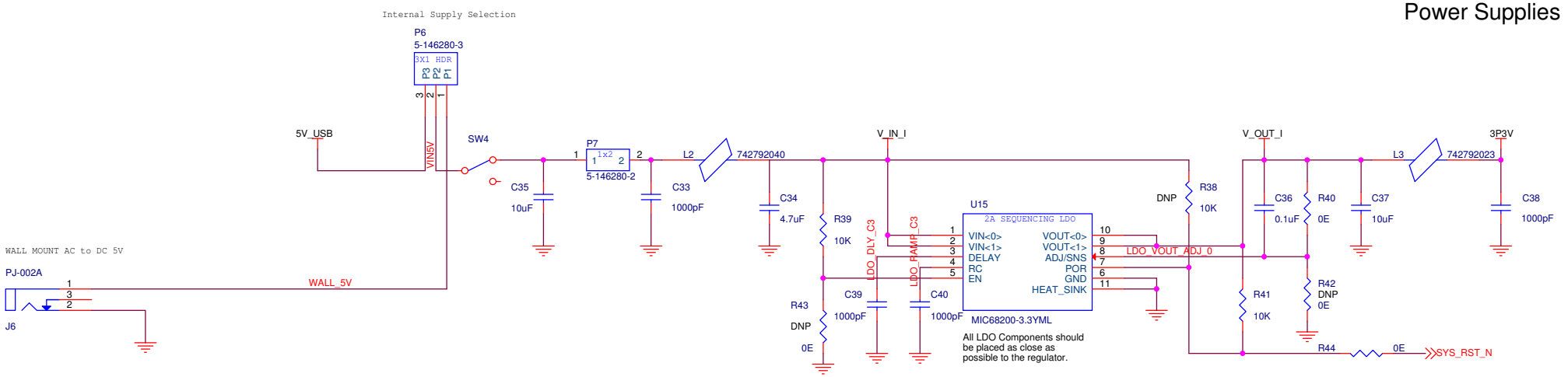
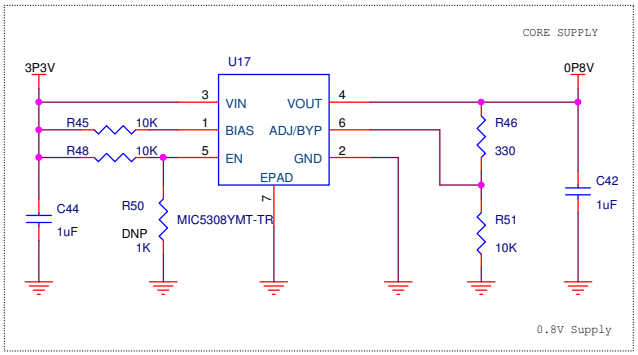
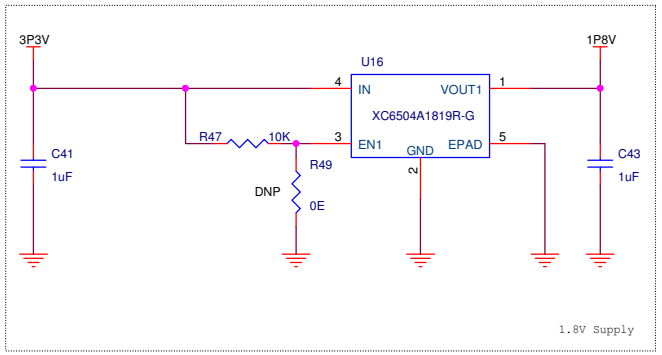
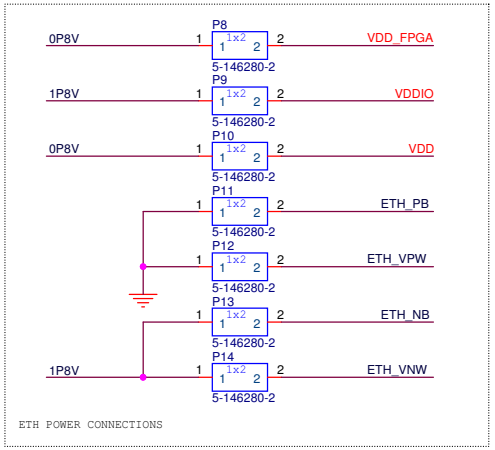
Power Supplies









VDDIO <<VDDIO
VDD <<VDD
ETH_PB <<ETH_PB
VDD_FPGA <<VDD_FPGA
ETH_NB <<ETH_NB

ETH_VPW <<ETH_VPW
ETH_VNW <<ETH_VNW
1P8V <<1P8V

QuickLogic	QuickLogic Headquarters 1277 Orleans Drive, Sunnyvale, CA 94089-1138 USA www.quicklogic.com Tel:(408) 990-4000 Fax:(408) 990-4040
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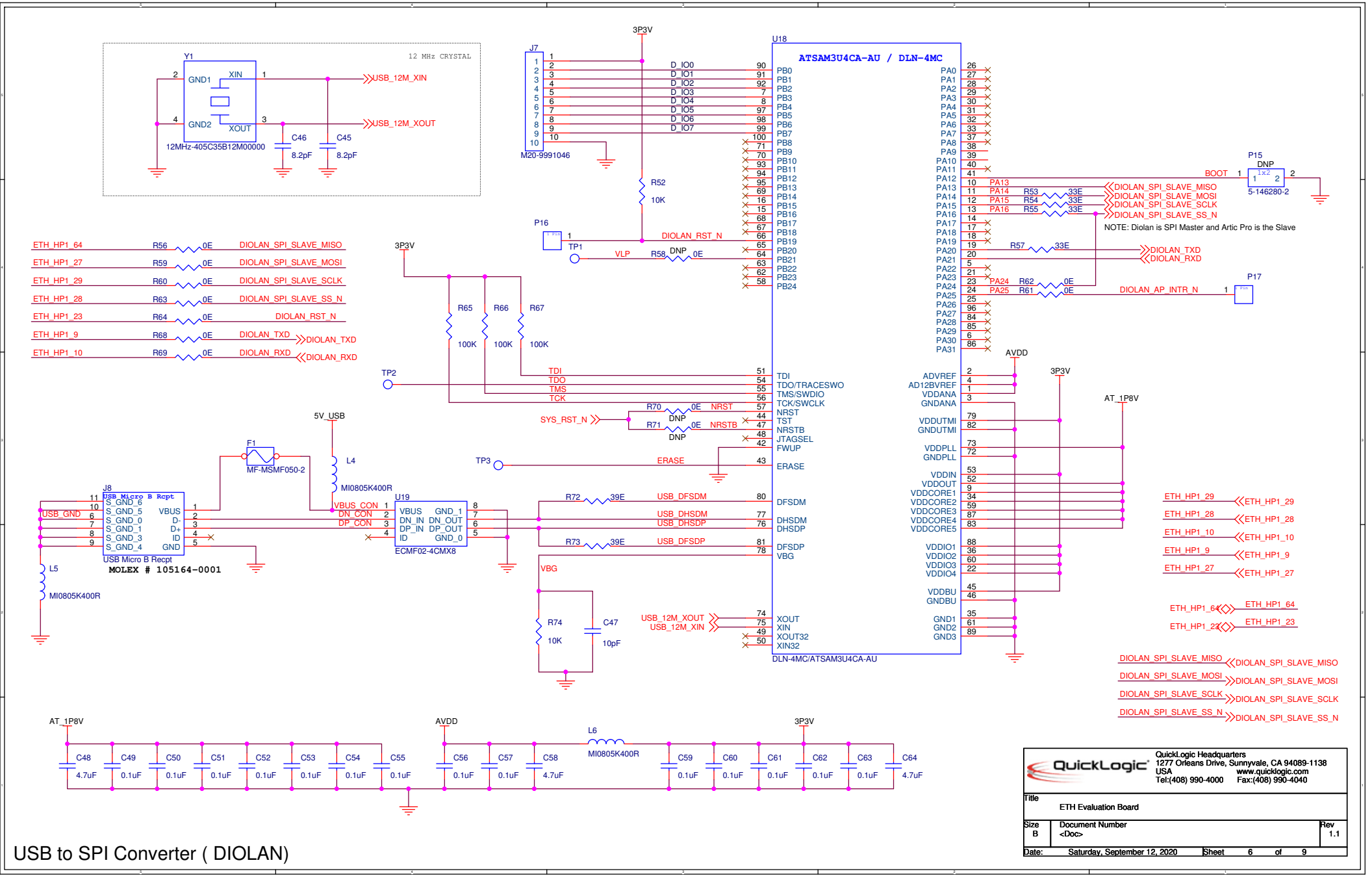


USB to SPI Converter (DIOLAN)

EXPANSION HEADERS

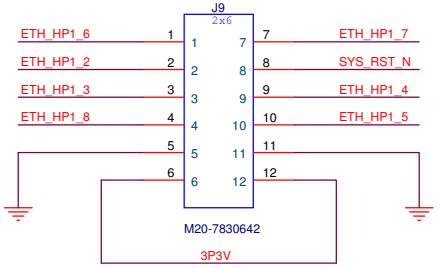
ETH_HP1_6 ETH_HP1_6
ETH_HP1_2 ETH_HP1_2
ETH_HP1_3 ETH_HP1_3
ETH_HP1_8 ETH_HP1_8
ETH_HP1_7 ETH_HP1_7
SYS_RST_N SYS_RST_N
ETH_HP1_4 ETH_HP1_4
ETH_HP1_5 ETH_HP1_5

3P3V 1P8V
3P3V 1P8V

ETH_HP1_22 ETH_HP1_22
ETH_HP1_19 ETH_HP1_19
ETH_HP1_21 ETH_HP1_21
ETH_HP1_18 ETH_HP1_18
ETH_HP1_20 ETH_HP1_20

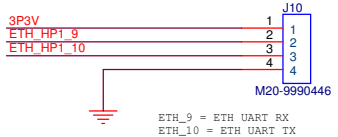
ETH_HP1_17 ETH_HP1_17
ETH_HP1_46 ETH_HP1_46
ETH_HP1_33 ETH_HP1_33
ETH_HP1_34 ETH_HP1_34
ETH_HP1_35 ETH_HP1_35
ETH_HP1_36 ETH_HP1_36
ETH_HP1_37 ETH_HP1_37
ETH_HP1_38 ETH_HP1_38
ETH_HP1_39 ETH_HP1_39
ETH_HP1_40 ETH_HP1_40
ETH_HP1_41 ETH_HP1_41
ETH_HP1_42 ETH_HP1_42
ETH_HP1_43 ETH_HP1_43
ETH_HP1_30 ETH_HP1_30
ETH_HP1_27 ETH_HP1_27
ETH_HP1_29 ETH_HP1_29
ETH_HP1_28 ETH_HP1_28

SPI MASTER (PMOD FLASH)



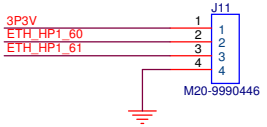
ETH_6 = PMOD CSn (1)
ETH_2 = PMOD SI/SDIO0 (2)
ETH_3 = PMOD SO/SDIO1 (3)
ETH_8 = PMOD SCK (4)
ETH_7 = PMOD NC/CSn1 (7)
SYS_RST_N = PMOD RSTn (8)
ETH_4 = PMOD WP/SDIO2 (9)
ETH_5 = PMOD HLC/SDIO3 (10)

UART



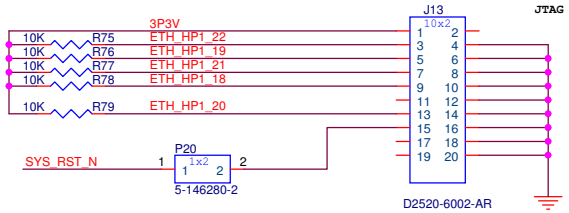
ETH_9 = ETH UART RX
ETH_10 = ETH UART TX

I2C

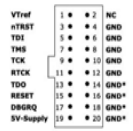


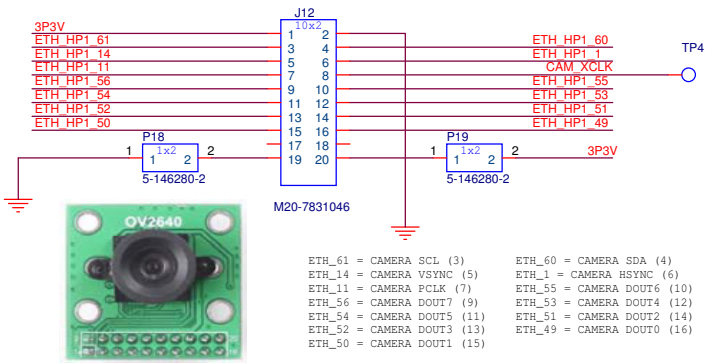
ETH_60 = I2C SDA
ETH_61 = I2C SCL

JTAG



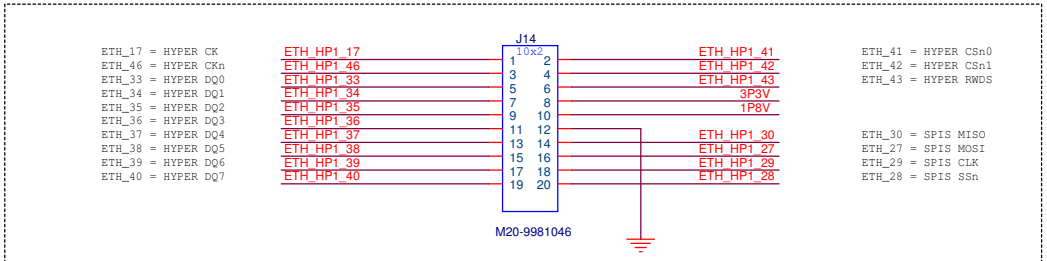
ETH_22 = JTAG RSTn (3)
ETH_19 = JTAG TDI (5)
ETH_21 = JTAG TMS (7)
ETH_18 = JTAG TCK (9)
ETH_20 = JTAG TDO (13)





ETH_61 = CAMERA SCL (3)
ETH_14 = CAMERA VSYNC (5)
ETH_11 = CAMERA PCLK (7)
ETH_56 = CAMERA DOUT7 (9)
ETH_54 = CAMERA DOUT5 (11)
ETH_52 = CAMERA DOUT3 (13)
ETH_50 = CAMERA DOUT1 (15)

ETH_60 = CAMERA SDA (4)
ETH_1 = CAMERA HSYNC (6)
ETH_55 = CAMERA DOUT6 (10)
ETH_53 = CAMERA DOUT4 (12)
ETH_51 = CAMERA DOUT2 (14)
ETH_49 = CAMERA DOUT0 (16)



ETH_17 = HYPER CK
ETH_46 = HYPER CKn
ETH_33 = HYPER DQ0
ETH_34 = HYPER DQ1
ETH_35 = HYPER DQ2
ETH_36 = HYPER DQ3
ETH_37 = HYPER DQ4
ETH_38 = HYPER DQ5
ETH_39 = HYPER DQ6
ETH_40 = HYPER DQ7

ETH_41 = HYPER CSn0
ETH_42 = HYPER CSn1
ETH_43 = HYPER RWDS

ETH_30 = SPIS MISO
ETH_27 = SPIS MOSI
ETH_29 = SPIS CLK
ETH_28 = SPIS SSn

ETH_HP1_9 ETH_HP1_9
ETH_HP1_10 ETH_HP1_10
ETH_HP1_14 ETH_HP1_14
ETH_HP1_11 ETH_HP1_11
ETH_HP1_56 ETH_HP1_56
ETH_HP1_54 ETH_HP1_54
ETH_HP1_52 ETH_HP1_52
ETH_HP1_50 ETH_HP1_50

ETH_HP1_60 ETH_HP1_60
ETH_HP1_61 ETH_HP1_61
ETH_HP1_1 ETH_HP1_1
ETH_HP1_55 ETH_HP1_55
ETH_HP1_53 ETH_HP1_53
ETH_HP1_51 ETH_HP1_51
ETH_HP1_49 ETH_HP1_49

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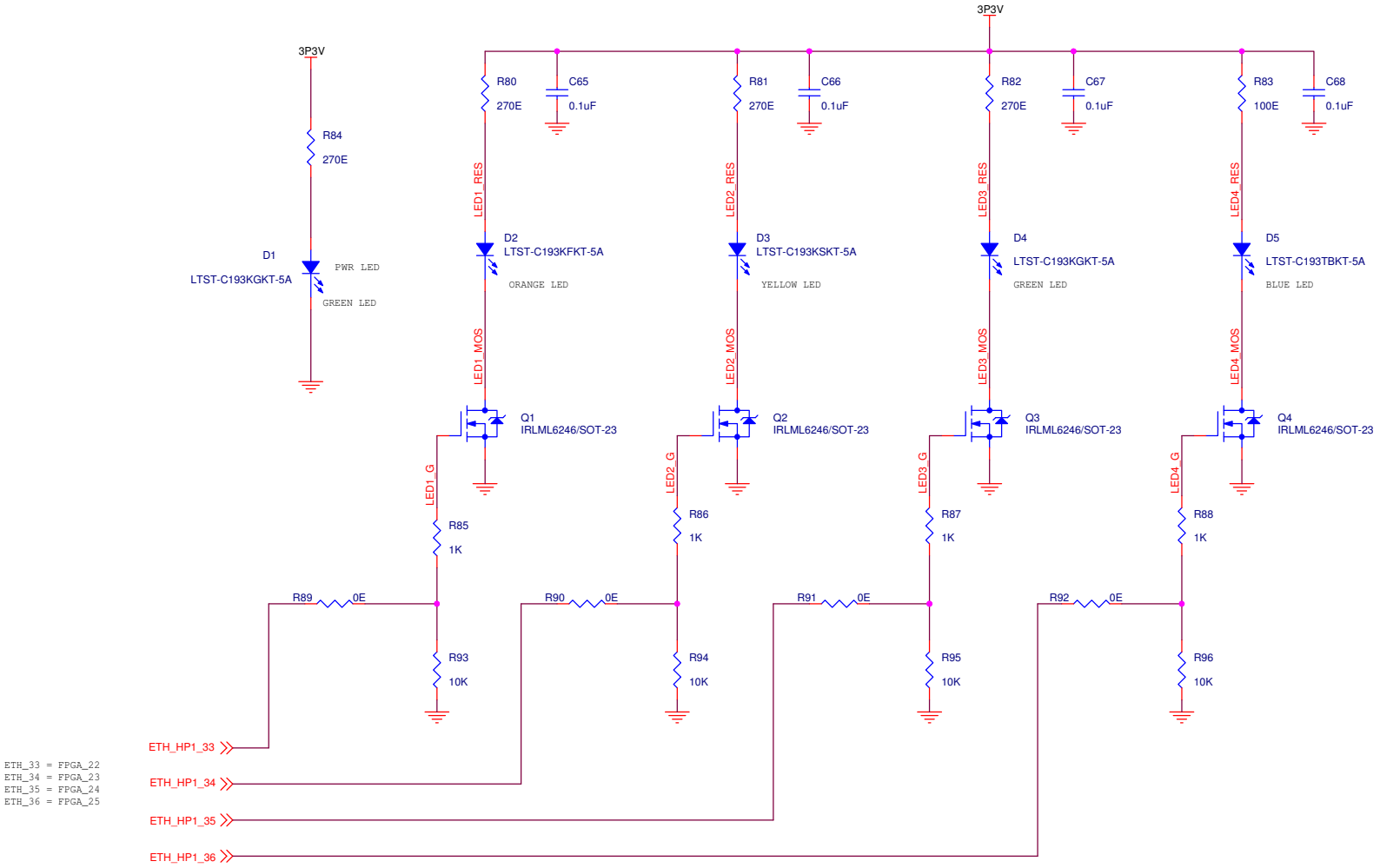
Date: Saturday, September 12, 2020	Sheet 7 of 9	

LEDs



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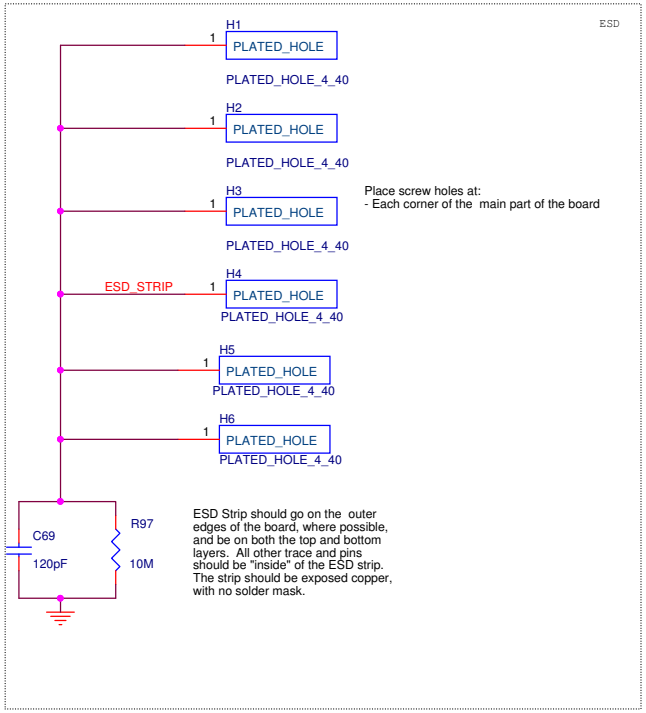
Mounting Holes and ESD Strip



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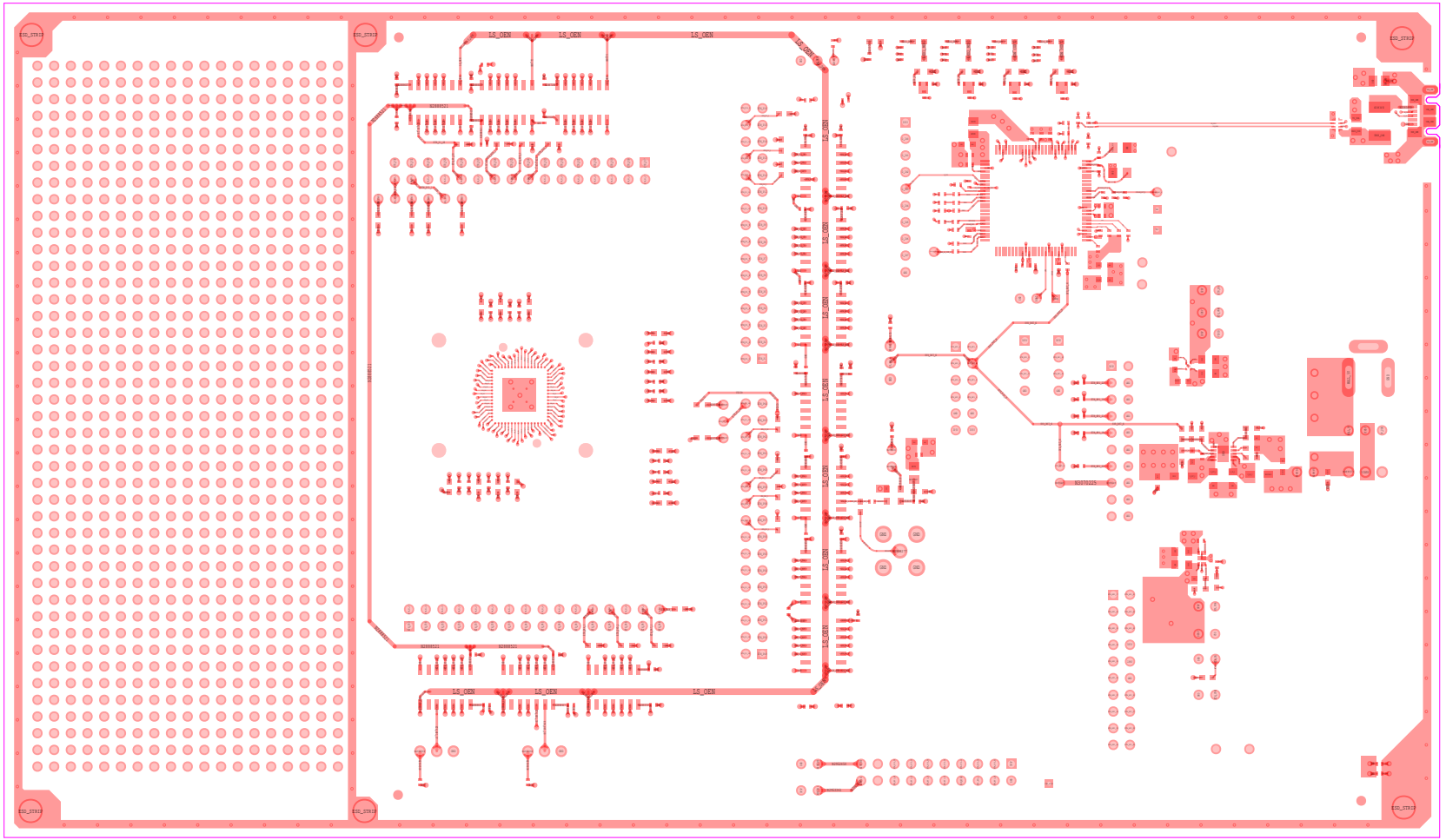
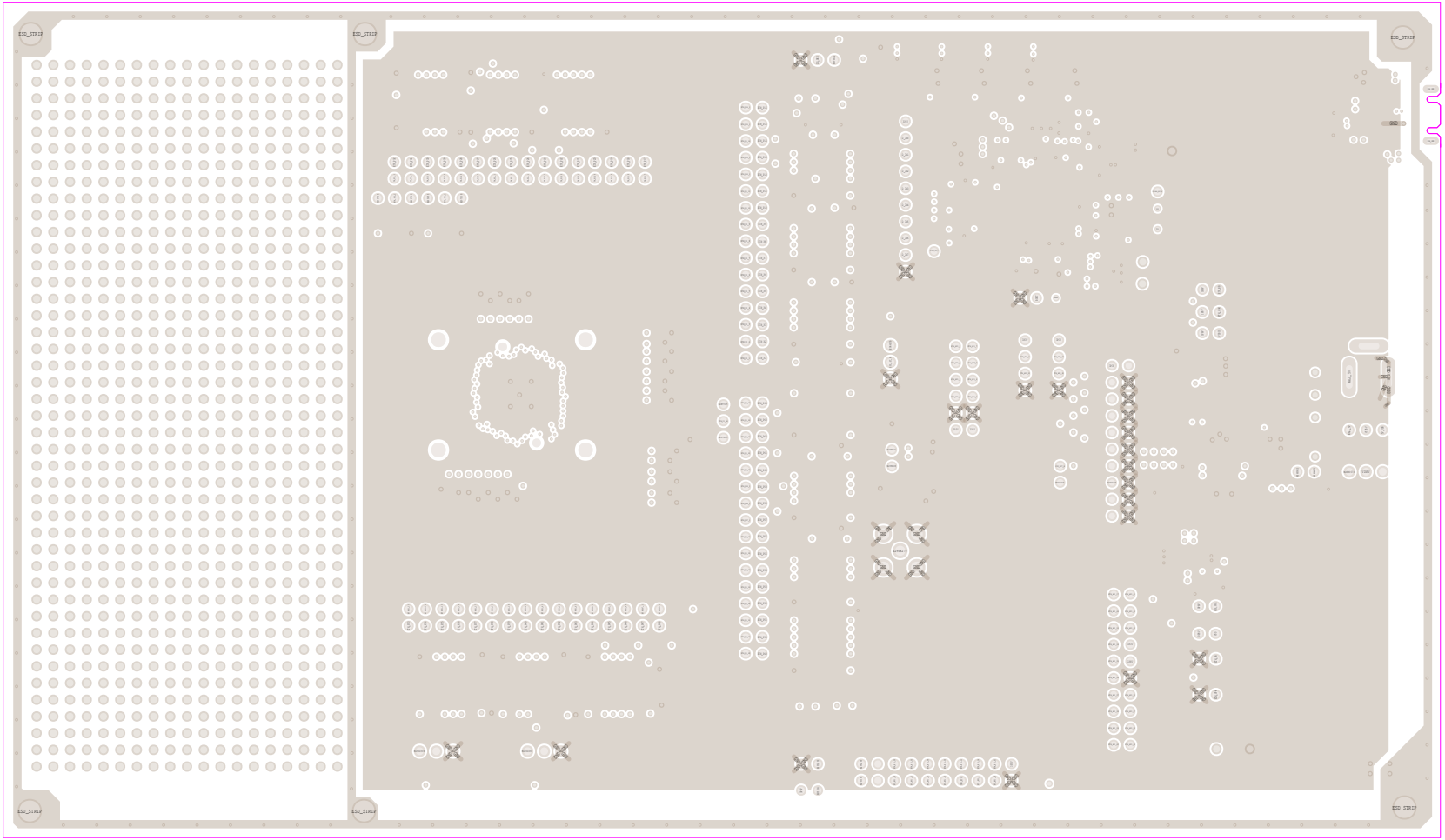
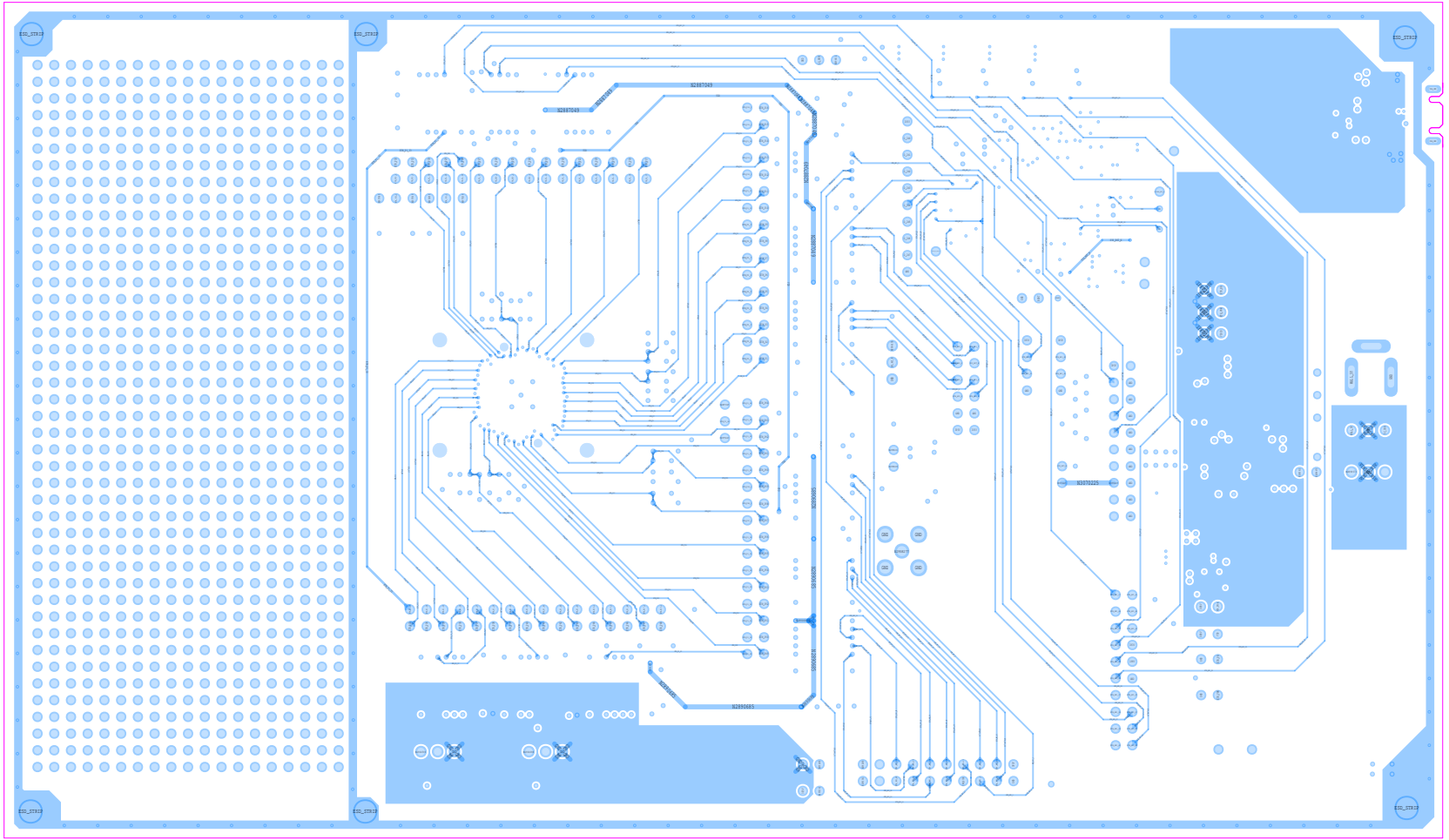


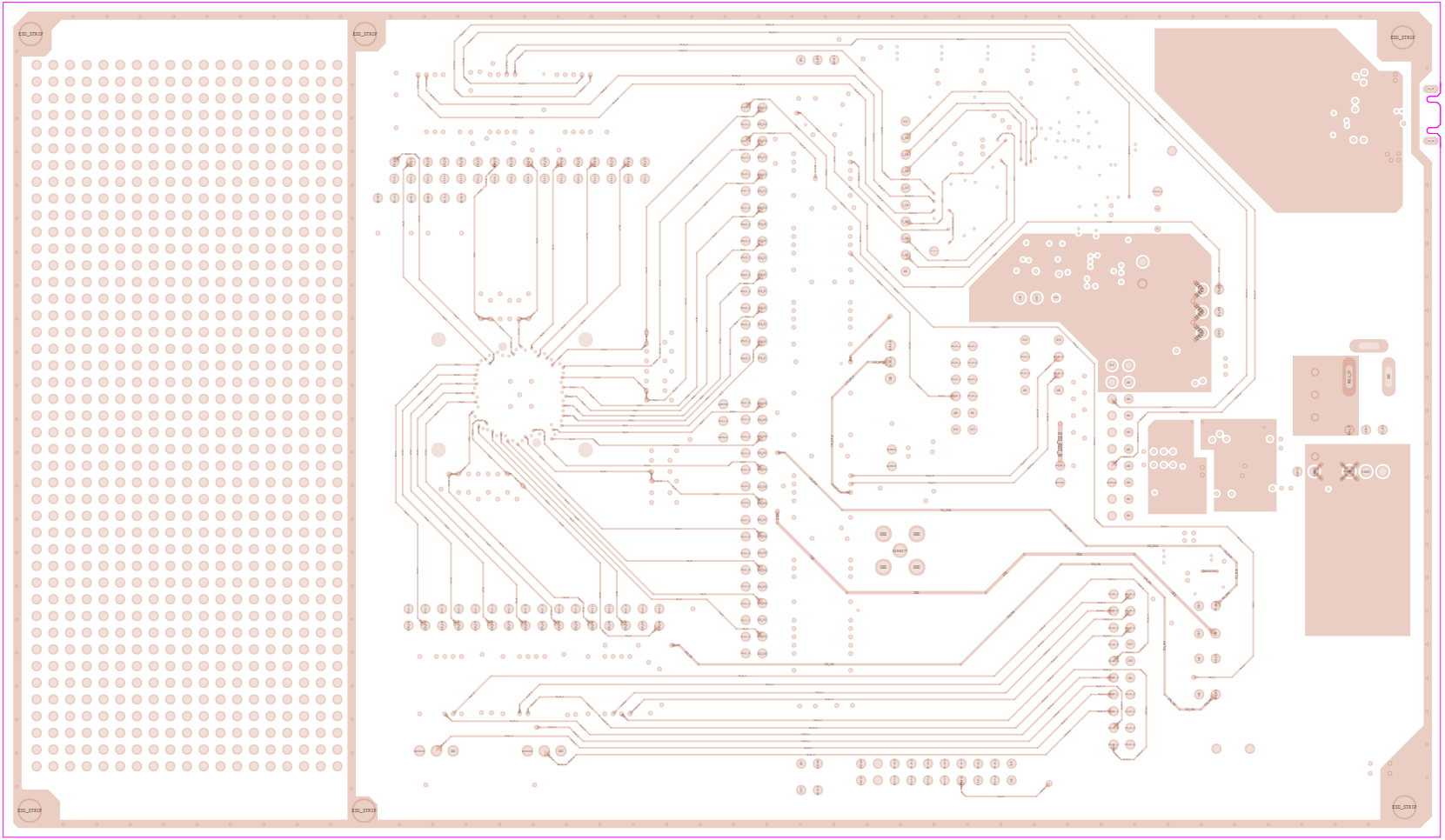
COMPONENT SIDE



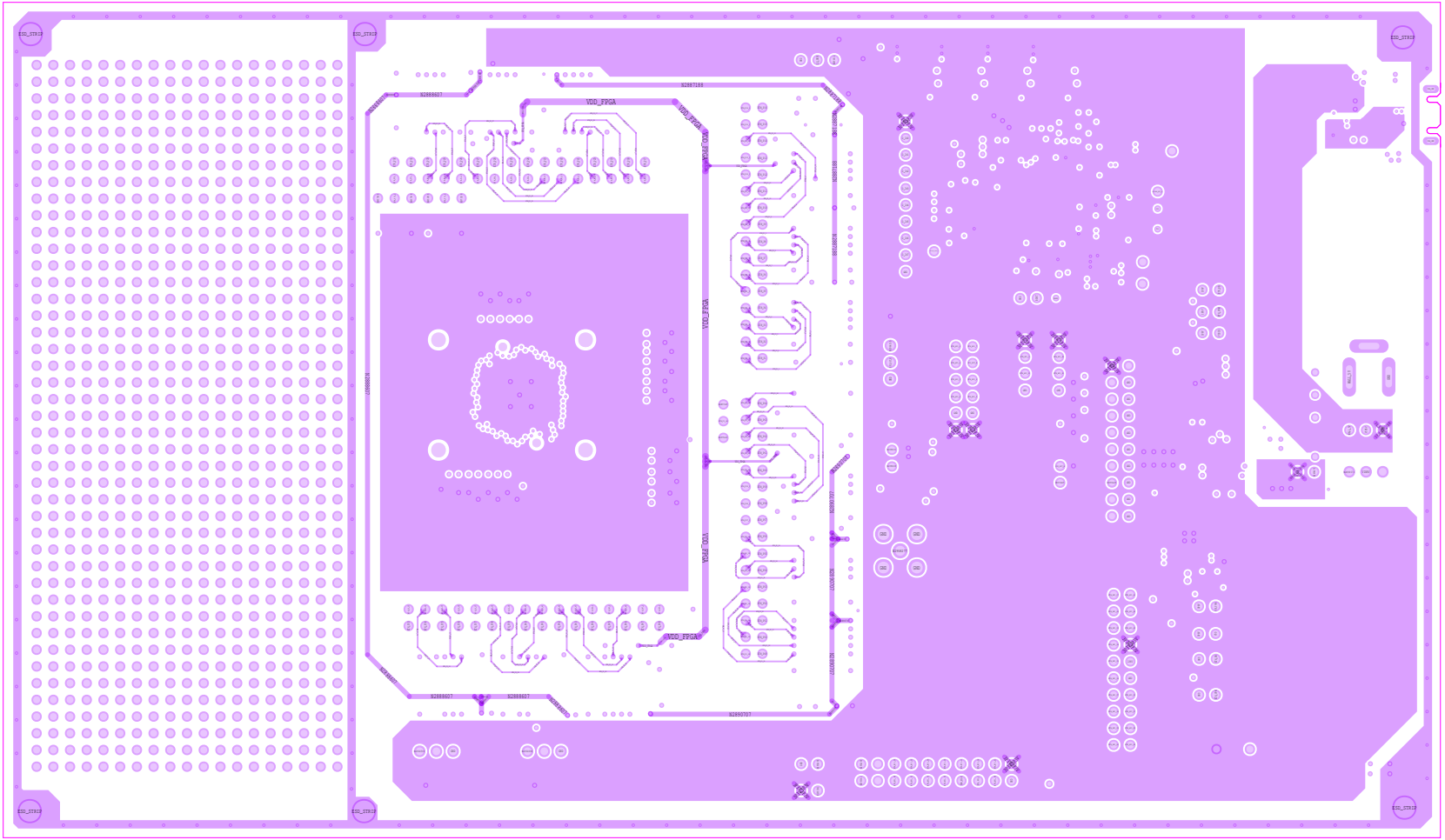
GND PLANE



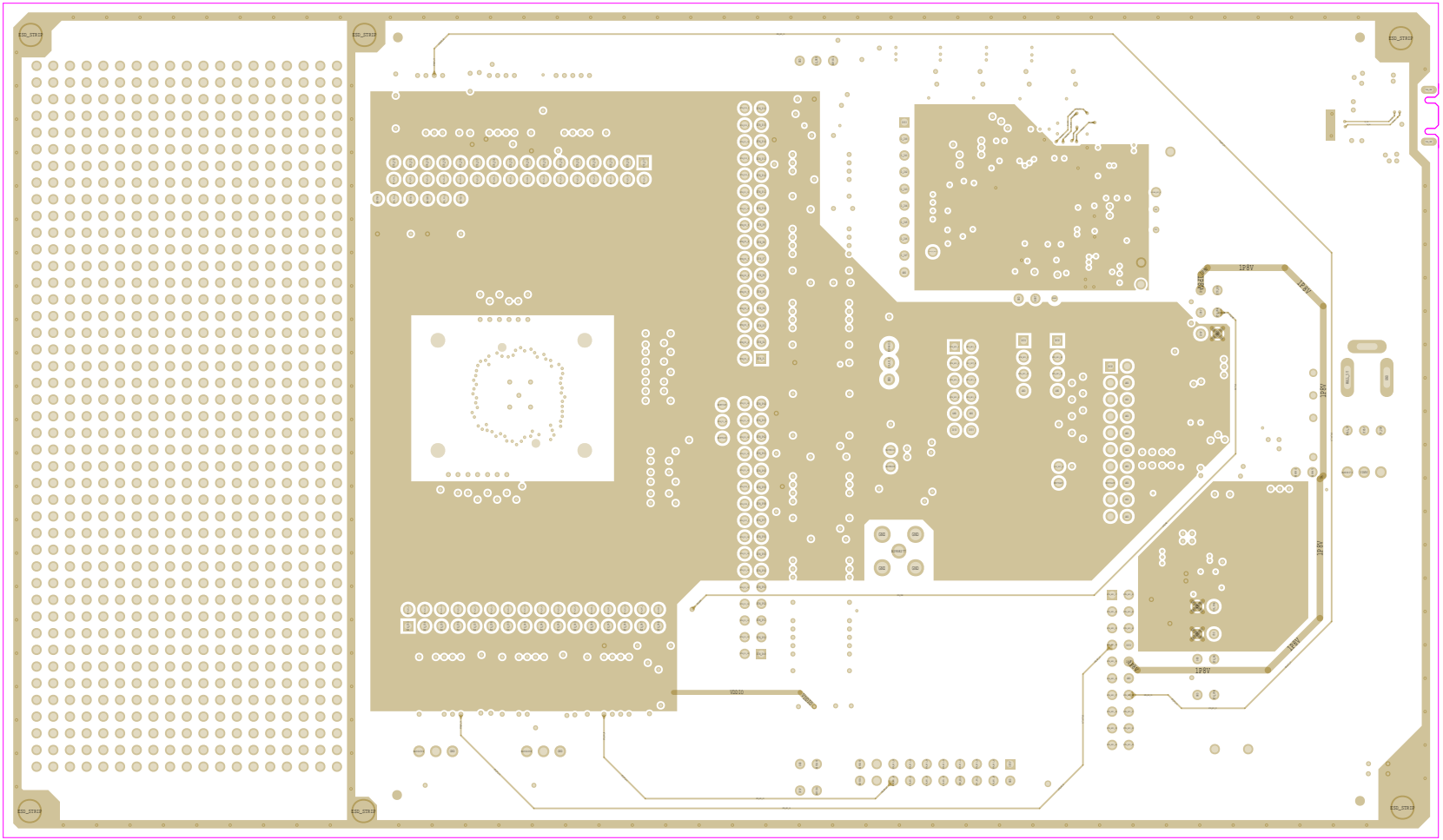
INTER1 LAYER



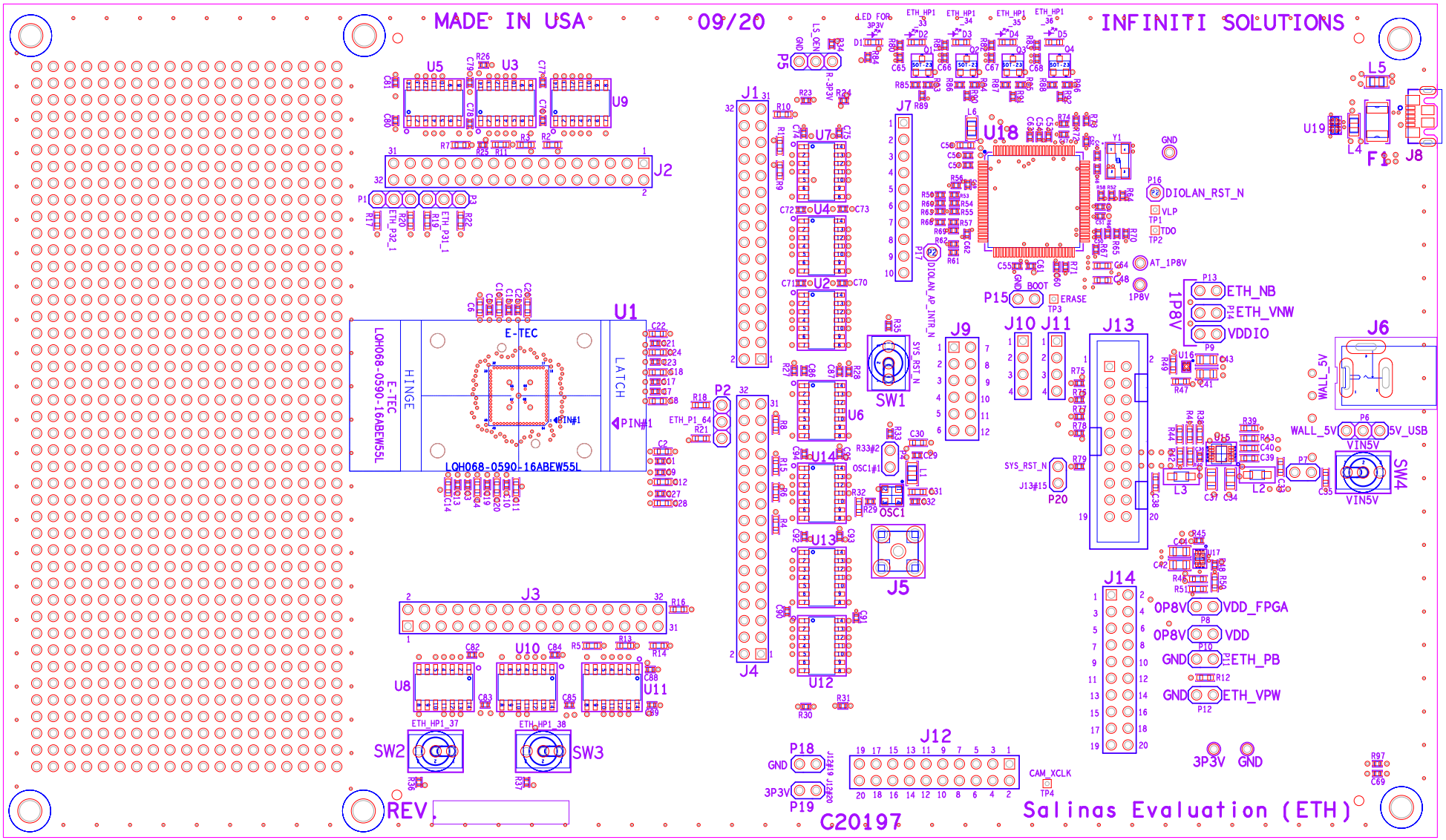
INTER2 LAYER



POWER PLANE

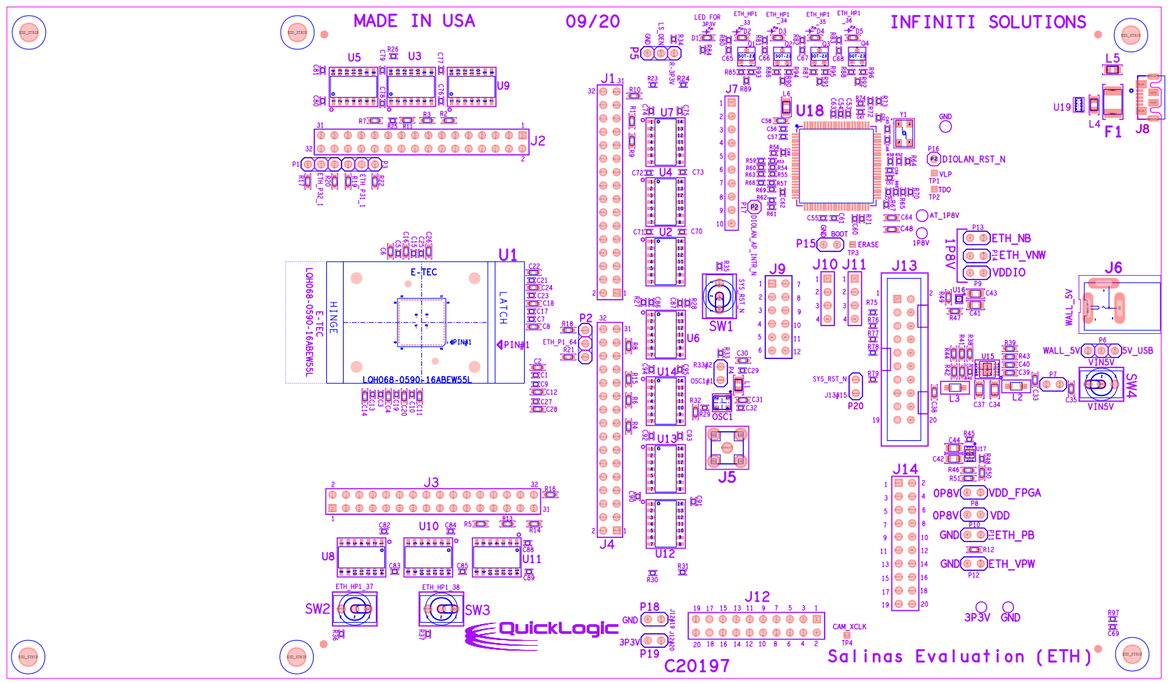


BOTTOM SIDE


MADE IN USA
09/20
INFINITI SOLUTIONS
U1
E-TEC
LQH068-0590-16ABEW55L
HINGE
LATCH
PIN#1
U18
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
J14
P2
P5
P15
P16
P17
P18
P19
P20
SW1
SW2
SW3
SW4
U5
U3
U9
U4
U2
U6
U7
U8
U10
U11
U12
U13
U14
OSC1
L5
L4
L3
L2
F1
U19
DIOLAN_RST_N
VLP
TDO
AT_1P8V
1P8V
BOOT
ERASE
ETH_NB
ETH_VNW
VDDIO
WALL_5V
5V_USB
VIN5V
OP8V
VDD_FPGA
VDD
ETH_PB
ETH_VPW
3P3V
GND
CAM_XCLK
SYS_RST_N
DIOLAN_AP_INTR_N
REV.
C20197
Salinas Evaluation (ETH)

REV. NO.	DATE	DESCRIPTION	REVISED BY	PASSED BY
1.1	09/12/20	CHANGE USB J8 AND SOME CONNECTION UPDATED IN LAYOUT	PMS	HMP

* PLEASE TAPPED OFF TEST PADS TP1-TP4 AND P5 WHILE WAVE SOLDERING.
* SOCKET U1&IT'S IC WILL BE SUPPLIED & INSTALLED BY QUICKLOGIC



ASSEMBLY TOP

50 OHM SINGLE ENDED IMPEDANCE CONTROL BOARD
100 OHM DOUBLE ENDED IMPEDANCE CONTROL BOARD
SILKSCREEN TOP REQUIRED (WHITE EPOXY)

0.063" +/- 10%

0.5oz	FOIL	
	PREPREG 0.008"	LAYER 1 (COMP. SIDE) — 50-OHM SINGLE ENDED, 11 MIL TRACE; 90-OHM DIFF IMPEDANCE, 9 MIL TRACE, 10 MIL SEPARATION.
0.5/0.5	CORE 0.014"	LAYER 2 (GND PLANE)
	PREPREG 0.008"	LAYER 3 (INTER-1)
0.5/0.5	CORE 0.014"	LAYER 4 (INTER-2)
	PREPREG 0.008"	LAYER 5 (PWR PLANE)
0.5oz	FOIL	LAYER 6 (SOLDER SIDE) — 90-OHM DIFF IMPEDANCE, 9 MIL TRACE, 10 MIL SEPARATION.

DFM ANALYSIS		
MINIMUM AIRGAP	LINE/LINE	0.0058"
	LINE/DRILL	0.010"
	DRILL/DRILL	0.010"
MIN. TRACE WIDTH		0.007"
MIN. DRILL		0.010"
FILLED VIAS		NO
IMPEDANCE		YES

FINGER PLATING: N/A

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN Millimeter
TOLERANCES ARE
.XXX = .005 .XX = .01

DSNR: SMM
DATE: 09/12/20
CHECKED:
DATE:
POSITIONS: 1

MATERIAL: HI TEMP. FR4 (170C Tg)

SOLDER MASK: GREEN LPI
LAYERS: 06

FOR BIB DESIGN	X	Y
MATRIX	--	--
STEP	------	-------

INFINITI SOLUTIONS
3910 N,FIRST STREET,
San Jose, CA 95134
Phone (408) 923-7300
FAX (408) 251-5431

CUSTOMER NAME: QUICKLOGIC

DEVICE: Salinas Evaluation (ETH)

IS DESIGN NO: C20197 DESIGN REV: 1.1

SCALE 1/1 SHEET 1 OF 1 SIZE: D