

Development of direct and indirect III-V on Si growth for solar cell applications

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Development of Direct and Indirect III-V on Si Growth for Solar Cell Applications

by

Hongfeng Wang

A thesis submitted to UNSW in fulfilment of the requirements for the degree of
Master of Philosophy



School of Photovoltaic and Renewable Energy Engineering

The University of New South Wales

October 2018



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III-V material solar cell on Si substrate has drawn a considerable amount of research interest due to the ability to deliver high energy conversion efficiency with reduced cost. However, challenges arise due to lattice constant mismatch and thermal expansion coefficient mismatch issue, as well as the anti-phase domain issue arising from polar on non-polar growth between III-V material and Si substrate. Two different approaches have been investigated in this work regarding the problems of crystalline III-V material integration on Si substrate. The first approach is to integrate III-V via virtual Ge. To this goal, growth procedures were developed for Migration Enhanced Epitaxy (MEE) initiation of GaAs deposition on offcut Ge substrate. Results showing that high temperature annealing prior to deposition plays a significant role on double atomic steps formation. Initiating the process at low temperature with group V material and applying low thermal energy group V material throughout the entire fabrication process improves the film quality. An alternative MEE initiation layer of AlAs was also investigated with results showing successful reduction of the substrate roughness. The other approach applies strained layer superlattice (SLS) as a dislocation filter (DF) on the substrate has been demonstrated and analysed. InAlAs based SLSs were fabricated with As₂ or As₄ to investigate the impact of different As sources implementation. Result indicates As₂ can improve DF performance. A novel III-V alloy with high shear modulus and low band gap energy, GaAsSb, was identified by applying selection rules from a literature search. The performance of GaAsSb SLS DF was compared with InAlAs based SLS DFs. Calculated dislocation densities for all samples shows that the GaAsSb SLS DF has the best performance in threading dislocation reduction with $\rho_{TD} = 1.07 \times 10^6 /cm^2$ at sample surface. Finally, a comparison has been made between AlAs/GaAs distributed Bragg reflector (DBR) and chirped DBR (CDBR) for increasing optical absorption in the III-V solar cells. Results indicate CDBR is more reliable by minimizing the impact from incident angle issue while maintain the reflectance at high level. The results taken together suggest successful integration of III-V on Si is achievable for solar cell application.

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Abstract

III-V material solar cell on Si substrate has drawn a considerable amount of research interest due to the potential to deliver high energy conversion efficiency with reduced cost. However, challenges arise due to lattice constant mismatch and thermal expansion coefficient mismatch issue, as well as the anti-phase domain issue arising from polar on non-polar growth between III-V material and Si substrate. Two different approaches have been investigated in this work regarding crystalline III-V material integration on Si substrate. The first approach is to integrate III-V via virtual Ge. To this goal, growth procedures were developed for Migration Enhanced Epitaxy (MEE) initiation of GaAs deposition on offcut Ge substrate. Results showing that high temperature annealing prior to deposition plays a significant role on double atomic steps formation. Initiating the process at low temperature with group V material and applying low thermal energy group V material throughout the entire fabrication process improves the film quality. An alternative MEE initiation layer of AlAs was also investigated with results showing successful reduction of the surface roughness. The other approach applied strained layer superlattice (SLS) acting as a dislocation filter (DF) on the substrate has been demonstrated and analysed. InAlAs based SLSs were fabricated with As₂ or As₄ to investigate the impact of different As sources. Results indicate As₂ can improve DF performance. A novel III-V alloy with high shear modulus and low band gap energy, GaAsSb, was identified by applying selection rules developed from a literature search. The performance of GaAsSb SLS DF was compared with InAlAs based SLS DFs. Calculated dislocation densities for all samples shows that the GaAsSb SLS DF has the best performance in threading dislocation reduction with $\rho_{TD} = 1.07 \times 10^6 /cm^2$ at sample surface. Finally, a comparison has been made between AlAs/GaAs distributed Bragg reflector (DBR) and chirped DBR (CDBR) for increasing optical absorption in the III-V solar cells. Results indicate CDBR is more reliable by minimizing the impact from incident angle issue while maintain the reflectance at high level. The results taken together suggest successful integration of III-V on Si is achievable for solar cell application.

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Chapter 1 Introduction

1.1 Motivation

During the past decades, the development in industrial silicon solar cell device has showcased new and promising approach towards renewable energy. The use of Si based photovoltaic device has grown rapidly during the past decades. Si is abundant, robust, and inexpensive with continuously improving effort; crystalline Si solar cell devices having reached high energy conversion efficiency up to 25% [1]. Si devices have undoubtable advantages over other material systems, which has led to Si being the dominant material in the photovoltaic market [2]. Despite the achievements for efficient energy conversion, there are still limits on single junction solar cells, such as the Shockley-Queisser (SQ) radiative efficiency limit.

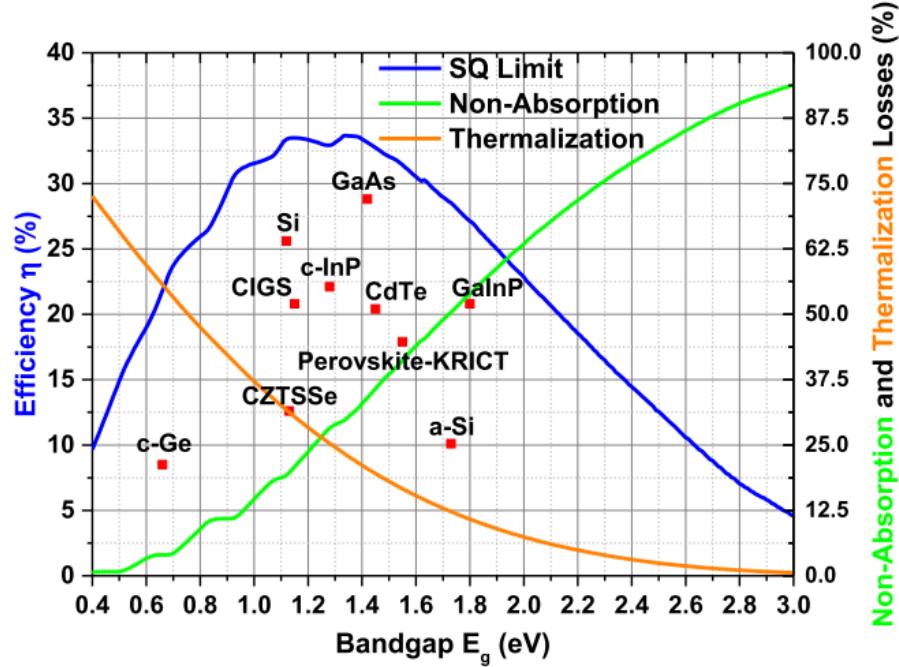


Figure 1.1: SQ efficiency limit for single p-n-junction device as a function of band gap under 1 sun AM1.5G (ASTM G173-03). The fraction of loss processes related to nonabsorption and thermalization are shown as well [3].

Figure 1.1 illustrates the SQ radiative efficiency limit for single homojunction solar cell as a function of band gap under 1 sun AM1.5G. The blue curve is Shockley-Queisser (SQ) radiative efficiency limit, which is determined by two fundamental physical losses that any single p-n junction solar cell device suffers from. One fundamental loss is the current loss caused by the non-absorption of photons with energies below the semiconductor band gap, which is shown as the green curve in Figure 1.1. The other one is the voltage loss, as indicated by the orange curve in Figure 1.1, caused by the thermalization resulting from the carriers with photon energies higher than the band gap. Taking Si for example, Si has a band gap of 1.12eV, therefore, photons with energy beyond the band gap in the solar irradiation cannot be converted to electricity at their full potential. As shown in Figure 1.1, though the efficiency of Si and GaAs single homojunction solar cell exceeded 25%, the SQ limits are expected to be higher than 30% at the bandgap of Si and GaAs. Three loss mechanisms causing the efficiency to be lower than the SQ limits are listed as followings [4]: collection losses due to photon reflection or absorption in poorly responding cell regions, non-radiative recombination occurring together with radiative recombination, and electrical losses including series resistance and shunt resistance in cell. Among the three losses mentioned above, collection loss and electrical loss can be optimized by cell design. Besides these two losses, the other loss can be quantified by calculating the external radiative efficiency (ERE). Since SQ theory assumes 100% ERE, ERE determines how closely an experimental cell approaches the ideal condition. For GaAs and Si, the ERE are 32.3% and 2.2% respectively, as non-radiative Auger recombination is stronger than radiative recombination in Si [4].

To reduce the losses and optimize the efficiency for a single junction device, it is essential to understand the parameters that quantitatively determine the energy conversion efficiency. The energy conversion efficiency can be defined by the following equation:

$$\eta = \frac{V_{oc}I_{sc}FF}{P_{in}} \quad (1)$$

where the four parameters are open circuit voltage (V_{oc}), short circuit current (I_{sc}), fill factor (FF), and input power (P_{in}). P_{in} can be considered as a constant, since the sun is the input power source and solar insolation can be assumed to be a constant variable independent of the material chosen. The other parameters are all material related. The η is proportional to V_{oc} and FF, which indicates that the higher the V_{oc} , the higher the efficiency of the device. High V_{oc} can be achieved by choosing a material with large band gap (E_g). However, a large band gap in semiconductor material will lead to a decrease in the carrier generation therefore reduction in I_{sc} , thus yielding the maximum power output.

To overcome the fundamental losses and boost the energy conversion efficiency, multi-junction solar cells are designed to cover a wider range of the irradiation spectrum with intent to better use the high energy photons in short wavelength range without losing the low energy photons in long wavelength. In this case, multiple materials are stacked up from the low band gap layer to higher band gap layers at the top of the device.

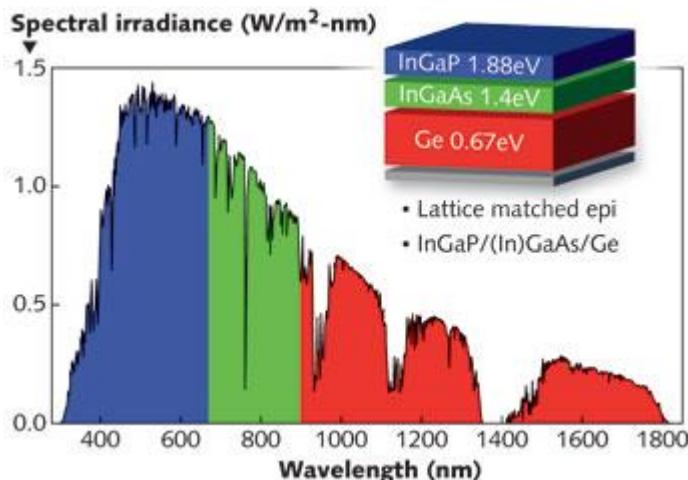


Figure 1.2: Structure and absorption of a conventional multi-junction solar cell. Light is incident on the top of the structure in the inset, with the top InGaP layer absorbing the part of the solar spectrum shown in blue, the centre InGaAs layer absorbing the green shaded area, and the bottom Ge layer absorbing the red-shaded wavelengths (Source: Courtesy of Solar Junction).

Figure 1.2 shows the structure and absorption of a conventional three-junction cell, with a bottom germanium (Ge) junction on a Ge substrate, covered by layers of indium gallium arsenide (InGaAs) and indium gallium phosphide (InGaP). The working mechanism of the multi-junction solar cell is that when photons enter the device, the photons with high energy (i.e. blue light) will be absorbed and generate carriers within the wide band gap junction (i.e. 1.88 eV InGaP), and then the photons with less energy (i.e. green) will bypass the first junction and to the lower band gap material (i.e. 1.4 eV InGaAs). Wavelengths longer than 900 nm are transmitted to the 0.7 eV Ge junction, which absorbs out to 1800 nm. Thermalization loss is minimised in this case. In such a way, it becomes possible to fabricate a high efficiency device. Figure 1.2 showcases the evolution of highest energy conversion efficiency for research cells, from 1976 to September 2015. The multi-junction cells take the lead and followed by the single junction GaAs cell as indicated by the purple curves. Recent study unveiled a novel modelling of triple-junction solar cell (InP substrate [5,6] and Si substrate [7]) has the potential to reach 50% conversion efficiency at high concentration ratio.

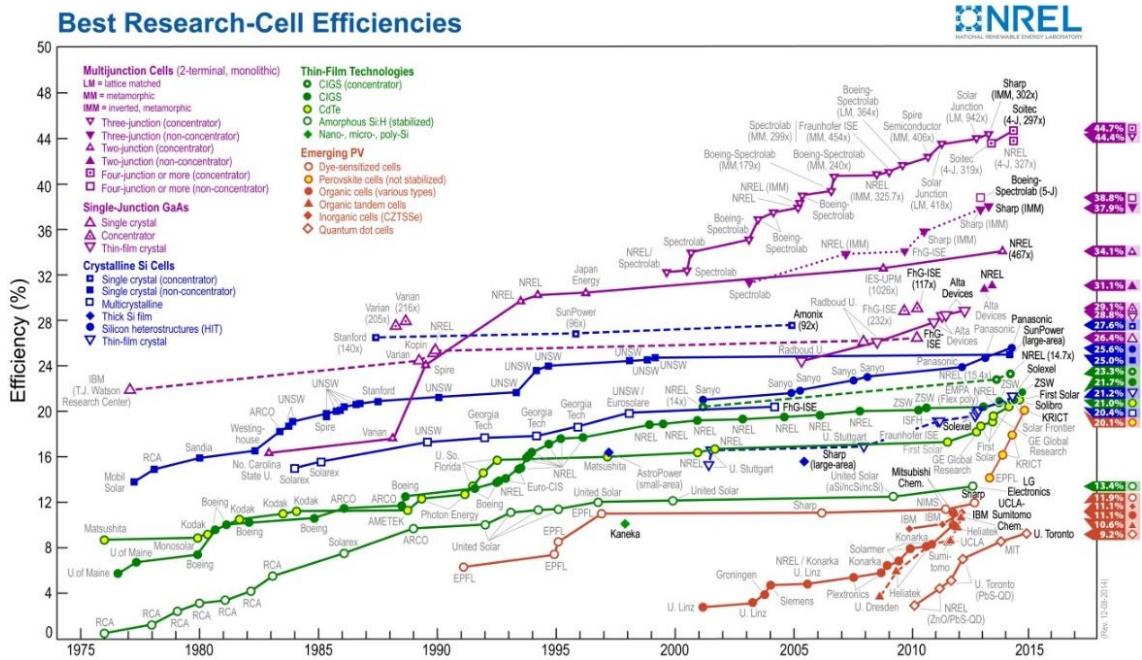


Figure 1.3: A plot of compiled values of highest confirmed conversion efficiencies for research cells, from 1976 to September 2015. (Source: Department of National Renewable Energy Laboratory).

Figure 1.4 illustrates the efficiency limits of two- and three-junction multi-terminal (Figure 1.4.a) and two-terminal (Figure 1.4.b) tandem stacks employing different materials as active substrates [3]. When comparing both plots, it is easy to notice that in either multi-terminal independent connection or two-terminal series connection structures, Si stands out for a double-stack structure, while Ge is more favourable in triple-stack structure.

By employing multi-junction structure, the efficiency can be boosted by lowering the thermalization loss. Hence higher voltage can be obtained, while the current generation in each junction may be mismatched. Studies have reported that the excess current generated by the low bandgap Ge in a triple stack may be wasted when the top junctions are current limiting, while Ge substrate generates twice the current of that generated by the top junctions [3]. One way of alleviating current wastage is by substituting Ge with a higher bandgap material, or even cheaper Si substrate. Apart from this current wastage

problem which would limit the efficiency, multi-junction solar cells face some other challenges.

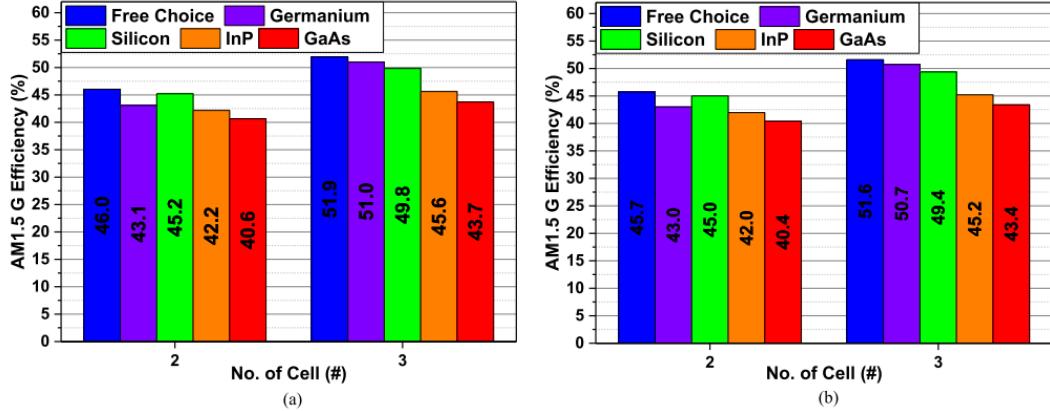


Figure 1.4: Radiative conversion efficiency of two- and three-junction cell structure using various materials as active substrate under 1 sun AM 1.5G (ASTM G173-03) spectrum in (a) multiterminal independent connection and (b) two-terminal series connection structures [3].

One major drawback, with multi-junction solar cells, is the high cost. III-V multi-junction solar cells are monolithically grown on expensive substrate (mainly III-V or Ge). Although the efficiency is high, the substrates are cost-prohibitive for significant market penetration as long as the expensive substrates are employed during the fabrication of multi-junction devices. This issue can be alleviated by the concentration of light, but substrate cost reduction is still required. As shown in Figure 1.4, there is no significant radiative conversion efficiency loss when the substrate is switched from Ge to Si for triple-stack structures. Besides, as mentioned above, Si substrate has a considerable advantage of low fabrication cost.

With this being addressed, the ideal device can be designed as a multi-junction III-V device fabricated on Si substrate. This device would take the advantages from each aspect and avoid the drawbacks of each single structure. To choose an appropriate III-V material for epitaxial growth onto Si substrate, two characteristics must be taken into consideration. One is the lattice mismatch between the III-V material and Si substrate.

The other is the band gap of this III-V material must be appropriate for further device fabrication. The lattice mismatch has to be small to avoid introducing a great number of defects. In such case, GaP is chosen for direct epitaxial integration on Si due to a small lattice mismatch to Si (0.37 % at 300 K) [8,9]. Under practical circumstance, the band gap of GaP is 2.26 eV which is high enough to pose no threat to the transmittance of the photons from the top junction to active Si substrate [10]. Therefore, a virtual GaP substrate would support subsequent epitaxy based on GaAsP and GaInP alloys towards high efficiency photovoltaic device [8]. Unfortunately, Phosphorus (P) brings fabrication issues and is unavailable in the fabrication laboratory where this work was conducted. Therefore, by considering the properties of several III-V materials, GaAs stands out for its high electron and hole mobility with wider band gap (1.42 eV) compared to Si (1.12 eV), which can serve as a great platform for subsequent high efficiency GaAs-based device fabrication. Meanwhile, as shown in Figure 1.1 and Figure 1.3, GaAs device shows great advantage in conversion efficiency. Hence, the targeting III-V material involved in this work is GaAs. However, the fundamental and severe challenges remain in depositing III-V directly on Si substrate.

The lattice constant of most III-V materials is much larger than that of Si. For example, the lattice mismatch between GaAs and Si is 4.1% (at room temperature), which causes high density of misfit dislocations and 3-dimensional island nucleation problems at the beginning of the growth process. This results in an unacceptably rough surface for continuing the deposition process. Even though there are still antiphase domain formation problems between Ge and GaAs, fortunately, the lattice constant of Ge (0.56578 nm) is almost identical to that of GaAs (0.56535 nm), and the lattice mismatch is only 0.07 %. Based on these materials characteristics, two approaches involving direct and indirect III-V material integration on Si substrate was investigated in this

work. First approach is to integrate III-V via virtual Ge on Si substrate. The other approach applies strained layer superlattice (SLS) as dislocation filter (DF) for GaAs growth on a Si substrate. The focus of this work is to investigate the III-V material integration on Si substrate, hence the Si substrate in this work only serves the role of mechanical support rather than being an active cell.

1.2 Objective and Outline

The objectives of this work are as follow: (1) reviewing the challenge of fabrication of III-V on Si, (2) searching for suitable approaches to resolve the challenge, (3) investigating and analysing the performance of the potential solutions, and (4) proposing further modification of the reviewed and investigated approaches.

In chapter 2, background knowledge regarding the challenge of III-V deposition on Si will be covered. Meanwhile, the two approaches be conducted in this work will be proposed. One is using an engineered substrate and the other is a dislocation filter approach. In chapter 3, the experimental equipment along with the characterization techniques involved in this work, which include molecular beam epitaxy (MBE), atomic force microscopy (AFM), X-ray diffraction (XRD) and transmission electron microscopy (TEM) will be presented. Chapter 4 covers engineered surface approach with detailed experiment procedure revealed. Three aspects regarding the experimental procedure were selected to examine how these would affect GaAs epitaxial film quality. Chapter 5 presents the fabrication details and the structural review of the approach of employing strained layer superlattice as dislocation filters. Changes and other optimizations regarding the performance of the dislocation filters were made based on the characterization results and the dislocation reduction observed. In chapter 6, in order to improve the optical absorption in III-V solar cell region, a comparison was conducted

regarding the performance of distributed Bragg reflector and a chirped distributed Bragg reflector. Finally, in chapter 7, the overall result of this work will be summarized and discussed in conjunction with ideas on how to refine the experiments, and future work towards the device fabrication on top of the studied structure.

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Chapter 2 Literature Review

2.1 Introduction of III-V material integration on Si

III-V material semiconductor solar cell with Si substrate is attractive to researchers for past several decades due to its potential high energy conversion efficiency [1] and reduced substrate costs. Si offers advantage over Ge and GaAs substrate such as high thermal conductivity, mechanically lighter and stronger, and with a mature industrial development, with Si substrate offering considerably low cost and large size [2-4]. Nevertheless, problems arise when integrating III-V material on Si substrate because of lattice constant mismatch and thermal expansion coefficient mismatch [1-4]. For instance, the mismatches in lattice constant and thermal expansion of GaAs/Si system are 4 % and ~63 %, which leads to significant defects generation in the active device region [2]. Furthermore, the difference between lattice structure of III-V and Si would result in anti-phase domain (APD) issue [2,4] caused by polar on non-polar deposition. Various methods and techniques have been proposed and implemented to control and reduce the defects generation. Thermally cycled growth of III-V intermediately layer can be employed to solve the thermal expansion mismatch problem. Lattice constant mismatch issue can be solved by inserting III-V buffer/superlattice structure at the interface, and/or employing engineered substrate surface to provide more suitable surface for III-V material deposition. Regarding the APD issue, off-cut wafers have been successfully adapted to extinguish these defects, meanwhile high temperature anneal has proven to be a suitable method to facilitate the formation of single domain Si surface [5]. The main techniques used in this thesis are targeting the lattice constant mismatch issue and the APD issue, the methods mentioned above will be employed as a combination to discuss the topic of III-V material integration on Si via both an engineered surface and III-V buffer layer.

2.2 III-V material integration on Si via Engineered Surface

As mentioned in Section 2.1, engineered surface technique can be employed to provide a more suitable surface for III-V deposition. An Engineered surface is a substrate surface which is created as a unique hybrid material offering more suitable material properties than a bare Si substrate. Such an approach is when gradual stepped composition SiGe layers are used to achieve high quality Ge on Si [6]. It has been shown that with a thin SiGe layer inserted between the epitaxial layer and Si substrate, since GaAs and Ge are nearly lattice matched, high quality GaAs can be achieved after the fabrication process is finished [7, 8]. Therefore, the ultimate goal of this approach is to deposit GaAs on Si substrate via sputtered virtual Ge layer. To simplify the fabrication process and concentrate on the development of growth procedure, all GaAs depositions in this work were conducted on 6° offcut [100] towards [110] plane Ge substrate.

2.2.1 Substrate Surface Configuration

To deposit III-V (GaAs) on an elemental substrate such as Ge or Si, one critical issue to be addressed is the polar on nonpolar growth problem [5], resulting in antiphase disorder on the III-V side of the material interface called antiphase domains (APDs). These are distinguished by a plane of wrong neighbor bonds, such as Ga-Ga bond or As-As bond, called antiphase boundary (APB), which would propagate into the later GaAs epitaxy as illustrated in Figure 2.1.

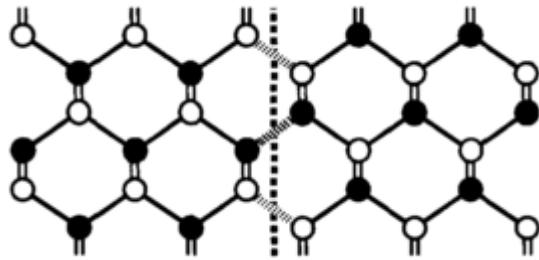


Figure 2.1: Antiphase boundary (APB) formation in GaAs. The configuration shown is a (110)-oriented APB, with alternating Ga-Ga and As-As bonds [5].

The Ge surface consists of terraces which can be categorized into two types of atom allocations: (a) one is dangling bonds of Ge atoms point parallel to the step edge, (b) the other is dangling bonds of surface Ge atoms point perpendicularly to the step edge [5].

Figure 2.2 illustrates both terraces on misoriented Ge [100] surface towards [011] direction with single atomic height steps (i.e. $a/4$ where a is the lattice constant). It has been pointed out that if the Ge surface contains only double atomic steps (i.e. $a/2$), the final GaAs layer is without antiphase defect [8]. On the other hand, if the GaAs was grown on a surface containing both terraces, the GaAs would exhibit different atomic stacking sequence corresponding to different terrace and edge combination which would lead to formation of APDs. Therefore, the double atomic step is essential for APDs free GaAs growth. Figure 2.3 [5] shows the APDs formation on both terraces, which is due to the single atomic steps on the substrate surface.

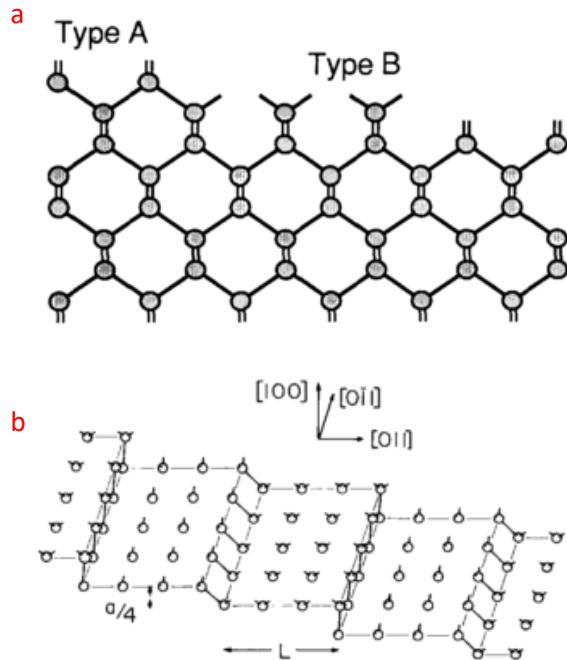


Figure 2.2: (a) two different dangling bond configuration of Ge [100] toward [011] direction misoriented plane single atomic height steps [5], (b) perspective view of this terraces with different types of dangling bond configuration[9].

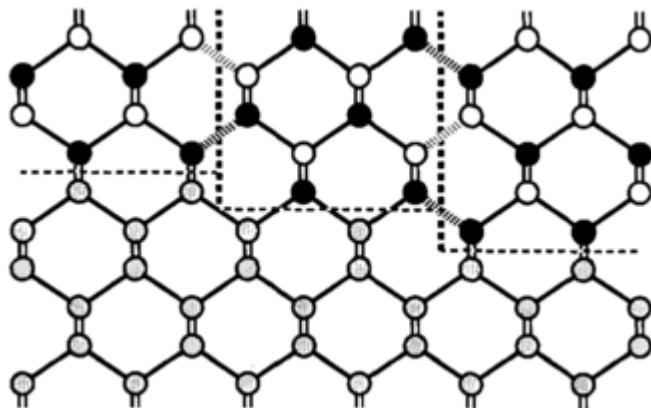


Figure 2.3: APBs (bold grey bonds between the atoms of the same colour) formation on a single atomic step surface with both type-A and type-B terraces orthogonal to the substrate surface (i.e. [100] direction) [5].

Many studies [5,11-13] have showcased the use of few degree (normally 2-6 degree toward [110]) offcut substrates to suppress the formation of APD during the nucleation of GaAs. To achieve the terraces transformation from single atomic step to double atomic step, a high temperature treatment is required to permit the diffusion of Ge from energetically unfavorable steps to the favorable ones [11]. In such case, all surface

reconstruction pattern variations are monitored by reflection high energy electron diffraction (RHEED). Observation of RHEED pattern change from (2×2) to (2×1) , which is an indication of the formation of double atomic steps, can be obtained after a pre-growth high temperature anneal. After the formation of double atomic steps is confirmed by RHEED, the epitaxy process can be continued for the next stage.

2.2.2 Initiation Layer

If the substrate surface (Ge layer) is ideally smooth and flat, the structural quality depends on the initiation layer. If the initiation layer is not precisely controlled, which will result in the appearance of both Ga and As atoms at the same stage, the final structure would contain APD. Therefore, to achieve the single-domain growth, initiation layer deposition is crucial and needs to be precisely controlled. Normally, an As initiation layer is preferred because the As background overpressure is always higher. Besides this, the arrival Ga atoms would land on an As-terminated surface where all dangling bonds are saturated with As dimers on substrate surface [2]. An alternative initiation layer (Ga) has been employed for GaAs deposition and reported by some research groups [14-16]. It is evident that Ga initiation layer showcased advanced surface morphology compared to As initiation layer. Experimental results illustrated that the sample employed As pre-layer contains has worse defects such as APDs propagating towards GaAs region [14]. In contrast, evidence has been shown that As can lower the substrate surface free energy [2]. It had been shown in previous study that As dimers could be added to a Si surface with an orientation which was perpendicular to step edges for substrate temperatures in the range of $400 - 600$ °C, and the surface had predominantly double layer steps [16]. Similar result can also be observed on Ge surface [16]. Therefore, all GaAs depositions in this work started with an As initiation

layer serving a role as a surfactant. The details and characterization of GaAs deposition on Ge substrate will be covered in Chapter 4.

2.3 III-V material integration on Si via buffer layer

2.3.1 Introduction of dislocation filter

As illustrated in Figure 2.4, a typical strained-layer superlattice (SLS) structure consists of thin alternative mismatched layers which provide compression and tension forces so that the lattice constants are equal in the strained region [14]. With the individual critical thickness calculated and adjusted, no new misfit dislocation will be generated such that the lattice mismatch is accommodated. As can be seen in the middle part of Figure 2.4, the distortion of layers occurs along the deposition direction. This is due to the Poisson effect which leads the SLS layers to be tetragonal rather than cubic structure [14].

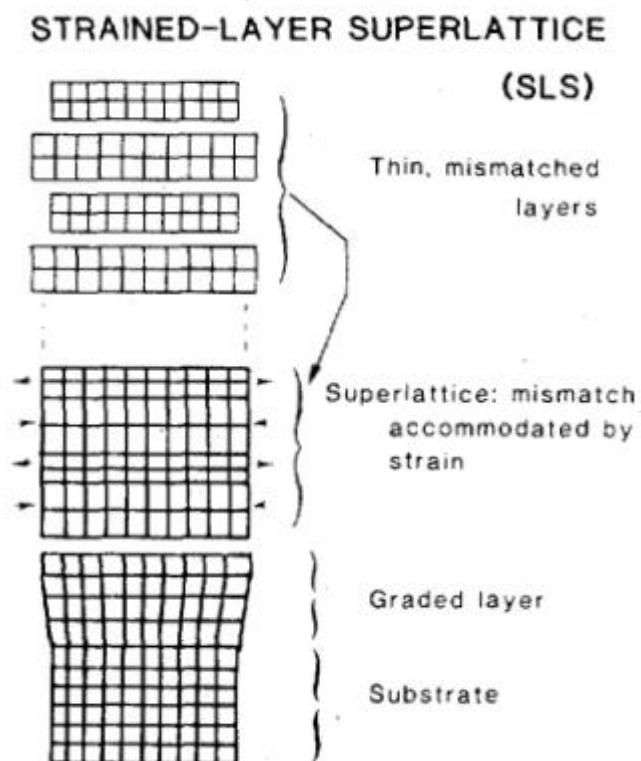


Figure 2.4: Schematic illustration of an SLS structure [14].

In the 1980's, several research groups revealed the observation of the unique ability of SLS to act as barriers against dislocation propagation through the grown film [14-17]. Since then, SLSs have drawn considerable interest because of the possibility to obtain high quality epitaxial layer grown on highly mismatched substrate [14]. SLS manipulates the dislocation motion in the perspective of moving, interacting and annihilation when the dislocation propagating along the grown direction [18]. With such an ability, to reduce defect density SLS has been widely adapted as dislocation filter layers (DFLs). The following schematic diagram of SLS DFLs structure has been adapted from other research groups as a reference structure [19-22]. This structure consists of four major components. First, a thin AlAs nucleation layer which was directly deposited on the substrate. Second, a graded GaAs buffer layer on top of the nucleation layer, followed by four stacks of SLS. The entire structure is finished with a GaAs capping layer. The detailed fabrication procedure of this structure will be elaborated in Chapter 5. The concept of this structure has been employed in various works and successfully reduced the threading dislocation density by several orders of magnitude.



Figure 2.5: Schematic Diagram of SLS DFLs.

The TEM image in Figure 2.6 [18] is one example illustrating the ability of an SLS structure reducing the threading dislocation density down to 10% compared to the initial amount after counting the dislocations crossed the marked line from 1 to 6.

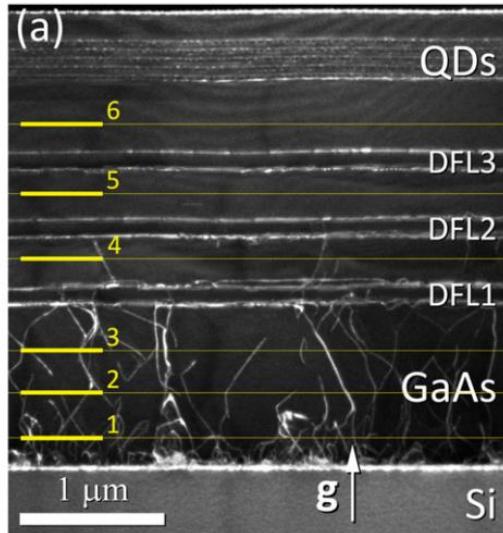


Figure 2.6: Dark field cross section TEM image illustrating epitaxial quantum dots structure on Si substrate with three sets of SLS acting as dislocation filter. The DFLs were grown after the deposition of GaAs buffer layer with an arrow pointing out the growth direction [18].

The observation of the above property of the SLS serving as DFLs has been explained with a threading dislocation annihilation mechanism. With the tension and compression that provided by the mismatched layers, the SLS system can be physically described as a balance driving force on threading dislocation, where the force is introduced by the strain in the misfit layer. There are two different types of threading dislocations, one is mobile (glissile) threading dislocations and the other is immobile (sessile) threading dislocations. The strain force allows the mobile ones to glide on the inclined planes. In such case, the mobile ones with opposite Burgers vectors can annihilate when they meet each other due to the attractive force. On the other hand, the immobile ones do not have an inclined plane, while they can react with a mobile one to produce a new mobile threading dislocation [23]. Therefore, it is necessary to consider dislocation

multiplication where repulsive dislocation interaction starts to dominate when dislocation pile-ups are produced by the multiplication sources [23]. This multiplication process can be understood as the reaction and recombination of misfit dislocations. In order to eliminate the dislocation, one essential approach is using the strain provided within the SLS to manipulate the movement of the dislocation, such that the reaction and recombination take place. As a result, the mobile dislocations are annihilated and the immobile dislocations become mobile which can be subsequently annihilated when the same circumstance applies [23]. Therefore, the threading dislocation density can be reduced by inserting SLS DFLs between the active region and substrate.

2.3.2 Dislocation motion analysis

Dislocation motion in GaAs/Si

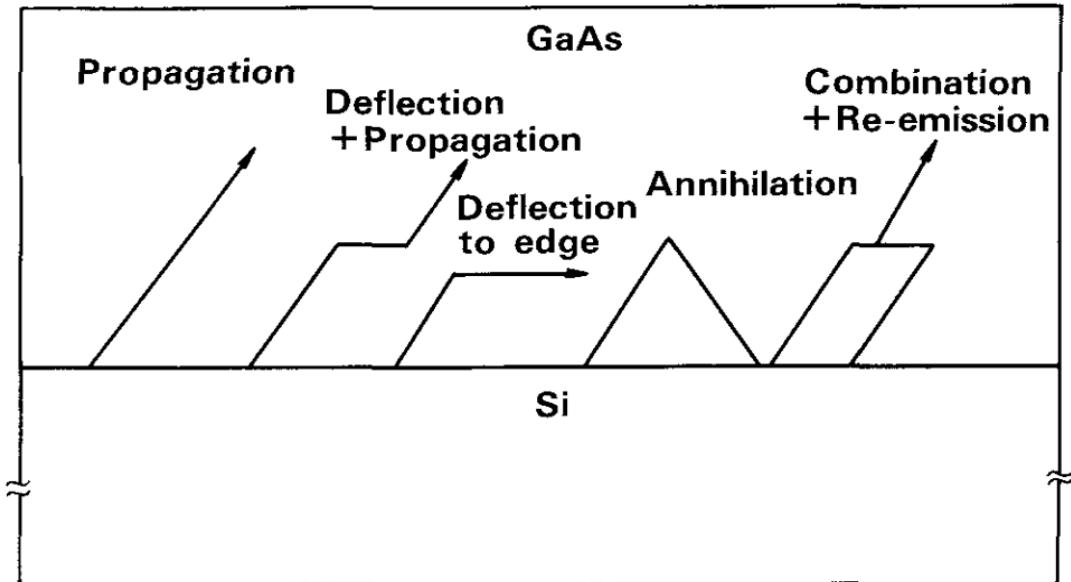


Figure 2.7: Dislocation motion in GaAs/Si system [27].

To obtain a deeper comprehension of how threading dislocation can be annihilated, it is essential to analyze the dislocation motion. As mentioned above, threading dislocation can be divided into two types, mobile (glissile) and immobile (sessile). The mobile ones

can glide along the inclined planes. When these dislocations encounter another dislocation (either mobile or immobile), the dislocations can react under an energetically favorable condition to combine and reproduce another dislocation. Figure 2.7 [27] illustrates the dislocation motion in a GaAs/Si system. As can be seen, the dislocation motion after encountering and reacting with another dislocation (either mobile or immobile) will be divided into two types. The deflection or combination occurs when the dislocation reacts with another dislocation, and the Burgers vectors can produce a positive product, then propagation continues. However, the dislocation will be trapped or blocked when the Burgers vector of these two dislocations are opposite, which means there is no reaction product [25]. Then the propagating dislocations will continue this loop while the motion is being encouraged and manipulated, such that the dislocation density will be reduced.

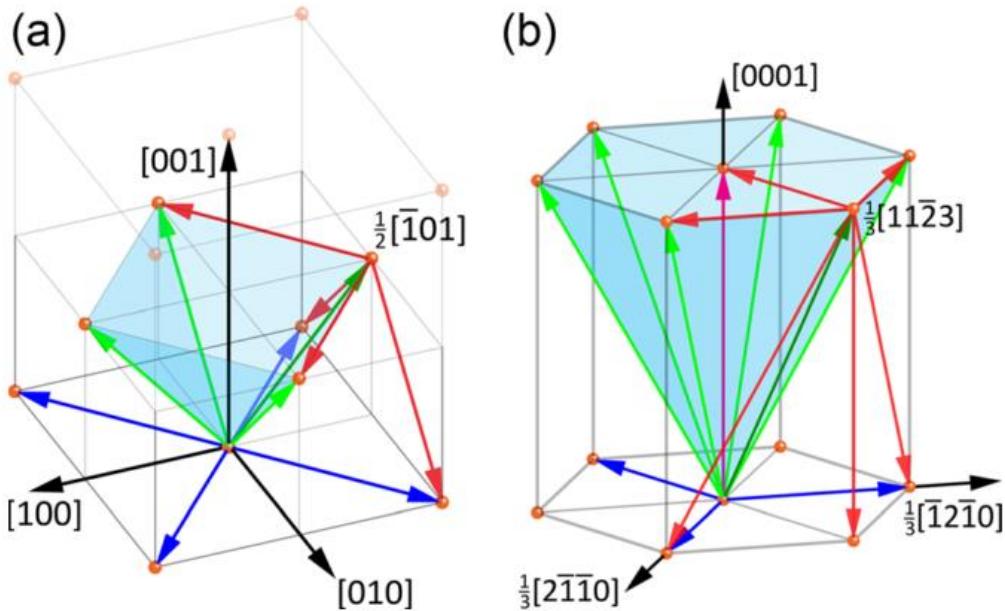


Figure 2.8: Burgers vectors in (a) $1/2 < 110 >$ fcc (i.e. GaAs) structure and (b) hexagonal (i.e. GaN) structure. Green arrows represent Burgers vectors of mobile threading dislocations, and the blue arrows stands for immobile threading dislocation. Four vectors with [00-1] components and seven vectors with [000-1] components are not shown in (a) and (b) respectively [25].

However, it must be noted that this dislocation reduction mechanism cannot be successfully applied to the hexagonal structure [25]. Figure 2.8 [25] illustrates the Burgers vectors in *fcc* and hexagonal structures. One mobile threading dislocation in *fcc* structure, taking $\frac{1}{2}[\bar{1}01]$ for example, can react with four other threading dislocations (red arrows) to generate a $\frac{1}{2}<110>$ reaction product. In hexagonal structure, one mobile threading dislocation, taking $\frac{1}{3}[11\bar{2}3]$ for example, can react with other six threading dislocations to give a reaction product. The immobile dislocations are unable to react even though a reaction may be energetically possible. It is worth emphasizing that unlike in *fcc* (i.e. GaAs) structure, the reaction product of two mobile dislocations in hexagonal structure (i.e. GaN) is two immobile dislocations, which is not helpful in dislocation density reduction [25]. This eventually would result in a scenario where all mobile threading dislocations are converted into immobile dislocations which are unreactive. This unique structural property would pose a severe restriction in selecting nitride material as suitable SLS material.

The dislocation motion can be quantitatively expressed by the concept of the threading dislocation velocity. The threading dislocation velocity in GaAs bulk crystal under a stress τ can be shown as the following equation [27]:

$$v = 9.86 \times 10^{-9} \tau^{1.6} \exp\left(-\frac{1.35eV}{kT}\right) \quad (cm/s) \quad (1)$$

where v is the dislocation velocity and τ is the stress. The threshold misfit stress needed for dislocation density reduction is found to be about $2 \times 10^5 \text{ dyn/cm}^2$, and the critical misfit stress for dislocation generation in GaAs layer was found to be around $1 \times 10^7 \text{ dyn/cm}^2$ [27]. Remarkable dislocation density reduction was found to be obtained with SLS layer thickness between the threshold layer thickness and critical layer thickness [27]. The threshold layer thickness needed for dislocation reduction is

correspond to the need for dislocation motion in the GaAs film region. As mentioned in section 2.3.1, this is caused by the misfit of the SLS, which can be inferred to correspond to the stress. In the case of an SLS thickness larger than the critical layer thickness, dislocations are expected to generate in the GaAs film region due to larger misfit stress [27]. These considerations suggest that further reduction of dislocation density in GaAs on Si substrate can be achieved by optimizing the SLS layers. A candidate SLS material selection, based around the dislocation motion velocity and mechanical properties will be elaborated in Chapter 5. Detailed fabrication procedures and the results of characterization will be discussed in Chapter 5.

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Chapter 3 Methodology

3.1 Introduction

In order to investigate the III-V deposition via engineered surface and buffer layer approaches were proposed in previous chapter. Molecular Beam Epitaxy (MBE) is employed to conduct the fabrication of all samples in this work. MBE offers features such as ultra-high vacuum (UHV) growth environment and *in situ* surface monitor by reflection high energy electron diffraction (RHEED) installed in the MBE equipment for precise control over growth. When the fabrication process is finished, atomic force microscopy (AFM) was be used to examine the surface morphology of the samples, X-ray diffraction (XRD) was be employed to analyse the structural properties of the thin films, as a complement to XRD, transmission electron microscopy (TEM) reveals the actual structural view of the deposited thin film. In this chapter, the basic working mechanism of equipment involved in this work is briefly introduced, offering general understanding of the role each equipment plays in this work.

3.2 Experimental Growth

3.2.1 Molecular Beam Epitaxy Growth

Molecular Beam Epitaxy (MBE) is a precisely monitored and controlled growth technique for thin epitaxial structure consists of various materials ranging from semiconductors to metals. The sources of reactants loaded in the MBE system are in solid phase. Group III and group V element sources are loaded in the effusion cells, the sources heat up and the material evaporates meaning a molecular beam emanates from the source. By controlling the shutters in front of the cell crucibles, collimated molecular beams reach the substrate surface, which allows precise growth timing.

Figure 3.1 illustrates a cross sectional schematic diagram of an MBE system.

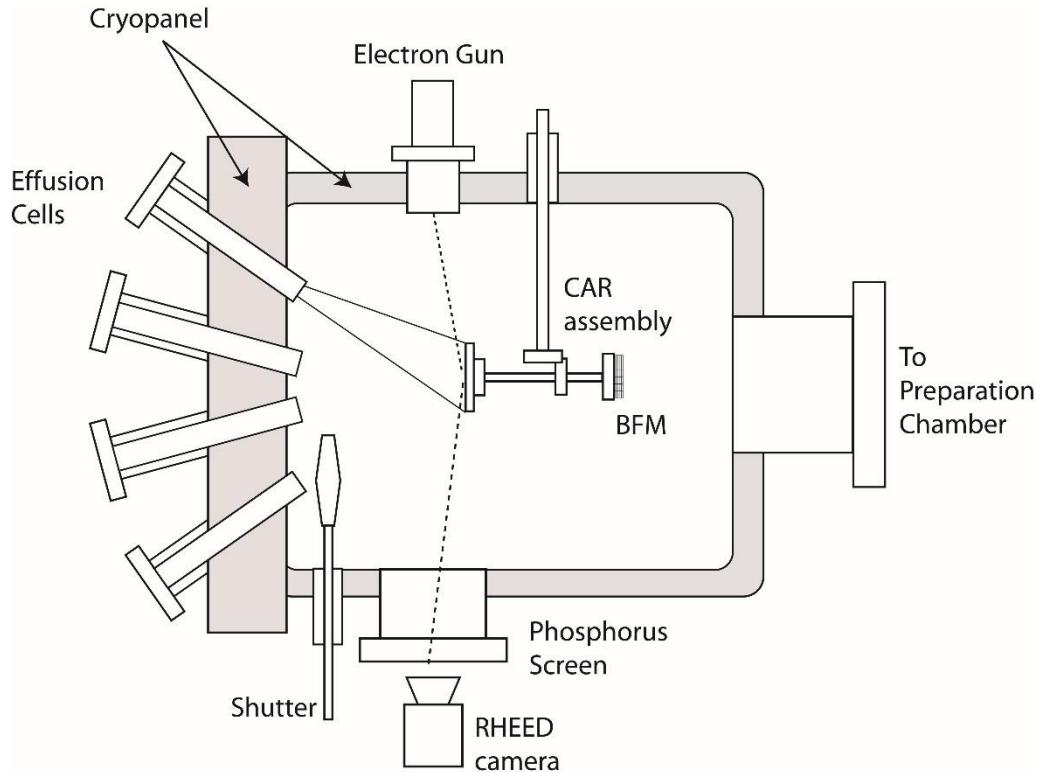


Figure 3.1: MBE schematic diagram.

When the growth process is initiated, MBE growth can be divided into three main stages where different actions take place. Molecular beams are generated in the first stage, while the beams mix together in the second stage, forming a sparse vapour landing on the substrate. In the last stage, crystallisation occurs at the growth surface.

The photo below shows the GEN930 Veeco MBE system, which is used in this work, that is located in the Australian National Fabrication Facility (ANFF), UNSW. As pointed out in the photo, three chambers are involved during the growth procedure: the load lock chamber, the buffer chamber, and the growth chamber. Prior to loading the substrates into MBE system, all substrates were cleaned with the wet chemical cleaning method, which will be elaborated in Chapter 4 and 5. Substrates are immediately loaded into the load lock chamber when they arrive in the MBE laboratory. Since the substrates are loaded at room atmosphere, substrates are annealed at 150 °C for 12 hours to remove the water vapour absorbed by substrate after the load lock pressure reaches a

level lower than 1×10^{-7} Torr. To further outgas, substrates are transferred to the buffer chamber for annealing when the initial bake process is finished. After the pre-growth heat treatment, substrates can be transferred to growth chamber for growth of structures.

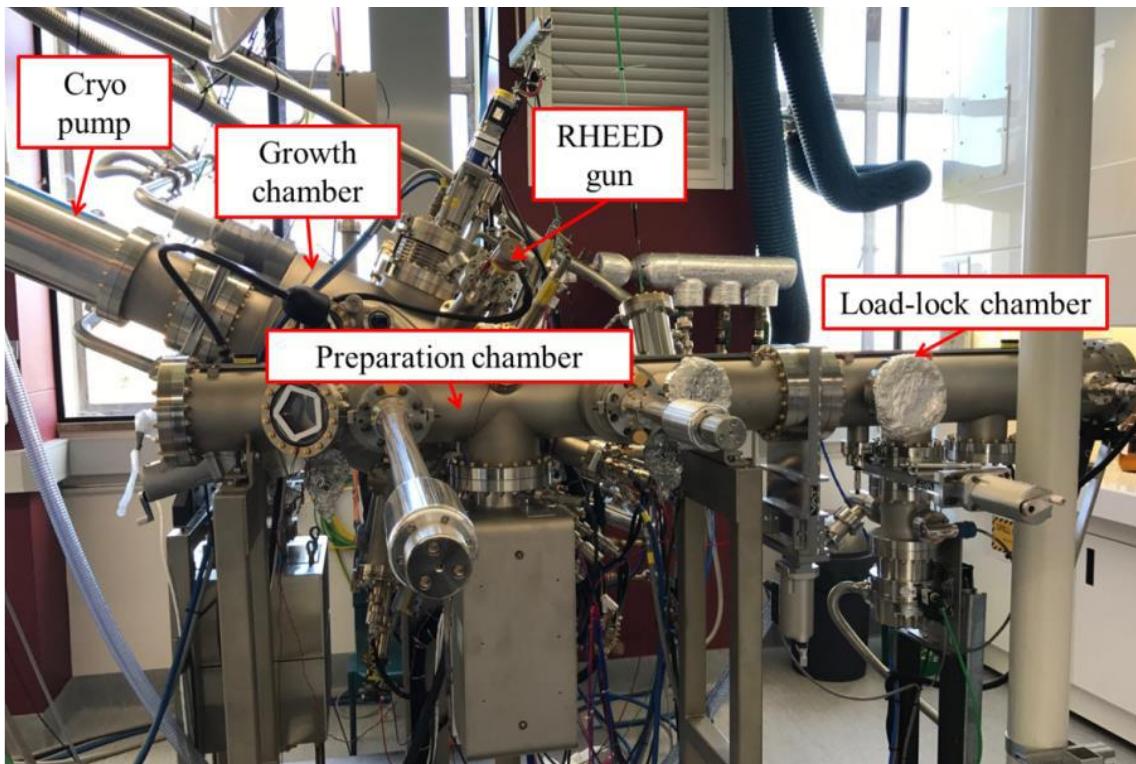


Figure 3.2: GEN930 Veeco MBE system used for sample fabrication in this project

This GEN930 MBE system is loaded with nine different sources, which can be divided into three categories as Group III element sources, Group V element sources and dopant sources. Two Gallium (Ga) sources, Indium (In) and Aluminium (Al) are serving as Group III growth sources. Arsenic (As), Antimony (Sb) and Bismuth (Bi) are serving as Group V growth sources. The dopant sources can be split into two sub-categories: n-type dopant and p-type dopant. A Si filament sources and GaTe are serving as n-type dopant, and one Be source is serving as p-type dopant.

The Group III growth sources are standard Knudsen cells, while Group V sources are “cracker” cells consisting of a large crucible for bulk evaporation with a valve allowing

beam flux to pass through a high temperature region that cracks the tetramers into dimmers. Effusion cells can supply Group III atoms or molecules from individual ceramic crucible. The evaporation rate, and therefore beam flux, is controlled by the cell temperature, hence the growth rate corresponds to the source temperature. Cracker cells are employed for Sb and As materials producing the tetramers As_4 and Sb_4 from elemental charges. The cracking region can provide thermal energy to crack the tetramers into dimers. Source temperatures are controlled by a Eurotherm proportional–integral–derivative controller (PID) thermocouple controller system. In front of each source cell, an independent pneumatic shutter is used to switch allow or block the beam, which enables monolayer scale deposition.

The growth chamber is the main component of the MBE system, where the ultra-high vacuum (pressure lower than 1×10^{-10} Torr) can be achieved by a pumping system including a cryo-pump, a liquid nitrogen filled cryo-shrouds and an ion pump. The liquid nitrogen keeps the sources panel and chamber shrouds cool. Such condition ensures the molecular beams pass through the chamber in a single path before reaching the substrate or condensing on the chamber wall. This preserves a pure growing layer and reduce the possibility of contamination from previous growth. A residual gas analyser (RGA) is mounted to diagnose the elemental components inside the chamber. To calibrate the substrate temperature, an out-of-chamber BASF TempeRaSure Pyrometer is mounted facing directly to the substrate surface to monitor the temperature via infrared radiation emission.

Prior to growth procedure takes place, all sources are normally set to be 50°C above the operation temperature to eliminate contamination which may result from condensation during idle. At typical growth temperature, the growth rate is dominated by Group III material due to the sticking coefficient of Group V materials is much lower than Group

III materials on a Group V terminated surface. Therefore, the III/V ratio is normally set to be 13-15 *beam equivalent pressure* (BEP) to ensure a Group V terminated surface. During the growth process, the RHEED is employed to monitor the surface condition, especially during the de-oxidization process. RHEED pattern will change from hazy spotty pattern to bright symmetrical streaky pattern indicating the completion of the de-oxidization process. Different surface reconstruction pattern will appear after de-oxidization process is finished. More details regarding RHEED pattern and growth settings will be revealed in later chapter.

3.2.2 Reflection High Energy Electron Diffraction

Reflection high energy electron diffraction (RHEED) is a commonly used in-situ monitoring tool in MBE growth. Due to the low electron beam penetration depth which is normally a few atomic layers, RHEED is highly sensitive to the surface condition of sample. RHEED is well suited to MBE during growth process since it must be performed in UHV environment such that no electron scattering would occur. The beam energy is normally 15 keV and the incident angle is lower than 5° upon the sample surface. Since the incident angle is small, the incident electrons only interact with the very top atomic layers, with the reflected and diffracted electrons hitting a phosphor screen producing a pattern corresponding to the surface structure as shown in Figure 3.3 [1]. RHEED is a useful surface monitoring tool both before and during the growth process. For instance: prior to epitaxy, observation of de-ox from sample surface, calibration of growth rate and determination of sufficient group V overpressure. Figure 3.4 illustrates the growth rate calibration with the help of RHEED intensity oscillation curve. When growth is initiated on a smooth substrate surface, the intensity of the RHEED pattern starts to oscillate [2]. The specular beam spot in Figure 3.3 pulses with the addition of monolayers, where it is bright when the monolayer is completed, and it

dims as the layer is formed. As the layer finishes, the surface becomes flat, leading to the specular spot intensity increasing. The oscillation frequency corresponds to the monolayer growth rate of III-V alloy. Then, information of surface morphology can be provided based on the appearance of the pattern mentioned above. The RHEED pattern exhibits a streaky feature of a smooth surface, whereas if the roughness of sample surface is high, the RHEED pattern will exhibit a spotty feature.

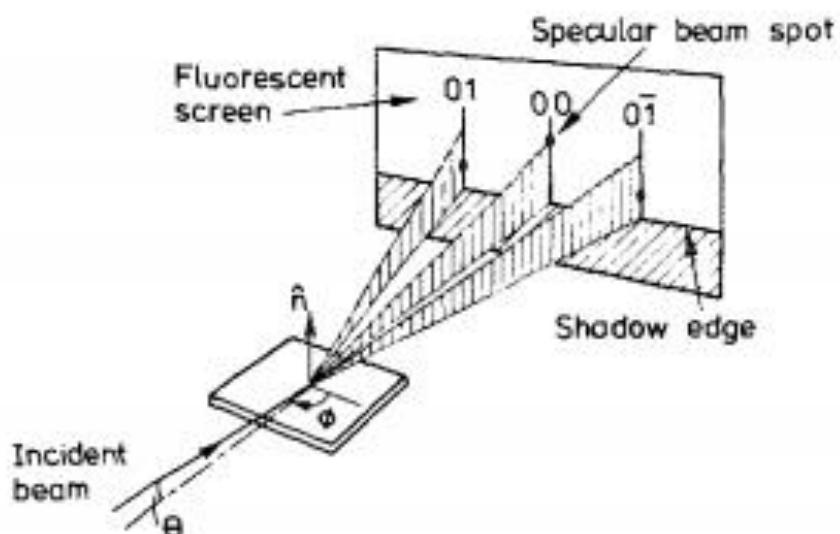


Figure 3.3: Schematic diagram of RHEED geometry showing the incident beam at an angle θ to the surface plane; azimuthal angle ϕ . The elongated spots indicate the intersection of the Ewald sphere with the 01 , 00 and $0\bar{1}$ rods [1]

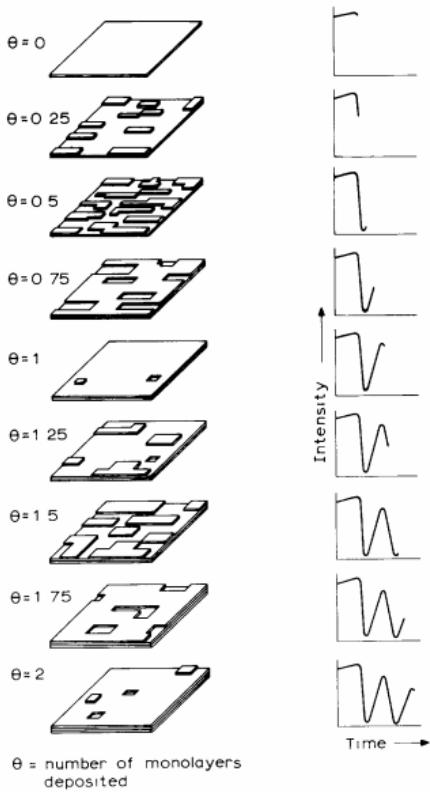


Figure 3.4: First order growth model (2 monolayers) in relation to the RHEED intensity behaviour [2].

3.3 Characterization of Semiconductor Thin Film

3.3.1 Atomic Force Microscopy

Atomic Force Microscopy (AFM) was employed to examine the surface morphology of samples. In AFM, a sharp probe is brought into proximity to sample surface. Probe subsequently moves in a raster pattern to obtain the surface morphology images. The AFM equipment involved in this work is the Bruker Dimension ICON SPM, which is shown in Figure 3.5, operating in advanced PeakForce Tapping mode, which is located in Electron Microscope Unit, Mark Wainwright Analytical Centre, UNSW. The PeakForce Tapping oscillation is performed at frequencies below the cantilever resonance, thus avoiding the filtering effect and dynamics of a resonating system. This mode has combined the benefits of contact mode and tapping mode that direct force control and avoidance of damaging lateral forces. The peakforce oscillation data was

extracted by the ScanAsyst system which decouples cantilever response from resonance dynamics, to automatically adjust the critical imaging parameters.

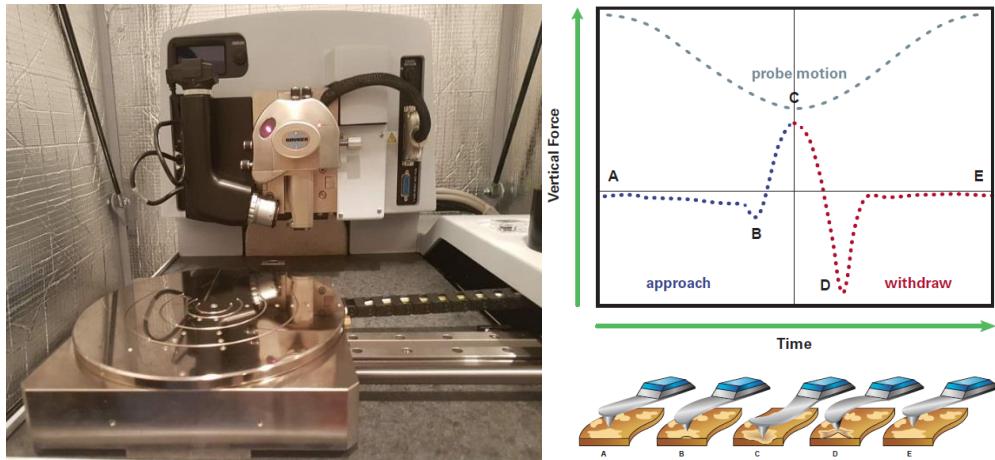


Figure 3.5: A photograph of the Bruker Dimension ICON SPM and the discipline of the peakforce tapping mode, where surface detail is collected by the oscillation of the cantilever [3].

After alignment and focus of sample surface by the CCD camera mounted on the equipment, the probe stage is lowered down to the sample surface. By adjusting the scanning size, scanning frequency and the peakforce energy level, high resolution images can be obtained from the AFM scan to reveal the surface morphology of samples. The AFM image below is one example of Si wafer scan. NanoScope Analysis software by Bruker can be employed to analyse the AFM image, where the surface roughness and other surface morphology can be obtained. The bright colour on the image indicate the tall region on the surface. In contrast, the darker colour on the image indicate the deep or vacancy region. Low surface roughness can be expected from a smooth surface. Detailed AFM image analysis will be addressed in Chapter 4 and 5.

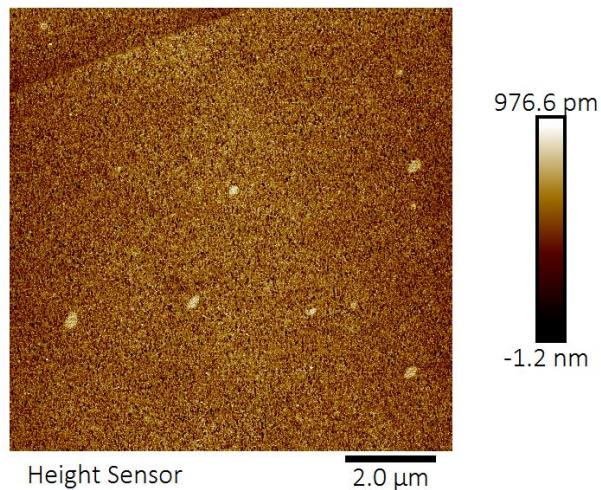


Figure 3.6: $10 \times 10 \mu\text{m}^2$ AFM scan of Si[100] 6° misoriented towards [110] plane.

3.3.2 X-ray Diffraction

X-ray Diffraction (XRD) is an essential technique for thin film structured analysis. X-rays are scattered by the electron distribution in a crystal. Diffraction of X-rays occurs when the scattered radiation is coherent, thus producing constructive interference at specific angles. When alignment is precisely controlled between X-ray and sample surface, various structure information can be obtained from the scanning curves, such as structural composition, crystal quality, film thickness, strain relaxation and dislocation density. Figure 3.7 illustrate the simplistic model of Bragg's Law which is the fundamental rule behind all XRD measurements.

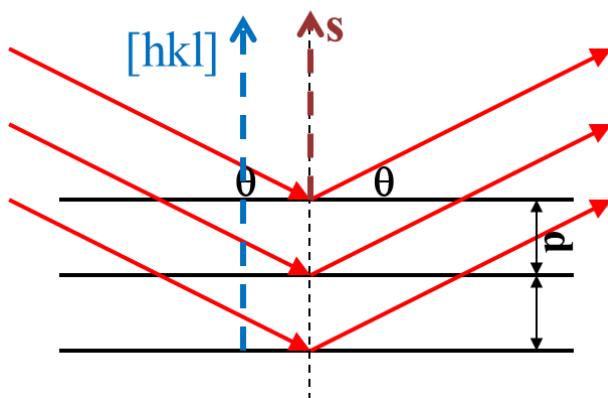


Figure 3.7: Bragg's law is a simplistic model

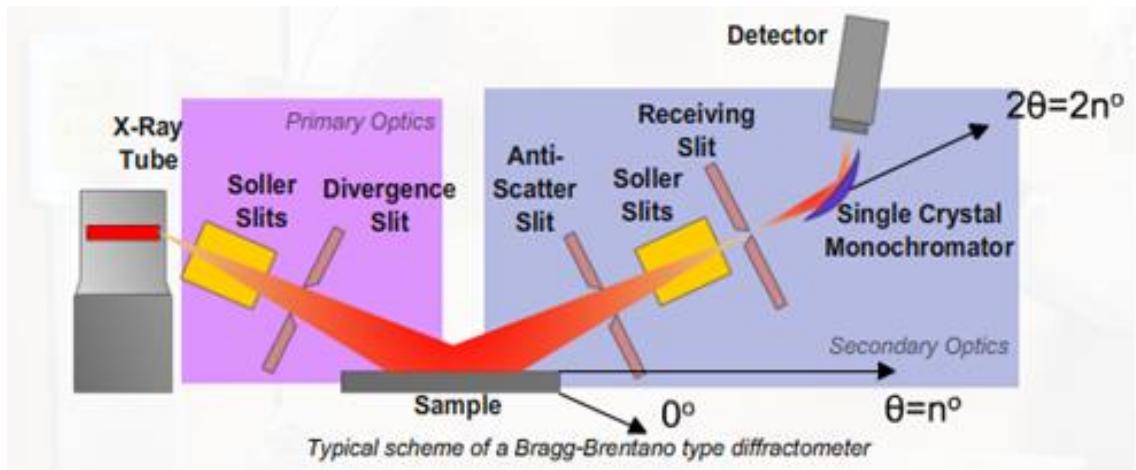
Bragg's Law can be expressed in the following equation:

$$n\lambda = 2ds\sin\theta \quad (1)$$

where n is the order of reflection, λ is the incident X-ray wavelength (normally $\lambda_{CuK\alpha} = 0.154 \text{ nm}$), d is the distance between lattice planes which can be written as

$$d = \frac{a}{\sqrt{h^2+k^2+l^2}} \quad (2)$$

where a is the lattice spacing, h , k and l are the Miller indices of the aligned Bragg plane, and θ is the X-ray incident angle, which is also called Bragg angle. Diffraction occurs when each atom in cubic lattice array scatters radiation coherently, producing concerted constructive interference at specific angles. Diffraction pattern is produced by the X-ray source with a wavelength magnitude similar to the d value of the substrate material incidents on different planes. The coherent scattering of atomic in the cubic lattice from the specific angle produces a strong peak in the diffraction curve, such strong peak is called the Bragg diffraction peak.



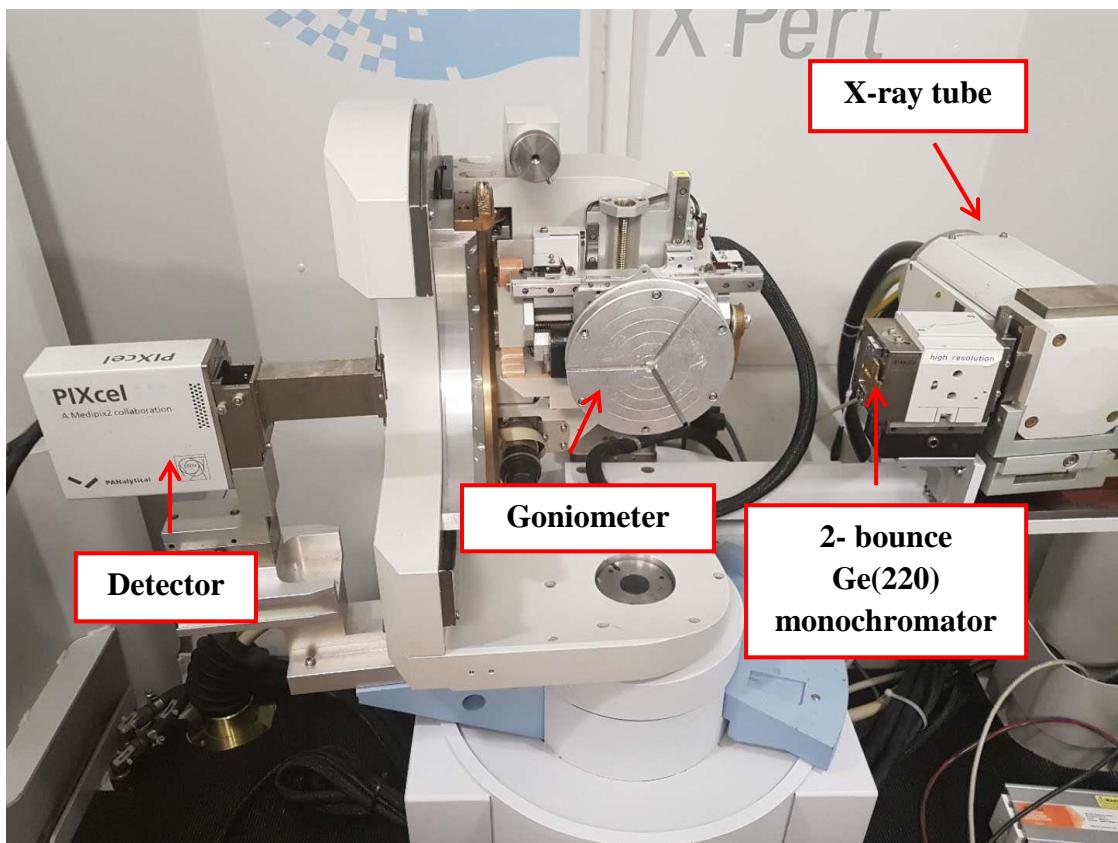


Figure 3.8: schematic diagram of a typical Bragg-Brentano type diffractometer for collecting omega-2 theta rocking curves [4] and photography of XRD equipment.

All XRD measurements in this work are taken by PANalytical Xpert Materials Research diffractometer (MRD) with the setting combination of high resolution module with the X-ray mirror and Ge (220) monochromator located in Solid State & Elemental Analysis Unit, Mark Wainwright Analytical Centre, UNSW. The schematic of a typical Bragg-Brentano type diffractometer with a photo illustrating the actual XRD equipment are shown in Figure 3.7. After the emission of X-ray from the X-ray tube, X-rays pass through a $\frac{1}{4}^\circ$ divergence slit, a Cu 0.2 attenuator before it enters the 2-bounce Ge (220) monochromators, then the beam will pass a 10mm wide mask to ensure that the X-ray will only irradiate the sample surface. Before the scattered beam enters high-resolution Pixel detector (1×10^{-4} degree) on the other side of the setting, in order to control the beam size to resulting in a high resolution scan, beam will pass through an anti-scattering slit of size 8mm and a 0.04 rad Soller slit. Attached to the sample goniometer,

the sample platform, which is located at the centre position of the instrumental setup, offers highly precise and reproducible movements for sample rotation, tilt, and x-, y- and z- translations, ensuring versatile and accurate sample positioning for the XRD measurements.

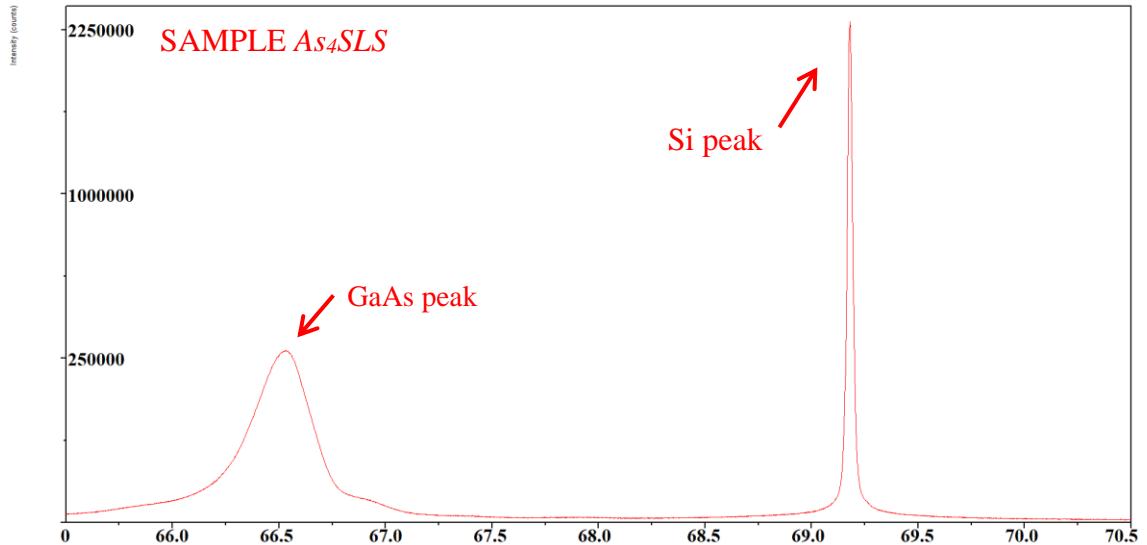


Figure 3.9 HRXRD $2\theta - Q$ scans of SAMPLE As4SLS

The plot above is one high resolution X-ray Diffraction (HRXRD) rocking curve of GaAs/Si structure with SLS DF. GaAs peak and Si peak are shown in the plot, where the position of Si peak is fixed by the reference $2\theta - Q$ position at 69.2° . The GaAs peak position is normally around 66.4° , however the peak position would shift due to macrostrain (i.e. lattice expansion or contraction) and the peak width would be symmetrically broadened due to mircostain (i.e. lattice distortion) which may be resulted from dislocations, defects or thermal effects. These are the guidelines for the structural analysis in Chapter 5.

3.3.3 Transmission Electron Microscopy

Although AFM can directly exam the sample surface morphology, it is not possible to gain the structural information from samples. Transmission electron microscopy (TEM) provided the possibility to observe dislocations and crystal defects inside the structure.

All TEM scans are obtained from the Philips CM200 field emission transmission electron microscope which is located in Electron Microscope Unit, Mark Wainwright Analytical Centre, UNSW. Philips CM200 allows high resolution images to be obtained from thin electron transparent materials. In the field emission gun, a strong electric field (200KV) is employed to extract electrons from a metal filament. This results in a high energy bright electron beam to project on the specimen. On the way through the specimen some parts of the material stop or deflect electrons more than other parts. The electrons are collected from below the sample onto a phosphorescent screen or through a CCD camera. In the regions where electrons do not pass through the sample the image is dark. Where electrons are not scattered, the image is brighter, and there are a range of greys in between depending on the way the electrons interact with and are scattered by the sample. The CM200 TEM allows structural, crystallographic and elemental studies of materials. This microscope has a Bruker QUANTAX energy dispersive x-ray spectroscopy system interfaced to it, which can allow elemental detection. In addition, it has a GATAN ORIUS camera for direct recording of digital images. Figure 3.8 is the layout of CM200 TEM.

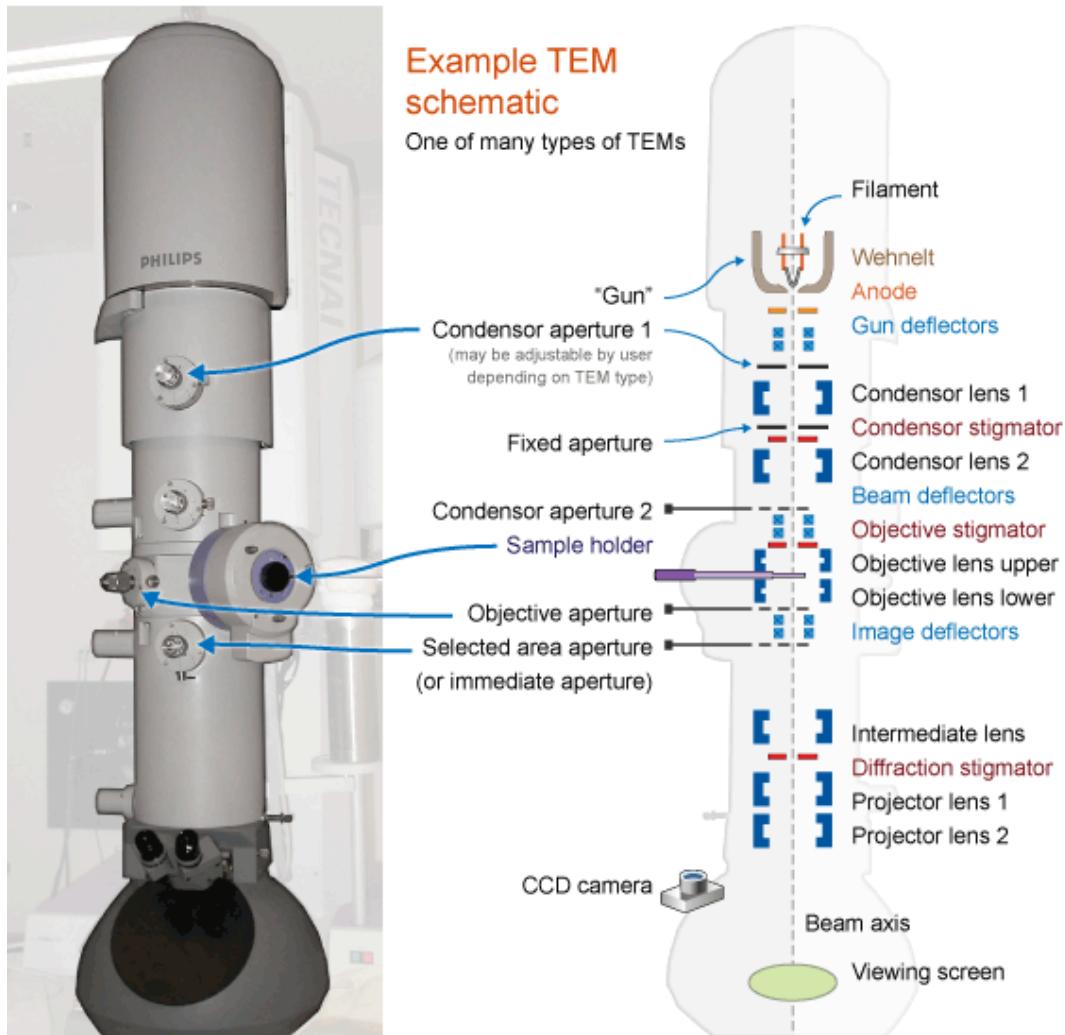


Figure 3.10: System layout of CM200 TEM equipment [5]

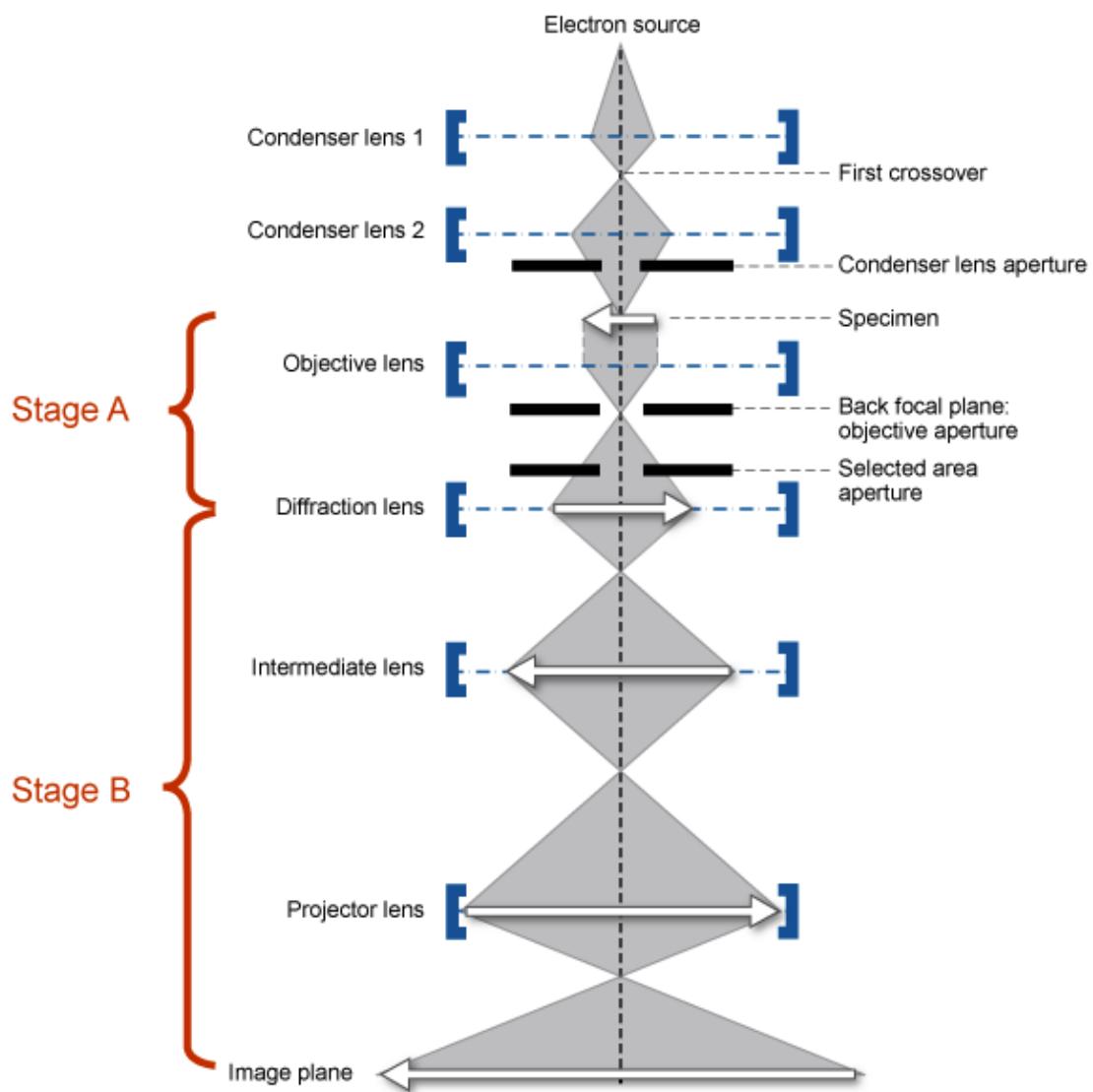


Figure 3.11: Image generation process in TEM system [6].

Figure 3.9 illustrates the image generation process of TEM system. Stage A is the scattering of an incident electron beam by a specimen. This radiation passes through an objective lens, which focuses it to form the primary image. Stage B takes this primary image and magnifies it with additional lenses to form a highly enlarged final image. In the process of forming the primary image the objective lens produces a diffraction pattern at its back focal plane. The diffraction pattern is a Fourier transform of the scattered electron wave. The primary image is the Fourier transform of the diffraction pattern [6].

A critical step in TEM characterization is sample preparation. All specimens are prepared by FEI Nova Nanolab 200, which is shown in Figure 3.10 with the schematic diagram, located in Electron Microscope Unit, Mark Wainwright Analytical Centre, UNSW. The specimen preparation includes gold coating, platinum (Pt) gas injection, gallium (Ga) ion beam milling and polishing. The epitaxial specimen must be milled down to less than 100nm to ensure electron transparency. Specimen quality affected by the preparation would consequently alter the characterization result. The software Gatan Digital Micrograph can be used during and after the measurement to inspect the structural properties, such as epitaxial layer thickness measurement and dislocation density calculation.

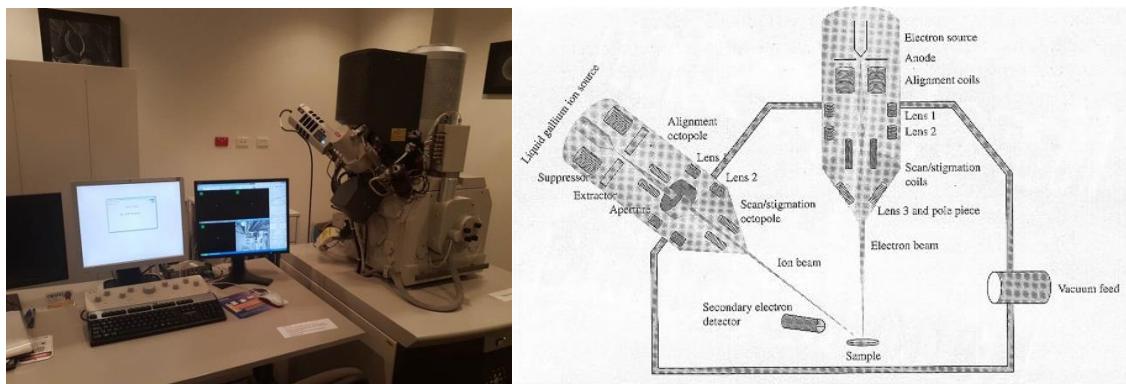


Figure 3.12: A FIB instrument showing the ion and electron columns and the specimen inside the vacuum chamber [7].

Reference:

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<https://www.asu.edu/clas/csss/NUE/FIB-Intro.html>

Chapter 4 GaAs Integration on Engineered Substrate

4.1 Introduction

As discussed in Chapter 2, one approach of reducing defects of III-V on Si substrate is employing an engineered surface. For Si, a typical approach is to use step graded SiGe towards high Ge content, which would be nearly lattice matched with GaAs layer to control the dislocation density in the grown GaAs. The focus of this work is to discuss and develop the suitable fabrication process of GaAs targeting virtual Ge (vGe), with the current objective to develop processes for a Ge substrate as a temporary template for the actual vGe engineered surface. The successful demonstration of GaAs epitaxy could lead to GaAs deposition on vGe substrate, fabricated by sputtering and anneal. In this chapter, several issues will be addressed and discussed such as the GaAs fabrication process towards anti-phase domain (APD) free deposition, and the aspects in the procedure that can be modified to improve the structural quality of the as-grown GaAs layer.

Table 4.1 below lists three sets of samples which were fabricated to investigate the three different aspects of the growth process impacting structural quality.

Table 4.1 Sample numbers and purpose of each sample patch

Sample Name	Difference and Variation in Samples	Purpose of Sample Patch
SAMPLE <i>Anneal</i>	650 °C annealing	The effect of annealing prior to the epitaxy
SAMPLE <i>NoAnneal</i>	No 650 °C annealing	
SAMPLE <i>As₂</i>	Apply As ₂ source	The effect of applying different As source in the fabrication process
SAMPLE <i>As₄</i>	Apply As ₄ source	

SAMPLE <i>AlAsMEE</i>	Apply AlAs MEE	The effect of employing different materials in the MEE process
SAMPLE <i>GaAsMEE</i>	Apply GaAs MEE	

4.2 GaAs deposition on Ge

4.2.1 Sample Preparation

Based on the as-grown surface morphology measured by AFM, the wet chemical cleaning method had been modified. Firstly, Ge substrate was cleaned by deionized water (DI) rinse to dissolve the native germanium oxide. After GaAs growth, sample was examined under AFM to verify the surface morphology. Figure 4.1 illustrates the surface morphology of GaAs grown on Ge sample with DI rinse. Only pin holes can be seen on the sample surface, which may due to surface contamination, which cannot be removed by DI rinse. Then, Acetone and Isopropyl alcohol (IPA) rinse were added to the cleaning process prior to the DI rinse. As shown in Figure 4.2, there are spots on the sample surface. Those spots are suspected to be a result of carbon contamination. Surface cleaning method was further improved by additional HCl and H₂O₂ treatment, and showed comparable results as shown in previous work [1]. In all, the wet chemical treatment employed in this work sufficiently removed the surface contamination.

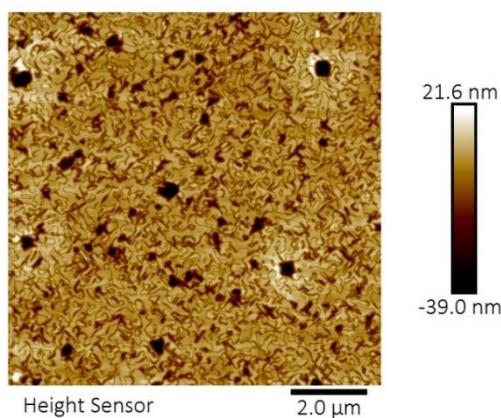


Figure 4.1: $10 \times 10 \mu\text{m}^2$ AFM images of GaAs/Ge sample with pin hole and cleavage feature on surface.

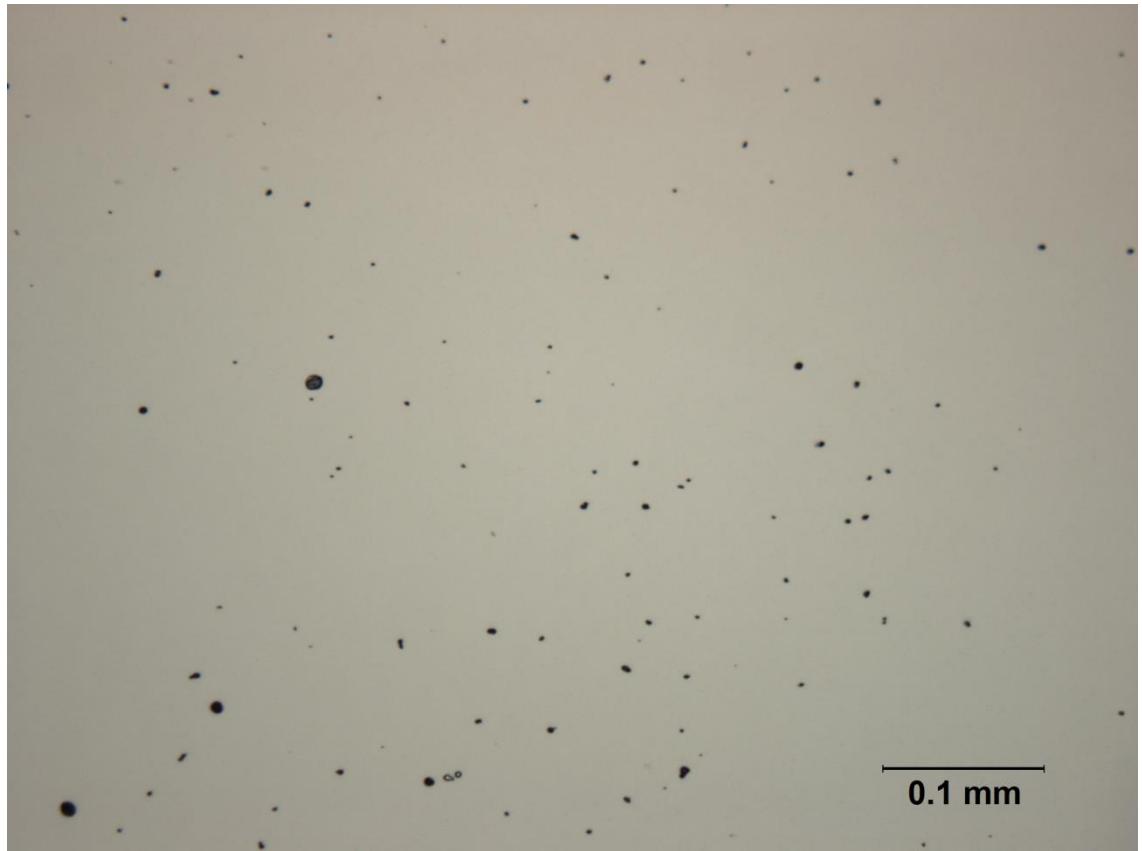


Figure 4.2: Optical microscope image of GaAs/Ge sample with spots on surface.

Ge substrates were cleaned by the wet chemical etch cleaning method elaborated above. When mounting the clean Ge wafer onto the wafer holder, one sapphire wafer was set to the back of Ge wafer serving a role of heat diffuser. Figure 4.3 illustrate the schematic diagram of the GaAs structure fabricated on Ge substrate, which was executed in this work. De-ox temperature of Ge substrate could be found at 380 °C as indicated by RHEED where the surface reconstruction pattern changed from hazy to streaky. To ensure the oxide was desorbed completely, the annealing temperature was raised 40 °C above the de-oxidation temperature after the RHEED pattern change was finished. Clear and sharp streaky RHEED pattern can be observed after 20 min, suggesting a completion of the de-oxidation process. As suggested by many research groups [2-8], a high temperature anneal for 15-20 min can provide a smoother surface for double atomic step offcut substrate. The temperature was set to be 650 °C and the anneal time

to be 20 min for SAMPLE *Anneal*. To compare how this anneal improves the surface morphology, the anneal process was removed from SAMPLE *NoAnneal* recipe while elsewhere remained the same. The growth process consists of three steps as follows: GaAs MEE (Migration Enhanced Epitaxy), low temperature (LT) GaAs growth and high temperature (HT) GaAs growth. During the MEE process, Ga and As source shutters were alternatively open with a 2 seconds pause in between. To ensure full monolayer coverage of III/V, the Ga growth rate was tuned to 0.1ML/sec by RHEED. The source shutter opening times are set to be 20 seconds and 10 seconds for As and Ga respectively. This cycle was repeated 25 times at 250 °C with a final As finishing shutter open for 20 seconds to provide an As rich surface for the later GaAs growth. GaAs growth was split into low temperature (LT) and high temperature (HT) steps, which were conducted at 500 °C and 600 °C for 1hr respectively. Meanwhile, the growth rate in these two steps was set to be 0.1 $\mu\text{m}/\text{hr}$ and 0.3 $\mu\text{m}/\text{hr}$ respectively.

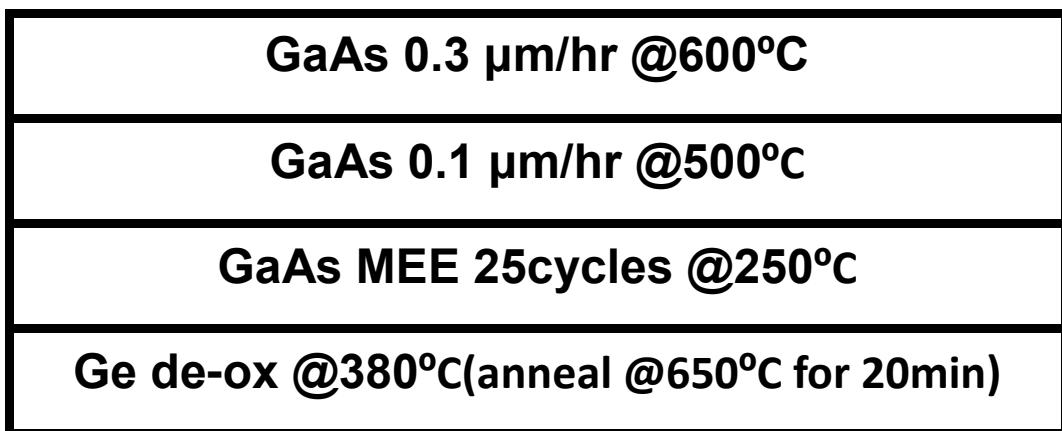


Figure 4.3: Schematic diagram of GaAs structure deposited on Ge

4.3 Experimental Procedure

4.3.1 Migration Enhanced Epitaxy

When epitaxy starts, the lateral migration of atoms along the substrate surface determines the atomic configuration and suppresses defects formation [2]. Many research groups demonstrated the technique using migration enhanced epitaxy (MEE) to

increase the lateral atoms migration length of the layer by layer deposition at low growth temperature to ensure the equilibrium atomic configuration [2-6]. Under such condition, MEE prevents the Ge outdiffusion and suppresses APD formation [2]. The key feature of MEE is the layer by layer deposition, which is achieved by alternate elemental source beams (Ga and As in this case) onto the substrate surface. Between Ga and As depositions, a short time interruption is required to allow the supplied atoms to migrate along the substrate surface to form a full monolayer coverage of this element on the substrate before bonding occurs. This layer by layer growth method affects the relaxation mechanism of the layer GaAs epitaxy.

The source shutter opening times are set to be 10-sec and 20-sec for Ga and As respectively with As overpressure of 3×10^{-7} Torr. The growth interruption is achieved by keeping both Ga and As shutters closed for 2-sec. The purpose of this growth pause is to enhance the migration of supplied Ga and As on the substrate surface. This layer by layer deposition was performed for 25 cycles, corresponding to 25ML GaAs growth. Many research groups performed GaAs MEE deposition with various growth temperatures [2-5] which play a significant role in the MEE process. AFM scans were performed to investigate the surface morphology after the MEE process [3]. MEE substrate temperatures were set to be 250 °C, 350 °C and 450 °C for three samples respectively, while the other growth conditions including growth rate, interruption time and deposition cycles remained the same. RMS values extracted from $10 \times 10 \mu\text{m}^2$ AFM scans of all samples. With a lower MEE substrate temperature, the RMS value is relatively low. The surface roughness of the sample whose MEE temperature is 250 °C is one order less than the sample whose MEE temperature is 450°C [3]. At high growth temperature, As dimers could evaporate from the initiation layer leaving As vacancies on the surface in such process. When Ga shutter opens in this situation, the arrival Ga

atoms occupy the As vacancies, generating APDs or acting as nucleation sites for GaAs islands which become the origins of defects [3]. Therefore, the growth temperature of MEE in this work is set to be 250 °C.

The RHEED pattern changed from (2 × 1) double atomic steps pattern to a (2 × 4) pattern right after the first several cycles of the MEE process and the pattern became brighter and sharper when the MEE process is finished. This streaky and sharp (2 × 4) pattern indicates the successful formation of layer-by-layer GaAs epitaxial layer serving a role of the buffer layer for later normal GaAs growth. After 25 cycles of GaAs MEE deposition, As source shutter was left open for another 20 seconds to ensure an As-rich surface for later GaAs growth.

4.3.2 GaAs epitaxy

The GaAs epitaxy after MEE process can be divided into two steps. The one is low temperature slow growth conducted at 500 °C with a growth rate of 0.1 $\mu m/hr$, the second step is high temperature fast growth conducted at 600 °C with growth rate of 0.3 $\mu m/hr$. It has been shown that the 600 °C growth temperature would lead to a smooth surface, the RMS values from AFM scans exhibited a decrease trend with an increment of growth temperature from 520 °C to 600 °C [9]. Each step lasts for one hour respectively, therefore the entire structure consists of 400 nm GaAs and 7 nm (25 monolayers) MEE GaAs.

4.4 Results and Discussion

4.4.1 Effect of annealing prior to growth

As mentioned in the previous section, the double atomic stepped surface can be obtained by high temperature anneal. In this section, the annealing temperature, annealing time length and how the annealing would improve the as-grown surface morphology will be discussed.

After mounting the substrate onto the growth stage inside the MBE growth chamber, the high temperature anneal is achieved by setting the substrate temperature to the desired value and keeping the substrate at this temperature annealing for 20 min. After the annealing was finished, the substrate temperature was ramped down to the growth temperature of MEE.

After removal from the chamber, AFM surface scans were performed with AFM surface RMS value are listed in Figure 4.5 and Table 4.1. It is evident that with an increment of annealing temperature, the RMS values decrease substantially [10]. This fits well to the mechanism mentioned above. At high temperature, the Ga atoms gain higher thermal energy allowing the atoms to diffuse from energetically unfavorable steps (i.e. non-double atomic steps) to the favorable ones (i.e. double atomic steps). At this point, the annealing temperature was set to 650 °C which are widely adopted in many studies [5-9, 12].

Figure 4.4 shows the SEM scans of as-grown GaAs/Ge sample. The grey spots most likely due to surface contamination. Based on the AFM results and SEM scans, the carbon contamination cannot be removed through high temperature anneal process. Besides the reason of surface contamination resulting in the cleavage feature, another source of the cleavage feature can be traced back to the initiation layer stage. Previous studies have compared between employing Ga initiation layer and As initiation layer for GaAs deposition [12]. Even though the APDs free surface can be obtained by employing either Ga or As initiation layer at high temperature (500 °C), APD can be observed when employing As initiation layer at low temperature (350 °C) [12]. Since the GaAs MEE involved in this work was initiated at 250 °C which is much lower than the studied temperature, it can be inferred that the surface feature is not only contributed by

the surface contamination but also resulted from the APD formation during the initiation layer deposition. This indicates the undesired surface morphologies illustrated by AFM images in this work are contributed by the As initiation layer. However, as mentioned in Chapter 2, smooth sample surface can be obtained by employing As initiation layer, the elaborated comparison between employing both initiation layer can be investigated in future work.

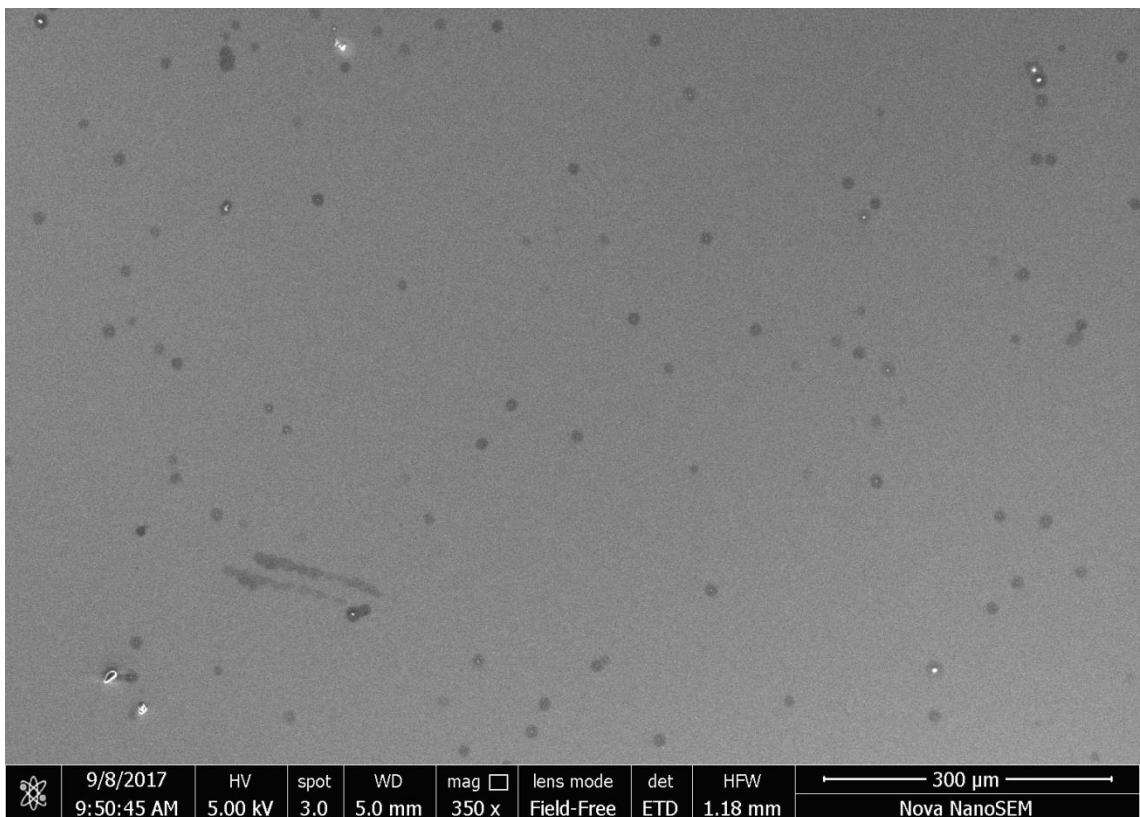


Figure 4.4: SEM scan of as-grown GaAs/Ge sample with spots on the sample surface. The spots are the results of carbon contamination which cannot be removed in the sample cleaning process or high temperature anneal.

There was one difference in the epitaxy procedures between SAMPLE Anneal and SAMPLE NoAnneal, where SAMPLE Anneal was annealed at 650 °C prior to MEE step but SAMPLE NoAnneal initiated the deposition right after the de-ox of the substrate is finished. Despite the appearance of the pinholes, SAMPLE Anneal exhibits less pinhole on both scans, which suggest a smoother surface compared to SAMPLE NoAnneal

AFM scans. The RMS values reveal the surface roughness of both samples. As listed in the table below, the RMS values (R_q) of SAMPLE Anneal are 7.99 nm (Figure 4.5.a) and 7.32 nm (Figure 4.5.b), which are less than the R_q of SAMPLE NoAnneal scans with values of 8.05 nm (Figure 4.5.c) and 7.53 nm (Figure 4.5.d). By selecting a non-pinhole $2 \times 2 \mu\text{m}^2$ region, as shown in Figure 4.6 and Table 4.2, RMS can be found to be reduced dramatically, which conclude that pinholes are dominating the RMS value. These data suggest that the high temperature anneal prior to the initiation can improve the substrate morphology by forming double atomic steps which is favourable for later GaAs epitaxy.

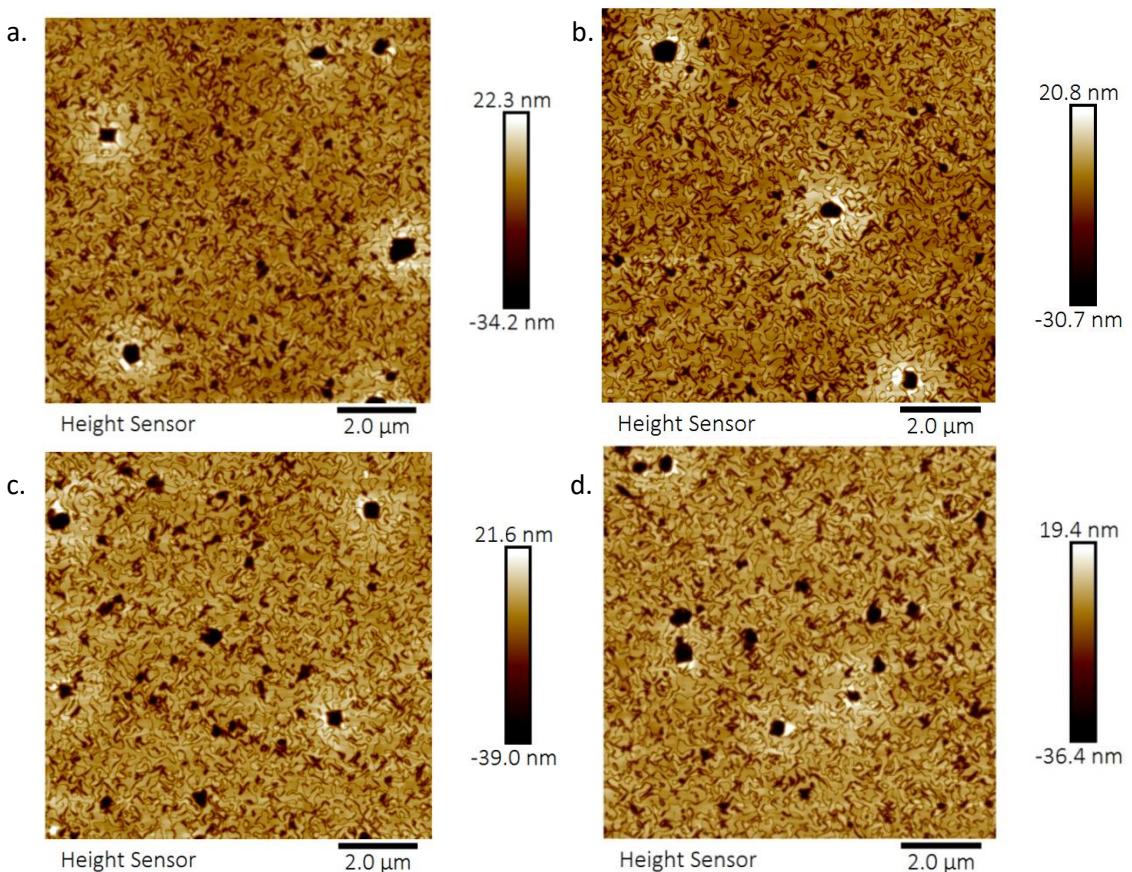


Figure 4.5: $10 \times 10 \mu\text{m}^2$ AFM scans of SAMPLE Anneal and SAMPLE NoAnneal. The appearance of pinhole is due to the carbon surface contamination. The RMS values are dominated by the pinhole distribution.

Table 4.1: surface roughness comparison of two different $10 \times 10 \mu\text{m}^2$ regions with pinholes distributed on sample surface with different pinhole densities.

	Figure 4.5.a/c.		Figure 4.5.b/d.	
	Ra(nm)	Rq(nm)	Ra(nm)	Rq(nm)
SAMPLE Anneal	5.38	7.99	5.16	7.32
SAMPLE NoAnneal	5.70	8.05	5.43	7.53

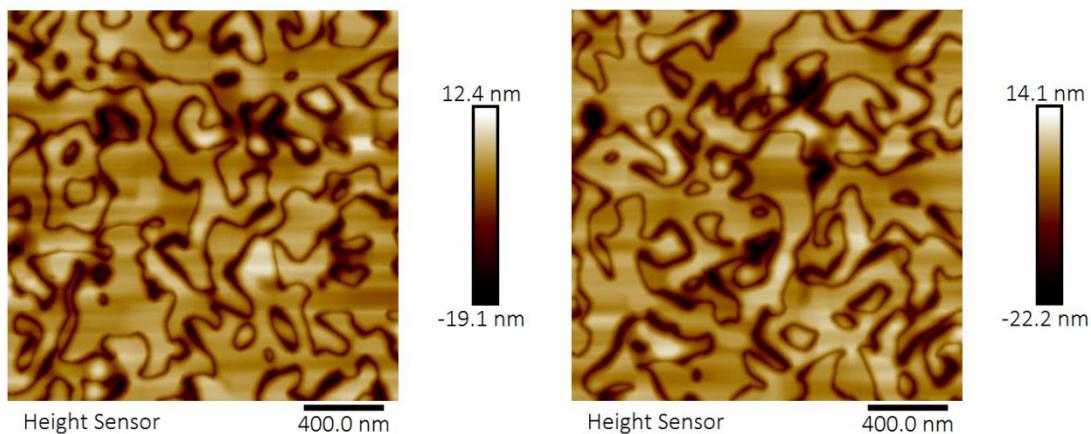


Figure 4.6: AFM images of Selected $2 \times 2 \mu\text{m}^2$ non-pinhole regions of both SAMPLE ANNEAL(left) and SAMPLE NoAnneal(right) sample

Table 4.2: Roughness comparison of the selected regions.

	Ra(nm)	Rq(nm)
SAMPLE Anneal	3.70	4.63
SAMPLE NoAnneal	4.26	5.33

4.4.2 Effect of employing different As source

The effect of employing different As source was investigated. Since the tetrameric As₄ (650°C cracker temperature) contains less thermal energy than dimer As₂ (950°C cracker temperature), epitaxy involved As₄ is expected to finish with different surface morphology to As₂. SAMPLE As₄ employed As₄ as As source while As₂ was applied for

SAMPLE As_2 . This set of samples shared the exact same recipe elaborated in Section 4.2. After removal from MBE system, AFM was employed to exam the surface morphology of these samples.

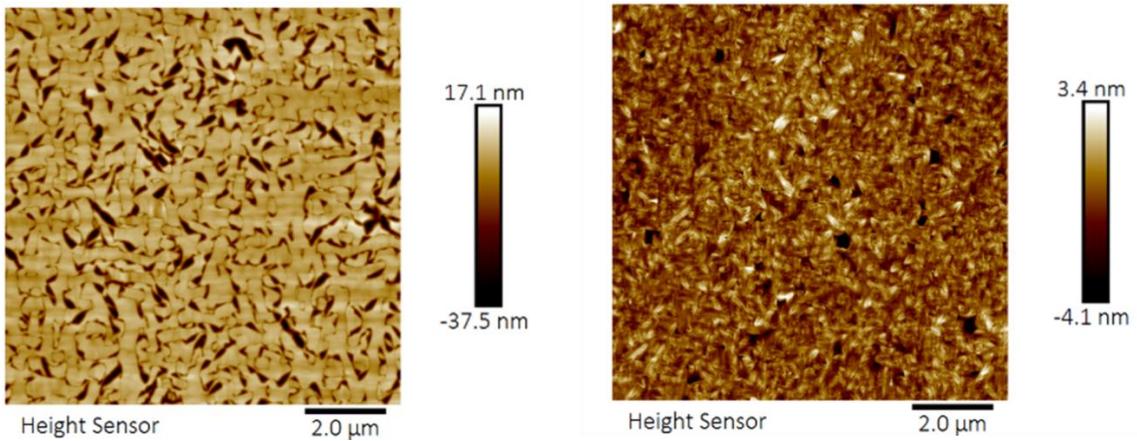


Figure 4.7: AFM scan of GaAs epitaxy on Ge with As_2 (left) and As_4 (right) respectively.

Table 4.3: Surface roughness of SAMPLE As_2 and SAMPLE As_4 .

	10um		2um	
	Ra(nm)	Rq(nm)	Ra(nm)	Rq(nm)
SAMPLE As_2	5.24	7.49	4.00	6.00
SAMPLE As_4	0.717	1.04	0.588	0.773

Figure 4.7 and Table 4.3 above show the $10 \times 10 \mu m^2$ AFM scan results and RMS values of $10 \times 10 \mu m^2$ and a $2 \times 2 \mu m^2$ selected region avoiding cleavage gaps. As can be seen from the table, SAMPLE As_4 has a significantly lower Rq value when compared to SAMPLE As_2 . This data suggest that As_4 can dramatically lower the RMS compared to As_2 , which is in agreement with another study [11]. However, as we can see from the AFM images, surface defects are still can be observed. SAMPLE As_2 shows a pattern

with cleavages on the surface, and SAMPLE As₄ exhibits pinholes. These may due to surface contamination and the difference between annealing time prior MEE growth. This is most likely due to As₄ having lower thermal energy when hitting surface.

4.4.3 AlAs MEE as nucleation layer

One other aspect worth investigating is whether other MEE material can improve the structural quality of the GaAs epitaxy. One candidate for MEE is AlAs, since the migration of Al is less than Ga under the same epitaxy circumstance [12], which provides a lower possibility of the formation of group III nucleation during the layer by layer deposition process. The other advantage corresponds to this Al property is as if the substrate is rough during the fabrication process, AlAs MEE may flatten the surface before GaAs epitaxy.

For instance, the cross section TEM images in Figure 4.8 were taken from one unmodified recipe initiating with GaAs MEE was applied on sputtered virtual Ge substrate. During the de-oxidation process, RHEED pattern was very spotty which indicates a relatively rough substrate surface. As shown in the bright field images, clear undulation surface can be observed. Despite the generation and propagation of threading dislocations, one assumption can be made that the rough surface dominated the undulation of the as-grown surface. Therefore, with a lower migration length, Al was adapted to help reduce the sample surface undulation when the substrate surface was rough. When taking lattice mismatch issue into consideration, the mismatch between AlAs ($a_0 = 0.5661$ nm) and GaAs ($a_0 = 0.5653$ nm) is quite small and negligible, which should not introduce a new lattice mismatch impact into the epitaxial process. Epitaxy initiated with AlAs MEE has also been adapted in strained layer superlattice dislocation filter fabrication [14], which will be discussed in Chapter 5.

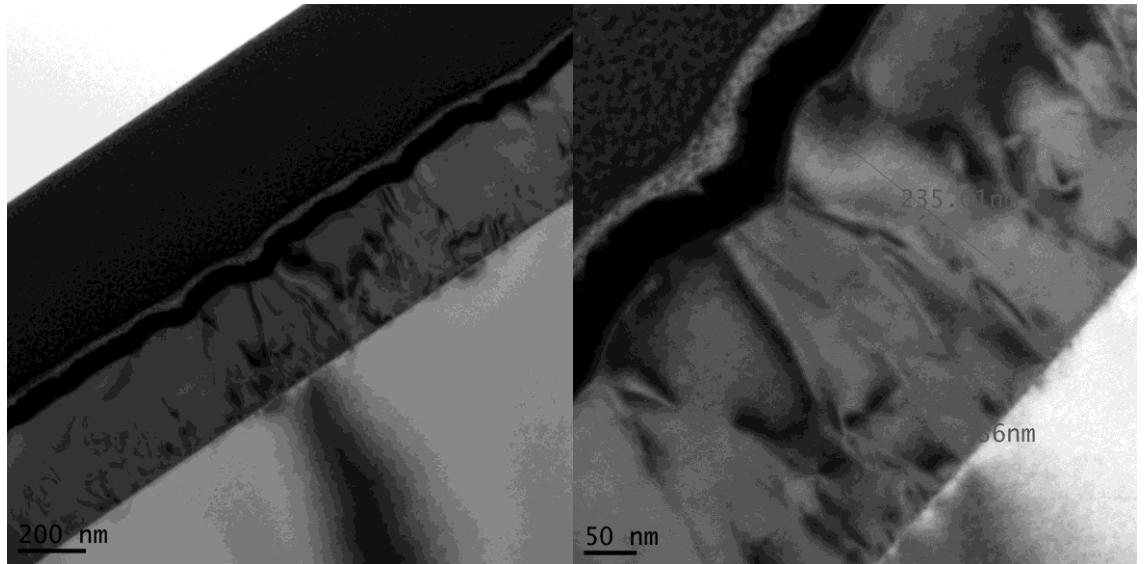


Figure 4.8: Cross section bright field TEM images of GaAs on vGe.

To investigate how AlAs MEE would affect the structure of GaAs, SAMPLE *AlAsMEE* was fabricated with AlAs MEE and SAMPLE *GaAsMEE* was fabricated with the same recipe elaborated as in Section 4.2. Al growth rate was tuned by RHEED prior to growth, to eliminate other potential variations; the growth rate was set to 0.1 ML/sec which is same as the Ga growth rate. Besides the employment of different group III source, all other parameters were remained unchanged to utilize a comparison with SAMPLE *GaAsMEE*. The following AFM scans reveal the surface morphology of these set of samples.

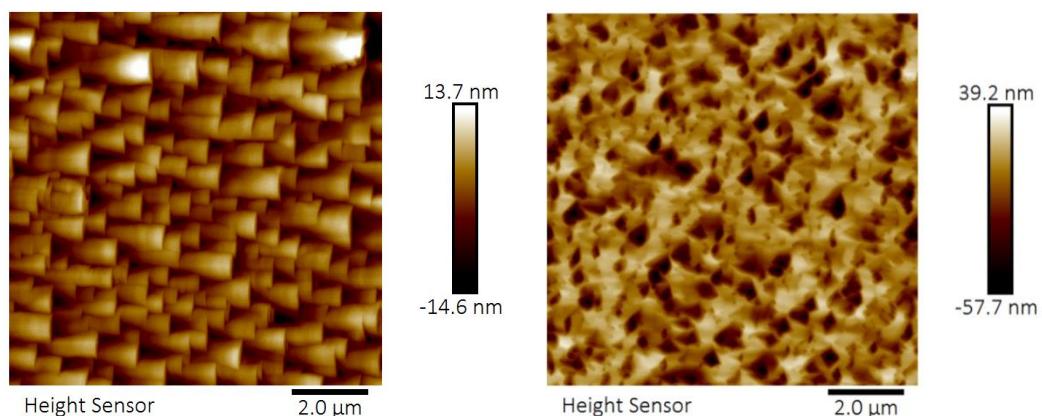


Figure 4.9: $10 \times 10 \mu\text{m}^2$ AFM images of SAMPLE GaAsMEE (left) and SAMPLE AlAsMEE (right).

The AFM of SAMPLE *GaAsMEE* in Figure 4.9 exhibits a “scale-like” feature on the surface while SAMPLE *AlAsMEE* shows a similar surface morphology like previous GaAs on Ge structures where pinholes dominate surface roughness. In the case of initiate with AlAs MEE, the surface contains evenly distributed humps rather than scale-shaped feature with uneven heights and sizes when compared with SAMPLE *GaAsMEE* as shown in Figure 4.10. Both samples in the *GaAsMEE* growth patch showcased this “scale-like” feature, which may be a result of carbon contamination during the wet chemical cleaning process. As discussed in Section 4.4.1, this feature might be a result of using group V element as the initiation layer, where APD would form thereby affect the surface morphology of the sample.

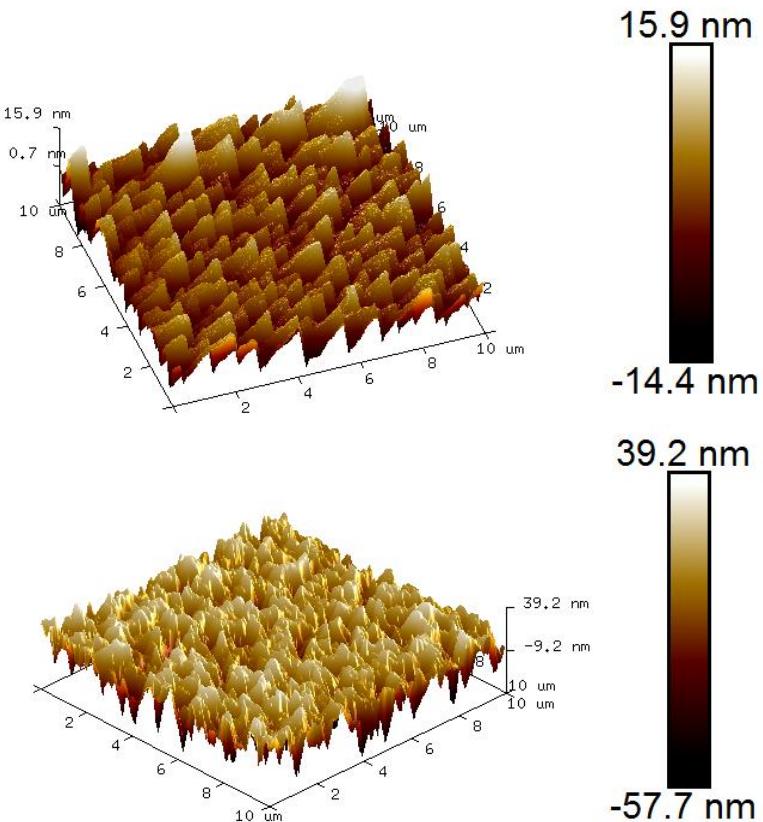


Figure 4.10: 3D view of $10 \times 10 \mu\text{m}^2$ AFM scans of SAMPLE *GaAsMEE* (top) and SAMPLE *AlAsMEE* (bottom).

As mentioned in the previous section, due to the lack of migration for Al, the structure initiated with AlAs MEE has low possibility to form droplets on the substrate surface. Samples were prepared out for TEM scans to exam whether the surface morphology was corresponding to the structural faults.

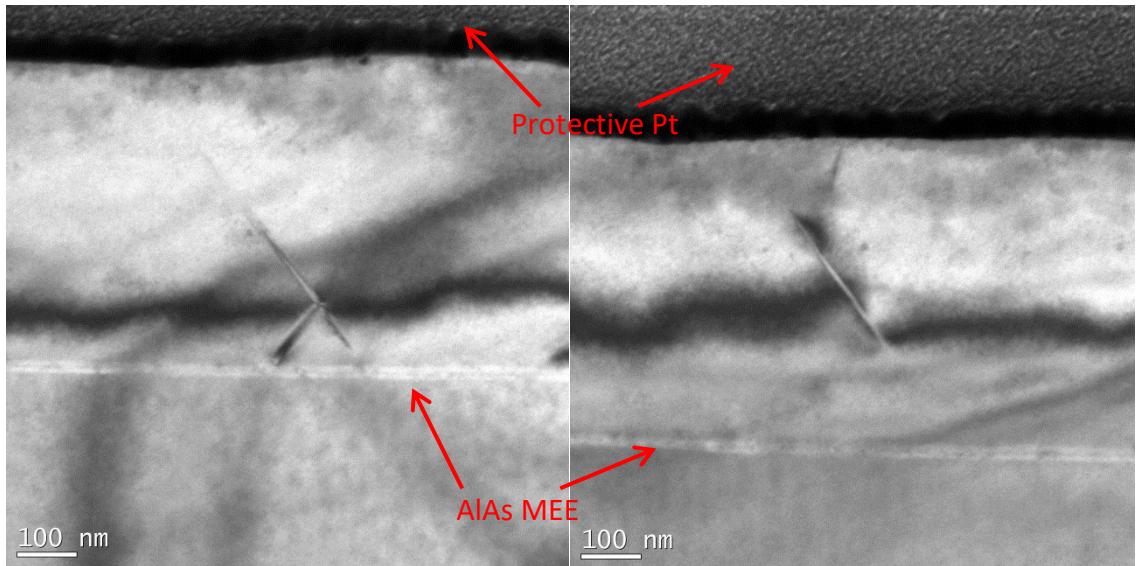


Figure 4.11: Cross section TEM images of SAMPLE AlAsMEE with plane defects shown as strokes propagating towards sample surface.

Figure 4.11 reveals the structural view of SAMPLE AlAsMEE. As shown in the TEM images, the undulation of sample surface can be easily spotted right under the protective Pt layer. Whereas, when taking SAMPLE AlAsMEE and previous GaAs/vGe TEM images into consideration, the sample surface undulation is greatly reduced in SAMPLE AlAsMEE, which indicating the AlAs MEE could help flatten the substrate surface when the substrate is rough. Meanwhile, clear features emerging from the interface between AlAs and GaAs which can be characterized as extended defects resulting from the contaminated surface. As explained in the previous section, carbon contamination contributes to the formation of pinholes on the sample surface. TEM scans offer a direct and clear view of how the substrate contamination will lead to structural defects which can be a result of undulating surface.

Figure 4.12 illustrates the cross section view of SAMPLE *GaAsMEE* sample. Since the MEE material is GaAs, there is no clear distinction between MEE layer and GaAs layer as indicated in SAMPLE *AlAsMEE* sample case. Visually, no extended defects emerging from the interface can be spotted due to the lattice constant mismatches between GaAs, AlAs and Ge being negligible. Unlike the SAMPLE *AlAsMEE* sample, there is no extended defect throughout the TEM images of SAMPLE *GaAsMEE* sample. Since the plane defects are mainly contributed by the surface contamination, it is likely that the SAMPLE *GaAsMEE* sample surface contains less amount of carbon residual than SAMPLE *AlAsMEE*.

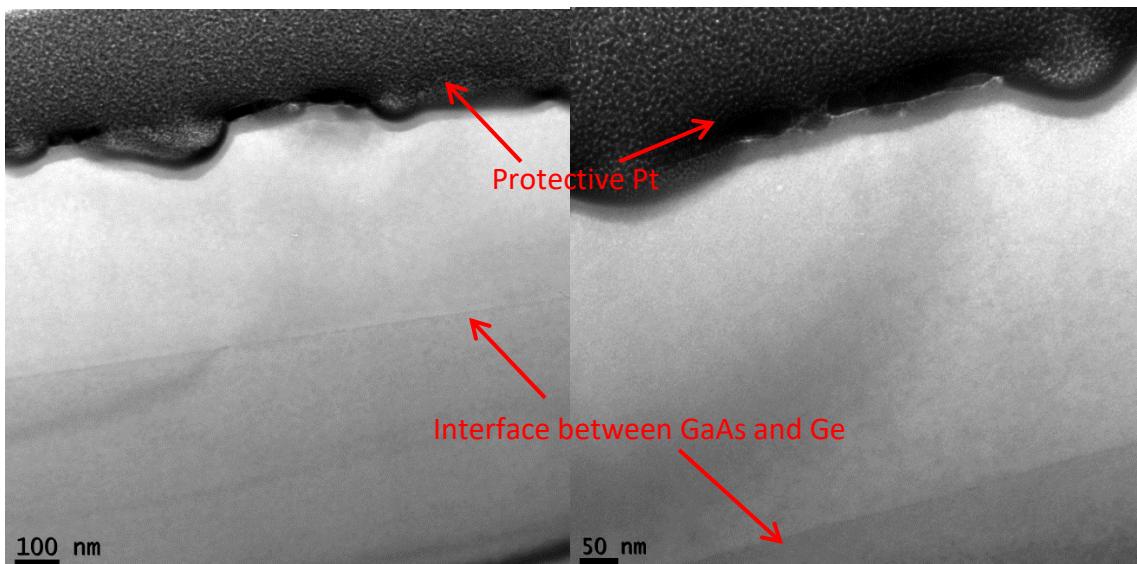


Figure 4.12: Cross section TEM images of SAMPLE GaAsMEE sample.

4.5 Conclusion

In summary, several fundamental issues regarding how to enhance the structural quality of GaAs epitaxy on offcut Ge substrate have been discussed. The formation of double atomic steps and how this configuration would improve the quality of GaAs deposition has been demonstrated by comparing the effect of high temperature anneal prior to initiation of epitaxy. The importance of the start of epitaxy with MEE and how different MEE material would affect the structural quality have also been discussed. If group V

material with less thermal energy (i.e. As₄) would improve the surface morphology has been investigated by comparing the RMS value based on AFM scans. After characterized by various characterization technique, the quality of GaAs epitaxy on offcut Ge substrate can be improved by a combination of employing high temperature anneal prior to growth, initiating the MEE at low temperature with group V material, applying group V material with low thermal energy throughout the entire epitaxy process and use alternative MEE material to flatten the rough substrate surface when needed.

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Chapter 5 Fabrication of Strained Layer Superlattice Dislocation Filter

5.1 Introduction

As addressed in Chapter 2, the other approach to achieve high quality epitaxial GaAs layer on Si substrate is employing Strained Layer Superlattice Dislocation Filter (SLS DF) to reduce the dislocation density to a tolerable range. As mentioned in Chapter 1, Si substrate in this work would serve the role of mechanical template rather than being active cell. Initially, the design elaborated in this chapter will not take optical effects into consideration. It has been successfully demonstrated that SLS DF can effectively suppress the propagation of threading dislocations [1]. High quality epitaxial GaAs layer can be successfully grown on top of the SLS DF layers. By noting the driving force of dislocation motion and comparing the structural properties among different materials, an alternative material could be selected to improve the performance of the SLS DF. In this chapter, the fabrication details of SLS are addressed for the candidate material, followed by a discussion of the structural properties and performance. The supporting characterization tools are AFM, XRD and TEM.

The table below list three groups, with differing number of samples. Each group has a different aspect that affects the epitaxy process.

Table 5.1 Sample numbers and purpose of each sample patch

Sample Name	Difference and Variation in Samples	Purpose of Sample Patch
SAMPLE InAlAs	InAlAs SLS DF	The effect of thermal expansion coefficient mismatch
SAMPLE GaAsSb	GaAsSb SLS DF	
SAMPLE As ₄ SLS	Apply As ₄ source in SLS	The effect of applying different As source in the fabrication process
SAMPLE As ₂ SLS	Apply As ₂ source in	

	SLS	
SAMPLE <i>GaAsSb(As₂)</i>	GaAsSb SLS with As ₂ source	The effect of applying innovative SLS material

5.2 Selection of Candidate Material

As discussed earlier, threading dislocations motion in different materials is strongly related to the material structural properties. Besides the structural preference in dislocation motion, the dislocation motion can be affected by various factors. In this section, two major factors will be discussed to reveal how to select suitable superlattice material for SLS DFLs. Dislocation motion velocity in a semiconductor system can be quantitatively expressed as a function of the stress τ and the temperature T when the crystals are ductile and T is not close to melting temperature [2]:

$$v = v_0(\tau/\tau_0)^m \exp(-Q/k_B T) \quad (1)$$

where v_0 , m and Q are experimentally determined values for dislocation in semiconductors, k_B is the Boltzmann constant (8.617×10^{-5} eV/K) and $\tau_0 = 1$ MPa. Dislocations motion needs a certain energy to break the bond between two atoms to initiate the gliding process [2]. This energy level is noted as activation energy (Q in Equation 5.1). The table below illustrates magnitudes of v_0 , m and Q in different semiconductor materials.

Table 5.1: Magnitudes of material properties regarding threading dislocation motion in various semiconductors [2,3]

	60°, α dislocation		
	v_0 (m/s)	m	Q (eV)
Si	1.0×10^4	1.0	2.30
Ge	2.9×10^2	1.7	1.62

GaP	2.1×10^2	1.3	1.45
GaAs	1.9×10^3	1.7	1.30
InP	4.0×10^4	1.6	1.60
InAs	5.6×10^4	1.7	1.40

To investigate the threading dislocation motion in different materials, variables parameters can be limited by fixing τ and T to a constant, which provides the same stress and temperature to the semiconductors above. For the III-V compound materials listed in Table 5.1, the dislocations move faster in In-V semiconductors than Ga-V semiconductors, while dislocation moves slower in III-P semiconductor than III-As semiconductors. From another perspective, the materials that allow dislocation to move faster have low dislocation motion activation energy. The relation between experimentally determined dislocation activation energy and band gap energy of various semiconductors are shown in Figure 5.1.

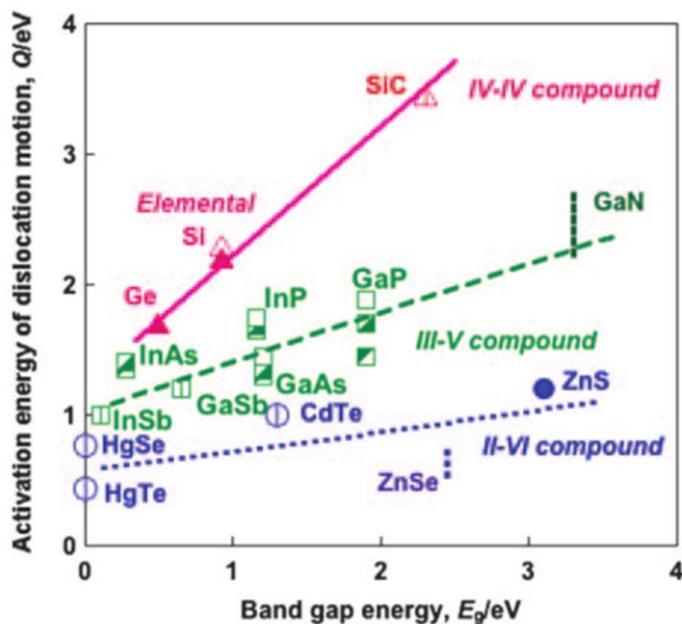


Figure 5.1: Relation between dislocation motion activation energy and band gap energy of different semiconductor compound [2].

The activation energy Q shares a linearly increasing relation with band gap energy in each group of semiconductors. The band gap increases with energy of interatomic bonding, such that the dislocation requires more energy to initiate the bond breaking process to allow the motion to take place [4]. The gradient of the line increases in the order of II-VI, III-V compounds and elemental Group IV semiconductors. This may be related to the fact that bonding in II-VI and III-V compound semiconductors has stronger iconicity compared to group IV compound [2]. In Figure 5.1, it is worth pointing out that a few materials like group IV and nitride compound are not quite suitable for SLS structure. As discussed in Chapter 2, the combination and re-emission mechanism is unlikely to happen even though it is energetically favorable in the hexagonal system (i.e. GaN) [5]. Besides this, the band gap of GaN in the plot presents a great barrier to the dislocation motion. As can be seen from the plot, Q of GaN is much higher than other III-V compounds, which could be problematic during the fabrication process where the energy is gained from annealing such that the structure would face the threat of reaching the melting temperature. Therefore, GaN is not recommended as the candidate for dislocation filter in the perspective of both lattice structure and active energy of dislocation motion. The same condition applies to the group IV material. Taking GeSn for example, although GeSn is attractive due to its property of direct band with low Sn content (~6-8 %), GeSn offers no major variation regarding both band gap energy and lattice constant to Ge due to the low Sn content. Recent research provided various approaches on how to obtain energy band gap for given Sn content [6-9]. Taking $\text{Ge}_{0.875}\text{Sn}_{0.125}$ for example, the band gap energy is about 0.55 eV which is close to the band gap energy of Ge (0.66 eV) resulting in activation energy Q to be 1.46 eV which is lower than Ge (1.62 eV) but close to GaAs (1.45 eV) according to Table 5.1. To reach this level of Q the anneal temperature would be higher

than the normal deposition temperature of GeSn (around 250-300 °C), which is attributed to low melting point of Sn (291.3 °C) [7], which is hardly achievable during the fabrication process. From this point, it becomes quite clear that employing group IV material to fabricate SLS has a few drawbacks. Firstly, the lattice constant of GeSn compound is very close to that of Ge which means very little strain formation during the SLS deposition. Secondly, GeSn will start to deform before the gained energy reaches the required Q level, which would be problematic during fabrication. From Figure 5.1, II-VI compounds can offer the lowest Q implying more suitable candidate materials. Unfortunately, the MBE involved in this work contains neither Group II nor Group VI material. Therefore, the material selection range must be narrowed down to III-V compound in this work. The investigation of II-VI material as SLS material can be conducted in future work. Nonetheless, for semiconductor material with low band gap energy, the activation energy Q is relatively low. This relation offers a direct conceptual conversion from activation energy Q to band gap energy E_g in Equation 5.1.

The other variable in Equation 5.1 is τ . Figure 5.2 shows how stress would affect the dislocation reduction ability of SLS. When taking a side-by-side performance comparison between InGaAs/GaAs SLS and InAlAs/GaAs SLS [10], it can be noticed that although the performance of both SLS cannot differ from each other before the second stack of the superlattice, visually, the amount of threading dislocation entering and propagating towards the sample surface in Figure 5.2 (b) is less than that in Figure 5.2 (a). Theoretically, the misfit in the SLS structure is the same, but due to different shear modulus and Poisson's ratio, the stress within different SLS layers is different. With the larger shear modulus of InAlAs, it is expected that the force in the strain field is larger than that in InGaAs/GaAs SLS structure. Therefore, material with larger shear

modulus in SLS structure can manipulate the threading dislocation propagation more effectively.

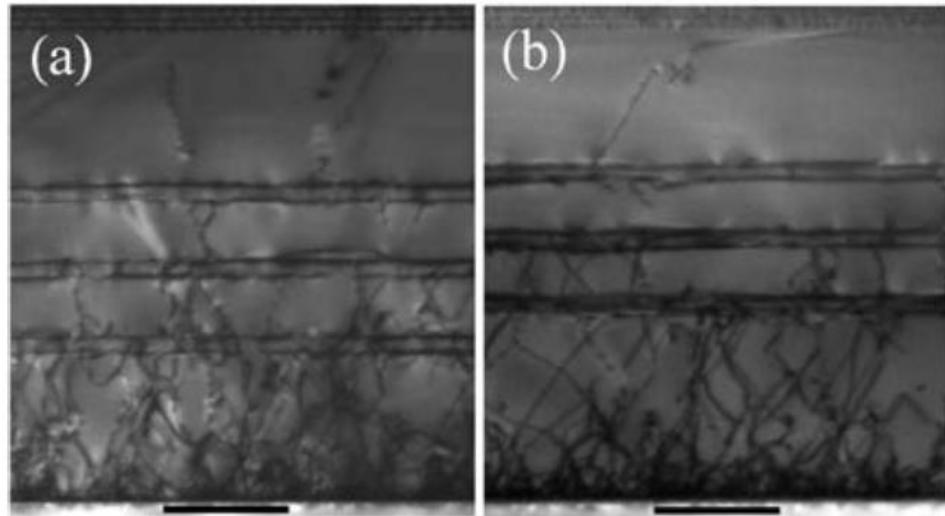


Figure 5.2: Cross sectional TEM dark field multi-beam images showing defect reduction induced by (a) InGaAs/GaAs SLS and (b) InAlAs/GaAs SLS. The scale bars are 1 μm . [9]

This phenomenon can be explained using Equation 5.1. The variable τ can be linked to shear modulus G with the following relation [11]:

$$G = \tau/\gamma \quad (2)$$

where τ is stress and γ is strain. As shown in the equation above, shear modulus is proportional to stress. Therefore, the variable τ in Equation 5.1 can be conceptually converted to material property shear modulus G .

So far, one conclusion can be drawn that for a given temperature T , to more effectively manipulate the dislocation motion, material should offer low dislocation activation energy Q and high stress τ . In other words, a material with low band gap energy (E_g) and relatively high shear modulus (G) is ideal for dislocation filters fabrication. The material properties regarding the dislocation motion of several III-V compounds, III-III-V and III-V-V ternary alloys are listed in the Table 5.2 [12]. Shear moduli for common

III-V compounds are obtained from literature, while the shear moduli for III-V ternary alloys are calculated from elastic constants:

$$C'(G) = (C_{11} - C_{12})/2 \quad (3)$$

The activation energies are obtained by fitting band gap energy values to the relation curve in Figure 5.1. After researching on the band gap energy (E_g) and elastic constant on these candidate materials, GaAsSb was found to be the material that matches the required feature among the three candidate III-V alloys.

Table 5.2: Material properties of different III-V compound and III-V alloys. All values are obtained at 300K.

	GaAs	GaSb	InSb	InAs	AlAs	GaAs _{1-x} Sb _x X=0.2	In _{1-x} Ga _x As X=0.8	InAs _{1-x} Sb _x X=0.2
elastic constant @300K (10¹¹ dyn/cm²)								
C11	11.90	8.83	6.67	8.34	12.02	10.98	11.19	8.006
C12	5.34	4.02	3.65	4.54	5.70	4.94	5.18	4.362
C44	5.96	4.32	3.02	3.95	5.89	5.47	5.56	3.764
Shear modulus (10¹¹ dyn/cm²)								
C'	3.28	2.405	1.51	1.9	3.16	3.105	3.004	1.822
lattice constant @300K(Å)								
	5.65325	6.09593	6.48	6.0583	5.6611	5.786054	5.7343	6.14244
Energy Gap (eV)	1.424	0.726	0.17	0.354	2.12	1.088	1.1392	0.21964
Activation Energy (eV)	1.25296	1.05054	0.8893	0.94266	1.4548	1.15552	0.9859	0.9037

After adjusting the composition, GaAs_{0.8}Sb_{0.2} stands out from the materials with a low band gap energy and high shear modulus compared to GaAs which is the main III-V material in the dislocation filter (DF) structure. Even though there are other materials that have either higher shear modulus (G) or lower band gap energy (i.e. activation energy Q), lattice constant mismatch poses a more significant impact on the dislocation velocity. The priority of the SLS material is to annihilate and eliminate dislocations

rather than introducing new defects in to the system. In this scenario, lattice constant mismatch can affect the selection rules. Taking InAsSb for example, although the Q is relatively low compared to other alloys, the great lattice constant mismatch to GaAs cause the potential of generating defects during the SLS fabrication process. On the contrary, despite the adjustment of composition, AlGaAs (not listed in the table) shows small lattice constant variation. Since AlAs and GaAs are nearly lattice matched, lattice constant of AlGaAs is always around 5.65 Å. No sufficient amount of strain will be introduced if employing AlGaAs/GaAs as SLS system. Another example can be made regarding AlAsSb (not listed in the table), similar to AlGaAs, despite the weak response in lattice constant variation, large band gap energy of AlAs (2.12eV) poses a threat to Q . With small Sb composition in AlAsSb alloy, the decrement in lattice constant could not reduce Q to a favourable level. Therefore, to select a suitable material, both G and Q need to be taken into consideration. Furthermore, one note should be addressed is that the GaAs_{0.8}Sb_{0.2} not only promises better performance among the potential candidate materials, but also showcases the advantage comparing to the reference InAlAs/GaAs SLS structure illustrated in the schematic diagram above. G and Q for the In_{0.15}Al_{0.85}As employed throughout the work [13-16] are $2.73 \times 10^{11} \text{ dyn/cm}^2$ [17] and 1.407 eV [18] respectively. Neither G nor Q of In_{0.15}Al_{0.85}As showcases the advantage in the comparison to GaAs_{0.8}Sb_{0.2}, which indicates the innovative material GaAsSb may perform better in the threading dislocation reduction aspect. Therefore, by taking both G and Q into consideration, GaAsSb/GaAs superlattice was included to fabricate SLS DFs.

5.3 Fabrication of SLS with InAlAs and GaAsSb

5.3.1 InAlAs SLS DF



Figure 5.3: Schematic Diagram of SLS DFLs.

As briefly discussed in Chapter 2, Figure 5.3 shows the schematic diagram of SLS DFLs structure [14,15]. 6° towards [110] plane offcut Si [100] wafers involved throughout the epitaxial growth were prepared by the wet chemical cleaning process with following sequence: RCA1(DI:H₂O₂:NH₄OH = 5:1:1) at 70 °C for 10 min, RCA2(DI:H₂O₂:HCl = 5:1:1) at 70°C for 10min and 10:1 buffered HF for 2min, with DI rinse for 6min between each step. NH₄OH can dissolve organic contamination from the sample surface. Metal contamination from the sample surface can be removed by dissolving in HCl. H₂O₂ is added to oxidise the sample surface to protect it from corrosion by NH₄OH or HCl. Native oxidation on Si can be removed by HF. Wafers were hydrophobic after the HF dip then blow dried with N₂. After the wet chemical cleaning, wafers were transferred to MBE lab in Acetone and IPA cleaned vacuum desiccator and loaded in MBE immediately.

After loading the freshly cleaned wafers into MBE system, wafers were outgassed then transferred into growth chamber for epitaxy. De-ox process was monitored by RHEED, the initiation of de-ox process can be confirmed when hazy RHEED pattern changed to clear and streaky. Substrate temperature was set to 900 °C to ensure the completion of de-ox. Meanwhile, as elaborated in Chapter 4, high temperature anneal is essential for double atomic steps formation, so the substrate heater temperature was kept at 900 °C for 30 min. Then 10nm refresh Si was deposited on the substrate at 650 °C to bury the potential carbon contamination which was found difficult to remove during the anneal step. This Si layer also serves a purpose for planarizing the substrate surface by obtaining double atomic steps for the later MEE epitaxy. After the deposition of Si, substrate temperature was brought to 800 °C for 20 min to initiate the high temperature annealing to produce the double atomic steps surface reconstruction [19]. When RHEED pattern exhibited the single domain (2×1) pattern, substrate temperature was set to 350 °C to start the AlAs MEE process. Elaborated MEE procedure was revealed in Chapter 4, where the growth rate of Al was set to 0.1 ML/sec. The role of this MEE layer was explained in Chapter 4.

On top of this MEE layer, a total thickness of $1 \mu\text{m}$ GaAs buffer layer was deposited using stepped growth technique [14]. The buffer layer consists of 30, 170 and 800nm grown at 350, 450 and 590°C with growth rate of 0.1, 1.0 and $1.0 \mu\text{m}/\text{h}$ respectively. After the deposition of stepped GaAs buffer layer, superlattice epitaxy took place at 420°C with growth rate of $0.7 \mu\text{m}/\text{h}$. One stack of superlattice structure consists of 5 layers of 10nm $\text{In}_{0.15}\text{Al}_{0.85}\text{As}$ and 10nm GaAs as illustrated in Figure 5.2, where the composition of InAlAs alloy was calibrated by RHEED prior to the initiation of epitaxy. Then the wafer was annealed at 660 °C for 6 min to accelerate threading dislocation motion at high thermal energy status, since dislocation motion velocity is directly

proportional to temperature as shown in Equation 5.1. The dependency between temperature and dislocation velocity has been investigated by several research groups [2,3,6], with results showing that the annihilation of dislocation was improved with increased thermal energy, in keeping with not only Equation 5.1, but also the dislocation reduction mechanism. After one stack of superlattice layer, one 300 nm spacing GaAs was deposited with unchanged temperature (i.e. 600 °C) and growth rate ($0.7 \mu\text{m}/\text{h}$). This superlattice stack was then repeated for 4 times of growth. Cycled anneal was also implemented [20]. So along with the repetition, the annealing was conducted for 4 times to accelerate the dislocation motion to annihilate portions of the defects before the deposition of subsequent stacks during the fabrication process [14]. The structure was finally capped with 100 nm GaAs, serving as a protective layer.

5.3.2 GaAsSb SLS DF

For the fabrication of GaAsSb SLS DF, besides the III-V alloys material variation, other deposition parameters remained unchanged. Prior to deposition, Sb source was tuned to be 2.5×10^{-7} Torr to obtain a nominally 20 % antimony composition in GaAsSb alloys. Then the growth rate of GaAsSb was monitored and calibrated by RHEED. After secured the growth condition, epitaxy was initiated with InAlAs replaced by GaAsSb.

5.4 Result and Discussion

5.4.1 Influence of Thermal Expansion Coefficient mismatch in III-V compound

When first group of InAlAs (SAMPLE *InAlAs*) and GaAsSb (SAMPLE *GaAsSb*) SLS samples was removed from the MBE system, sample surfaces exhibited a cloudy feature with one hazy ring located at the centre of wafers. This unexpected surface feature was suspected due to the thermal expansion coefficient mismatch of different III-V materials since the cooling rate was set to $10^\circ\text{C}/\text{min}$ during the cool down process. Another

contribution to this unwanted feature could be due to the unevenness of heat radiation in the substrate heater. Figure 5.4 illustrates the as-grown sample surface with the hazy and ring features. After removal from the MBE system, the wafer was bent, the hazy sample surface was attributed to an uneven heat distribution. The substrate holder acts as a heat sink. This results in the temperature reduction on the edge of the substrate, resulting in temperature non-uniformity across the substrate. During the deposition process, the temperature difference on the substrate would result in flaws on the sample surface, which, in this case, are the hazy disc and hazy ring. The two-zone heater can be tuned to solve this problem, where the power output of the outer heater needs to be calibrated carefully to increase the temperature on the substrate holder to avoid the temperature drop on the substrate edge. Unfortunately, the modification of calibrating the substrate heater is out of the scope of this work, therefore is considered as future work.

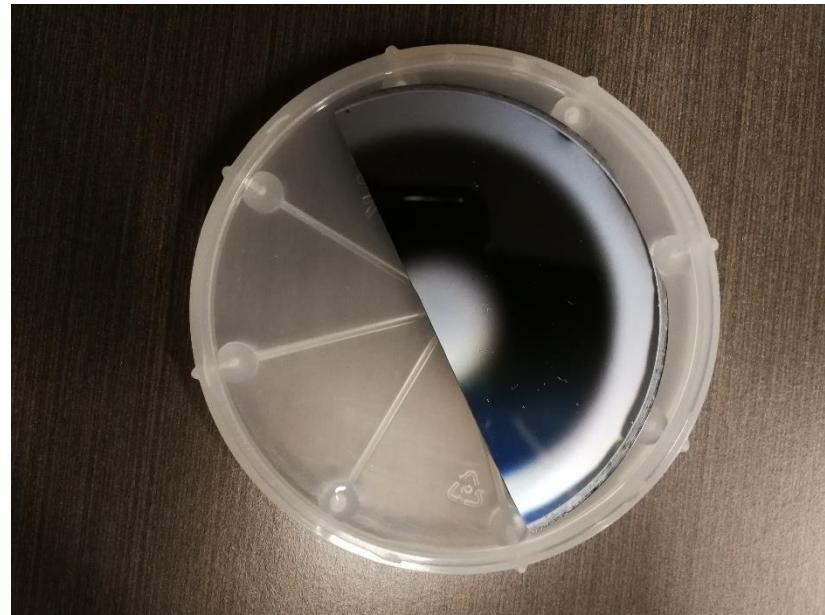


Figure 5.4: Hazy and ring features can be easily observed on the sample surface.

AFM was employed to exam the surface morphology after sample removal. As shown in Figure 5.5, these two $10 \times 10 \mu\text{m}^2$ scans revealed similar surface feature where the terraces are both horizontal and the RMS values are 5.24 nm and 5.46 nm respectively.

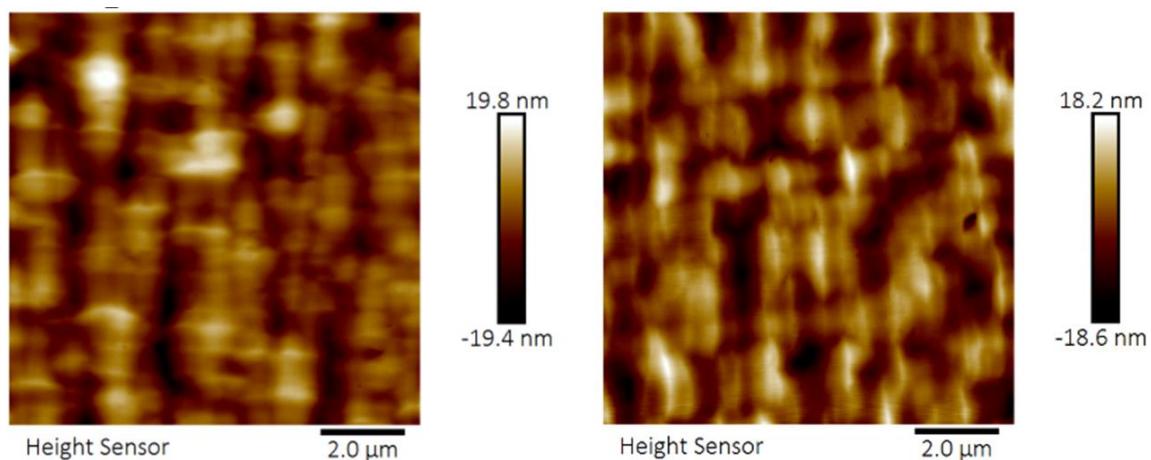


Figure 5.5: AFM of SAMPLE GaAsSb of clear (left) and hazy (right) region.

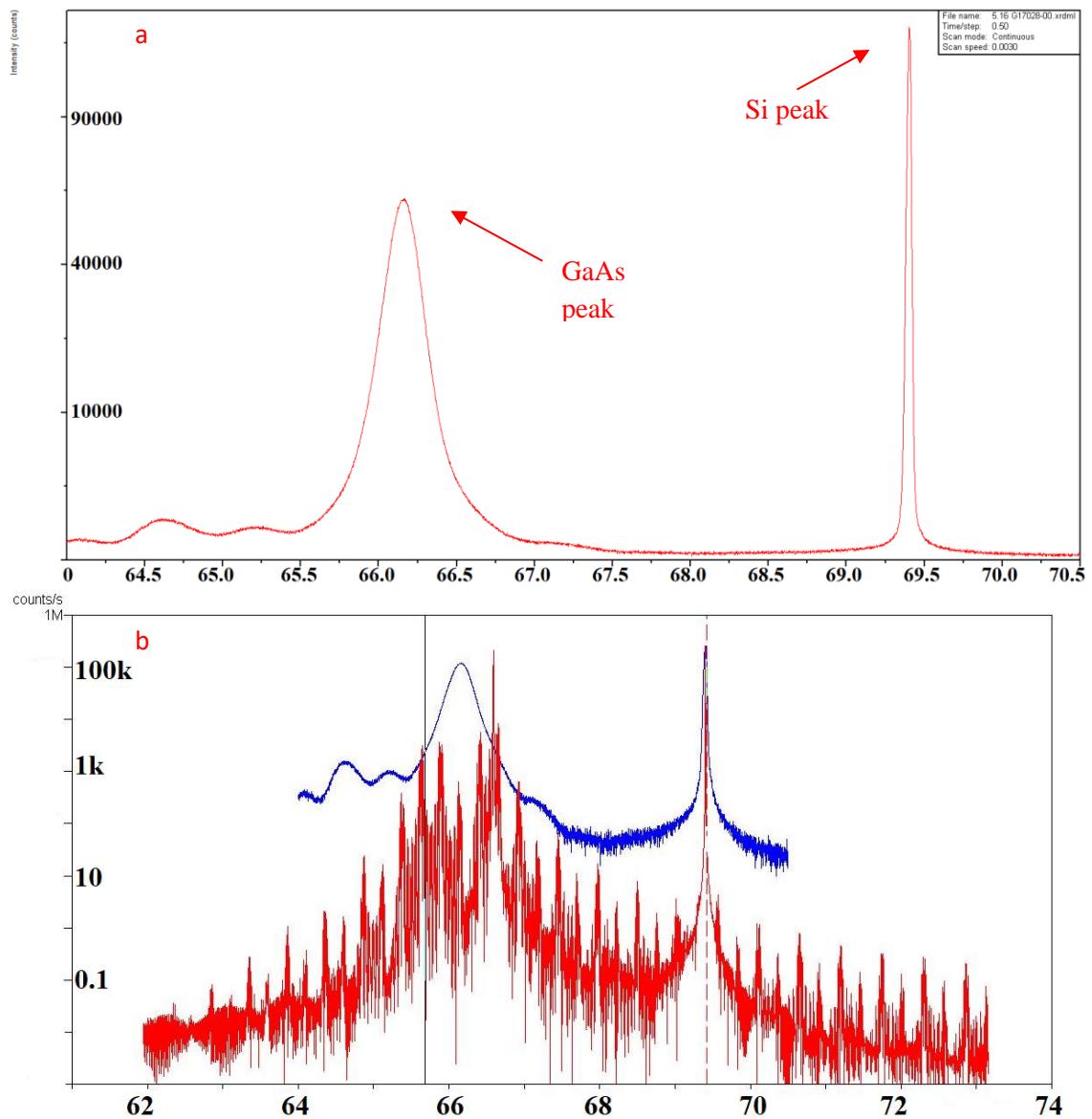
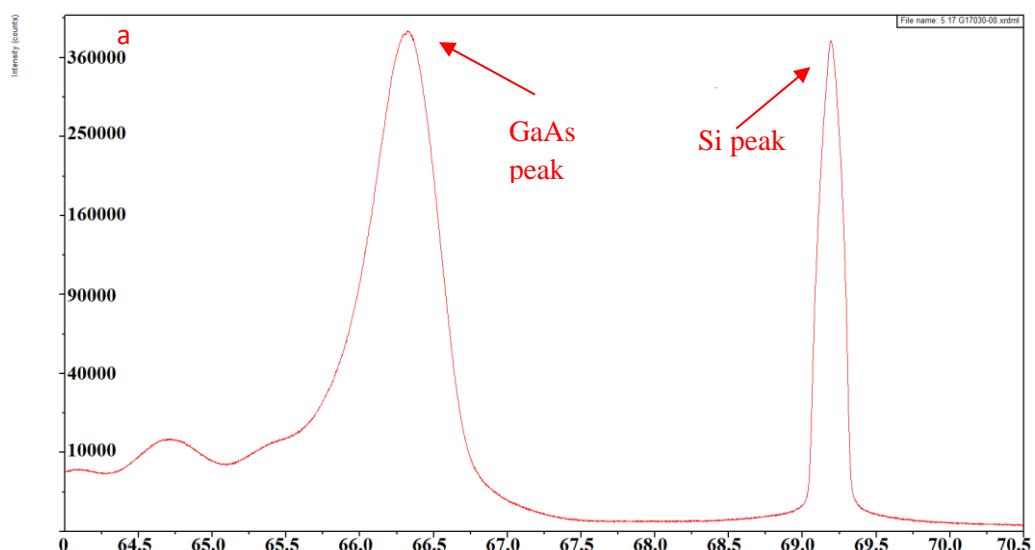


Figure 5.6: HRXRD scan on SAMPLE InAlAs (a) with simulation fitting curve (b).



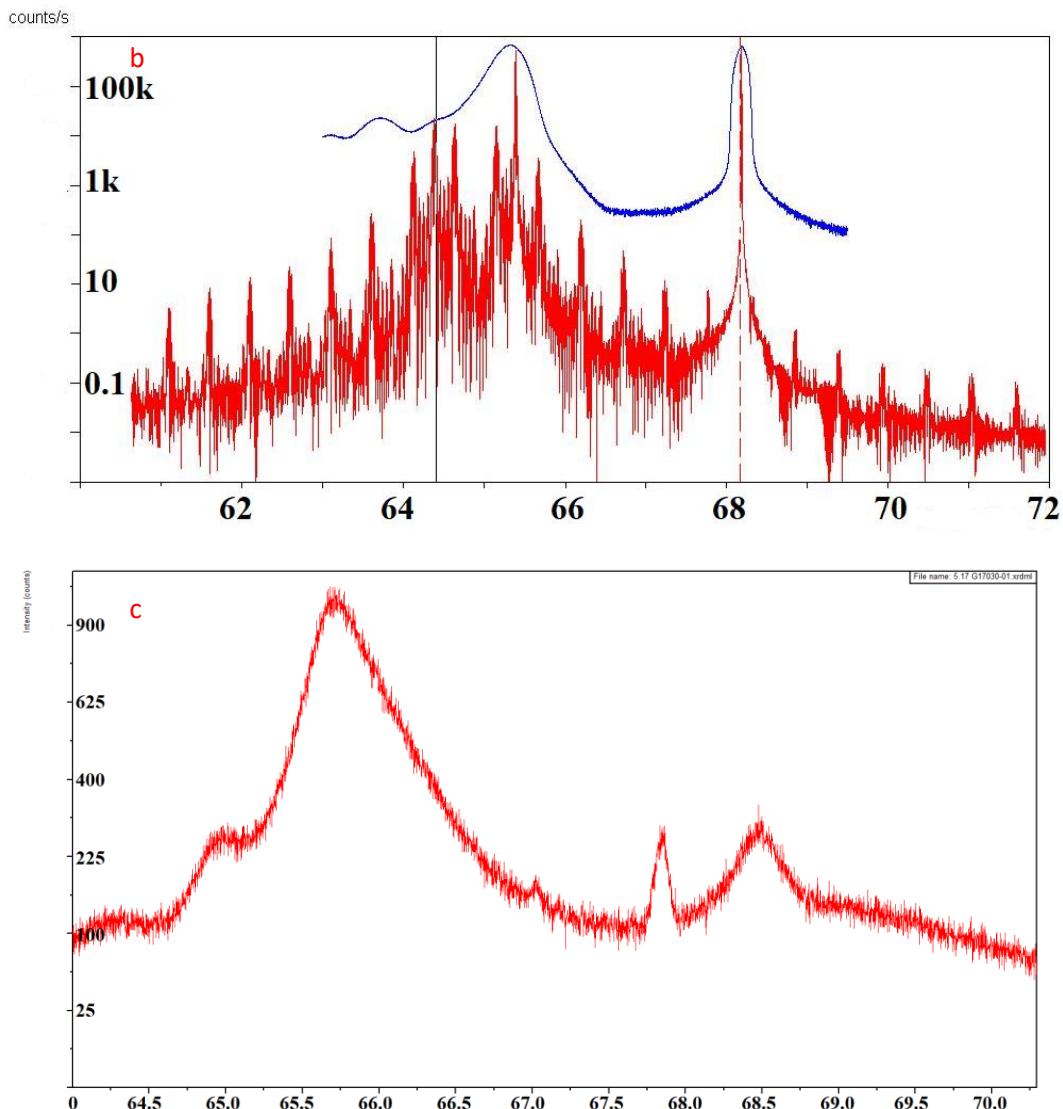


Figure 5.7: HRXRD scan on SAMPLE GaAsSb hazy (a) and clear (c) region with simulation fitting curve of hazy region (b).

After surface morphology examine by AFM, XRD and TEM scans were conducted to characterize the structural quality of the samples. HRXRD ω - 2θ rocking curves were obtained to assess the SLS structure. The peak on the right side of all curves is the substrate peak (Si) that is set to be reference peak. While the peak on the left side is the feature peak that reveal the structural information. For SAMPLE InAlAs, when fitting the scan result (blue curve) to the simulated structure curve (red curve) by aligning the substrate peak (Si peak at 69.2° 2θ position) as illustrated in Figure 5.6.b, it is easy to

observe a lower angle shift of feature peak due to the strain caused by the lattice constant expansion in the SLS layers. Even though the peaks were aligned for SAMPLE *GaAsSb* (Figure 5.7.b), it is inevitable that the feature peak is broadened by non-uniform strain. The scan result on the clear part exhibits an abnormal situation in both peak intensity and peak position. As shown in Figure 5.7.c, there are no substrate peak around 69.2° which indicates an absence of Si signal and the intensity of GaAs peak (the peak on the left) was quite low (less than 1000 counts) compared to the hazy area. This phenomenon may be explained by the thermal expansion coefficient mismatch. As mentioned in the explanation to Figure 5.4.b, the uneven temperature distribution from substrate heater will resulted in not only hazy surface but also bent and flexible sample. When mounting sample onto XRD sample stage, SAMPLE *GaAsSb* was physically detected to be bent and flexible, resulting in unusual scan results that could not be overcome. The bowing of the substrate can explain the poor match between scan result and simulation as shown in Figure 5.7.b.

Cross section TEM offered the structural view to understand how the thermal expansion coefficient mismatch would affect the entire structure. From Figure 5.8, TEM scan of SAMPLE *InAlAs*, stacking fault can be observed as straight strikes propagating to sample surface (marked with red arrow). Unlike the dislocations in the image, the propagating direction cannot be changed even after passing through the SLS. Although the existence of stacking fault is not negligible, the function of SLS remains as highlighted in the figure, after two layers of DF, the threading dislocations were successfully annihilated. It should be noticed, the contrast in the top two layers of SLS resulting from the deformation of SLS as shown in TEM images of SAMPLE *GaAsSb*.

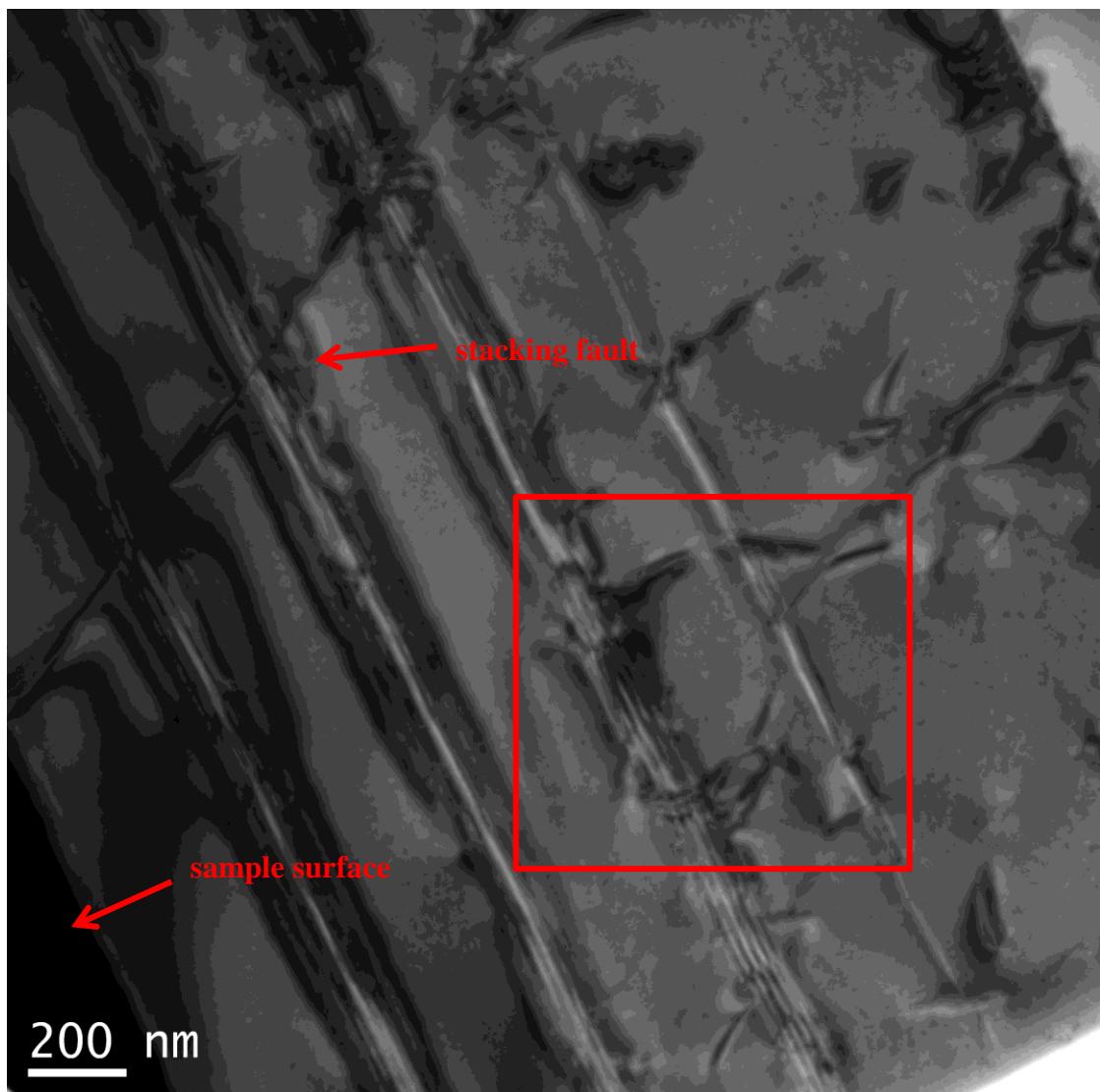


Figure 5.8: TEM image of SAMPLE InAlAs with stacking fault.

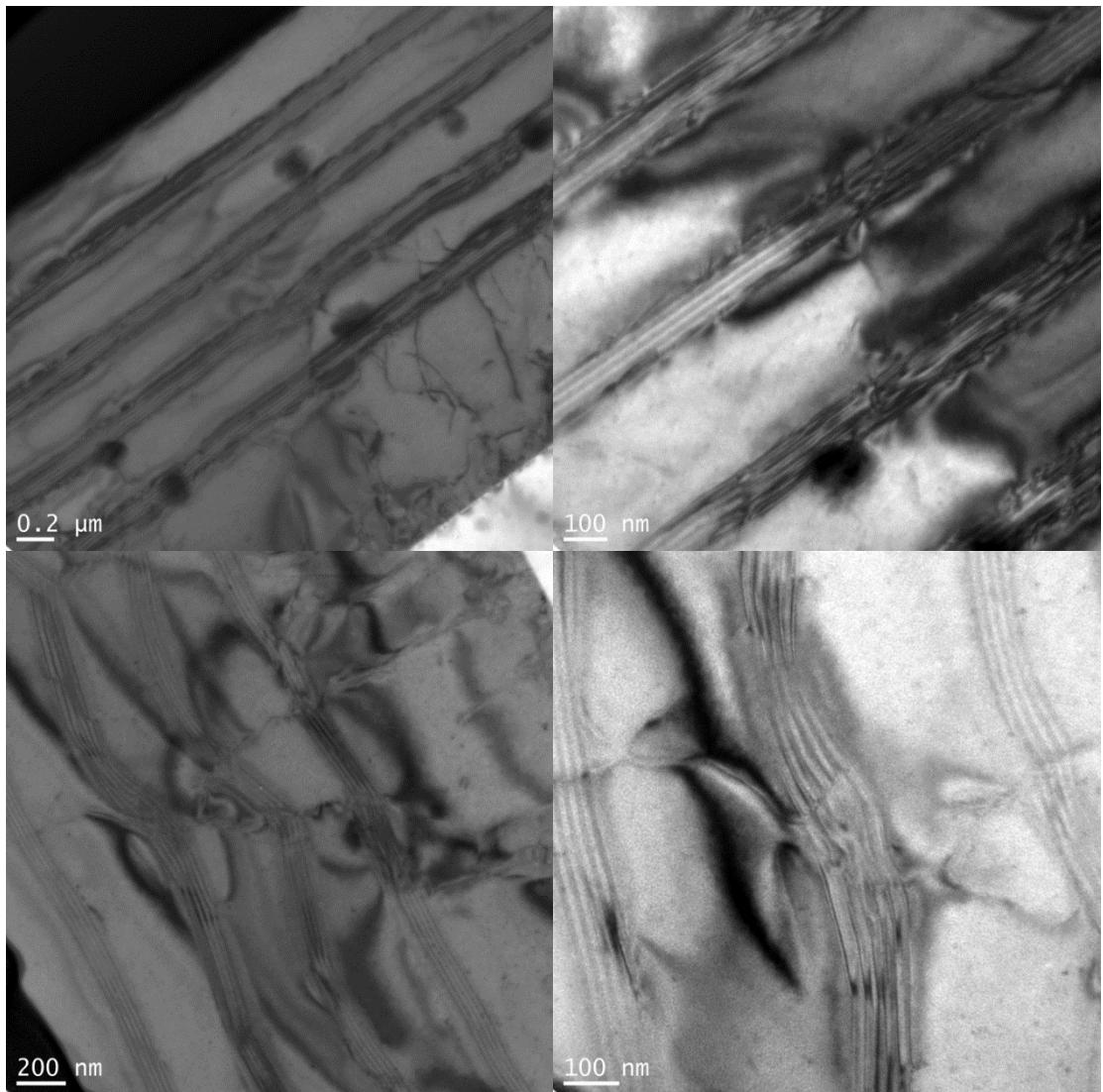


Figure 5.9: Cross section TEM images of SAMPLE GaAsSb on clear (a and b) and hazy region (c and d).

Figure 5.9 showcases TEM scans of both clear (Figure 5.9.a and 5.9.b) and hazy (Figure 5.9.c and 5.9.d) region of SAMPLE *GaAsSb*. Despite the dark dots on Figure 5.9.a suspected to be result from the milling process, the major difference between clear and hazy region is the undulation of SLS. By combining the effects of SLS deformation and blurry sample surface, it can be confirmed that the thermal gradient across the wafer contributes the structural deformation which leading to undesired surface morphology. Nevertheless, the function of dislocation filter remains even when the structure was deformed.

The cool down rate was set to be $10^{\circ}\text{C}/\text{min}$ as mentioned in the beginning of this section; all characterization results suggested this setting is too aggressive for this SLS structure. To resolve this problem, the cool down rate in the post-deposition process was lowered to $2^{\circ}\text{C}/\text{min}$, while all other parameters in the recipe remained unchanged in the subsequent patch epitaxy. With this optimized cool down setting, cross section TEM revealed the uniformly distributed SLS without undulation.

5.4.2 Influence of applying different As source in InAlAs DF

Discussion has been made in section 4.3.2 regarding whether employing different As sources would affect the quality of fabrication. In this section, identical concept was borrowed from section 4.4.2 to see whether the same situation can be applied in SLS DF. One set of InAlAs SLS DFs were fabricated with As_4 (SAMPLE As_4SLS) and As_2 (SAMPLE As_2SLS) sources to facilitate a comparison of DF performance. As justified in Chapter 4, As_4 can reduce the surface roughness so the step grown $1\ \mu\text{m}$ GaAs buffer layer was fabricated with As_4 which can allow the initiation of SLS layer growth on a relatively smooth surface. Meanwhile, with the identical initiation condition, the performance variation can be traced back to the application of different As sources in the SLS region. After deposition, the samples were characterized by AFM, XRD and TEM to explore the role played by different As sources.

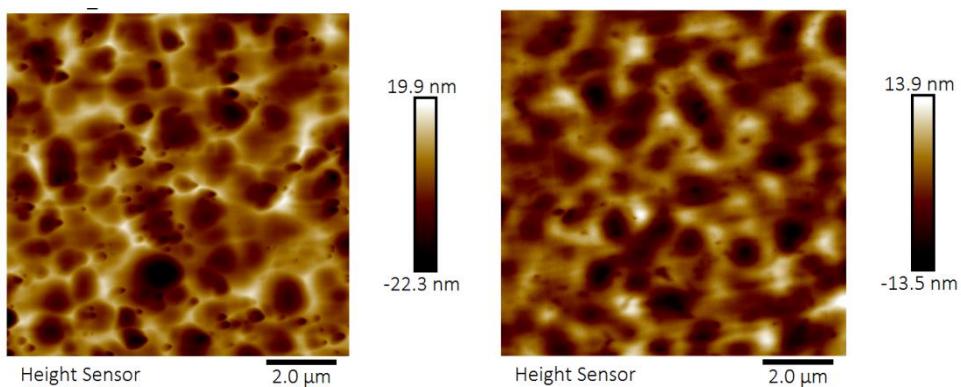


Figure 5.10: AFM images of InAlAs employing As_4 (left) and As_2 (right)

Table 5.3: Surface Roughness comparison of SAMPLE As₄SLS and SAMPLE As₂SLS

	Ra(nm)	Rq(nm)
SAMPLE As ₄ SLS	4.75	5.99
SAMPLE As ₂ SLS	3.19	3.94

Figure 5.10 shows the $10 \times 10 \mu\text{m}^2$ AFM scans taken from as-grown SAMPLE As₄SLS and SAMPLE As₂SLS. Both SAMPLE As₄SLS and SAMPLE As₂SLS share similar surface morphology, whereas the SAMPLE As₄SLS image is sharper and more contrasted which indicating the roughness of SAMPLE As₄SLS would be higher than SAMPLE As₂SLS. The listed surface roughness values showed agreement with the observation from the images. The RMS value of SAMPLE As₄SLS is nearly 6nm while for SAMPLE As₂SLS the RMS is close to 4nm. The HRXRD scans in Figure 5.11 reveal the structural views of these two samples. No major difference can be noticed from the feature peak position and full width at half maximum (FWHM) value listed in Table 5.4. However, from Figure 5.11, SAMPLE As₂SLS exhibits fringes on the left shoulder of feature peak indicating a better structural quality than SAMPLE As₄SLS in SLS Bragg angle region. Since the initiation statuses of these two samples are identical, the difference from XRD is a straight reflection of structural quality in SLS region.

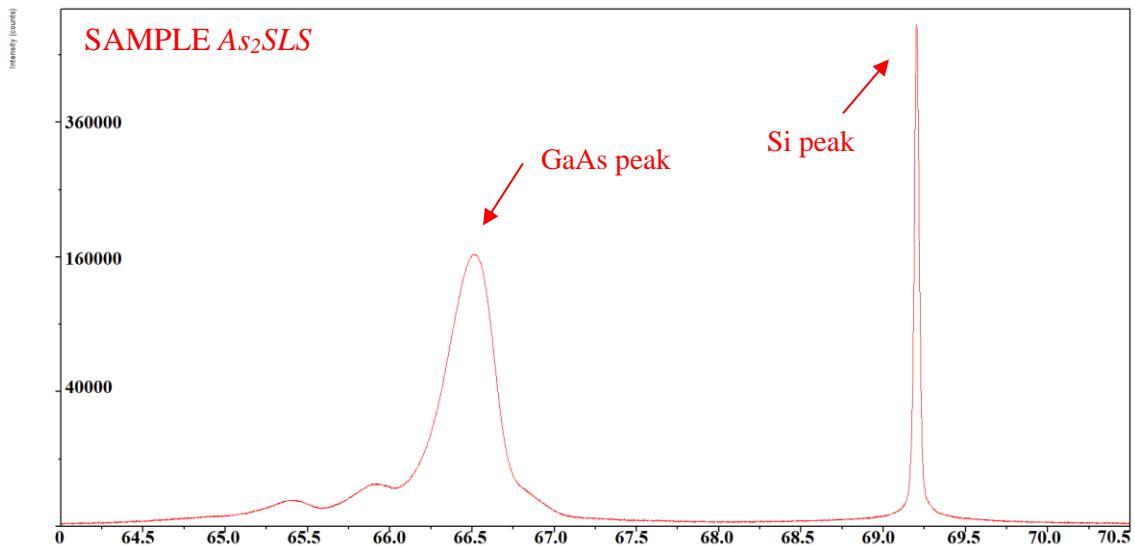
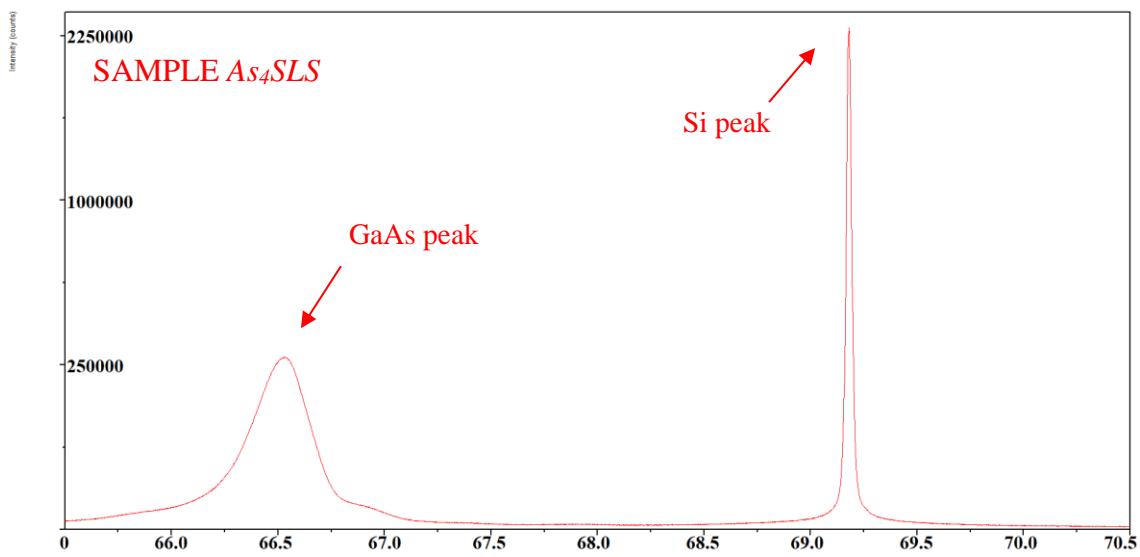


Figure 5.11: HRXRD 2θ-Ω scans of SAMPLE *As*₄*SLS* and SAMPLE *As*₂*SLS* respectively

Table 5.4: featured peak positon and FWHM of SAMPLE *As*₄*SLS* and SAMPLE *As*₂*SLS*

	Peak position(°2θ)	FWHM(°)
SAMPLE <i>As</i> ₄ <i>SLS</i>	66.53	0.223
SAMPLE <i>As</i> ₂ <i>SLS</i>	66.51	0.238

Cross section TEM was employed to facilitate a direct visual comparison between SAMPLE As_4SLS and SAMPLE As_2SLS . As shown in Figure 5.12, the performance of SAMPLE As_2SLS is visually better than SAMPLE As_4SLS . The contrasted spots can be seen throughout all stacks of SLS as shown in Figure 5.12.a. There are great amount of small spots still can be spotted even on top of the last layer of SLS in Figure 5.12.c, which is an indication of threading dislocation exiting the SLS DF system. On the other hand, when comparing Figure 5.12.a and c with Figure 5.12.b, it is easy to notice the dislocation density reduction ability of SAMPLE As_2SLS is better than SAMPLE As_4SLS . Firstly, after first two stacks of SLS, there are only few threading dislocations can be visually spotted in SAMPLE As_2SLS , showcasing the difference in SLS performance. Secondly, as illustrated in Figure 5.12.e and f, the SLS layers suffer from undulation in SAMPLE As_4SLS . As mentioned in Section 5.3.1, the thermal expansion coefficient mismatch would affect the deformation of SLS. Since the cool down rate was adjusted to avoid this issue, the undulation in this scenario is assumed to be mainly resulted from the strain introduced by threading dislocation.

The results from all three characterization approaches agree with each other that SAMPLE As_2SLS exhibits smoother sample surface, better structural quality and better performance in threading dislocation density reduction. These phenomena can be explained by the mechanism of dislocation motion. Dislocation needs to break the bond for motion, in other words, bond strength dominates the dislocation motion feasibility [2, 4]. From Figure 5.1, the gradation of the dislocation motion activation energy follows the increasing order from II-VI, III-V, and to elemental semiconductors corresponds to the degree of iconicity among these material systems. SAMPLE As_2SLS shows better performance than SAMPLE As_4SLS . The As source adapted in SAMPLE As_4SLS was As_4 which contains less thermal energy and greater bond strength since the dimmer As_2 .

was cracked from tetramer As₄. Therefore, the dislocation motion in As₂ sourced SLS system is more favoured by the motion mechanism.

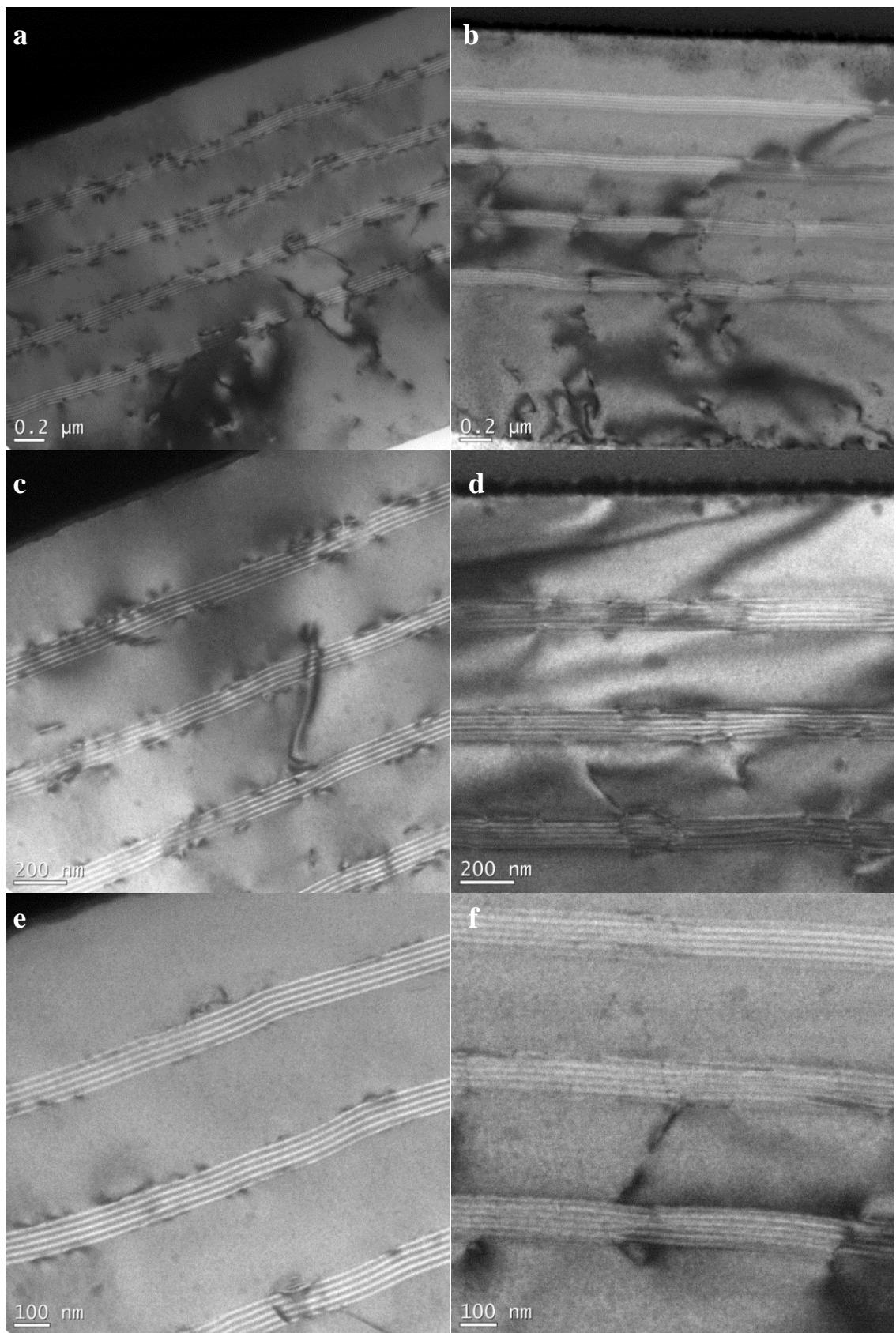


Figure 5.12: Cross section TEM of SAMPLE As₄SLS (a,c and e) and SAMPLE As₂SLS (b, d and f)

By taking the all characterization results into consideration, it can be concluded that As₂ source is more suitable for SLS fabrication by providing more favoured condition regarding dislocation motion mechanism. Therefore, the fabrication of GaAsSb SLS DF (SAMPLE *GaAsSb(As₂)*) structure took the same path employing As₂ source in SLS layers fabrication procedure.

5.5 Threading Dislocation Density Comparison Among Different DF Structures

One significant aspect to judge the function and performance of the dislocation filter (DF) is the dislocation density reduction ability. In this section, all three DFs (SAMPLE *As₄SLS*, SAMPLE *As₂SLS* and SAMPLE *GaAsSb(As₂)*) were characterized to determine which SLS system could offer best dislocation density reduction ability.

First, after removal from MBE system, AFM was employed to examine the surface morphology of SAMPLE *GaAsSb(As₂)* sample. As shown in Figure 5.13 and Table 5.5, the surface feature is generally the same as the InAlAs SLS DF sample. The surface roughness value is positioned in the middle between SAMPLE *As₂SLS* and SAMPLE *As₄SLS*, which may be the result from sensitivity of thermal expansion coefficient mismatch corresponding to the cool down rate. Although the cool down rate was turned down to 2 °C/min, this rate could still be aggressive to some superlattice systems with the thickness of 1.6 μm .

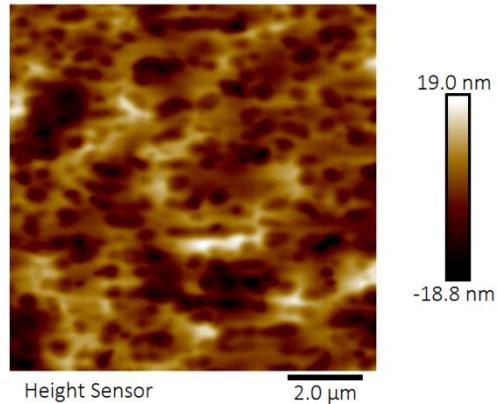
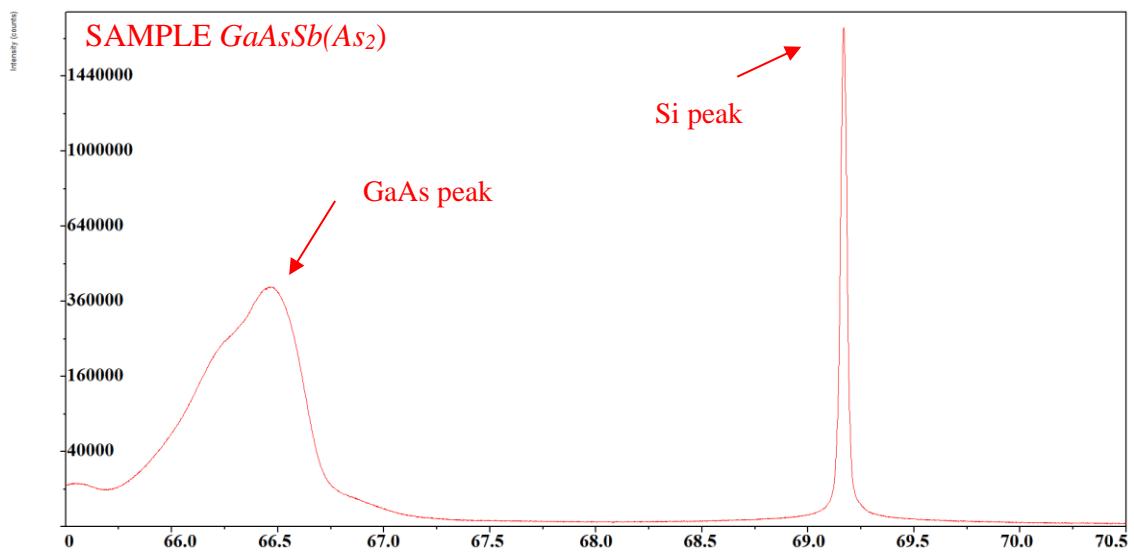


Figure 5.13: AFM image of the surface SAMPLE GaAsSb(As₂) SLS DF

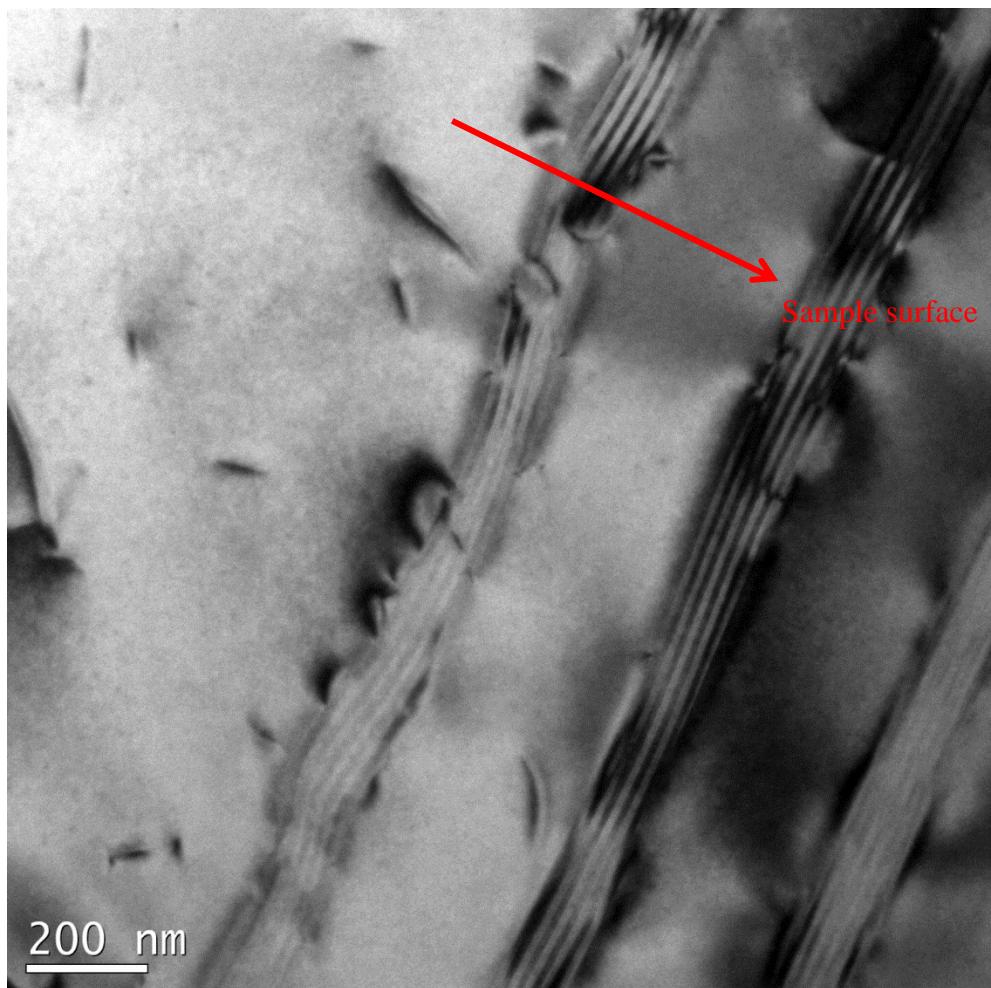
Table 5.5: surface roughness value of SAMPLE GaAsSb(As₂)

	R _a (nm)	R _q (nm)
SAMPLE GaAsSb(As ₂)	4.09	5.24

Then, with the assumption made above, HRXRD was employed to determine if the surface morphology is related to crystal defect. Figure 5.14 is the ω - 2θ scan of SAMPLE GaAsSb(As₂) from 65.0° to 70.5°. Unlike the previous XRD curves of other sample groups, the feature peak in Figure 5.14 is broadened and one hump can be noticed on the left shoulder. The FWHM of the feature peak is 0.399° which is almost twice as the value for InAlAs/GaAs SLS system. The broadening of the feature peak implies crystal defect generated due to the lattice constant mismatch.



*Figure 5.14: HRXRD 2θ- Ω scan of SAMPLE *GaAsSb(As₂)* from 65.0°-70.5°.*



*Figure 5.15: cross section TEM of SAMPLE *GaAsSb(As₂)* with SLS undulation in the first stack. The arrow points at the direction of sample surface.*

Cross section TEM was adapted to verify the reason of XRD curve broadening. Figure 5.15 is the TEM image of SAMPLE $GaAsSb(As_2)$, it is clear from the image that the SLS suffers from undulation in the first stack. This is a good addition to the XRD rocking curve that the broadening of the feature peak is not only resulting from the lattice constant mismatch but also the structural defects in the SLS region.

5.5.1 Threading Dislocation Density (average volume) Calculation by XRD

Nevertheless, as mentioned at the beginning of this section, despite the defects in the SLS system, one aspect to judge the performance of DF is threading dislocation density reduction ability. Several techniques have been demonstrated to obtain the dislocation density, such as XRD [21-24], TEM [25 and 26] and etch pit density (EPD) [27-29]. EPD involving molten KOH etch method was unavailable, hence the techniques used to obtain dislocation density in this work are XRD and TEM.

To use the method which has been demonstrated in various reports [21-24] to calculate dislocation density from the perspective of XRD rocking curves, the mechanism of how dislocation in epitaxial film would affect the shape of rocking curves must be clarified. In semiconductor systems, dislocations broaden the XRD rocking curves from two perspectives. One is the dislocation rotates the crystal lattice, hence broadening the rocking curve directly. The other is the strain field surrounding the dislocation leads to a non-uniform Bragg angle of the crystal which is reflected by the broadening of rocking curve [21]. With these two perspectives being pointed out, the broadening of rocking curves can be expressed in the following equation [21]:

$$\beta^2 = K_\alpha + K_\epsilon \tan^2 \theta \quad (4)$$

where β is the broadening of the rocking curves, K_α is the broadening factor resulted from angular rotation, K_ϵ is the broadening resulted from strain field and θ is the Bragg angle. Dislocation density can be obtained from the equation below [21]:

$$D = K_\alpha / 4.36b^2 \quad (5)$$

where D is the dislocation density and b is the magnitude of Burgers vector. In this case, for 60° dislocation gliding on the (111) planes, the Burger vector is $\frac{a}{2} <110>$. The curves of Equation 5.4 can be plotted with intercept K_α and slope K_ϵ when at least three sets of Bragg angle θ and FWHM β were obtained from XRD rocking curves. Then dislocation density can be determined by the intercept value K_α .

With the method elaborated above, 2θ rocking curves of (002), (004) and (006) planes were obtained from all three samples (SAMPLE As_4SLS , SAMPLE As_2SLS and SAMPLE $GaAsSb(As_2)$) as shown in Figure 5.16 – Figure 5.18. FWHM values were extracted from the Bragg angles for each plane. Three curves of $\tan^2 \theta$ vs β^2 of SAMPLE As_4SLS , SAMPLE As_2SLS and SAMPLE $GaAsSb(As_2)$ with least square fitting curves are listed in Figure 5.19. The intercept value K_α , the R^2 and the uncertainty values are listed in Table 5.7. The uncertainty of the least square fitting of intercept is calculated with Equation 5.6.

$$\text{Intercept Error} = S \times \sqrt{\frac{\sum x_i^2}{(\sum x_i^2) - (\sum x_i)^2}} \quad \text{with} \quad S = \sqrt{\frac{\sum (y_i - ax_i - b)^2}{n-2}} \quad (6)$$

Where x_i is the value of $\tan^2 \theta$ listed on the x-axis, y_i is the value of β^2 listed on y-axis. n is the number of data ($n=3$ in this case), a and b are the slope and the intercept of the fitting curve respectively. The relative intercepts values are also listed in Table 5.7. Then the dislocation density of each sample was calculated by substitute intercept value

K_α into Equation 5.5. By combining the dislocation density calculated with intercept value K_α and medium value of the uncertainty ranges of dislocation density, the estimated average dislocation densities are $(3.57 \pm 1.98) \times 10^8$, $(3.13 \pm 1.54) \times 10^8$ and $(3.25 \pm 2.44) \times 10^8 /cm^2$ for SAMPLE As_4SLS , SAMPLE As_2SLS and SAMPLE $GaAsSb(As_2)$ respectively.

It should be emphasized that the dislocation density obtained using this method is the dislocation density for in the entire X-ray beam interacting volume (ρ_{vol}). Since the $\omega - 2\theta$ rocking curves in Figure 5.11 and Figure 5.14 contains substrate peaks which implies beam reached the Si substrate, implies the dislocation density calculated from 2θ rocking curves can be considered as the average dislocation density existing within the entire volume covered by the X-ray path, which are still reliable and representative.

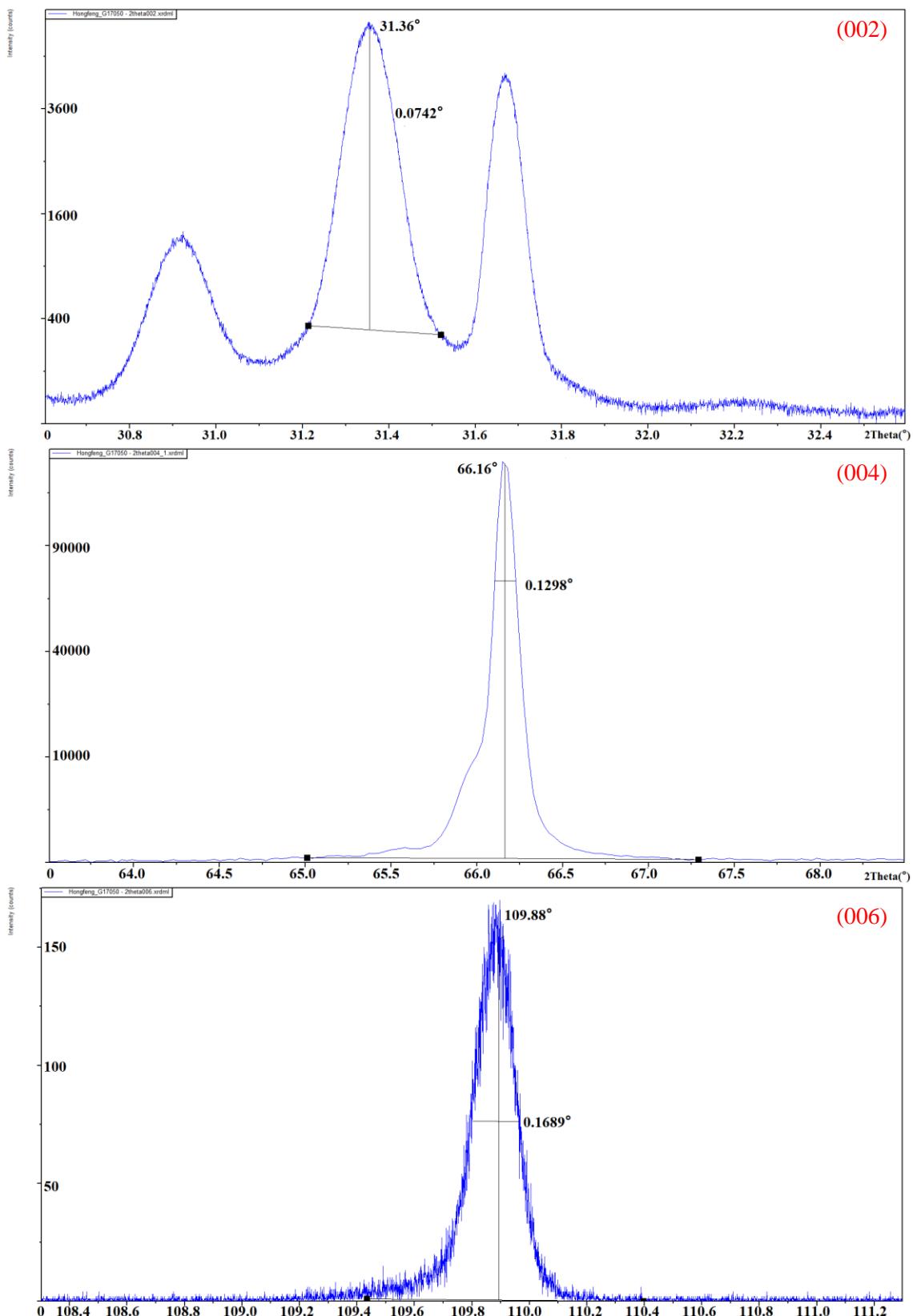


Figure 5.16: 2θ Rocking curve of SAMPLE As₄SLS on (002), (004) and (006) reflection plane (from top to bottom respectively).

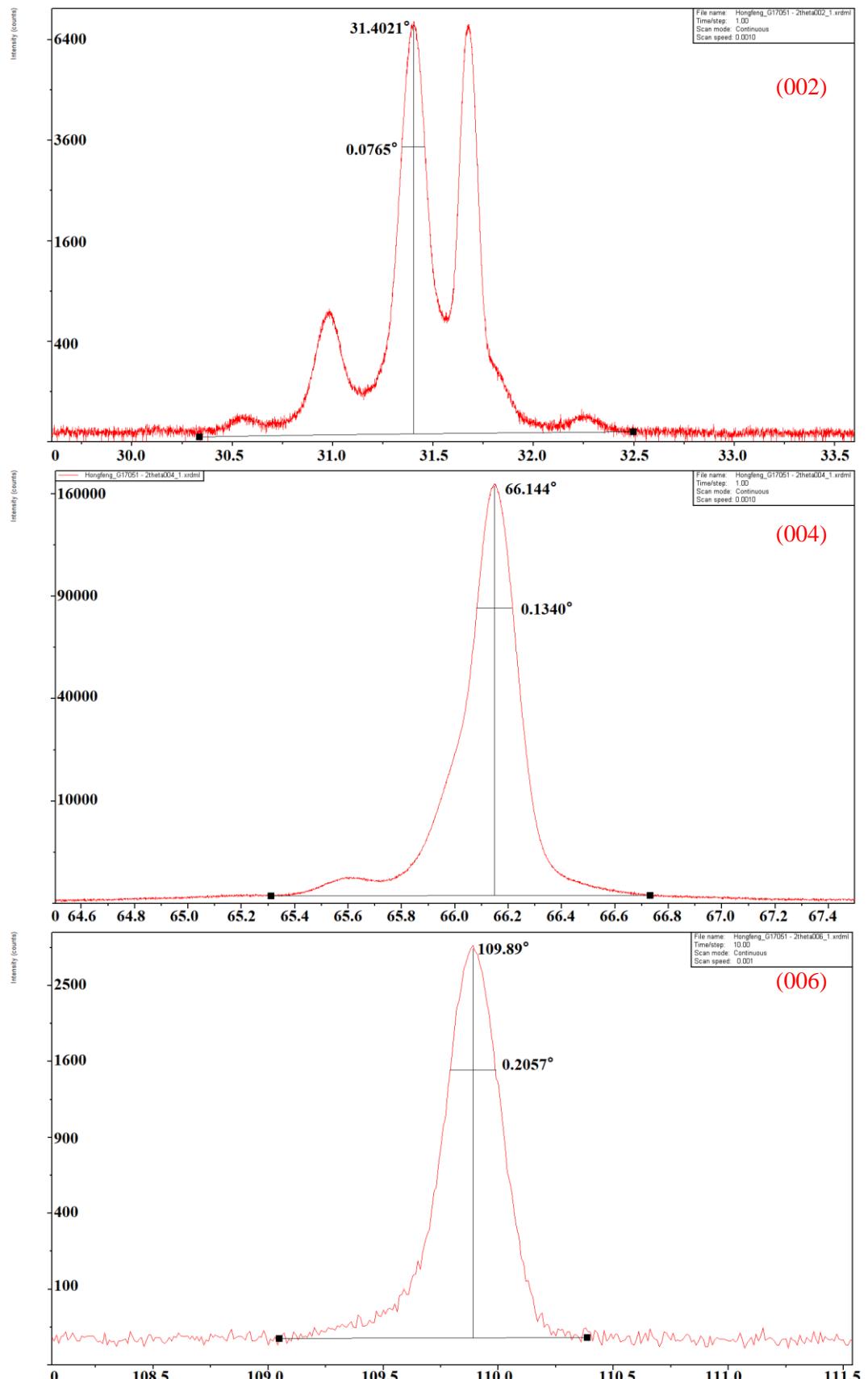


Figure 5.17: 2θ Rocking curve of SAMPLE As_2SLS on (002), (004) and (006) reflection plane (from top to bottom respectively).

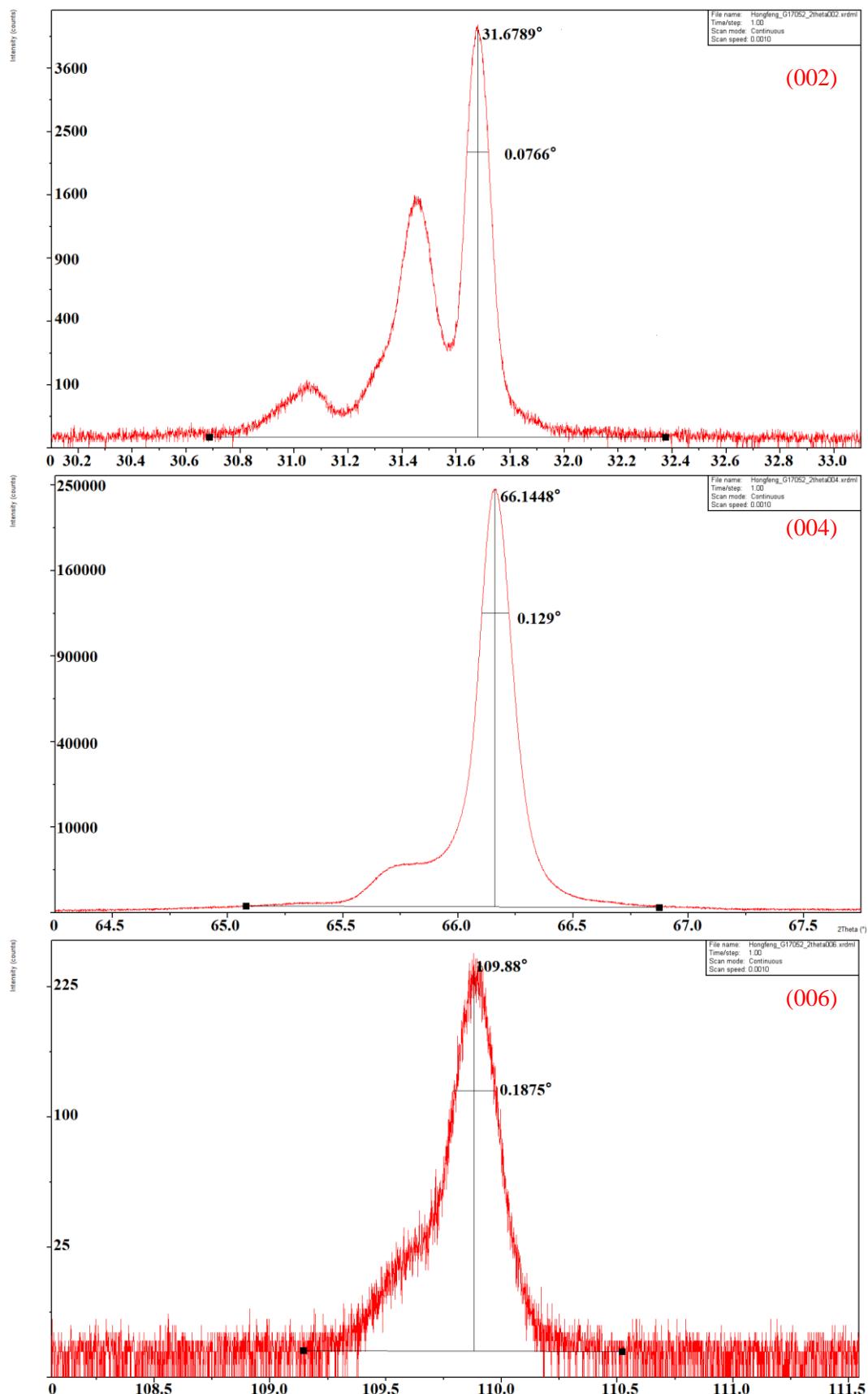


Figure 5.18: 2θ Rocking curve of SAMPLE GaAsSb(As₂)on (002), (004) and (006) reflection plane (from top to bottom respectively).

Table 5.6: Value of FWHM extracted from Figure 5.15 and bragg angle of different reflection planes.

	Plane	$\beta(^{\circ})$	$\beta(\text{rad})$	β^2	$2\theta(^{\circ})$	$\tan^2\theta$
SAMPLE <i>As₄SLS</i>	(002)	0.0742	0.001295	1.68×10^{-6}	31.36	0.078799
	(004)	0.1298	0.002265	5.13×10^{-6}	66.16	0.424380
	(006)	0.1689	0.002948	8.69×10^{-6}	109.88	2.030539
SAMPLE <i>As₂SLS</i>	(002)	0.0765	0.001335	1.78×10^{-6}	31.402133	0.079021
	(004)	0.134	0.002339	5.47×10^{-6}	66.144	0.424056
	(006)	0.2057	0.003590	1.29×10^{-5}	109.89	2.031292
SAMPLE <i>GaAsSb(As₂)</i>	(002)	0.0766	0.001337	1.79×10^{-6}	31.6789	0.080494
	(004)	0.129	0.002252	5.07×10^{-6}	66.1448	0.424069
	(006)	0.1875	0.003273	1.07×10^{-5}	109.88	2.030539

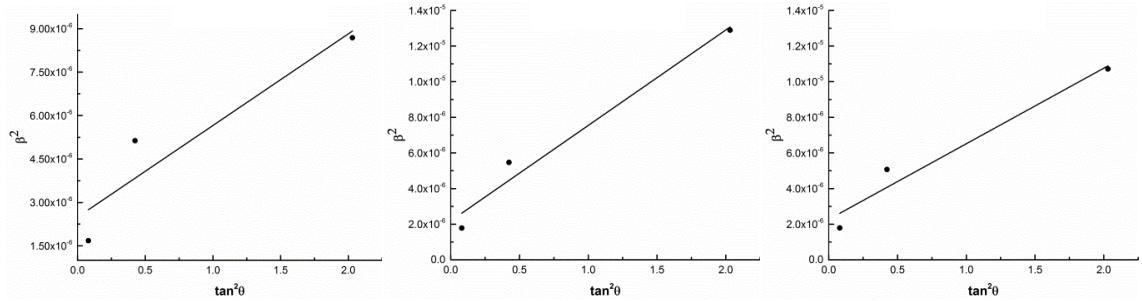


Figure 5.19: Plots of $\tan^2\theta$ vs β^2 of SAMPLE As₄SLS, SAMPLE As₂SLS and SAMPLE GaAsSb(As₂) (left to right) with forecasted trend line.

Table 5.7: Intercept value (K_a), R^2 and relative intercept error values of above plots. The uncertainty ranges of dislocation density are also listed.

		SAMPLE As ₄ SLS	SAMPLE As ₂ SLS	SAMPLE GaAsSb(As ₂)
Intercept		2.49×10^{-6}	2.18×10^{-6}	2.27×10^{-6}
R^2		0.8829	0.9726	0.9580
Relative Intercept Error		55.45%	49.30%	46.91%
Uncertainty Range (/cm ²)	Max	5.548×10^8	4.675×10^8	7.648×10^8
	Min	1.590×10^8	1.587×10^8	2.764×10^8

5.5.2 Threading Dislocation Density (sample surface) Calculation by TEM

Conventional method to calculate the threading dislocation density at sample surface involving cross section TEM have been elaborated in literature [26,27]. To determine the dislocation density reaching sample surface with this method, a measurement of the

total length (L) of dislocation reached the sample surface is required, the other essential parameter is the volume (V) of the specimen that contains the dislocations previously mentioned. Then the dislocation density (D) is calculated by dividing L with V . The surface dislocation densities (ρ_{sur}) of *SAMPLE As₄SLS*, *SAMPLE As₂SLS* and *SAMPLE GaAsSb(As₂)* estimated by this method are 7.25×10^6 , 4.17×10^6 and $1.07 \times 10^6 /cm^2$ respectively. As shown in Equation 5.7 the threading dislocation reduction efficiency (η_{red}) of these three SLS DFs can be obtained by the fraction of the dislocations that removed by the DFs [25]. The efficiencies of *SAMPLE As₄SLS*, *SAMPLE As₂SLS* and *SAMPLE GaAsSb(As₂)* are listed in Table 5.8.

$$\eta_{red} = 1 - \frac{\rho_{sur}}{\rho_{vol}} \quad (7)$$

Table 5.8: The efficiencies of SAMPLE As₄SLS, SAMPLE As₂SLS and SAMPLE GaAsSb(As₂)

	$\rho_{vol}(/cm^2)$	$\rho_{sur}(/cm^2)$	η_{red}
SAMPLE As ₄ SLS	3.57×10^8	7.25×10^6	98.0%
SAMPLE As ₂ SLS	3.13×10^8	4.17×10^6	98.7%
SAMPLE GaAsSb(As ₂)	3.25×10^8	1.07×10^6	99.7%

These values agree with the previous characterization results and prove a better performance of *SAMPLE As₂SLS* than *SAMPLE As₄SLS*. With the innovative SLS material being selected, *SAMPLE GaAsSb(As₂)* suggested an improved ability in dislocation density reduction among these three DF structure. Nevertheless, all three DFs successfully reduced the threading dislocation density to be in the range of the critical level ($\sim 10^6 /cm^2$) which allows further device fabrication on top of the SLS structure without affecting the device performance due to the existence of defects [30].

5.6 Conclusion

In this chapter, the goal was to investigate a suitable material to fabricate SLS DF structure. By taking the mechanism of dislocation motion into consideration, two factors that determine the dislocation motion velocity were conceptional converted to material properties. To ensure high performance in dislocation reduction, material with low band gap energy (E_g) and high shear modulus (G) is ideal for SLS DFs. Therefore, after investigation among several III-V compounds and III-V alloys, innovative material GaAsSb was selected for SLS DFs fabrication. Along with the elaborated epitaxy procedure, investigation of whether different As sources could affect the structural quality of SLS system has been conducted by applying As₄ and As₂ on identical SLS structure. Characterization techniques including AFM, XRD and TEM were employed to judge the performance and function of SLS DF. With good agreement among these three characterization results, As₂ offered a smoother sample surface, better structural quality and less SLS deformation against As₄. The threading dislocation density for all samples were calculated. The average dislocation densities existing within the examined volume were calculated by XRD rocking curves, whereas the surface dislocation densities were calculated by the conventional cross section TEM involved method. The conclusion can be drawn that SAMPLE *GaAsSb(As₂)* sample showed the best dislocation density reduction ability.

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Chapter 6 Distributed Bragg Reflector

6.1 Introduction

The fabrication processes in both Chapter 4 and 5 showcased a feasible approach to provide a surface with defects in a tolerable range. The ultimate goal after the deposition of GaAs on Si substrate is the fabrication of a GaAs solar cell device, in which the Si serves the role of mechanical template. To enhance the performance of the solar cell, one crucial issue is how to increase the optical path length in the active region of the device, which is essential for the enhancement of incident light absorption. In simple words, once the incident photons entered the device their mean residing time in active region must be long enough such that photons are absorbed before escaping the device [1]. When designing the base thickness of the solar cell, the minority carrier diffusion length is the main reason that limits the device thickness, thereby limiting the photon absorption near the band gap region [2]. Distributed Bragg reflector (DBR) can be adapted as the solution to boost the absorption by selectively reflecting the non-absorbed photons [3], which offers a second bounce of incident light to achieve the requirement of optical path length enhancement. This allows to reduce the device thickness without losing of long wave sensitivity and decrease the influence of diffusion length degradation on the electrical parameters of the cells such as short circuit current and open circuit voltage. Like superlattice structure, a DBR is a multilayer structure of materials with different refractive indices, with the intent to reflect light with a certain wavelength range [3-6]. Several DBR structures were investigated to search for a suitable structure to boost the performance of the solar cell.

6.2 Distributed Bragg Reflector

6.2.1 Reflectance Calculation

The materials selected to fabricate the DBR are GaAs and AlAs, which not only have the similar lattice constant but also can help flatten the surface for later device fabrication. Another benefit choosing GaAs and AlAs as the DBR materials is that the difference between the refractive indices provides a better reflect result. In this scenario, the thickness of the solar cell is assumed to be around 1.5 to 2 μm , which is the typical thickness of a single junction solar cell. The targeting wavelength point of the DBR is determined by the transmitted ratio within the band gap range of GaAs. Based on the absorption coefficient curve of GaAs [5], GaAs will not absorb the light with wavelength longer than 870 nm. Therefore, three reference wavelength points are selected to calculate the transmitted ratio.

$$I = I_0 e^{-\alpha l} \quad (1)$$

Equation 6.1 is Beer-lambert Law which is used to determine the transmitted ratio of incident light at targeting wavelength point. I_0 is the intensity of the incident light, I is the intensity of the transmitted light, α is the absorption coefficient of the material which is GaAs in this case, l is the thickness of the material which is assumed to be either 1.5 or 2 μm . By substituting the absorption coefficient at selected wavelength point, the transmitted ratio is around 20 % at 860 nm, which is the least absorbed wavelength, such that the targeting wavelength of the DBR is 860nm.

$$d = \frac{\lambda}{4n \times \cos\theta} \quad (2)$$

The refractive indices of GaAs and AlAs at this wavelength are around 3.64 and 2.99 respectively at 860 nm [6, 7]. The calculated thicknesses of GaAs and AlAs layer are

59nm and 72 nm [8]. In Equation 6.2, λ is the wavelength which is 860 nm in this case, θ is the incident angle which is set to be 0° by assuming the light enters the DBR orthogonally and n is the refractive index. The reflectance can be calculated using Equation 6.3 [8] which is listed below,

$$R = \left(\frac{1-Y}{1+Y}\right)^2 \text{ where } Y = \left(\frac{n_H}{n_L}\right)^{2p} \times \frac{n_H^2}{n_S \times n_0} \quad (3)$$

where n_H is high index of refraction, n_L is low index of refraction, n_S is the refractive index of substrate, n_0 is the refractive of medium material and normally the DBR consists of $(2p+1)$ layers in the stack. It is pointed out that $p = 10$ can guarantee a high reflectance for DBR implementation in solar cell [1,3]. Therefore, all DBRs discussed in this section contain 10 stacks of paired AlAs/GaAs structure. Under such circumstance, n_H is 3.64 (GaAs), n_L is 2.99 (AlAs), n_S and n_0 are also 3.64 since the DBR is inserted between the GaAs solar cell and the SLS DFs. The information of all three reference points has been listed in Table 6.1, which is also used to plot the curves in Figure 6.1. From the plot, it is obvious that the reflectance of DBR targeting 860nm stands out among all three structures. Despite the AlAs (70 nm) / GaAs (58 nm) structure has same reflectance as the AlAs (72 nm) / GaAs (59 nm) at 840 nm, the reflectance of the AlAs (72 nm) / GaAs (59 nm) structure exceeds 80% at 860 nm, whereas AlAs (70 nm) / GaAs (58 nm) could just reach 80%.

Table 6.1: Bragg Reflector design information for reference wavelength point at 800, 840 and 860nm.

Target Wavelength(nm)	800		840		860	
Absorption coefficient(cm^{-1}) [7]	15000		12000		9500	
Thickness (μm)	2	1.5	2	1.5	2	1.5

Transmitted ratio	0.07	0.13	0.09	0.16	0.15	0.24
Thickness(nm) AlAl/GaAs	68/56		70/58		72/59	
Reflective index AlAs/GaAs [8,9]	3.02/3.69		3.00/3.66		2.99/3.64	

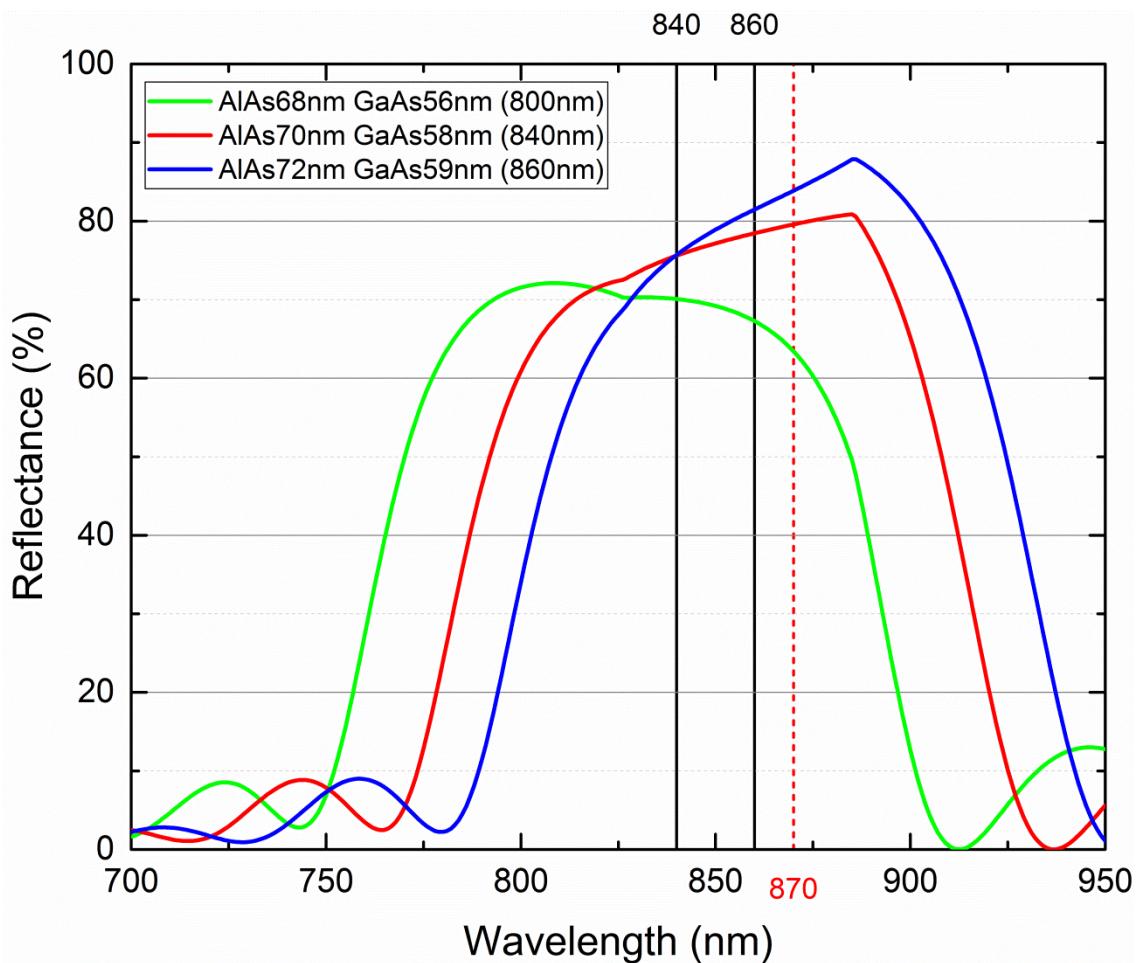


Figure 6.1: Reflectance of different DBRs (10 stacks) targeting different wavelengths, which are noted in legend box. Vertical lines indicate the selected wavelengths. Red dot line indicates the band gap of GaAs.

6.3 Chirped Distributed Bragg Reflector

The performance of normal DBR would be affected dramatically when the incident angle is non-zero [11]. As the incident angle increases, the peak reflectance would decrease for a constant number of pairs in the DBR [5]. In other words, by increasing θ

in Equation 6.2, the thickness d changes accordingly, which can be considered as broadening the reflectance wavelength band. An advanced DBR structure called Chirped DBR (CDBR) can resolve this problem. The CDBR varies the thickness arithmetically from the bottom of CDBR to the top surface, such that the impact of changing incident angle can be minimized. Five CDBR structures were designed to adjust the targeting reflectance bandwidth position, all of which consist of 10 pairs of AlAs/GaAs by modifying the AlAs (72 nm) / GaAs (59 nm) DBR structure which offers the best reflectance among the three DBR structure.

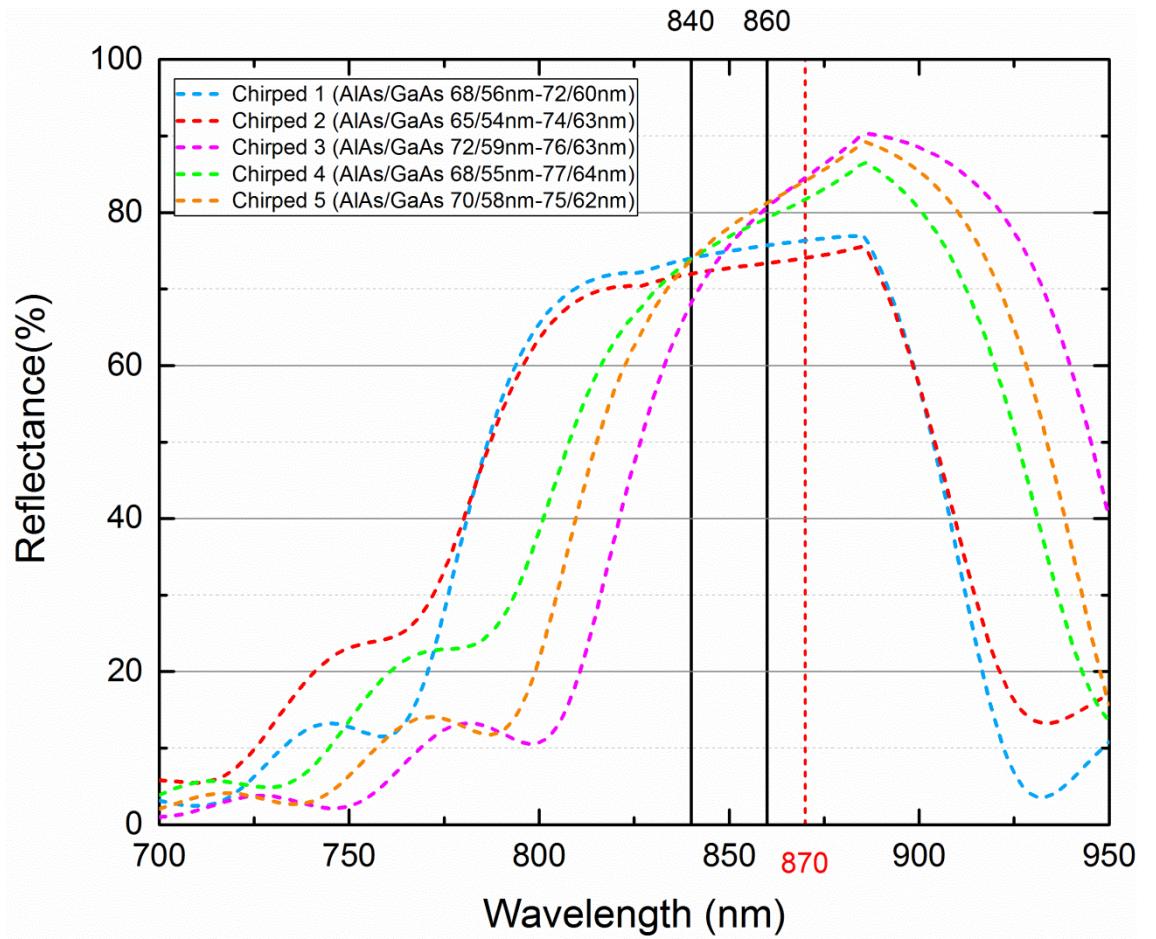


Figure 6.2: Reflectance of different CDBRs (10 stacks) with different Chirped structure. Vertical lines indicate the selected wavelengths. Red dot line indicates the band gap of GaAs.

The first one has bottom pair of AlAs (72 nm)/GaAs (60 nm) and top pair of AlAs (58 nm) / GaAs (56 nm) with decrement of 1 nm after repetition of every two pairs. The

second one has bottom pair of AlAs (74 nm)/GaAs (63 nm) and top pair of AlAs (65 nm)/GaAs (54 nm) with decrement of 1nm after every pair. The third one has bottom pair of AlAs (76 nm)/GaAs (63 nm) and top pair of AlAs (72 nm) / GaAs (59 nm) with decrement of 1nm after repetition of every two pairs. The forth one has bottom pair of AlAs (77 nm) / GaAs (64 nm) and top pair of AlAs (68 nm)/GaAs (56 nm) with decrement of 1nm after every pair. The last one has bottom pair of AlAs (75 nm)/GaAs (62 nm) and top pair of AlAs (70 nm)/GaAs (58 nm) with decrement of 1nm after repetition of every two pairs. The structural information of all CDBRs is listed in Table 6.2.

Table 6.2: Layer thickness information of five different proposed CDBRs

	Chirped 1	Chirped 2	Chirped 3	Chirped 4	Chirped 5
AlAs (nm)	68	65	72	68	70
GaAs (nm)	56	54	59	55	58
AlAs (nm)	68	66	72	69	70
GaAs (nm)	56	55	59	56	58
AlAs (nm)	69	67	73	70	72
GaAs (nm)	57	56	60	57	59
AlAs (nm)	69	68	73	71	72
GaAs (nm)	57	57	60	58	59
AlAs (nm)	70	69	74	72	73
GaAs (nm)	58	58	61	59	60
AlAs (nm)	70	70	74	73	73
GaAs (nm)	58	59	61	60	60
AlAs (nm)	71	71	75	74	74

GaAs (nm)	59	60	62	61	61
AlAs (nm)	71	72	75	75	74
GaAs (nm)	59	61	62	62	61
AlAs (nm)	72	73	76	76	75
GaAs (nm)	60	62	63	63	62
AlAs (nm)	72	74	76	77	75
GaAs (nm)	60	63	63	64	62

All five reflectance curves are plotted in Figure 6.2. Besides Chirped 1 and 2, which unable to reach 80 % at 860 nm, all other Chirped structures showcase similar tendency in general curve shape, but the gradient of the curve decrease following the order of Chirped 4, 5 and 3 in the range from 800 nm to 860 nm. Around 800 nm, Chirped 3 and 5 barely reflect, however the other Chirped structures have relatively high reflectance. The Chirped 3 and 5 are the modification of AlAs (72 nm) / GaAs (59 nm) DBR with the thickness of top pair thicker than other Chirped structures. This shifts the target wavelength to close to the GaAs band gap which is marked as red vertical line. Along with the target wavelength shift, the covered reflectance range shifts to higher wavelength as well.

6.4 Performance Comparison with Incident Angle

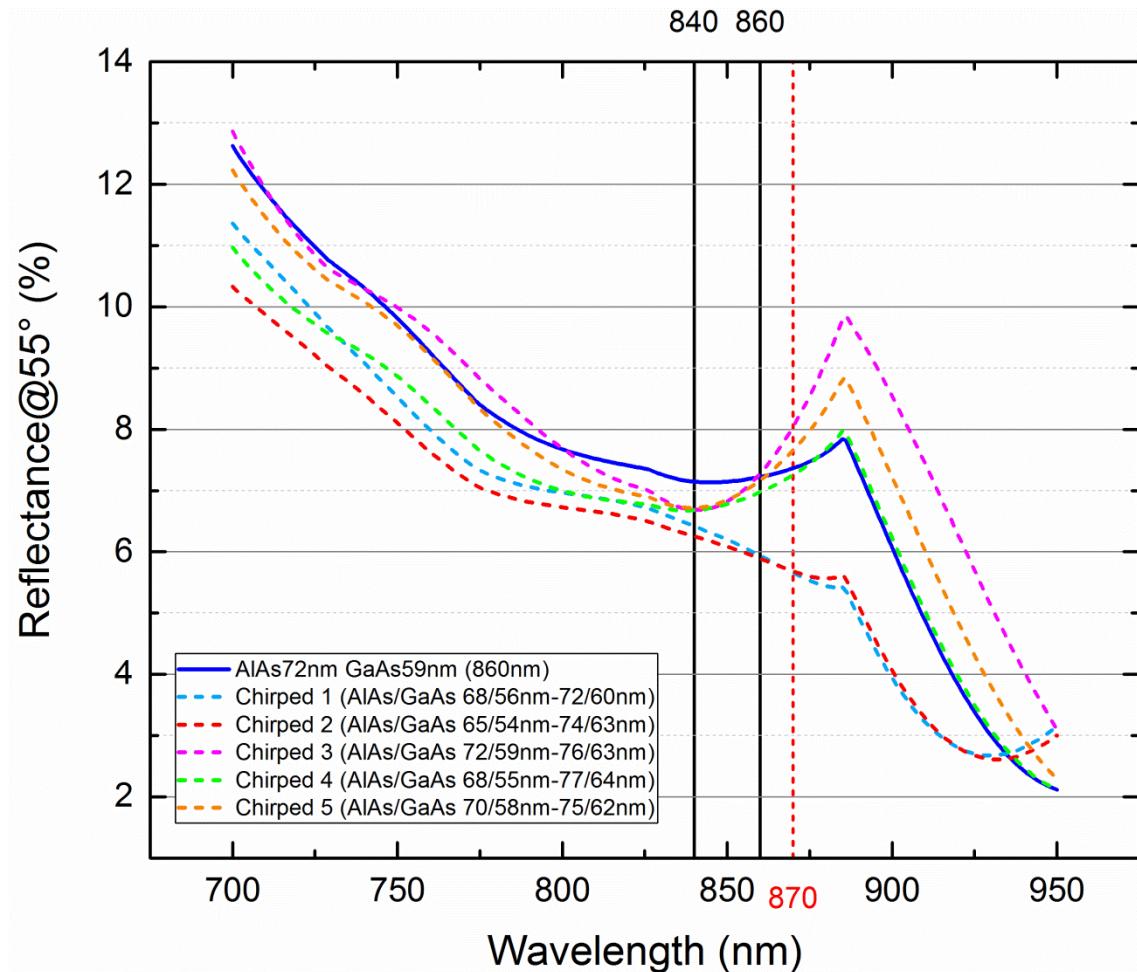


Figure 6.3: Reflectance of different CDBRs structures with AlAs (72nm) / GaAs (59nm) DBR, all of which are 10 stacks. Vertical lines indicate the selected reference wavelengths. Red dot line indicates the band gap of GaAs. The simulated incident angle is 55°.

It seems like it is hard to distinguish the reflectance at 860 nm amongst Chirped 3 to 5 at normal incident condition, therefore, the incident angle has been varied. As said above, the main feature of CDBR is minimizing the impact of incident angle from light irradiation. Taking 55° as the boundary condition, the reflectance curves are plotted in Figure 6.3. All CDBRs showcased significant low reflectance with such high incident angle. However, all DBRs and CDBRs are built beneath one GaAs cell. In this case, the light enters the GaAs solar cell first, then to the DBR, such that the transmitted angle from solar cell will be the incident angle of the DBR.

Snell's Law is employed to determine the transmitted angle:

$$n_1 \sin \theta_1 = n_2 \sin \theta_2 \quad (3)$$

where n is the refractive index and θ is the angle measured from the normal to the interface. Therefore, if selecting the incident angle to be 55° for the boundary condition, the transmitted angle will be 16° . Figure 6.4 exhibits the simulated reflectance of AlAs (72 nm) / GaAs (59 nm) DBR and all CDBR to investigate the performance under the situation where incident angle equals 16° .

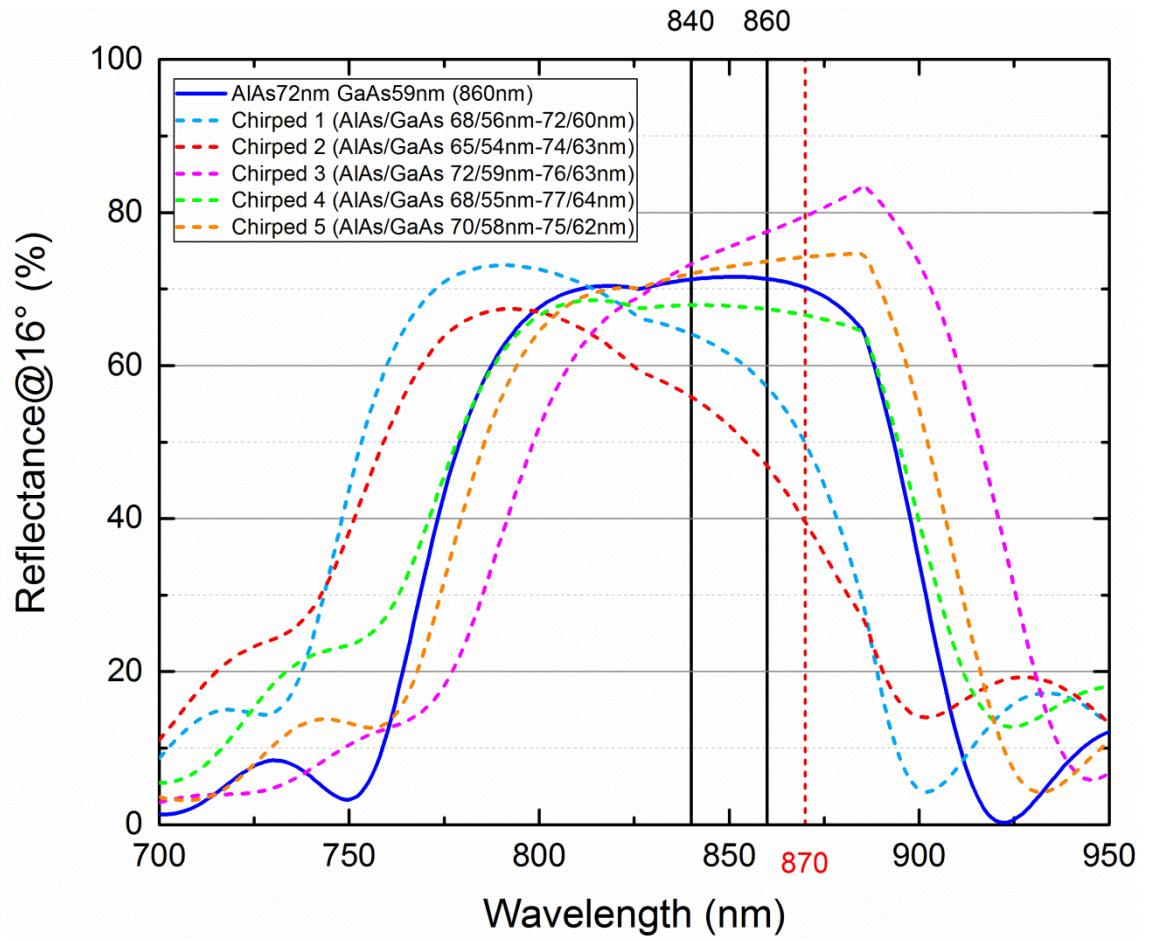


Figure 6.4: Reflectance of different CDBRs structures with AlAs (72 nm) / GaAs (59 nm) DBR, all of which are 10 stacks. Vertical lines indicate the selected reference wavelengths. Red dot line indicates the band gap of GaAs. The simulated incident angle is 16° .

From the plot, it is obvious that AlAs (72 nm) / GaAs (59 nm) DBR shows a decent performance as the reflectance of the target range (800-860nm) does not drop dramatically, keeping around 70 %. On the contrary, Chirped 1 and 2 showcase significant reflectance drop at 840 nm and 860 nm. Interestingly, the reflectance curve of Chirped 4 in the range of 800-860 nm shares the similar shape with Chirped 3 with even lower reflectance in this range. At 800 nm, Chirped 5 has reflectance exceeding 60 % which is higher than Chirped 3 (around 55 %). Reflectance curves of AlAs (72 nm) / GaAs (59 nm) DBR and Chirped 3 and 5 cross around 840nm, the reflectance of all DBRs exceeds 70 % with Chirped 3 shows slight advantage. However, after 840 nm, all reflectance curves start to separate with the increasing of wavelength. At 860 nm, AlAs (72 nm) / GaAs (59 nm) DBR keeps the reflectance at 70 %. Chirped 5 has better performance compared to AlAs (72 nm) / GaAs (59 nm) DBR, but the reflectance of Chirped 3 is very close to 80% at this wavelength. This separation continues and the separation becomes more obvious at the band gap (870 nm). When taking the performance at all target wavelengths into consideration, the incident angle impact on AlAs (72 nm) / GaAs (59 nm) DBR is not as severe as expected and Chirped 3 has the best response with respect to the impact of incident angle.

The situation above is the boundary condition for the maximum incident angle. It is worth checking the entire varying angle range to ensure the reflectance maintains at high level. Figure 6.5 shows the plots of the reflectance at three selected wavelength of AlAs (72 nm) / GaAs (59 nm) DBR and Chirped 3 CDBR with the variation of incident angle from normal to boundary condition. It is obvious that the reflectance at 800nm increases with the increment of the incident angle for both DBRs, which agrees with the calculation based on Equation 4.2 and 4.3. For AlAs (72 nm) / GaAs (59 nm) DBR, the reflectance at 860 nm starts to drop from 6° and the gradient become more dramatic

with the increment of incident angle, which ends lower than 70% at the boundary condition. However, the reflectance of Chirped 3 stays above 80% until 10° and remains above 75 % even at 16°. The reflectance at 840nm of AlAs (72 nm) / GaAs (59 nm) DBR shares the similar tendency with 860nm, which starts from slightly above 75% ends right at 70 %. On the contrary, the reflectance at 840 nm of Chirped 3 exhibits an overall increasing tendency with starting reflectance slightly lower than 70 % and ends a little lower than 75 %.

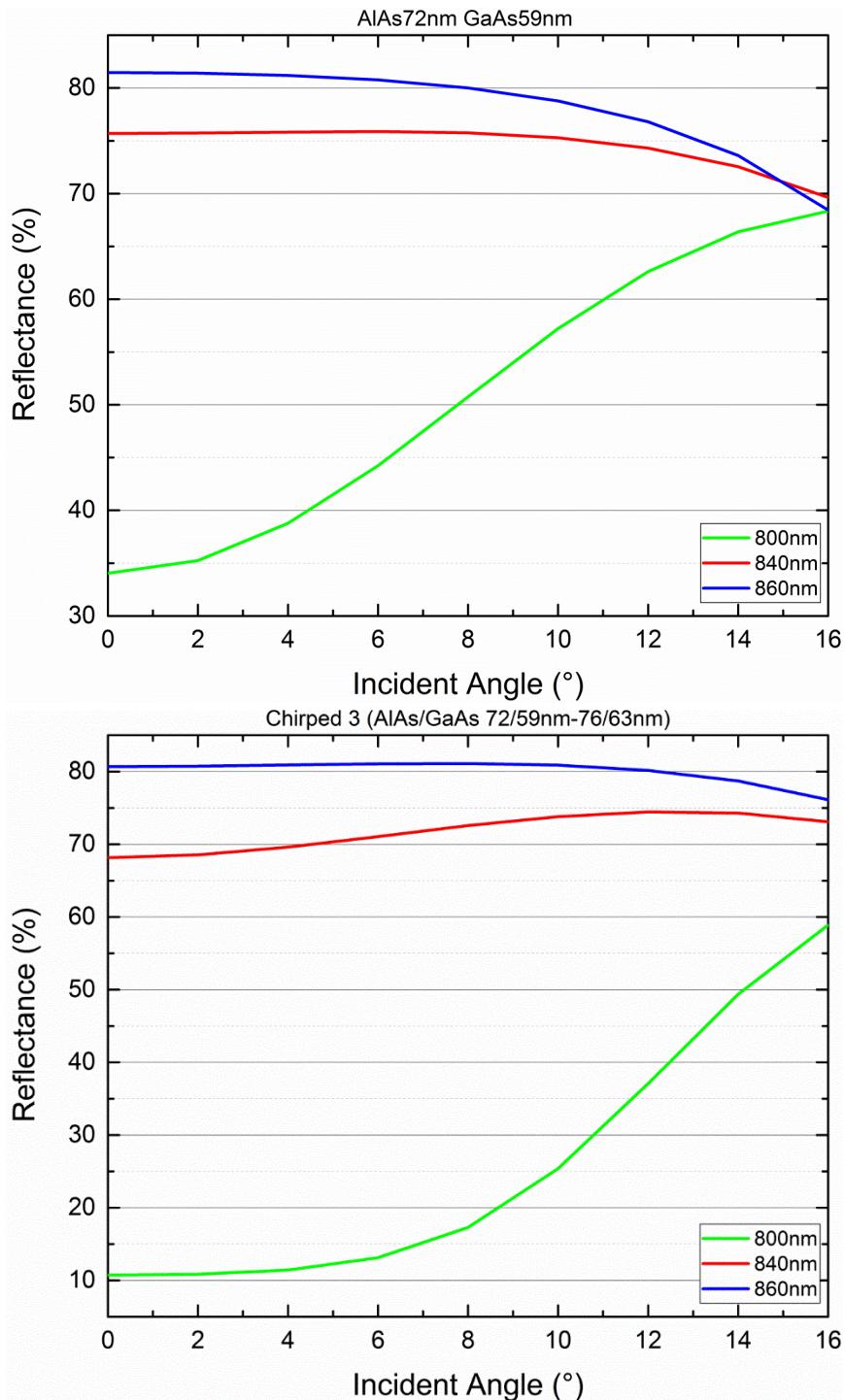


Figure 6.5: Reflectance at three selected wavelength of AlAs (72nm) / GaAs (59nm) DBR and Chirped 3 CDBR with the variation of incident angle.

6.5 Conclusion

To enhance the light absorption, DBR structure was investigated. Three targeting wavelength points were selected to design DBRs. When considering the incident angle

problem in practical situation, five CDBRs were proposed to minimize the impact from incident angle issue. After comparing reflectance of the overall performance, Chirped 3 is more reliable that the impact of incident angle issue can be minimized by maintaining the reflectance at high level throughout the incident angle variation range. With this being concluded, the Chirped 3 structure displays the best performance among all the Bragg reflectors. One note should be made that this chapter only provides one of the designing rules and verification methods of CDBR implementation for GaAs solar cell device application in the perspective of theoretical modelling. The performance of Chirped 3 structure is only valid among the proposed five CDBRs, which cannot be treated as the ultimate CDBR that suits the single junction GaAs solar cell the best. Further investigation and research involving software simulation along with experimental fabrication and measurement is needed to optimize the CDBR design in the future work.

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Chapter 7 Conclusion and Future Work

7.1 Conclusion

This thesis focused on III-V integration with Si by taking two fundamental issues into consideration. One is GaAs fabrication on offcut Ge substrate targeting the implementation of this on virtual Ge substrate, the other is employing strained layer superlattice structure as dislocation filter to generate a suitable surface to later device fabrication.

Firstly, several fundamental issues regarding how to improve the structural quality of GaAs epitaxy on offcut Ge substrate have been examined. The formation of double atomic steps and how this configuration would improve the quality of GaAs deposition has been demonstrated by comparing the effect of high temperature anneal prior to initiation of epitaxy. The importance of starting epitaxy with MEE and how different MEE material would affect the structural quality have been examined. Whether group V material with less thermal energy (i.e. As₄) would improve the surface morphology was investigated by comparing the RMS value based on AFM scans. Using various characterization technique, the quality of GaAs epitaxy on offcut Ge substrate can be improved by a combination of employing high temperature anneal prior to growth, initiating the MEE at low temperature with group V material, applying group V material with low thermal energy throughout the entire epitaxy process and use alternative MEE material to flatten the rough substrate surface when needed.

Regarding the dislocation filter structure, the goal was to select a suitable material for use in SLS DF structure fabrication. By taking the mechanism of dislocation motion into consideration, two factors that determine the dislocation motion velocity were conceptional converted to material properties. To ensure high performance in

dislocation reduction, material with low band gap energy (E_g) and high shear modulus (G) is ideal for SLS DFs. Therefore, after investigated several III-V compounds and III-V alloys, innovative material GaAsSb was selected for SLS DFs fabrication. Along with the elaborated epitaxy procedure, investigation of how different As sources could affect the structural quality of SLS system has been conducted by applying As₄ and As₂ on identical SLS structure. AFM, XRD and TEM were employed to judge the performance and function of SLS DF. With good agreement among these three characterization results, As₂ offered a smoother sample surface, better structural quality and less SLS deformation against As₄. The threading dislocation density for all samples were calculated. The average dislocation densities (from AlAs/Si interface) were calculated by XRD rocking curves, whereas the surface dislocation densities were calculated by the conventional cross section TEM method. The conclusion can be drawn that SAMPLE *GaAsSb(As₂)* sample showed the best dislocation density reduction ability which is a great approval of the innovation about material selection.

7.2 Future Work

7.2.1 GaAs/vGe

As discussed in Section 5.2.1, cycled annealing would effectively reduce the dislocation density while fabricating SLS DF. This could be borrowed to investigate whether the quality of GaAs epitaxy on vGe could be improved by applying post grown annealing to the sample. When the fabrication process is finished, firstly the sample would be cooled down to room temperature and then annealed at 800°C for 30 min. this annealing process would be repeated for several times to allow a good understanding of the role of the anneal to be developed. The other aspect worth taking a further exam is whether longer annealing time after the RHEED pattern exhibited a double atomic steps feature would affect the as-grown surface morphology.

7.2.2 SLS DFs

The working mechanism and fabrication along with the performance of SLS DFs have been demonstrated in this work. However, based on the fabrication procedure elaborated in Chapter 5, several aspects still can be improved to investigate and improve the performance of SLS DFs.

Firstly, as discussed in Section 5.3.1, the cool down rate plays an important role in thermal gradient across samples. Although the cool down rate was lowered to $2^{\circ}\text{C}/\text{min}$, this rate may be too aggressive since the SLS undulation still exists in SAMPLE $\text{GaAsSb}(\text{As}_2)$ sample. This rate can be turned lower to prevent the issue resulted from thermal expansion coefficient mismatch. Secondly, regarding the threading dislocation reduction result, it has been shown that the amount of annealing cycles plays a more effective role than annealing time [1]. Therefore, more cycles of 660°C anneal should be adapted to further activate the annihilation of threading dislocations. Thirdly, the III-V alloys listed in Table 5.2 pose no limitation to material selection range. Other III-V alloys with low band gap energy and high shear modulus could also be taken into consideration. Fourthly, as shown in the cross section TEM images in Chapter 5, the majority of dislocations are annihilated in the first two or three SLS layers, the composition of III-V alloy in the SLS stacks can be tuned to provide gradually changing shear modulus and band gap energy to boost the dislocation reduction ability. By combining the idea of choosing other SLS materials and providing gradually changing shear modulus and band gap energy, one innovative SLS stacks involving two different III-V alloys can be proposed. By keeping the same stacking number of SLS layers, the material employed for first two layers SLS can be high shear modulus material, the other two layers can be low band gap energy material to achieve the goal of boosting the performance of threading dislocation reduction. One reversed setting can be applied to

investigate which stacking option would provide better performance. Many research groups have demonstrated using quantum dots (QDs) structure as dislocation filter for laser fabrication [2-5]. The feasibility of combining SLS and QDs together as an innovative DFs structure to offer enhancing performance is worth investigating. Also, as mentioned in Figure 5.1, II-IV compounds offer lower Q at high band gap energy compared to III-V material. Therefore, the performance of SLS DFs fabricated with II-IV material is worth investigating.

7.2.3 Distributed Bragg Reflector

With this CDBR insertion between the GaAs and the solar cell device, the quality and the performance of the solar cell will be improved. Since the DBR and SLS DFs share the same pairing and altering structure, the possibility of combining these two structures to minimize the thickness under the solar cell was investigated. It turns out that to avoid introducing new defects to the structure, the critical thickness of SLS must be 10-20nm which is too thin for the DBR [1], needless to say the 300nm spacing layer in the SLS DFs structure. With this being addressed, it seems unreasonable to combine DBR and SLS DFs together. However, it still worth further investigation to minimize the thickness under the solar cell in the future works.

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