

# Homework 3

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CIS-655 ADVANCED COMPUTER ARCHITECTURE

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**Question 1:**

A. Assume no forwarding unit.

Instruction	Clock Cycles																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
LD R1, 0(R2)	IF	ID	EX	M	W													
DADDI R1, R1, #1		IF	S	S	ID	EX	M	W										
SD 0(R2), R1					IF	S	S	ID	EX	M	W							
DADDI R2, R2, #4								IF	ID	EX	M	W						
DSUB R4, R3, R2									IF	S	S	ID	EX	M	W			
BENZ R4, Loop												IF	S	S	ID	EX	M	W

Comments: In clock cycle 9, the instruction can be DADDI R2, R2, #4 instruction can be decoded as the ALU executes the previous instruction because there are no data dependencies between the two instructions.

B. Assume forwarding unit.

Instruction	Clock Cycles																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
LD R1, 0(R2)	IF	ID	EX	M	W													
DADDI R1, R1, #1		IF	ID	S	EX	M	W											
SD 0(R2), R1			IF	S	ID	EX	M	W										
DADDI R2, R2, #4					IF	ID	EX	M	W									
DSUB R4, R3, R2						IF	ID	EX	M	W								
BENZ R4, Loop							IF	ID	EX	M	W							

**Question 2:**

Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache.

Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle. What is the average memory access time?

$$AMAT = HitTime_{L_1} + MissRate_{L_1}(HitTime_{L_2} + LocalMissRate_{L_2} * MissPenalty_{L_2})$$

$$MissRate_{L_1} = \frac{\frac{Misses \text{ per } 1,000 \text{ instructions}}{1,000}}{\frac{Memory \text{ Access Per Instruction}}{1}} = \frac{\frac{40}{1,000}}{1} = 0.04$$

$$LocalMissRate_{L_2} = \frac{\frac{Misses \text{ per } 1,000 \text{ instructions}}{1,000}}{\frac{Memory \text{ Access Per Instruction}}{1}} = \frac{\frac{20}{40}}{1} = 0.5$$

$$AMAT = 1 + 0.04(10 + 0.5 * 200) = 5.4 \text{ cycles}$$

Question 3:

## Performance Evaluation

You are investigating the possible benefits of a way-predicting level 1 cache. Assume that the 32 KB two-way set-associative single-banked level 1 data cache is currently the cycle time limiter. It takes one cycle to hit this cache.

As an alternate cache organization, you are considering a way-predicted cache modeled as a 16 KB direct-mapped cache with 85% prediction accuracy. Unless stated otherwise, assume a mispredicted way access that hits in the cache takes one more cycle.

What is the average memory access time of the current cache versus the way-predicted cache?

Given:

Miss rate for 2 way Least Recently Used (LRU) is 0.0056

Miss rate for Direct-mapped is 0.015

Miss penalty is 20 cycles for both types

Hit time= Hit Rate\* Hit Cycles

$$AMAT = HitTime + (MissRate * MissPenalty)$$

For the current system (two-way, set-associative single-banked level 1 data cache): Miss Rate = 0.0056. Miss Penalty = 20 cycles. Hit Time = 1 – Miss Rate.

$$AMAT = (1 - MissRate) + (MissRate * MissPenalty)$$

$$AMAT = 0.9944 + (0.0056 * 20) = 1.1064$$

For the 16KB way-predicted, direct-mapped cache, prediction accuracy = 85%.

$$AMAT = HitTime + (MissRate * MissPenalty)$$

$$HitTime = HitRate * HitCycles$$

$$HitRate = 1 - MissRate$$

$$HitCycles = CyclesCorrect * PercentageCorrect + CyclesIncorrect * PercentageIncorrect$$

$$HitCycles = 1 * 0.85 + 2 * (1 - 0.85) = 1.15 \text{ cycles}$$

$$HitTime = (1 - MissRate) * 1.15 = (1 - 0.015) * 1.15 = 1.13275$$

$$AMAT = 1.13275 + (0.015 * 20) = 1.43275$$

Therefore, the average memory access time for the way-predicted cache is greater than that of the current cache system (two-way, set-associative single-banked level 1 data cache).