## CSC258 Prelab Four

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February 1, 2017

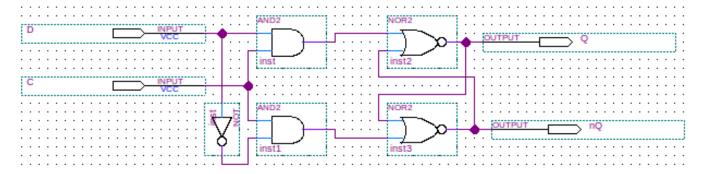
### 1 SR Latch Truth Table

$\mathbf{C}$	$\mathbf{S}$	$\mathbf{R}$	Q	Q'
0	Χ	Χ	Χ	Χ
1	0	0	X	X
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

#### Notes:

- The clock does not play a major role in the truth table
  - When the clock is 0, we are always in a latch state and retain the previous value (Denoted by X)

### 2 Diagram of a D latch



# 3 Diagram of a D Flip Flop

