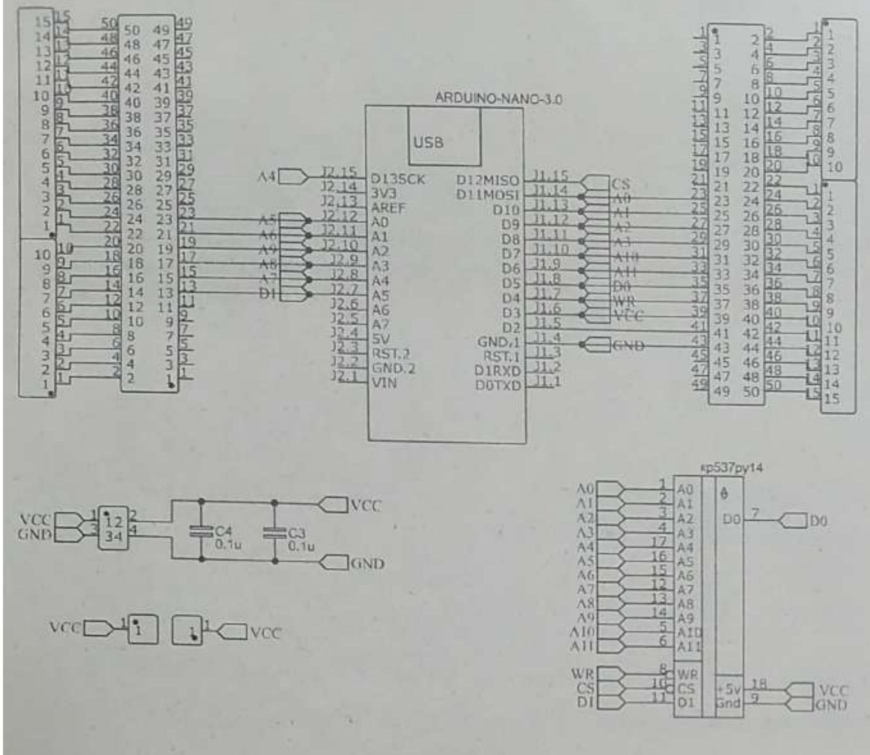
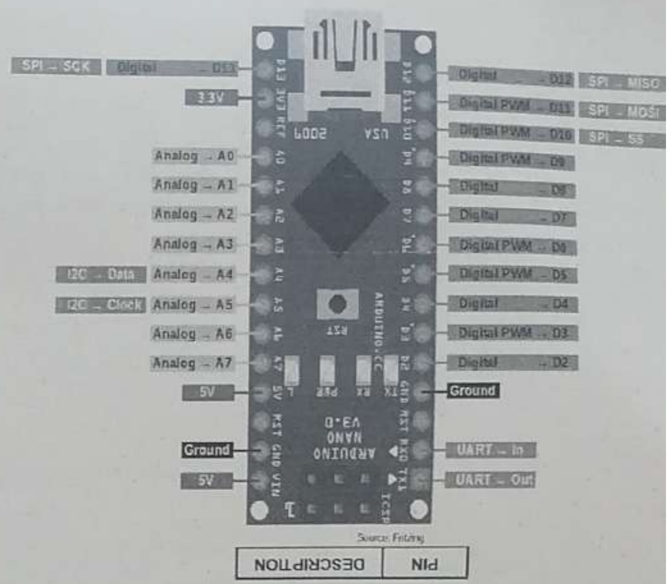
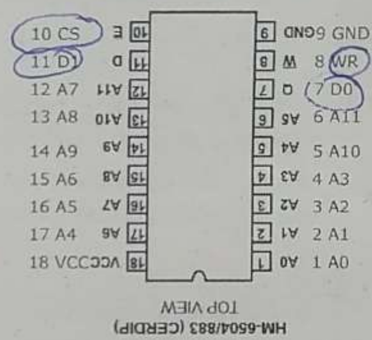




Вывод	Назначение	Вывод	Назначение
№1	Вход адреса A0	№10	Вход сигнала «Выбор микросхемы» CS
№2	Вход адреса A1	№11	Вход информационный D1
№3	Вход адреса A2	№12	Вход адреса A7
№4	Вход адреса A3	№13	Вход адреса A8
№5	Вход адреса A10	№14	Вход адреса A9
№6	Вход адреса A11	№15	Вход адреса A6
№7	Вывод информационный D0	№16	Вход адреса A5
№8	Вход сигнала «Запись» WR	№17	Вход адреса 4
№9	Общий вывод 0V	№18	Вывод питания от источника напряжения U



TITLE: Sheet_2 REV: 1.0

嘉立创EDA Company: Your Company Sheet: 1/1

Date: 2022-10-28 Drawn By: Mikita Malyeika

Arduino nano 3.0

Pin AtM328	Pin перехідн.	Pin РУ14
~~21~~ 23 PC0	A0	A5 16
~~24~~ 24 PC1	A1	A6 15
25 PC2	A2	A9 14
26 PC3	A3	A8 13
27 PC4	A4	A7 12
28 PC5	A5	DI 11
16 PB4	D12	CS 10
15 PB3	D11	A0 1
14 PB2	D10	A1 2
13 PB1	D9	A2 3
12 PB0	D8	A3 4
11 PD7	D7	A10 5
10 PD6	D6	A11 6
9 PD5	D5	D0 7
PD4	D4	WR 8
2 PD3	D3	Vcc 18 ?
		GND 9 ?
17. PB5	D13	A4 17

~~Pin P~~

0 = 1

D

A0÷A11

A

ещі дві руки
ещі дві руки
ещі дві руки
ещі дві руки

Timing Waveforms (Continued)

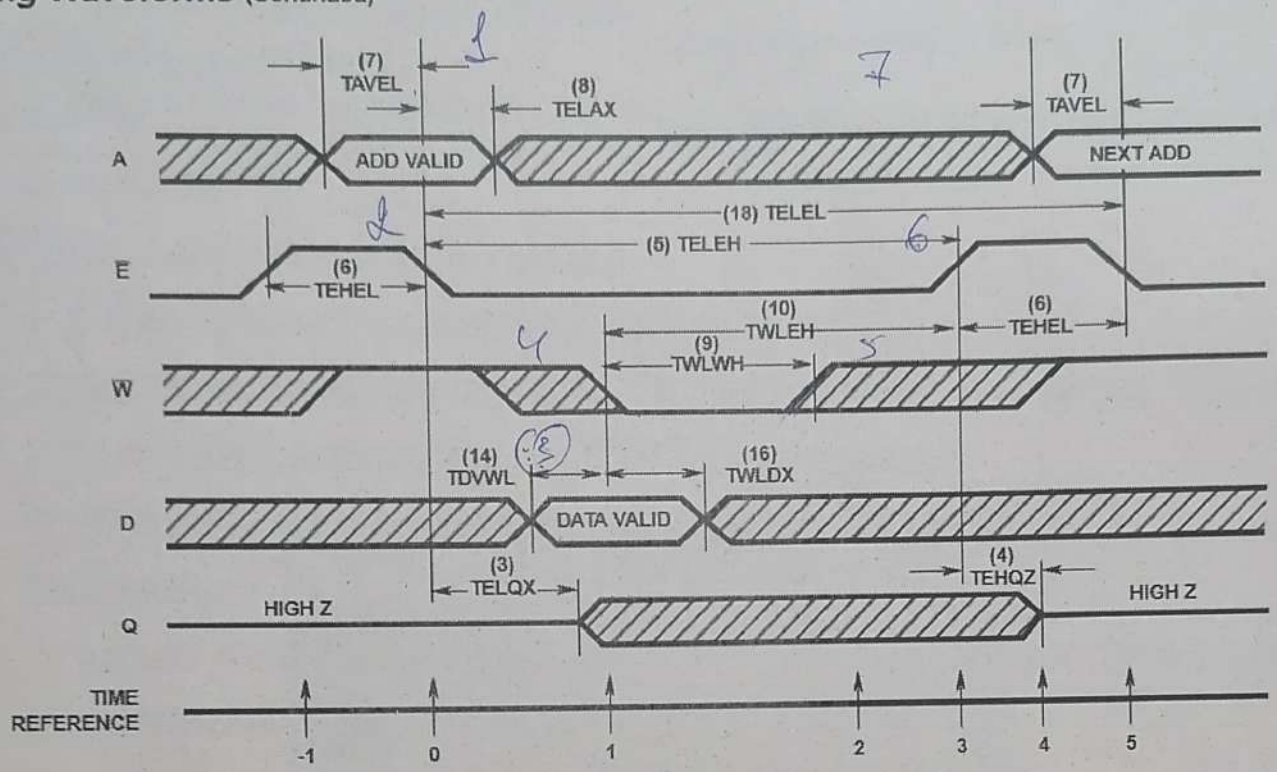


FIGURE 3. LATE WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↘	X	V	X	Write Begins, Data is Latched
2	L	H	X	X	X	Write In Progress Internally
3	↗	H	X	X	X	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write, the output is guaranteed to remain high impedance, and in the read-modify-write, the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data setup, data hold, write setup and write pulse widths are observed.

Timing Waveforms

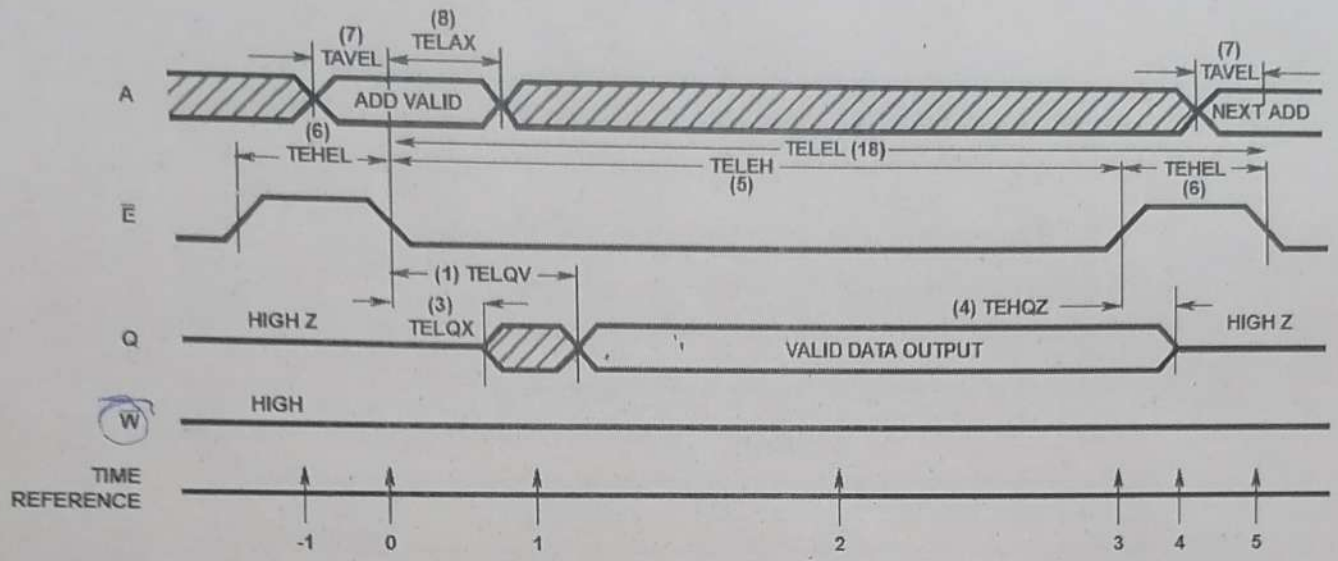


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS			OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	Q	
-1	H	X	X	Z	Memory Disabled
0	↘	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↗	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on-chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all input, and ready the RAM for the next memory cycle (T = 4).

Timing Waveforms (Continued)

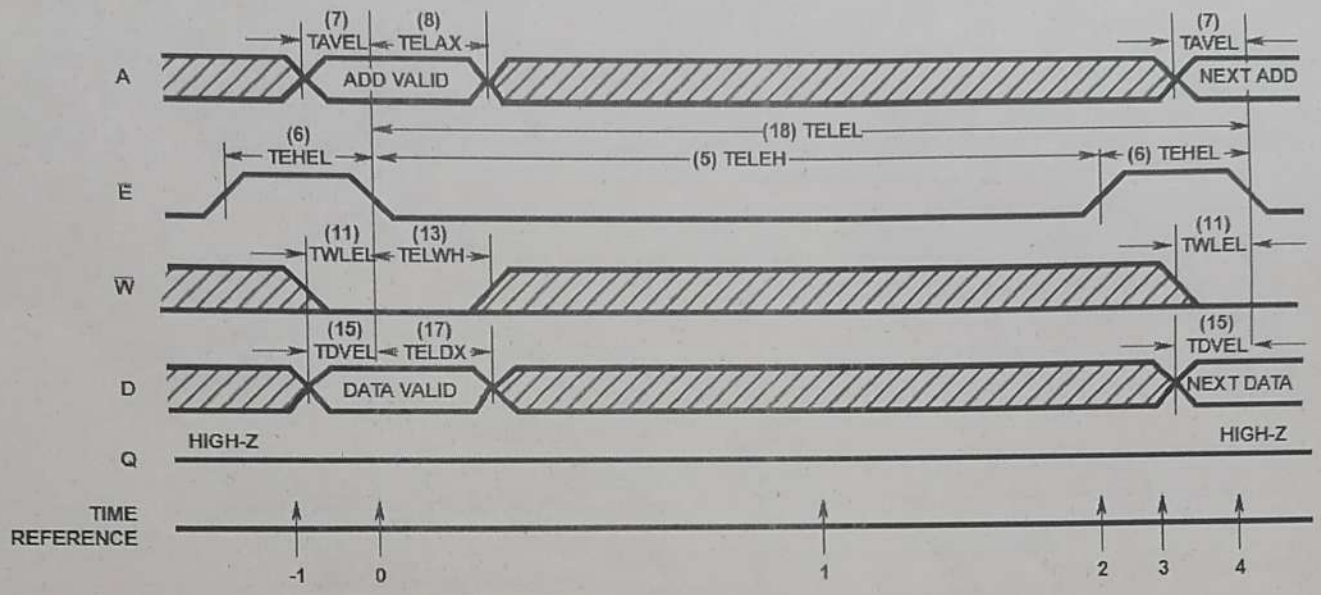


FIGURE 2. EARLY WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↗	X	X	X	Z	Write Completed
3	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
4	↘	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on-chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore, data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state, the output buffer and all inputs are disabled and all signals are unlatched. The device is now ready for the next cycle.

Die Characteristics

DIE DIMENSIONS:
136 x 169 x 19 ±1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

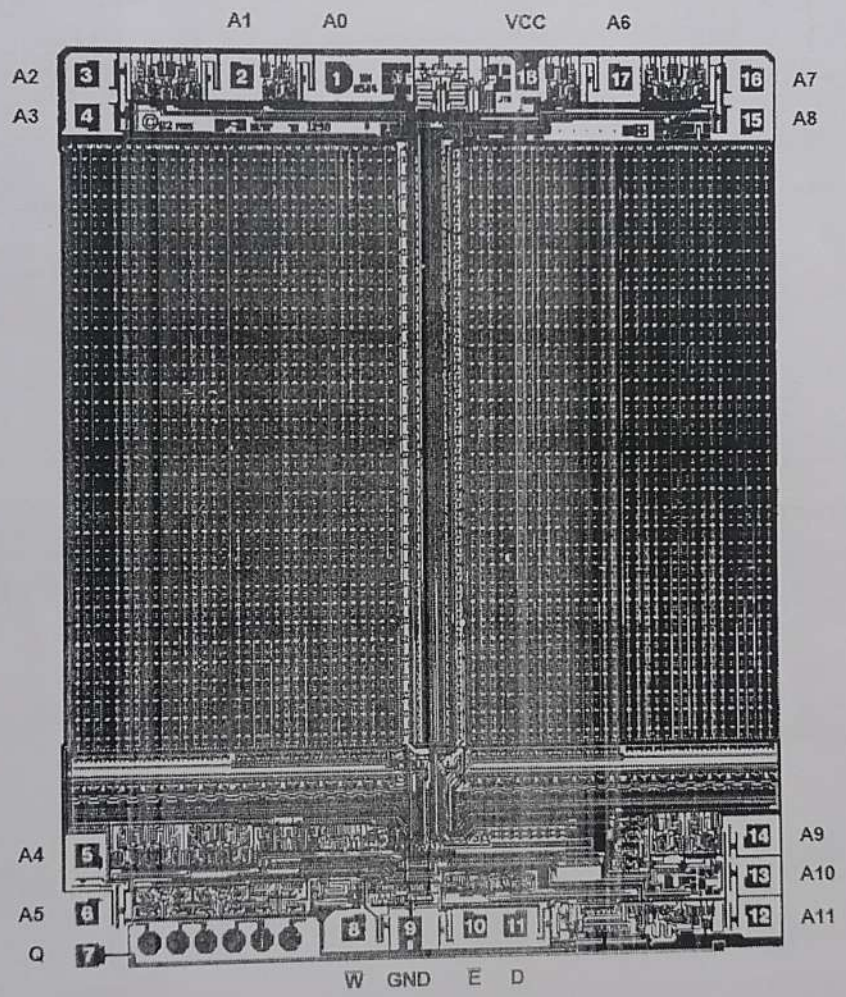
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.79×10^5 A/cm^2

LEAD TEMPERATURE (10s soldering):
≤ 300°C

Metallization Mask Layout

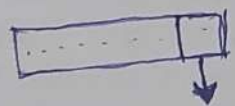
HM-6504/883



NOTE:

1. Pin numbers correspond to DIP Package only.

~~PC0~~	A0	PB3
~~C1~~	A1	PB2
~~C2~~	A2	B1
~~C3~~	A3	B0
	A4	B5
	A5	C0
	A6	C1
	A7	C4
	A8	C3
	A9	C2
	A10	D7
	A11	D6
	DI	C5
	D0	D5
	CS	B4
	WR	D4
		+Un



if a=0
b=0
a=1
b=1

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
11	10	9	8	7	6	5	4	3	2	1	0
D6	D7	C2	C3	C4	C1	C0	B5	B0	B1	B2	PB3

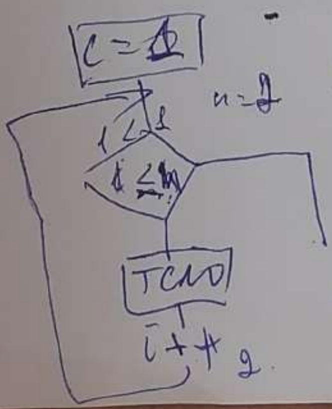
+1
+ 2
+ 3
+ .

Port C.1 = 0a0
Port C.1 = 0
Port C.1 = 1

B3 = A = PB3 = A0[0]
B2 = A[1]

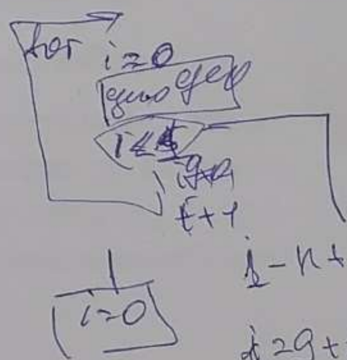
сувен if

a ~~inte~~;
a = 00180 ;
~~8:20~~ ~~10:20~~ if a = 0 { ~~Port~~ Pin B.3 = 0
~~9:20~~ else PinB.3 = 1 .
a >> 1



1 - 2 - 1

i = 1
i < 2
n = 2 .
i = 1 - 1 раз
i = 2 - 1 раз
2 раза.
i ≤ n до n раз
i < n до n-1 раз



1 - n + 1 = 2 раза
i = 9 + 1
n = 2 i < n
i ≤ n раз . i = 1
до 1 раз n = 1

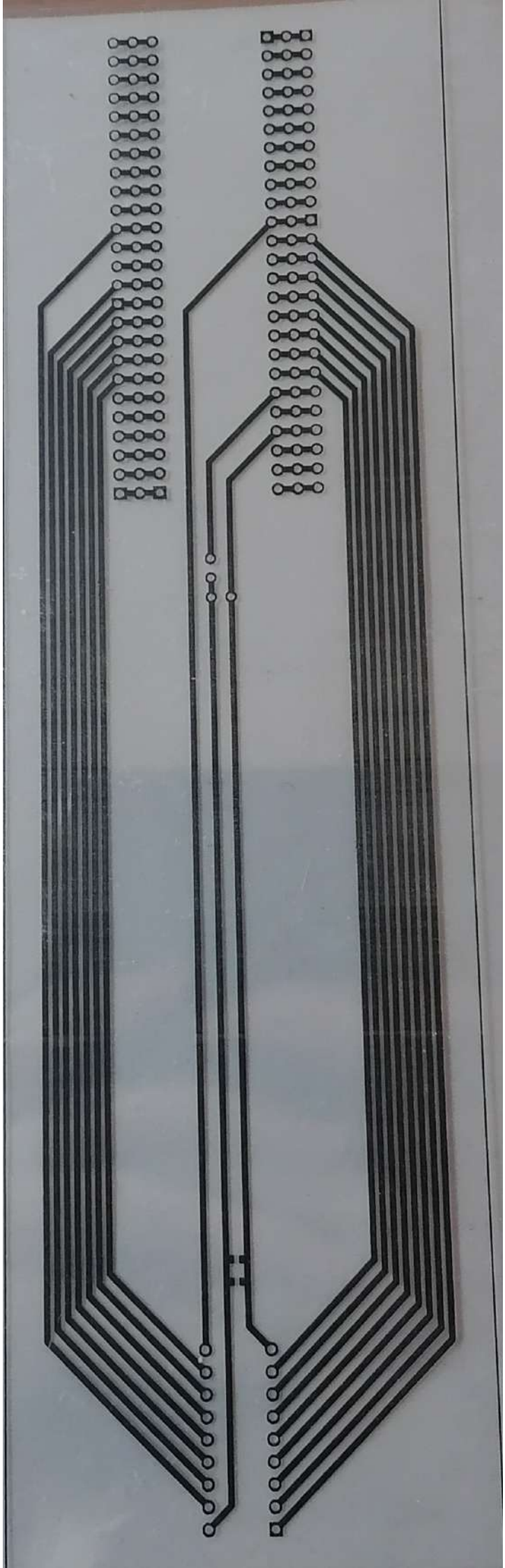
Ex 9.2

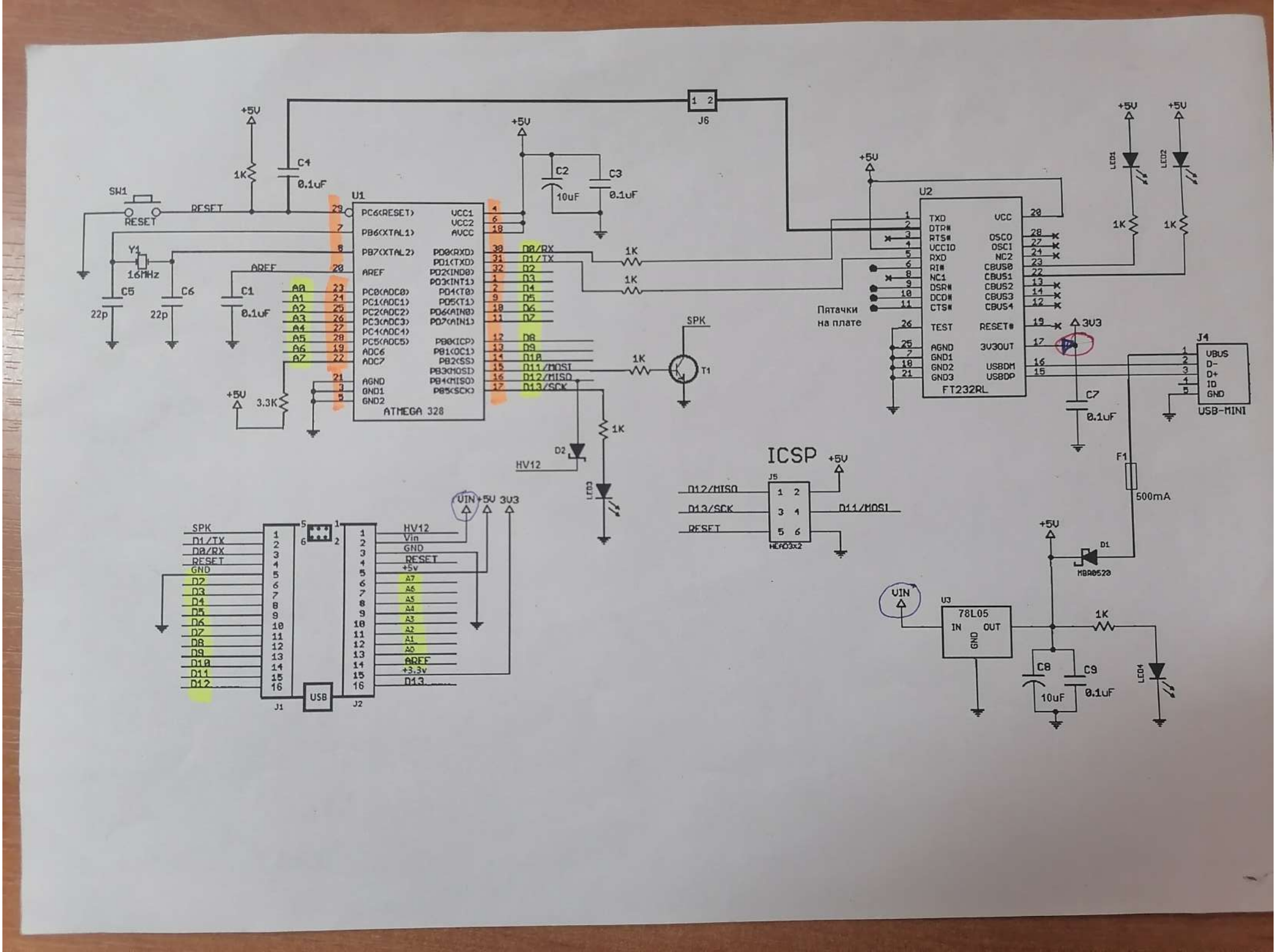
```
for (i=1; i<=11; i++)
{ a = a & 0x0001 & 0;
if a { a = b
       b = 0x0001 & b;
       if (b=0) Pin C.1 = 0;
       else Pin C.1 = 1;
       a >>= 1; }
       b = 0x0001 & a
       if (b=0) Pin C.2. = 0
```

```
int a=0; b=0;
a = b;
b = 0x0001 & a;
if (b==0) Port B.3 = 0;
else Port B.3 = 1;
b = 0x0010 & a;
if (b==0) Port B.2 = 0;
else Port B.2 = 1;
b = 0x0040 & a;
if (b==0) Port B.1 = 0
else Port B.1 = 1
```

0.1

Address.(a);




U1
ATMEGA 328
U2
FT232RL
Патачки
на плате
ICSP
HERO3x2
J1
J2
J4
USB-MINI
J5
J6
SW1
RESET
Y1
16MHz
C1
C2
C3
C4
C5
C6
C7
C8
C9
10uF
0.1uF
22p
1K
3.3K
T1
SPK
D1
D2
F1
500mA
MBR0520
U3
78L05
IN
OUT
GND
VIN
+5V
3V3
HV12
LED1
LED2
LED3
LED4
USB
D0/RX
D1/TX
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11/MOSI
D12/MISO
D13/SCK
RESET
AREF
A0
A1
A2
A3
A4
A5
A6
A7