ARM® Instruction Set
Quick Reference Card

Key to Tables	
{cond}	Refer to Table **Condition Field**. Omit for unconditional execution.
<Operand2>	Refer to Table **Flexible Operand 2**. Shift and rotate are only available as part of Operand2.
<fields>	Refer to Table **PSR fields**.
<PSR>	Either CPSR (Current Processor Status Register) or SPSR (Saved Processor Status Register)
{S}	Updates condition flags if S present.
C*, V*	Flag is unpredictable in Architecture v4 and earlier, unchanged in Architecture v5 and later.
Q	Sticky flag. Always updates on overflow (no S option). Read and reset using MRS and MSR.
x,y	B meaning half-register [15:0], or T meaning [31:16].
<immed_8r>	A 32-bit constant, formed by right-rotating an 8-bit value by an even number of bits.
{X}	RsX is Rs rotated 16 bits if X present. Otherwise, RsX is Rs.
<prefix>	Refer to Table **Prefixes for Parallel instructions**
<p_mode>	Refer to Table **Processor Modes**
R13m	R13 for the processor mode specified by <p_mode>
{endianness}	Can be BE (Big Endian) or LE (Little Endian).

<a_mode2>	Refer to Table **Addressing Mode 2**.
<a_mode2P>	Refer to Table **Addressing Mode 2 (Post-indexed only)**.
<a_mode3>	Refer to Table **Addressing Mode 3**.
<a_mode4L>	Refer to Table **Addressing Mode 4 (Block load or Stack pop)**.
<a_mode4S>	Refer to Table **Addressing Mode 4 (Block store or Stack push)**.
<a_mode5>	Refer to Table **Addressing Mode 5**.
<reglist>	A comma-separated list of registers, enclosed in braces { and }.
<reglist-PC>	As <reglist>, must not include the PC.
<reglist+PC>	As <reglist>, including the PC.
{!}	Updates base register after data transfer if ! present.
+/-	+ or –. (+ may be omitted.)
§	Refer to Table **ARM architecture versions**.
<iflags>	Interrupt flags. One or more of a, i, f (abort, interrupt, fast interrupt).
{R}	Rounds result to nearest if R present, otherwise truncates result.

Operation		§	Assembler	S updates	Q	Action
Arithmetic	Add		ADD{cond}{S} Rd, Rn, <Operand2>	N Z C V		Rd := Rn + Operand2
	with carry		ADC{cond}{S} Rd, Rn, <Operand2>	N Z C V		Rd := Rn + Operand2 + Carry
	saturating	5E	QADD{cond} Rd, Rm, Rn		Q	Rd := SAT(Rm + Rn)
	double saturating	5E	QDADD{cond} Rd, Rm, Rn		Q	Rd := SAT(Rm + SAT(Rn * 2))
	Subtract		SUB{cond}{S} Rd, Rn, <Operand2>	N Z C V		Rd := Rn – Operand2
	with carry		SBC{cond}{S} Rd, Rn, <Operand2>	N Z C V		Rd := Rn – Operand2 – NOT(Carry)
	reverse subtract		RSB{cond}{S} Rd, Rn, <Operand2>	N Z C V		Rd := Operand2 – Rn
	reverse subtract with carry		RSC{cond}{S} Rd, Rn, <Operand2>	N Z C V		Rd := Operand2 – Rn – NOT(Carry)
	saturating	5E	QSUB{cond} Rd, Rm, Rn		Q	Rd := SAT(Rm – Rn)
	double saturating	5E	QDSUB{cond} Rd, Rm, Rn		Q	Rd := SAT(Rm – SAT(Rn * 2))
	Multiply	2	MUL{cond}{S} Rd, Rm, Rs	N Z C*		Rd := (Rm * Rs)[31:0]
	and accumulate	2	MLA{cond}{S} Rd, Rm, Rs, Rn	N Z C*		Rd := ((Rm * Rs) + Rn)[31:0]
	unsigned long	M	UMULL{cond}{S} RdLo, RdHi, Rm, Rs	N Z C* V*		RdHi,RdLo := unsigned(Rm * Rs)
	unsigned accumulate long	M	UMLAL{cond}{S} RdLo, RdHi, Rm, Rs	N Z C* V*		RdHi,RdLo := unsigned(RdHi,RdLo + Rm * Rs)
	unsigned double accumulate long	6	UMAAL{cond} RdLo, RdHi, Rm, Rs			RdHi,RdLo := unsigned(RdHi + RdLo + Rm * Rs)
	Signed multiply long	M	SMULL{cond}{S} RdLo, RdHi, Rm, Rs	N Z C* V*		RdHi,RdLo := signed(Rm * Rs)
	and accumulate long	M	SMLAL{cond}{S} RdLo, RdHi, Rm, Rs	N Z C* V*		RdHi,RdLo := signed(RdHi,RdLo + Rm * Rs)
	16 * 16 bit	5E	SMULxy{cond} Rd, Rm, Rs			Rd := Rm[x] * Rs[y]
	32 * 16 bit	5E	SMULWy{cond} Rd, Rm, Rs			Rd := (Rm * Rs[y])[47:16]
	16 * 16 bit and accumulate	5E	SMLAxy{cond} Rd, Rm, Rs, Rn		Q	Rd := Rn + Rm[x] * Rs[y]
	32 * 16 bit and accumulate	5E	SMLAWy{cond} Rd, Rm, Rs, Rn		Q	Rd := Rn + (Rm * Rs[y])[47:16]
	16 * 16 bit and accumulate long	5E	SMLALxy{cond} RdLo, RdHi, Rm, Rs			RdHi,RdLo := RdHi,RdLo + Rm[x] * Rs[y]
	Dual signed multiply, add	6	SMUAD{X}{cond} Rd, Rm, Rs		Q	Rd := Rm[15:0] * RsX[15:0] + Rm[31:16] * RsX[31:16]
	and accumulate	6	SMLAD{X}{cond} Rd, Rm, Rs, Rn		Q	Rd := Rn + Rm[15:0] * RsX[15:0] + Rm[31:16] * RsX[31:16]
	and accumulate long	6	SMLALD{X}{cond} RdHi, RdLo, Rm, Rs		Q	RdHi,RdLo := RdHi,RdLo + Rm[15:0] * RsX[15:0] + Rm[31:16] * RsX[31:16]
	Dual signed multiply, subtract	6	SMUSD{X}{cond} Rd, Rm, Rs		Q	Rd := Rm[15:0] * RsX[15:0] – Rm[31:16] * RsX[31:16]
	and accumulate	6	SMLSD{X}{cond} Rd, Rm, Rs, Rn		Q	Rd := Rn + Rm[15:0] * RsX[15:0] – Rm[31:16] * RsX[31:16]
	and accumulate long	6	SMLSLD{X}{cond} RdHi, RdLo, Rm, Rs		Q	RdHi,RdLo := RdHi,RdLo + Rm[15:0] * RsX[15:0] – Rm[31:16] * RsX[31:16]
	Signed most significant word multiply	6	SMMUL{R}{cond} Rd, Rm, Rs			Rd := (Rm * Rs)[63:32]
	and accumulate	6	SMMLA{R}{cond} Rd, Rm, Rs, Rn			Rd := Rn + (Rm * Rs)[63:32]
	and subtract	6	SMMLS{R}{cond} Rd, Rm, Rs, Rn			Rd := Rn – (Rm * Rs)[63:32]
	Multiply with internal 40-bit accumulate	XS	MIA{cond} Ac, Rm, Rs			Ac := Ac + Rm * Rs
	packed halfword	XS	MIAPH{cond} Ac, Rm, Rs			Ac := Ac + Rm[15:0] * Rs[15:0] + Rm[31:16] * Rs[31:16]
	halfword	XS	MIAxy{cond} Ac, Rm, Rs			Ac := Ac + Rm[x] * Rs[y]
	Count leading zeroes	5	CLZ{cond} Rd, Rm			Rd := number of leading zeroes in Rm

ARM Addressing Modes
Quick Reference Card

Operation		§	Assembler	S updates	Q	Action
Parallel arithmetic	Halfword-wise addition	6	`<prefix>ADD16{cond} Rd, Rn, Rm`			Rd[31:16] := Rn[31:16] + Rm[31:16], Rd[15:0] := Rn[15:0] + Rm[15:0]
	Halfword-wise subtraction	6	`<prefix>SUB16{cond} Rd, Rn, Rm`			Rd[31:16] := Rn[31:16] – Rm[31:16], Rd[15:0] := Rn[15:0] – Rm[15:0]
	Byte-wise addition	6	`<prefix>ADD8{cond} Rd, Rn, Rm`			Rd[31:24] := Rn[31:24] + Rm[31:24], Rd[23:16] := Rn[23:16] + Rm[23:16], Rd[15:8] := Rn[15:8] + Rm[15:8], Rd[7:0] := Rn[7:0] + Rm[7:0]
	Byte-wise subtraction	6	`<prefix>SUB8{cond} Rd, Rn, Rm`			Rd[31:24] := Rn[31:24] – Rm[31:24], Rd[23:16] := Rn[23:16] – Rm[23:16], Rd[15:8] := Rn[15:8] – Rm[15:8], Rd[7:0] := Rn[7:0] – Rm[7:0]
	Halfword-wise exchange, add, subtract	6	`<prefix>ADDSUBX{cond} Rd, Rn, Rm`			Rd[31:16] := Rn[31:16] + Rm[15:0], Rd[15:0] := Rn[15:0] – Rm[31:16]
	Halfword-wise exchange, subtract, add	6	`<prefix>SUBADDX{cond} Rd, Rn, Rm`			Rd[31:16] := Rn[31:16] – Rm[15:0], Rd[15:0] := Rn[15:0] + Rm[31:16]
	Unsigned sum of absolute differences	6	`USAD8{cond} Rd, Rm, Rs`			Rd := Abs(Rm[31:24] – Rs[31:24]) + Abs(Rm[23:16] – Rs[23:16]) + Abs(Rm[15:8] – Rs[15:8]) + Abs(Rm[7:0] – Rs[7:0])
	and accumulate	6	`USADA8{cond} Rd, Rm, Rs, Rn`			Rd := Rn + Abs(Rm[31:24] – Rs[31:24]) + Abs(Rm[23:16] – Rs[23:16]) + Abs(Rm[15:8] – Rs[15:8]) + Abs(Rm[7:0] – Rs[7:0])
Move	Move		`MOV{cond}{S} Rd, <Operand2>`	N Z C		Rd := Operand2
	NOT		`MVN{cond}{S} Rd, <Operand2>`	N Z C		Rd := 0xFFFFFFFF EOR Operand2
	PSR to register	3	`MRS{cond} Rd, <PSR>`			Rd := PSR
	register to PSR	3	`MSR{cond} <PSR>_<fields>, Rm`			PSR := Rm (selected bytes only)
	immediate to PSR	3	`MSR{cond} <PSR>_<fields>, #<immed_8r>`			PSR := immed_8r (selected bytes only)
	40-bit accumulator to register	XS	`MRA{cond} RdLo, RdHi, Ac`			RdLo := Ac[31:0], RdHi := Ac[39:32]
	register to 40-bit accumulator	XS	`MAR{cond} Ac, RdLo, RdHi`			Ac[31:0] := RdLo, Ac[39:32] := RdHi
	Copy	6	`CPY{cond} Rd, <Operand2>`			Rd := Operand2
Logical	Test		`TST{cond} Rn, <Operand2>`	N Z C		Update CPSR flags on Rn AND Operand2
	Test equivalence		`TEQ{cond} Rn, <Operand2>`	N Z C		Update CPSR flags on Rn EOR Operand2
	AND		`AND{cond}{S} Rd, Rn, <Operand2>`	N Z C		Rd := Rn AND Operand2
	EOR		`EOR{cond}{S} Rd, Rn, <Operand2>`	N Z C		Rd := Rn EOR Operand2
	ORR		`ORR{cond}{S} Rd, Rn, <Operand2>`	N Z C		Rd := Rn OR Operand2
	Bit Clear		`BIC{cond}{S} Rd, Rn, <Operand2>`	N Z C		Rd := Rn AND NOT Operand2
Compare	Compare		`CMP{cond} Rn, <Operand2>`	N Z C V		Update CPSR flags on Rn – Operand2
	negative		`CMN{cond} Rn, <Operand2>`	N Z C V		Update CPSR flags on Rn + Operand2
Saturate	Signed saturate word, right shift	6	`SSAT{cond} Rd, #<sat>, Rm{, ASR <sh>}`		Q	Rd := SignedSat((Rm ASR sh), sat). `<sat>` range 0-31, `<sh>` range 1-32.
	left shift		`SSAT{cond} Rd, #<sat>, Rm{, LSL <sh>}`		Q	Rd := SignedSat((Rm LSL sh), sat). `<sat>` range 0-31, `<sh>` range 0-31.
	Signed saturate two halfwords	6	`SSAT16{cond} Rd, #<sat>, Rm`		Q	Rd[31:16] := SignedSat(Rm[31:16], sat), Rd[15:0] := SignedSat(Rm[15:0], sat). `<sat>` range 0-15.
	Unsigned saturate word, right shift	6	`USAT{cond} Rd, #<sat>, Rm{, ASR <sh>}`		Q	Rd := UnsignedSat((Rm ASR sh), sat). `<sat>` range 0-31, `<sh>` range 1-32.
	left shift		`USAT{cond} Rd, #<sat>, Rm{, LSL <sh>}`		Q	Rd := UnsignedSat((Rm LSL sh), sat). `<sat>` range 0-31, `<sh>` range 0-31.
	Unsigned saturate two halfwords	6	`USAT16{cond} Rd, #<sat>, Rm`		Q	Rd[31:16] := UnsignedSat(Rm[31:16], sat), Rd[15:0] := UnsignedSat(Rm[15:0], sat). `<sat>` range 0-15.

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Operation		§	Assembler	Action	Notes
Pack	Pack halfword bottom + top	6	`PKHBT{cond} Rd, Rn, Rm{, LSL #<sh>}`	Rd[15:0] := Rn[15:0], Rd[31:16] := (Rm LSL sh)[31:16]. sh 0-31.	
	Pack halfword top + bottom	6	`PKHTB{cond} Rd, Rn, Rm{, ASR #<sh>}`	Rd[31:16] := Rn[31:16], Rd[15:0] := (Rm ASR sh)[15:0]. sh 1-32.	
Signed unpack	Halfword to word	6	`SUNPK16TO32{cond} Rd, Rm{, ROR #<sh>}`	Rd[31:0] := SignExtend((Rm ROR (8 * sh))[15:0]). sh 0-3.	
	without rotation	6	`SEXT16{cond} Rd, Rm`	As `SUNPK16TO32` with sh = 0.	Preferred alias when sh = 0.
	Two bytes to halfwords	6	`SUNPK8TO16{cond} Rd, Rm{, ROR #<sh>}`	Rd[31:16] := SignExtend((Rm ROR (8 * sh))[23:16]), Rd[15:0] := SignExtend((Rm ROR (8 * sh))[7:0]). sh 0-3.	
	Byte to word	6	`SUNPK8TO32{cond} Rd, Rm{, ROR #<sh>}`	Rd[31:0] := SignExtend((Rm ROR (8 * sh))[7:0]). sh 0-3.	
	without rotation	6	`SEXT8{cond} Rd, Rm`	As `SUNPK8TO32` with sh = 0.	Preferred alias when sh = 0.
Unsigned unpack	Halfword to word	6	`UUNPK16TO32{cond} Rd, Rm{, ROR #<sh>}`	Rd[31:0] := ZeroExtend((Rm ROR (8 * sh))[15:0]). sh 0-3.	
	without rotation	6	`UEXT16{cond} Rd, Rm`	As `UUNPK16TO32` with sh = 0.	Preferred alias when sh = 0.
	Two bytes to halfwords	6	`UUNPK8TO16{cond} Rd, Rm{, ROR #<sh>}`	Rd[31:16] := ZeroExtend((Rm ROR (8 * sh))[23:16]), Rd[15:0] := ZeroExtend((Rm ROR (8 * sh))[7:0]). sh 0-3.	
	Byte to word	6	`UUNPK8TO32{cond} Rd, Rm{, ROR #<sh>}`	Rd[31:0] := ZeroExtend((Rm ROR (8 * sh))[7:0]). sh 0-3.	
	without rotation	6	`UEXT8{cond} Rd, Rm`	As `UUNPK8TO32` with sh = 0.	Preferred alias when sh = 0.
Signed unpack with add	Halfword to word, add	6	`SADD16TO32{cond} Rd, Rn, Rm{, ROR #<sh>}`	Rd[31:0] := Rn[31:0] + SignExtend((Rm ROR (8 * sh))[15:0]). sh 0-3.	
	Two bytes to halfwords, add	6	`SADD8TO16{cond} Rd, Rn, Rm{, ROR #<sh>}`	Rd[31:16] := Rn[31:16] + SignExtend((Rm ROR (8 * sh))[23:16]), Rd[15:0] := Rn[15:0] + SignExtend((Rm ROR (8 * sh))[7:0]). sh 0-3.	
	Byte to word, add	6	`SADD8TO32{cond} Rd, Rn, Rm{, ROR #<sh>}`	Rd[31:0] := Rn[31:0] + SignExtend((Rm ROR (8 * sh))[7:0]). sh 0-3.	
Unsigned unpack with add	Halfword to word, add	6	`UADD16TO32{cond} Rd, Rn, Rm{, ROR #<sh>}`	Rd[31:0] := Rn[31:0] + ZeroExtend((Rm ROR (8 * sh))[15:0]). sh 0-3.	
	Two bytes to halfwords, add	6	`UADD8TO16{cond} Rd, Rn, Rm{, ROR #<sh>}`	Rd[31:16] := Rn[31:16] + ZeroExtend((Rm ROR (8 * sh))[23:16]), Rd[15:0] := Rn[15:0] + ZeroExtend((Rm ROR (8 * sh))[7:0]). sh 0-3.	
	Byte to word, add	6	`UADD8TO32{cond} Rd, Rn, Rm{, ROR #<sh>}`	Rd[31:0] := Rn[31:0] + ZeroExtend((Rm ROR (8 * sh))[7:0]). sh 0-3.	
Reverse bytes	In word	6	`REV{cond} Rd, Rm`	Rd[31:24] := Rm[7:0], Rd[23:16] := Rm[15:8], Rd[15:8] := Rm[23:16], Rd[7:0] := Rm[31:24]	
	In both halfwords	6	`REV16{cond} Rd, Rm`	Rd[15:8] := Rm[7:0], Rd[7:0] := Rm[15:8], Rd[31:24] := Rm[23:16], Rd[23:16] := Rm[31:24]	
	In low halfword, sign extend	6	`REVSH{cond} Rd, Rm`	Rd[15:8] := Rm[7:0], Rd[7:0] := Rm[15:8], Rd[31:16] := Rm[7] * &FFFF	
Select	Select bytes	6	`SEL{cond} Rd, Rn, Rm`	Rd[7:0] := Rn[7:0] if GE[0] = 1, else Rd[7:0] := Rm[7:0] Bits[15:8], [23:16], [31:24] selected similarly by GE[1], GE[2], GE[3]	
Branch	Branch		`B{cond} label`	R15 := label	label must be within ±32Mb of current instruction.
	with link		`BL{cond} label`	R14 := address of next instruction, R15 := label	label must be within ±32Mb of current instruction.
	and exchange	4T,5	`BX{cond} Rm`	R15 := Rm, Change to Thumb if Rm[0] is 1	
	with link and exchange (1)	5T	`BLX label`	R14 := address of next instruction, R15 := label, Change to Thumb	Cannot be conditional. label must be within ±32Mb of current instruction.
	with link and exchange (2)	5	`BLX{cond} Rm`	R14 := address of next instruction, R15 := Rm[31:1] Change to Thumb if Rm[0] is 1	
	and change to Java state	5J, 6	`BXJ{cond} Rm`	Change to Java state	
Processor state change	Change processor state	6	`CPSID <iflags> {, #<p_mode>}`	Disable specified interrups, optional change mode.	Cannot be conditional.
		6	`CPSIE <iflags> {, #<p_mode>}`	Enable specified interrups, optional change mode.	Cannot be conditional.
	Change processor mode	6	`CPS #<p_mode>`		Cannot be conditional.
	Set endianness	6	`SETEND <endianness>`	Sets endianness for loads and saves.	Cannot be conditional.
	Store return state	6	`SRS<a_mode4S> #<p_mode>{!}`	[R13m] := R14, [R13m + 4] := CPSR	Cannot be conditional.
	Return from exception	6	`RFE<a_mode4L> Rn{!}`	PC := [Rn], CPSR := [Rn + 4]	Cannot be conditional.
	Breakpoint	5	`BKPT <immed_16>`	Prefetch abort *or* enter debug state.	Cannot be conditional.
Software interrupt	Software interrupt		`SWI{cond} <immed_24>`	Software interrupt processor exception.	24-bit value encoded in instruction.
No Op	No operation	5	`NOP`	None	