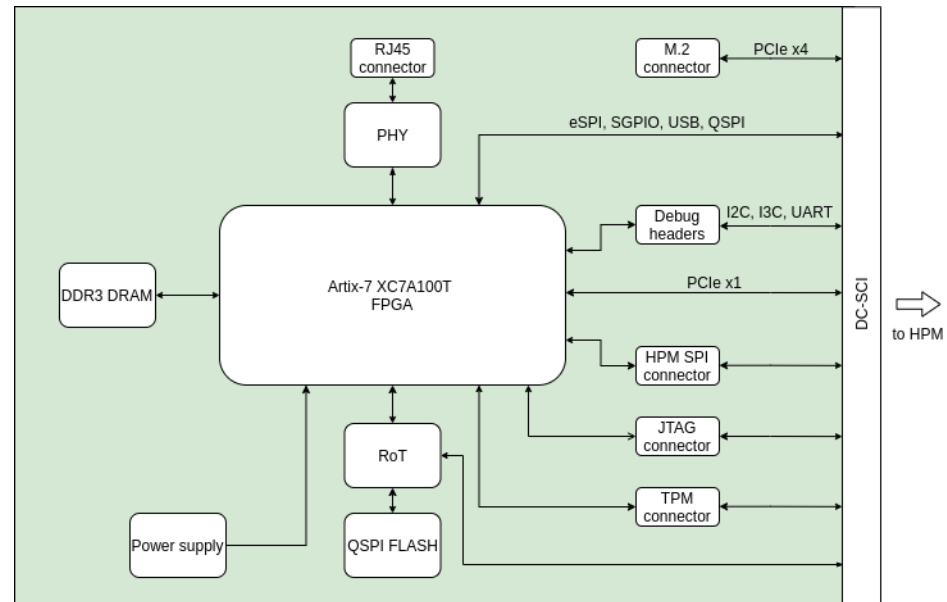
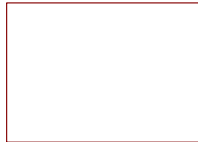


## Artix – Datacenter Secure Control Module (DC-SCM)



Ethernet



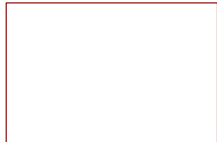
File: ethernet.sch

PCIe-connector



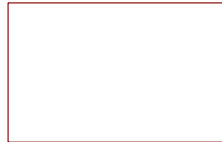
File: pcie-conn.sch

RoT



File: rot.sch

Edge connector



File: edge-connector.sch

Interfaces



File: interfaces.sch

DDR3



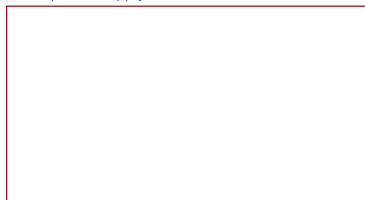
File: ddr3.sch

Power supply



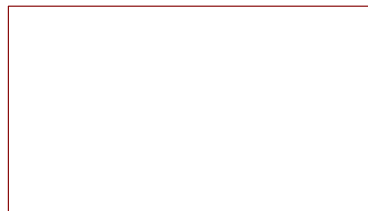
File: power-supply.sch

FPGA power supply



File: fpga-power-supply.sch

FPGA banks



File: fpga-banks.sch

Logo N2 oshw\_logo

Logo N1 antmicro\_logo



MP1  
PCB\_Mount\_Hole\_2.9\_5.5



MP2  
PCB\_Mount\_Hole\_2.9\_5.5

Sheet: /

File: artix-dc-scm.sch

**Title: Artix – Datacenter Secure Control Module (DC-SCM)**

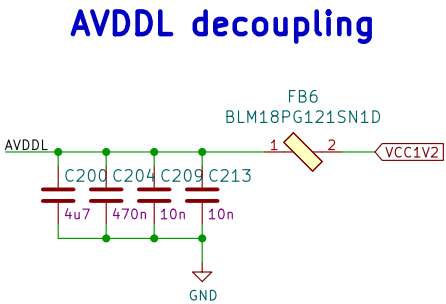
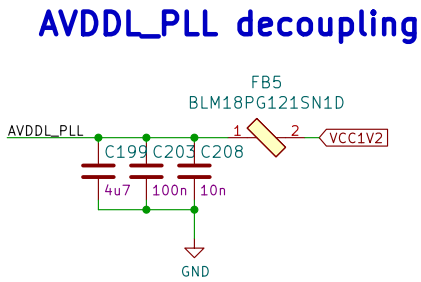
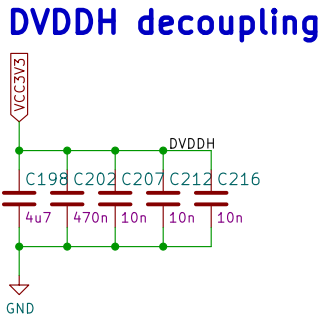
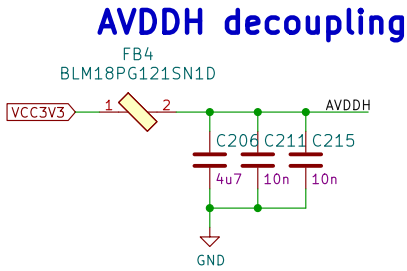
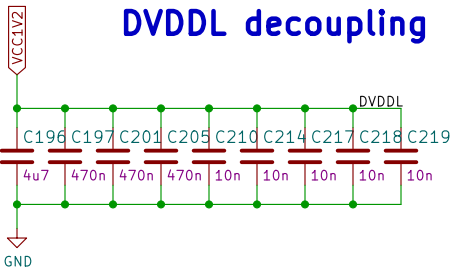
Size: A4

Date:

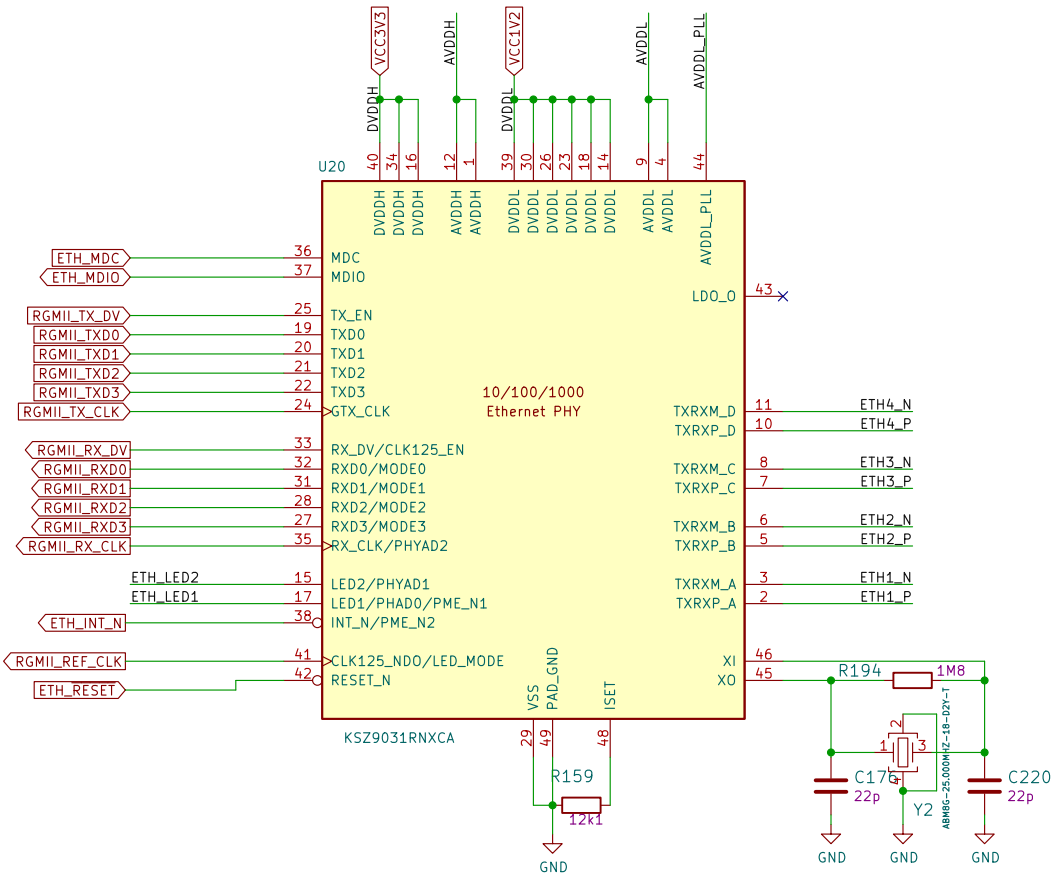
Rev: 1.1.0

KiCad E.D.A. kicad 6.0.5+dfsg-1~bpo11+1

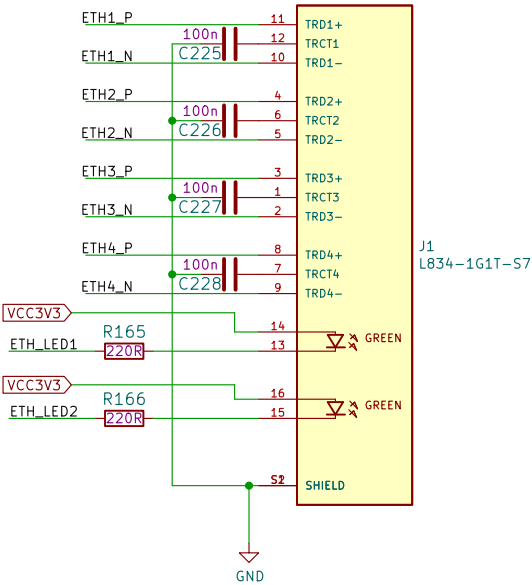
Id: 1/10



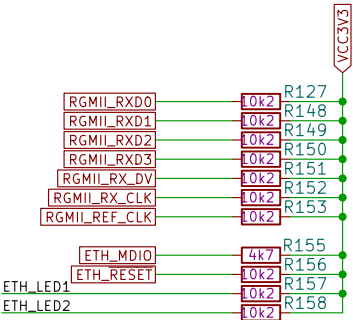
**PHY**



**RJ45 Connector**

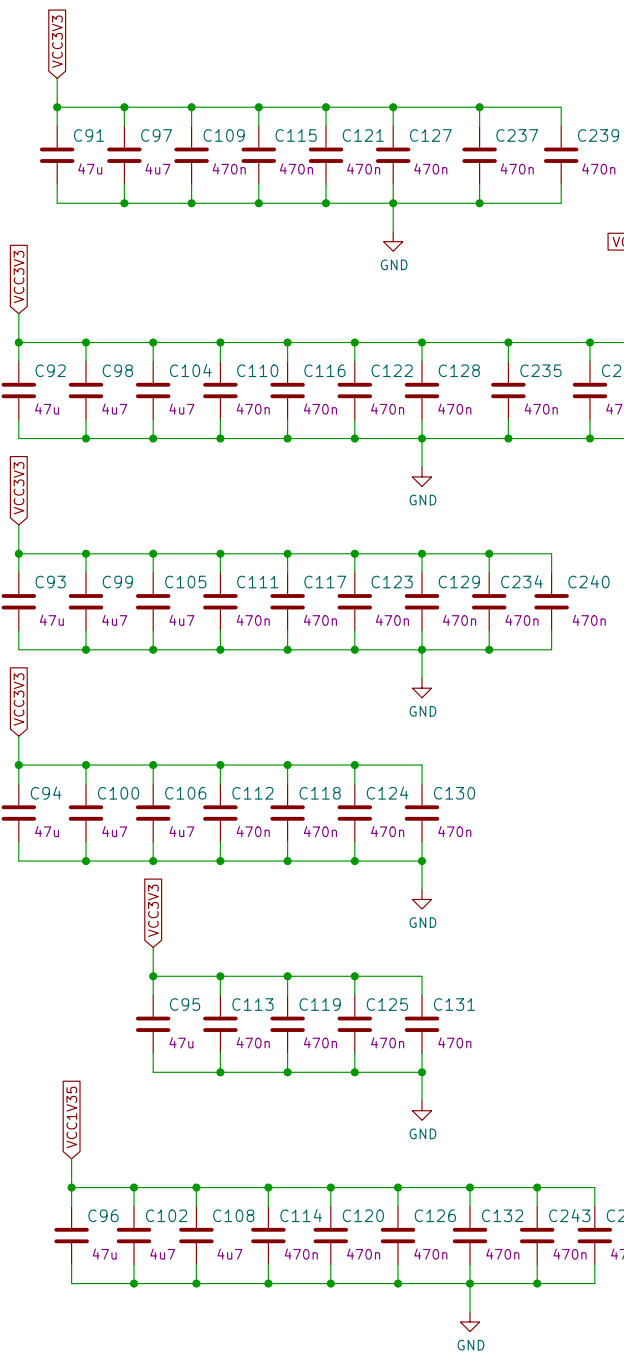


**Pull up resistors**

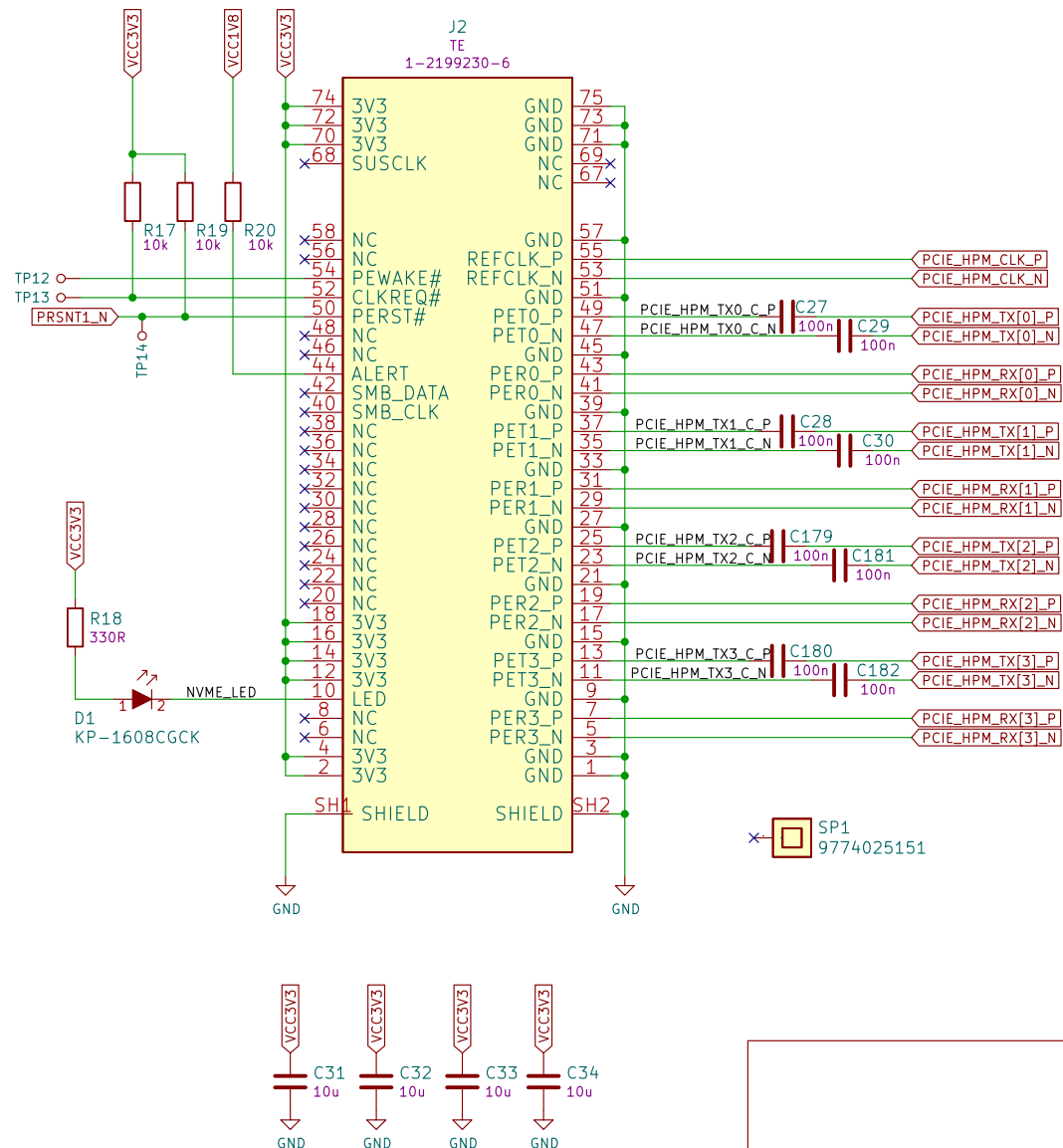


FPGA power supply

Banks decoupling



## NVMe SSD



Sheet: /PCIe-connector/  
File: pcie-conn.sch

**Title: Artix – Datacenter Secure Control Module (DC-SCM)**

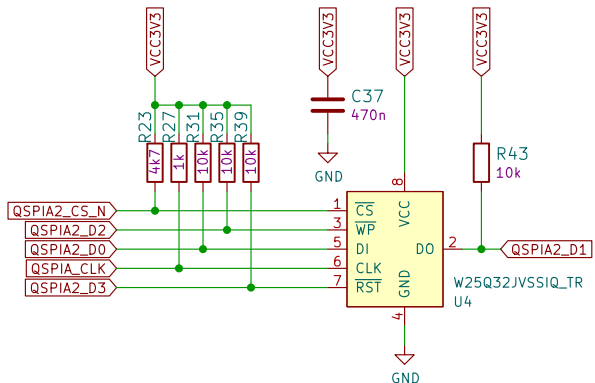
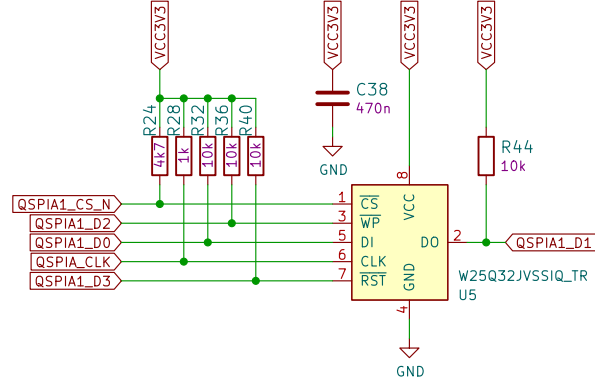
Size: A4	Date:
KiCad E.D.A. kicad 6.0.5+dfsg-1~bpo11+1	

Rev: 1.1.0  
Id: 4/10



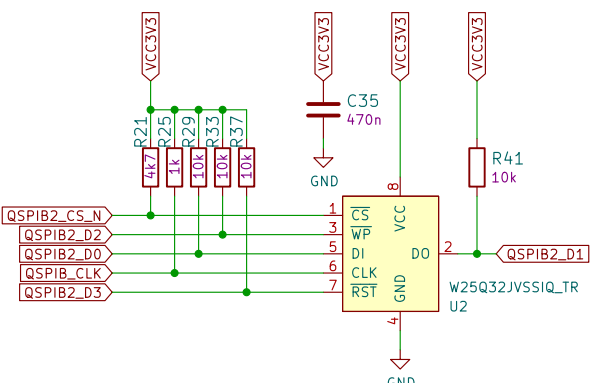
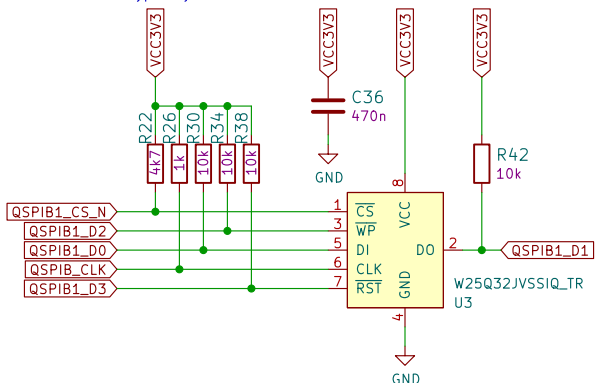
# BIOS flash

One or typically two flash devices used to contain the BIOS firmware image

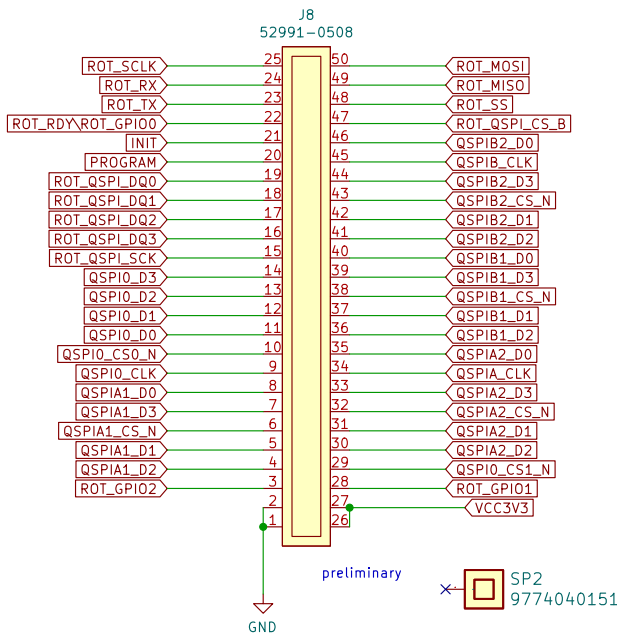


# BMC flash

One or typically two flash devices used to contain the BMC firmware image



# RoT module connector

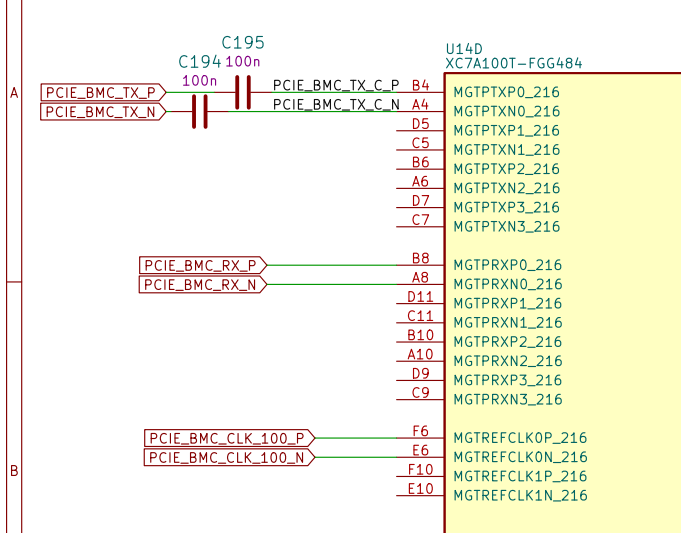


# TPM connector

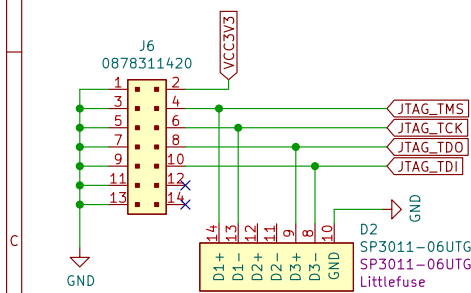




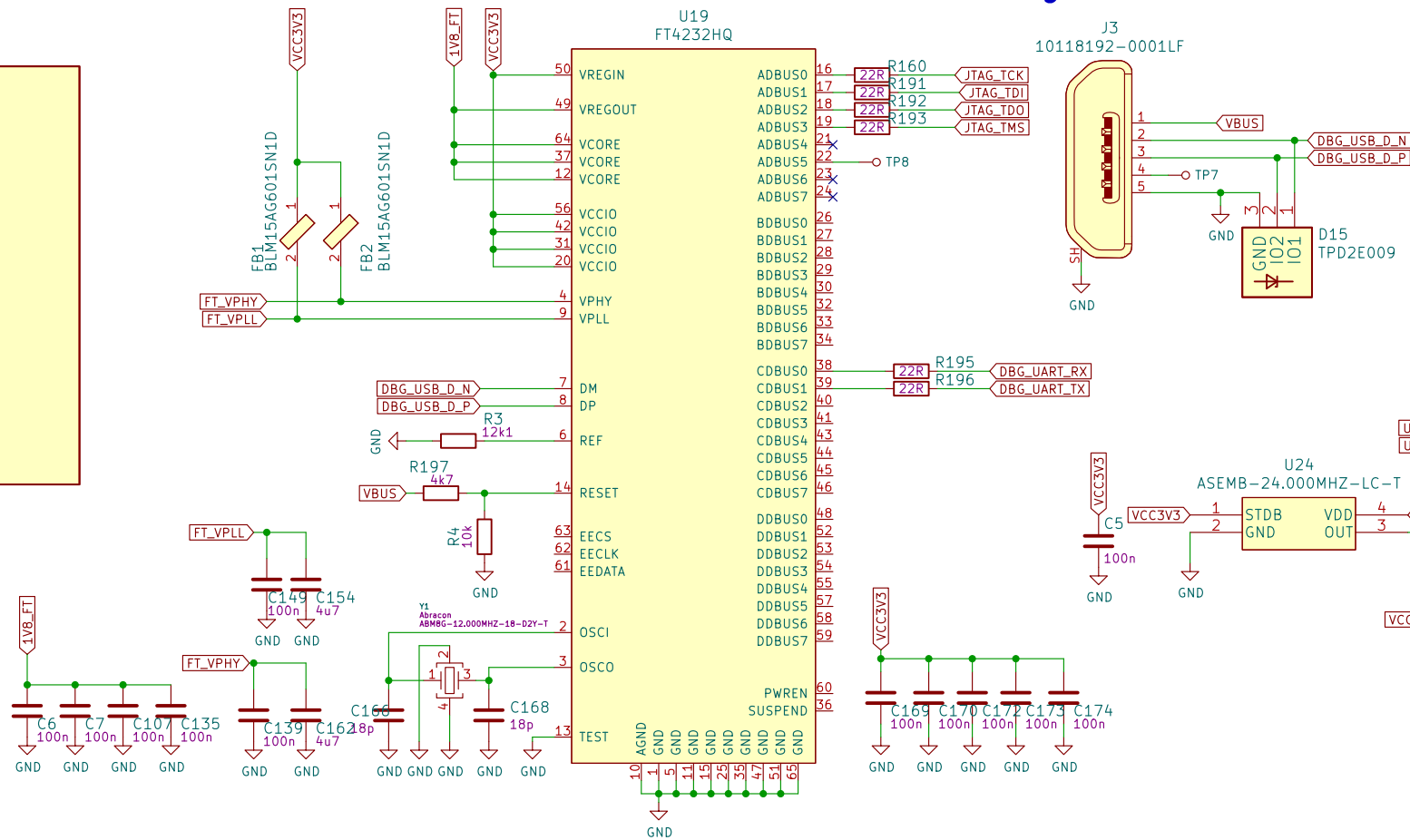
## PCIe x1



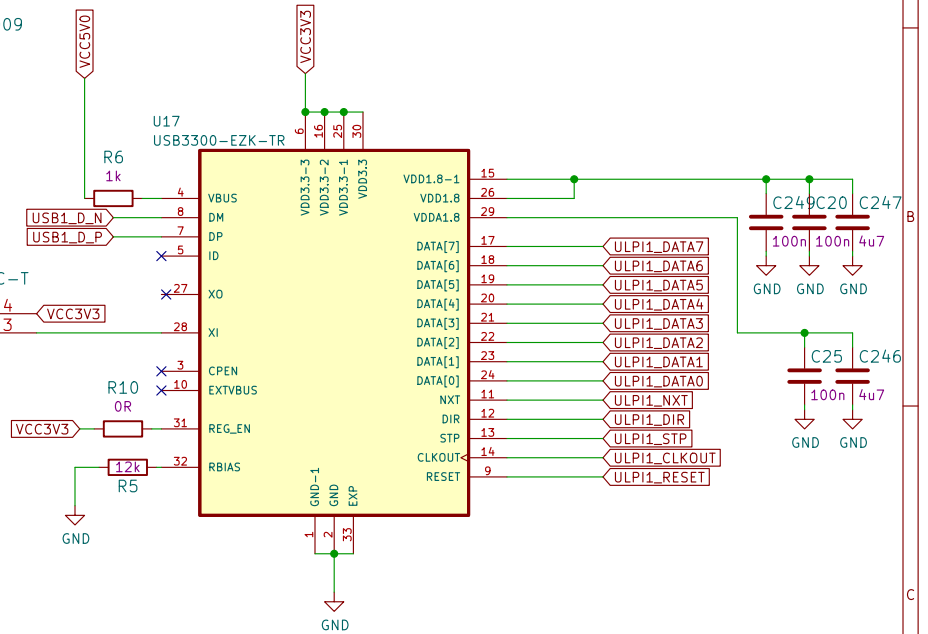
## JTAG



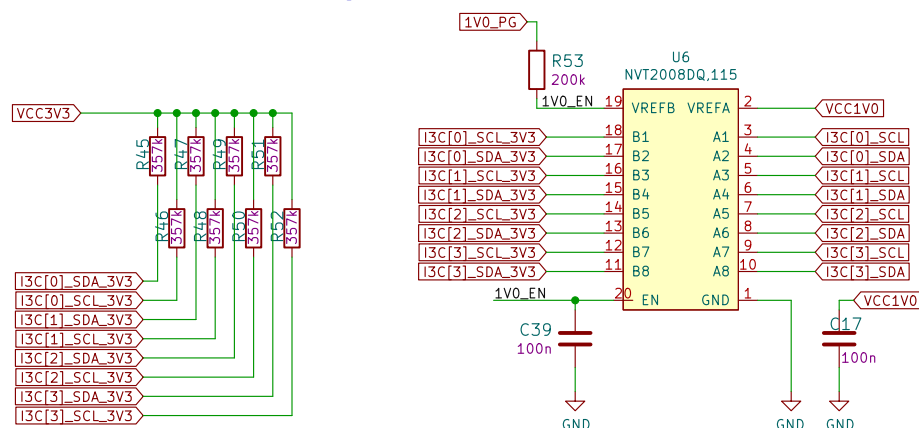
## Debug USB



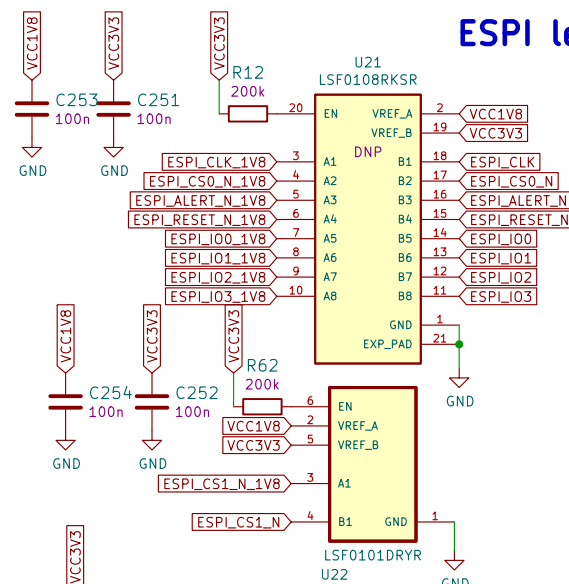
## USB HOST



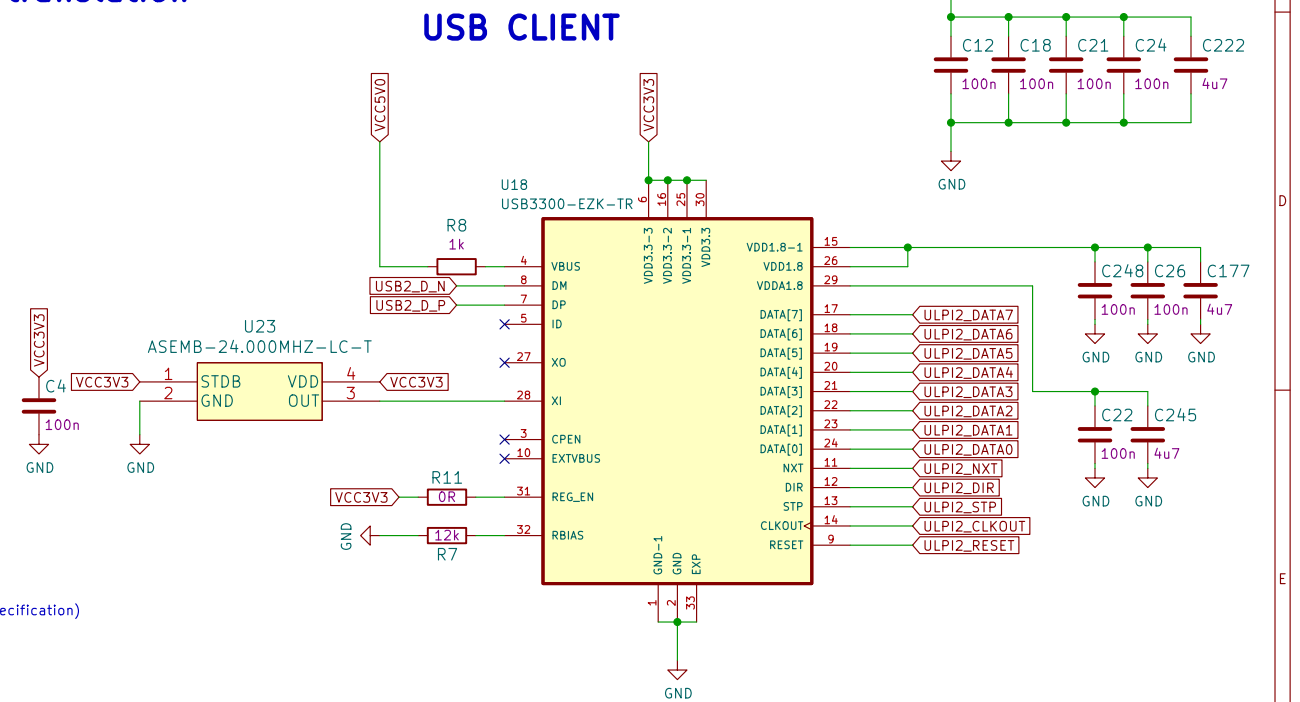
## I3C voltage level translation



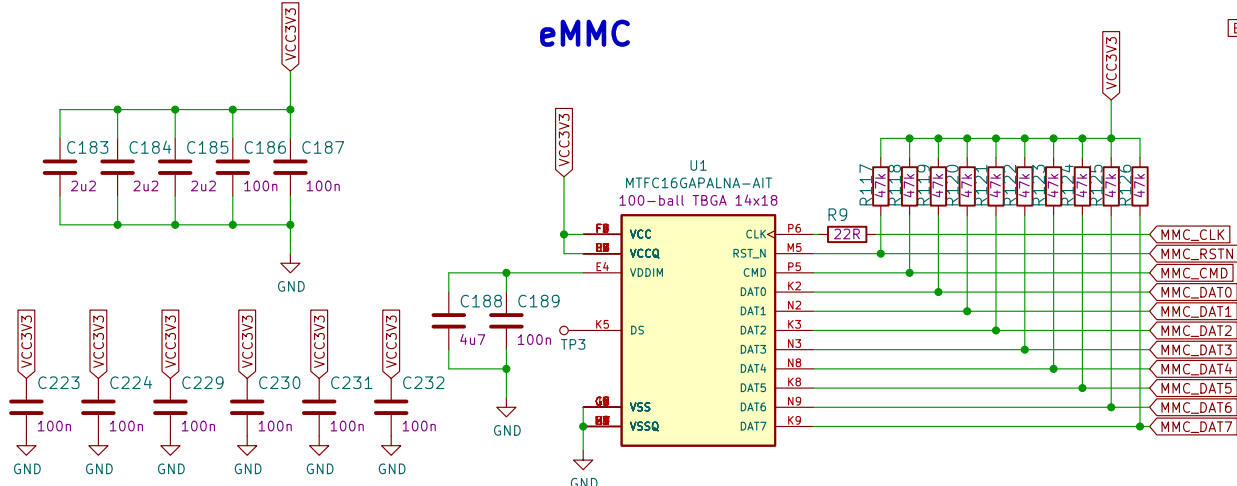
## ESPI level translation



## USB CLIENT

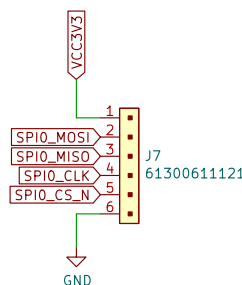


## eMMC

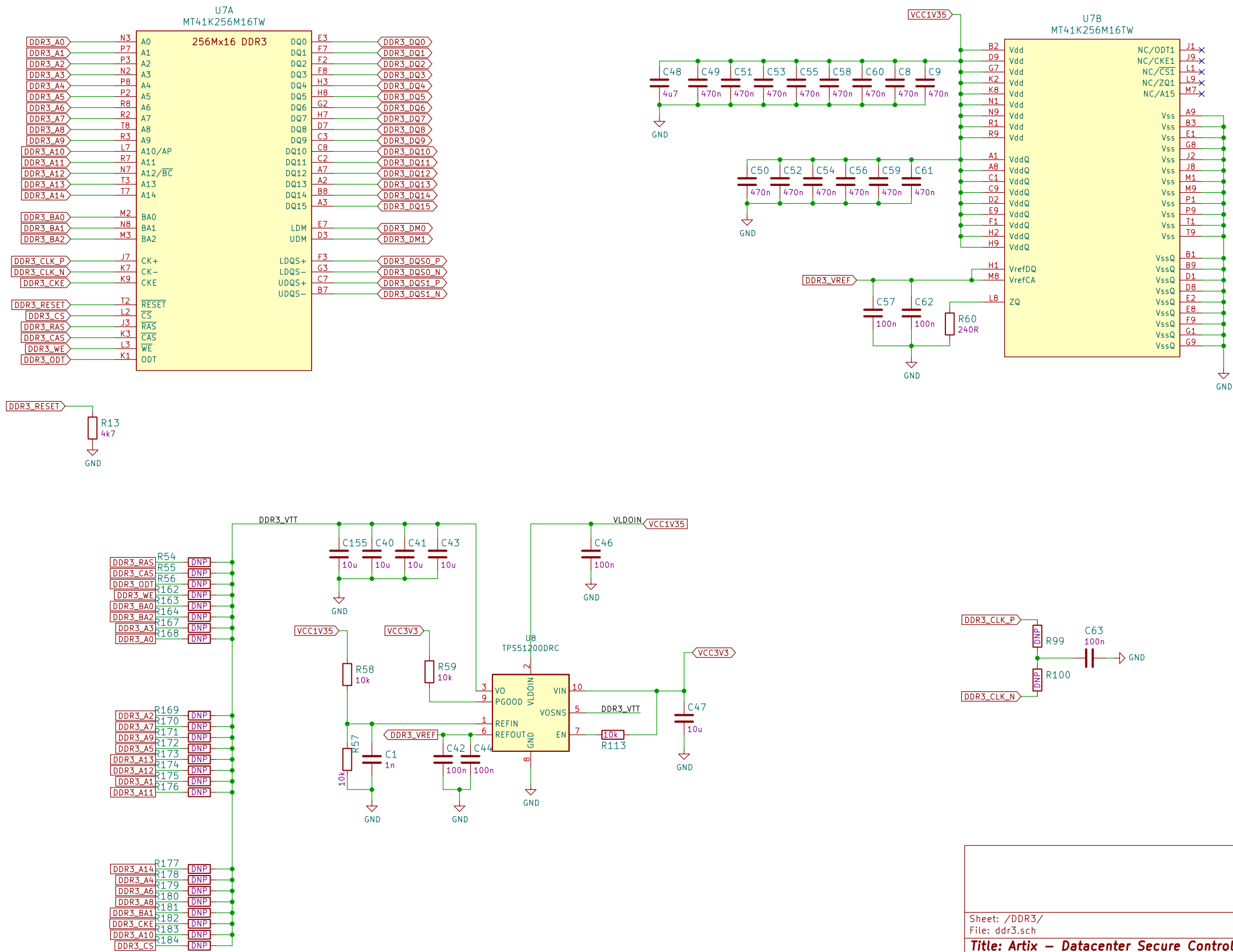


## HPM SPI

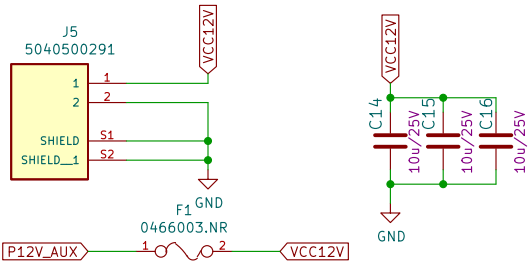
reserved for future use (as of DC-SCI OPC specification)



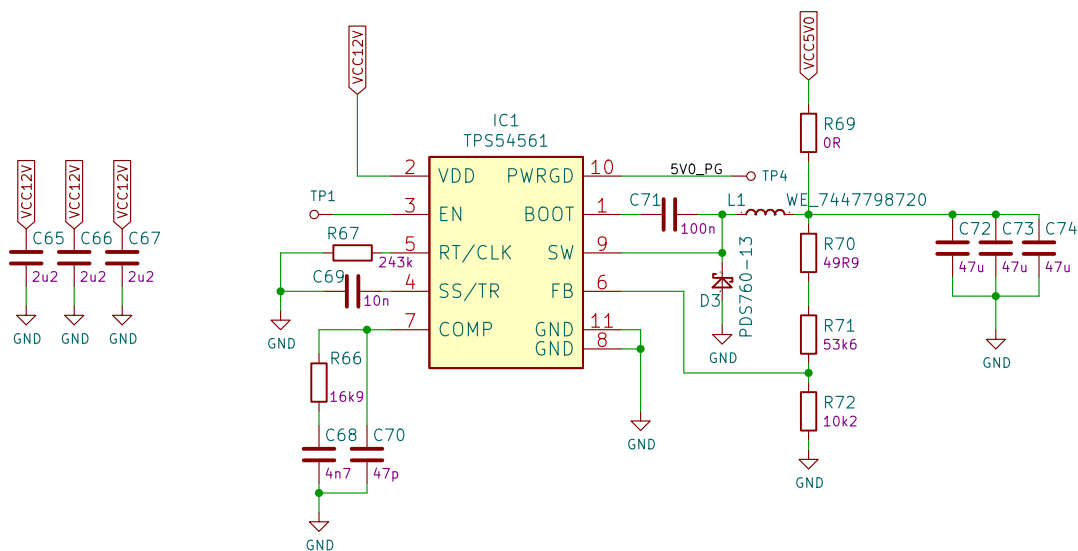




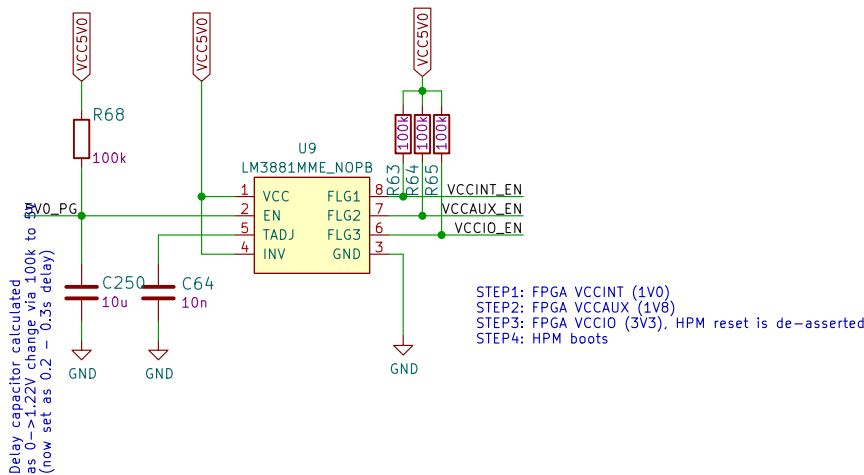
External 12V supply



MainSupply (5V 5A)

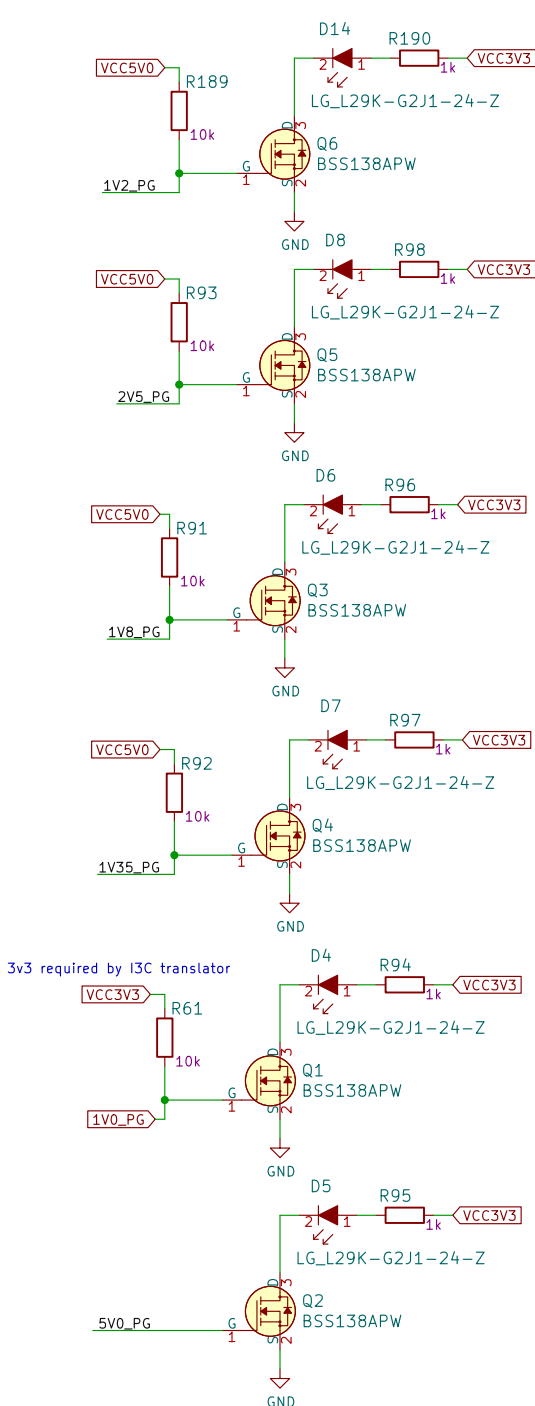


Power sequencer

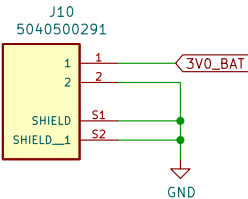


STEP1: FPGA VCCINT (1V0)  
STEP2: FPGA VCCAUX (1V8)  
STEP3: FPGA VCCIO (3V3), HPM reset is de-asserted  
STEP4: HPM boots

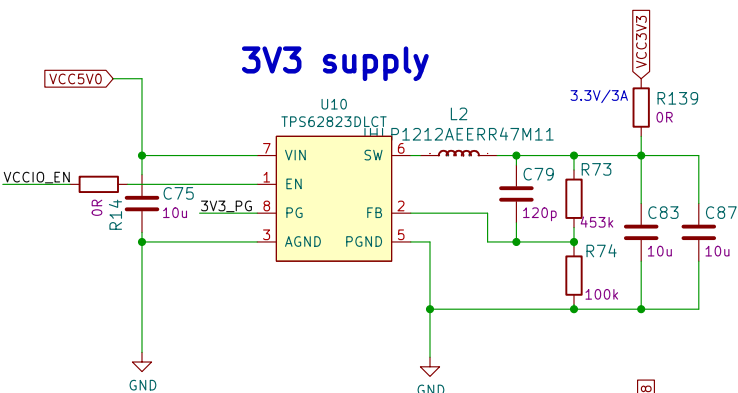
PWR\_LED Indicators



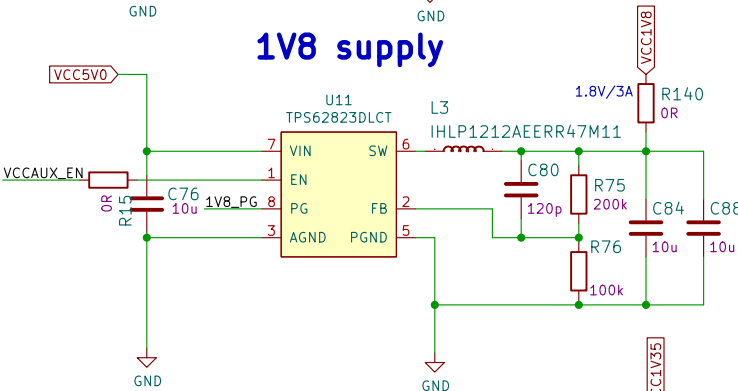
Battery connector



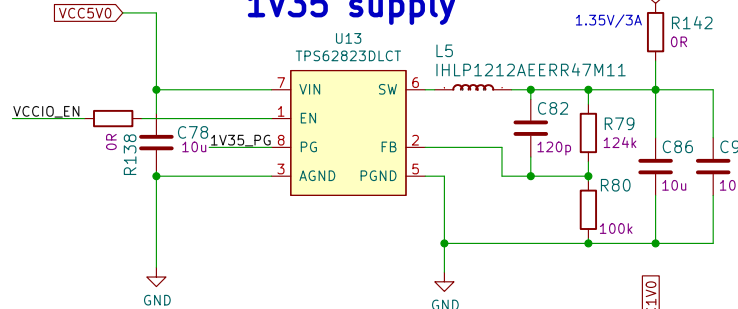
3V3 supply



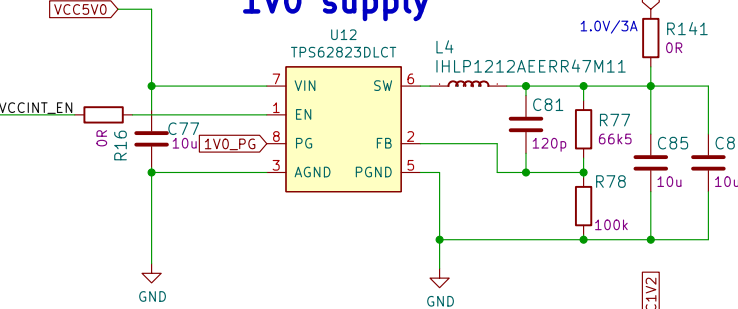
1V8 supply



1V35 supply



1V0 supply



1V2 supply

