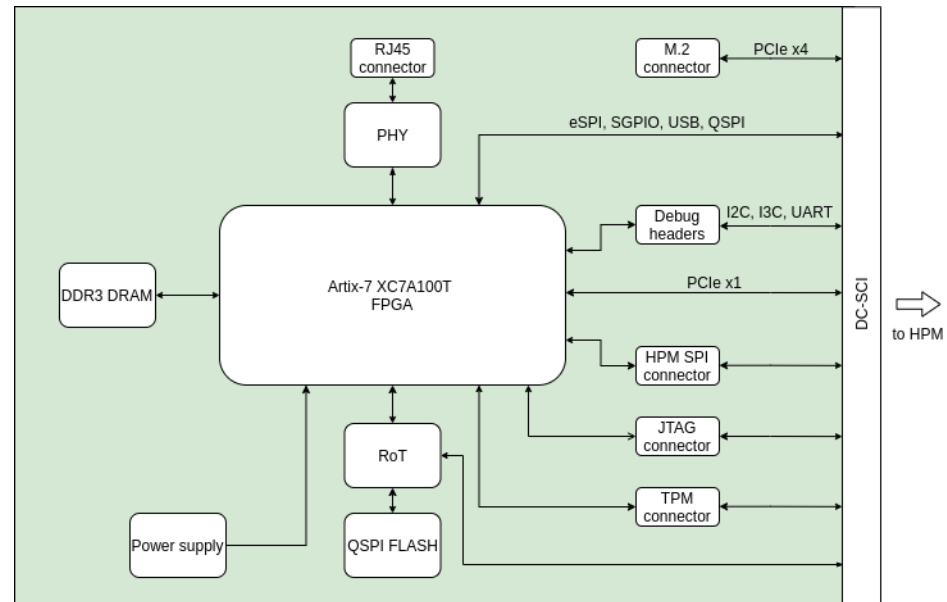
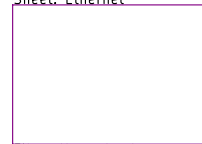


Artix – Datacenter Secure Control Module (DC-SCM)



Sheet: Ethernet



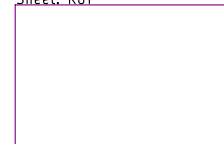
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Sheet: PCIe-connector



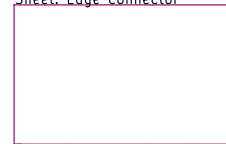
File: pcie-conn.sch

Sheet: RoT



File: rot.sch

Sheet: Edge connector



File: edge-connector.sch

Sheet: Interfaces



File: interfaces.sch

Sheet: DDR3



File: ddr3.sch

Sheet: Power supply



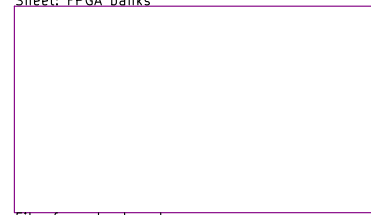
File: power-supply.sch

Sheet: FPGA power supply



File: fpga-power-supply.sch

Sheet: FPGA banks



File: fpga-banks.sch

Logo N2 oshw_logo

Logo N1 antmicro_logo



MP1
PCB_Mount_Hole_2.9_5.5

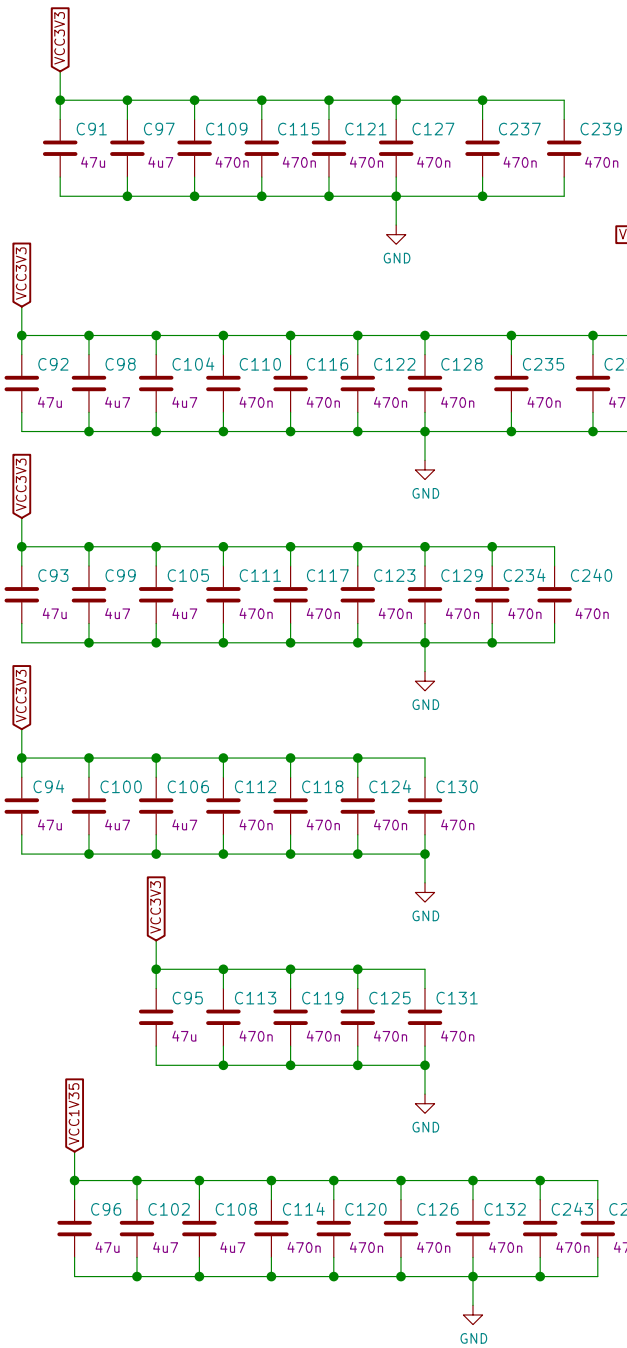


MP2
PCB_Mount_Hole_2.9_5.5

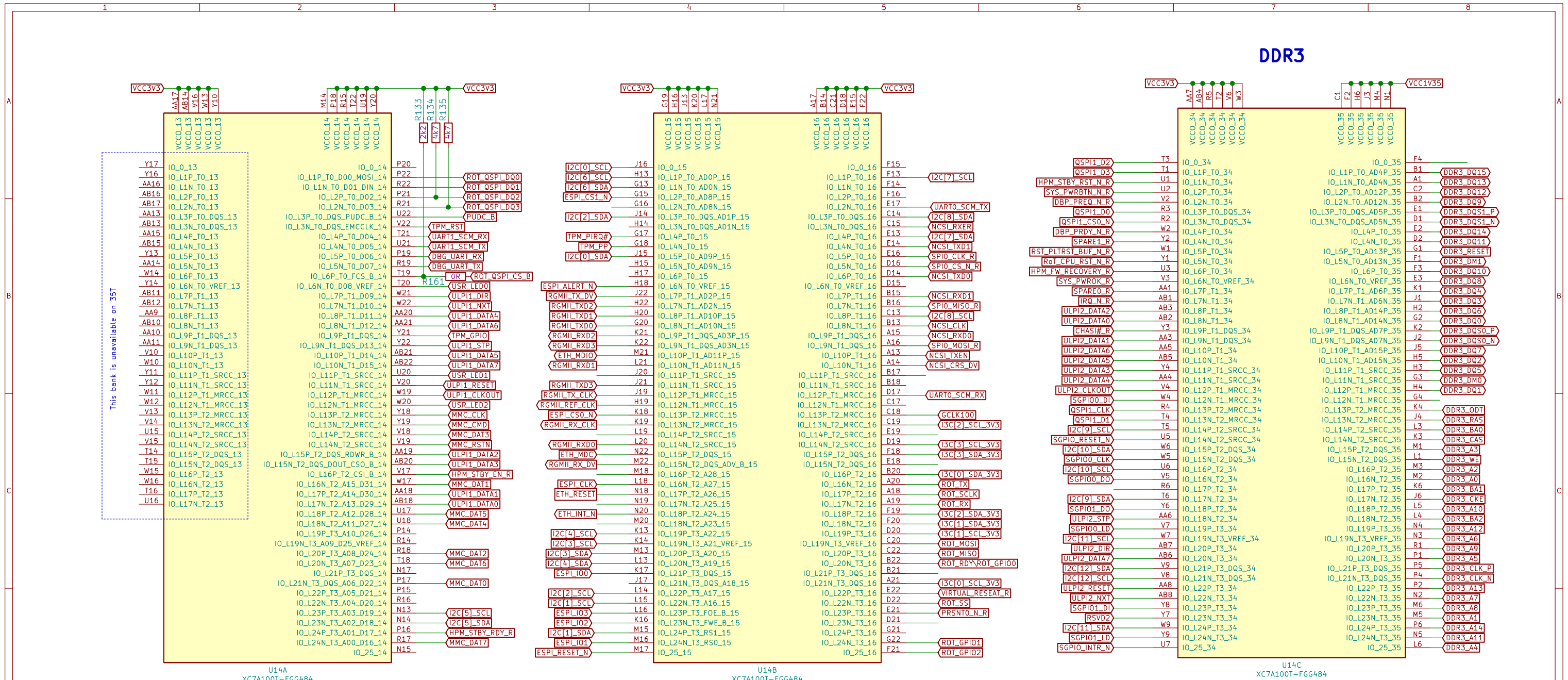
Sheet: /	
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Title: Artix – Datacenter Secure Control Module (DC-SCM)	
Size: A4	Date:
KiCad E.D.A. eeschema 5.1.5+dfsg1-2bpo10+1	
Rev: 1.0.6	
Id: 1/10	

FPGA power supply

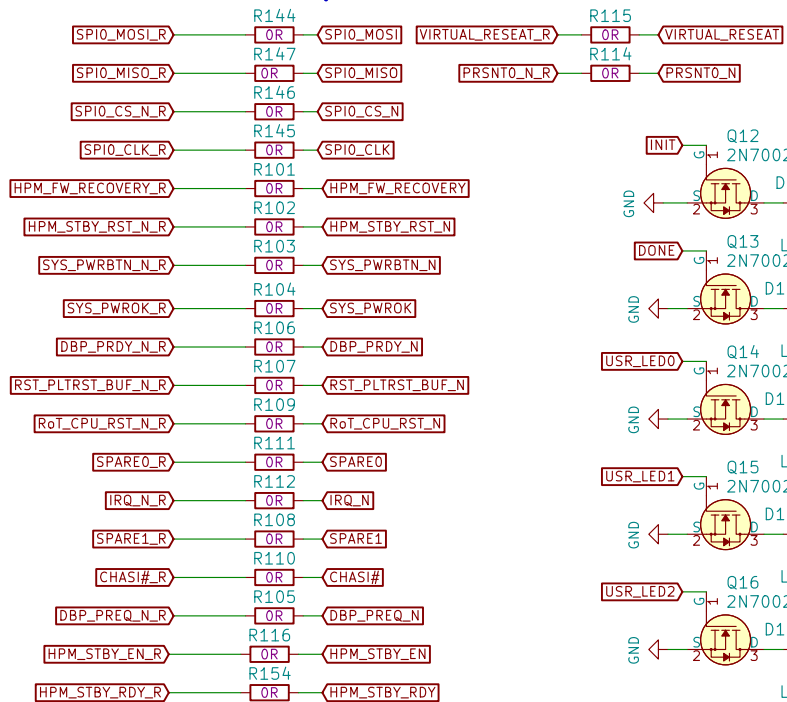
Banks decoupling



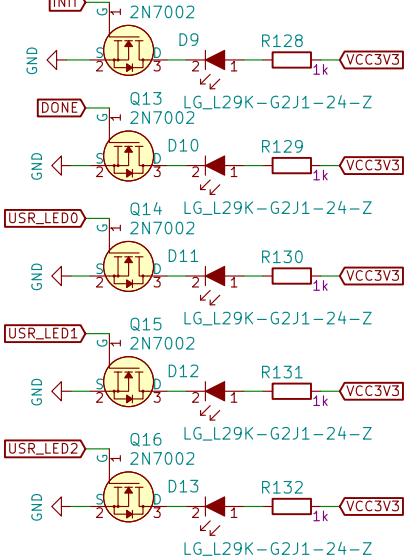
DDR3



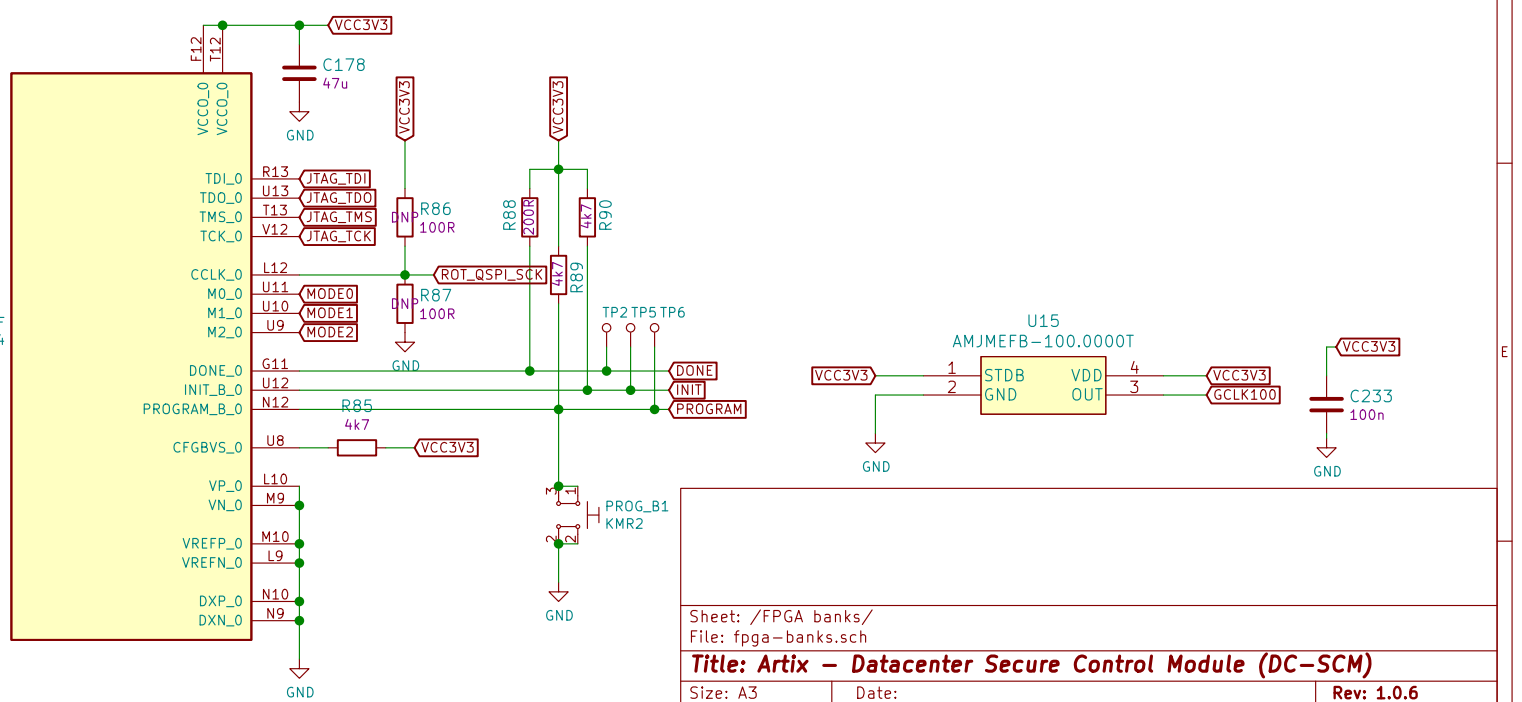
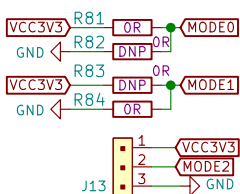
HPM Control Jumpers



Status LEDs



Configuration modes



External 12V supply

J5 5040500291

SHIELD SHIELD_1

F1 GND 0466003.NR

P12V_AUX VCC12V

MainSupply (5V 5A)

IC1 TPS54561

VDD PWRGD EN BOOT RT/CLK SW SS/TR FB COMP GND GND

TP1 TP4

R67 243k R69 0R R70 49R9 R71 53k6 R72 10k2

C65 2u2 C66 2u2 C67 2u2

C68 4n7 C69 10n C70 47p

C71 100n C72 47u C73 47u C74 47u

L1 WE_7447798720

D3 PDS760-13

Power sequencer

U9 LM3881MME_NOPB

VCC EN FLG1 FLG2 FLG3 INV TADJ GND

VCCINT_EN VCCAUX_EN VCCIO_EN

R68 100k

C250 10u C64 10n

Delay capacitor calculated as 0->1.22V change via 100k to 5V (now set as 0.2 - 0.3s delay)

STEP1: FPGA VCCINT (1V0)
STEP2: FPGA VCCAUX (1V8)
STEP3: FPGA VCCIO (3V3), HPM reset is de-asserted
STEP4: HPM boots

PWR_LED Indicators

D14 D8 D6 D7 D4 D5 Q6 Q5 Q3 Q4 Q1 Q2

BSS138APW

R189 10k R93 10k R91 10k R92 10k R61 10k R94 1k R95 1k

D1 LG_L29K-G2J1-24-Z D8 LG_L29K-G2J1-24-Z D6 LG_L29K-G2J1-24-Z D7 LG_L29K-G2J1-24-Z D4 LG_L29K-G2J1-24-Z D5 LG_L29K-G2J1-24-Z

VCC5V0 1V2_PG 2V5_PG 1V8_PG 1V35_PG 3V3V3 1V0_PG 5V0_PG

3V3 supply

U10 TPS62823DLCT

VIN SW EN EN FB PG FB AGND PGND

L2 IHLP1212AEERR47M11

C75 10u C79 120p R73 453k R74 100k C83 10u C87 10u

VCC5V0 VCCIO_EN VCC3V3

1V8 supply

U11 TPS62823DLCT

VIN SW EN EN FB PG FB AGND PGND

L3 IHLP1212AEERR47M11

C80 120p R75 200k R76 100k C84 10u C88 10u

VCC5V0 VCCAUX_EN VCC1V8

1V35 supply

U13 TPS62823DLCT

VIN SW EN EN FB PG FB AGND PGND

L5 IHLP1212AEERR47M11

C82 120p R79 124k R80 100k C86 10u C90 10u

VCC5V0 VCCIO_EN VCC1V35

1V0 supply

U12 TPS62823DLCT

VIN SW EN EN FB PG FB AGND PGND

L4 IHLP1212AEERR47M11

C81 120p R77 66k R78 100k C85 10u C89 10u

VCC5V0 VCCINT_EN VCC1V0

1V2 supply

U16 TPS62823DLCT

VIN SW EN EN FB PG FB AGND PGND

L6 IHLP1212AEERR47M11

C3 120p R186 100k R187 100k C101 10u C103 10u

VCC5V0 VCCIO_EN VCC1V2

Battery connector

J10 5040500291

SHIELD SHIELD_1

3V0_BAT

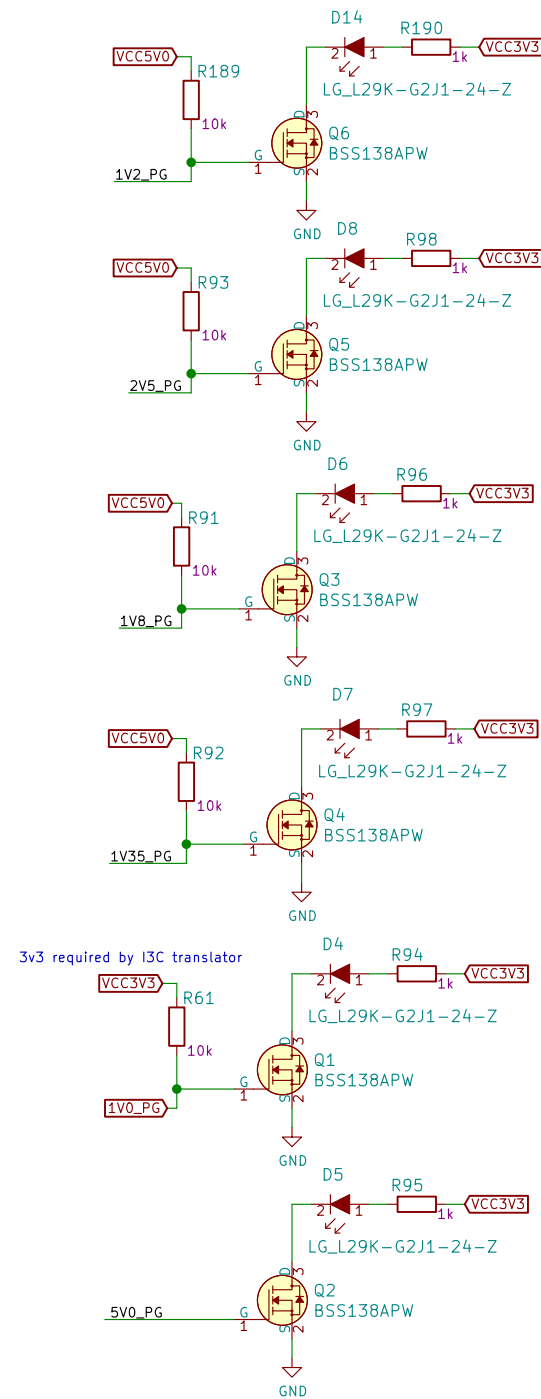
Table:

Ref	Value	Part	Notes
U10	TPS62823DLCT	TPS62823DLCT	3V3V3
U11	TPS62823DLCT	TPS62823DLCT	1V8V
U13	TPS62823DLCT	TPS62823DLCT	1V35V
U12	TPS62823DLCT	TPS62823DLCT	1V0V
U16	TPS62823DLCT	TPS62823DLCT	1V2V
U9	LM3881MME_NOPB	LM3881MME_NOPB	Power sequencer
Q1-Q6	BSS138APW	BSS138APW	MOSFETs
D1-D8	LG_L29K-G2J1-24-Z	LG_L29K-G2J1-24-Z	Diodes
L1-L6	IHLP1212AEERR47M11	IHLP1212AEERR47M11	Inductors
C1-C10	Various	Various	Capacitors
R1-R10	Various	Various	Resistors

Title: Artix - Datacenter Secure Control Module (DC-SCM)

Size: A3 Date: Rev: 1.0.6

KiCad E.D.A. eeschema 5.1.5+dfsg1-2bp010+1 Id: 4/10



The diagram illustrates a 3V3 supply circuit. It features a TPS62823DLCT (U10) converter. The input side includes a VCC5V0 source connected to the VIN pin (pin 7) through a 0R resistor (R14) and a 10uF capacitor (C75). The EN pin (pin 1) is connected to VCCIO_EN through a 0R resistor (R14). The PG pin (pin 8) is connected to the 3V3_PG signal. The AGND pin (pin 3) and PGND pin (pin 5) are connected to GND. The output side includes an inductor L2 (HLLP1212AEERR47M11) connected to the SW pin (pin 6). The FB pin (pin 2) is connected to the output through a 120pF capacitor (C79) and a 453k resistor (R73). The output is also connected to a 3.3V/3A source through a 0R resistor (R139) and a 10uF capacitor (C83). A 100k resistor (R74) is connected between the output and GND. A 10uF capacitor (C87) is connected between the output and GND. The output voltage is labeled as 3V3.

The diagram shows a 1V35 supply circuit. The input is VCC5V0, which goes through a 0Ω resistor (R138) to the VIN pin (pin 7) of the TPS62823DLCT (U13). The EN pin (pin 1) is connected to VCCIO_EN through a 10μF capacitor (C78). The PG pin (pin 3) is connected to AGND. The SW pin (pin 6) is connected to an inductor (L5, IHL P1212AEERR47M11). The FB pin (pin 2) is connected to a voltage divider consisting of a 120pF capacitor (C82) and a 100k resistor (R80) to ground, and a 124k resistor (R79) to the output. The PGND pin (pin 5) is connected to ground. The output is 1.35V/3A, which goes through a 0Ω resistor (R142) to the VCCIO_V35 pin. The output is also connected to a 10μF capacitor (C86) and a 10μF capacitor (C90) to ground.

J10
5040500291

1 1
2 2

SHIELD
SHIELD_1

S1
S2

3V0_BAT

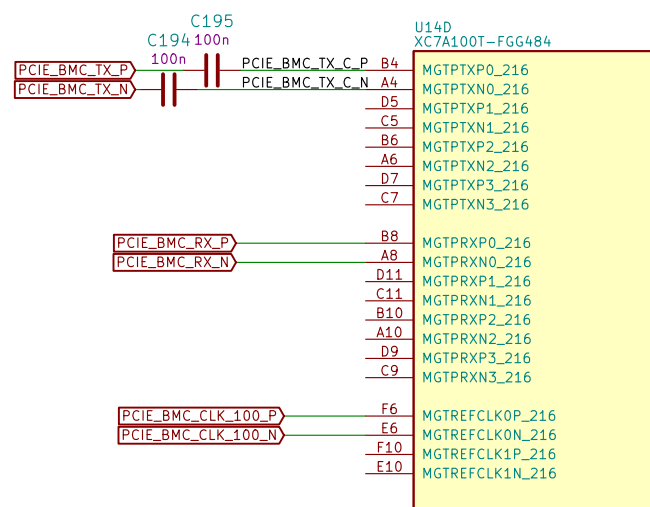
GND

Title: Artix – Datacenter Secure Control Module (DC-SCM)

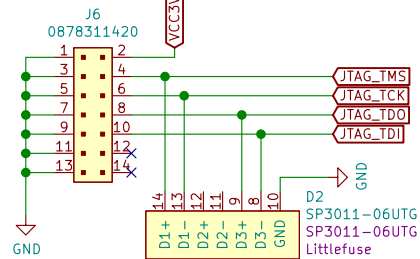
Rev: 1.0.6

Id: 4/10

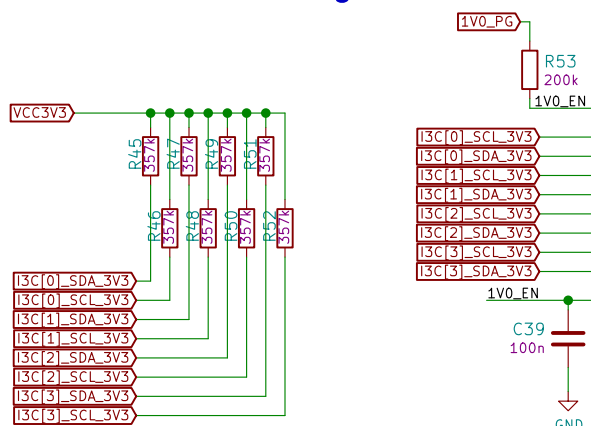
PCIe x1



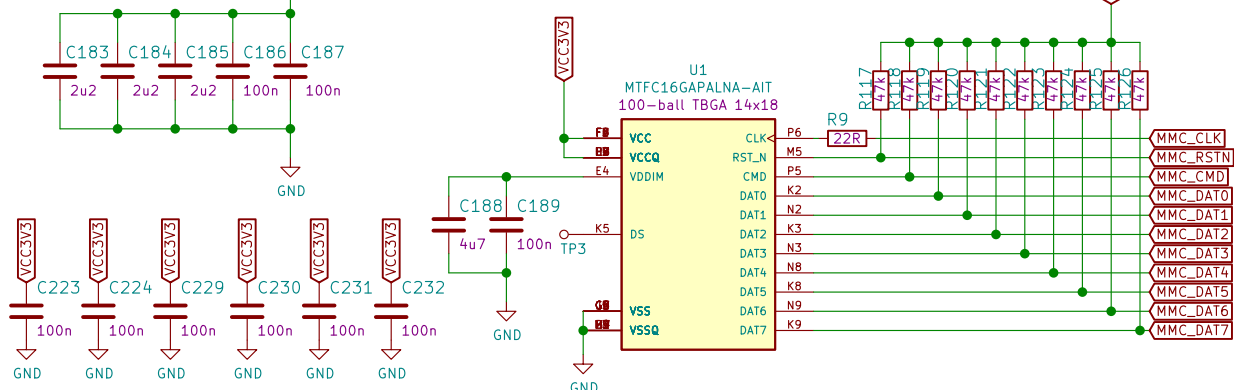
JTAG



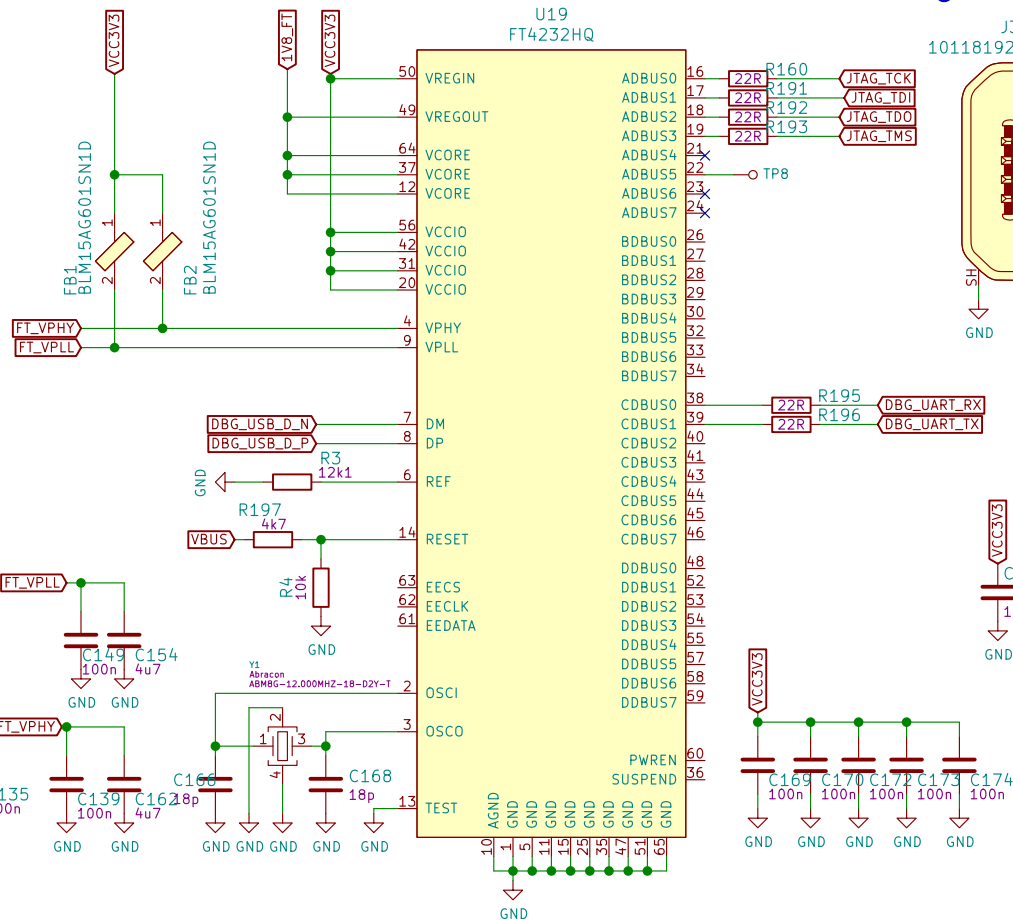
I3C voltage level translation



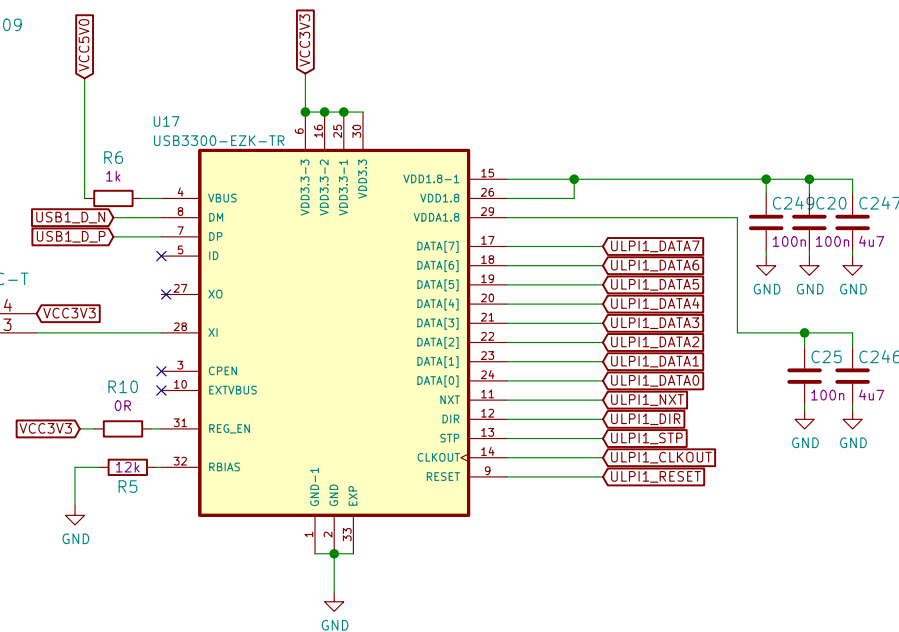
eMMC



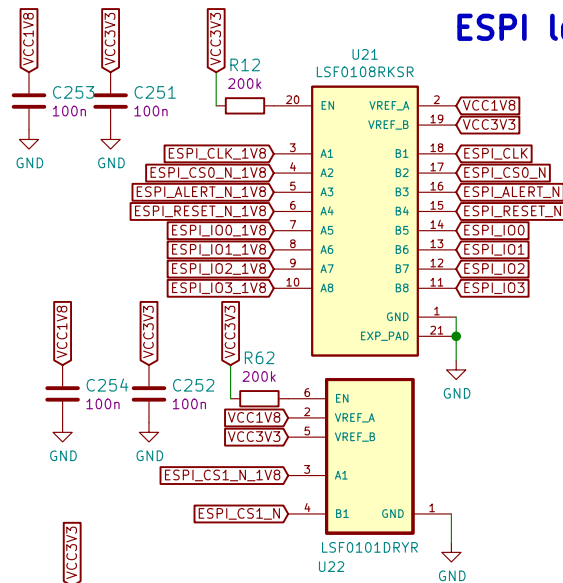
Debug USB



USB HOST

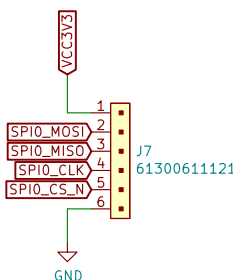


ESPI level translation

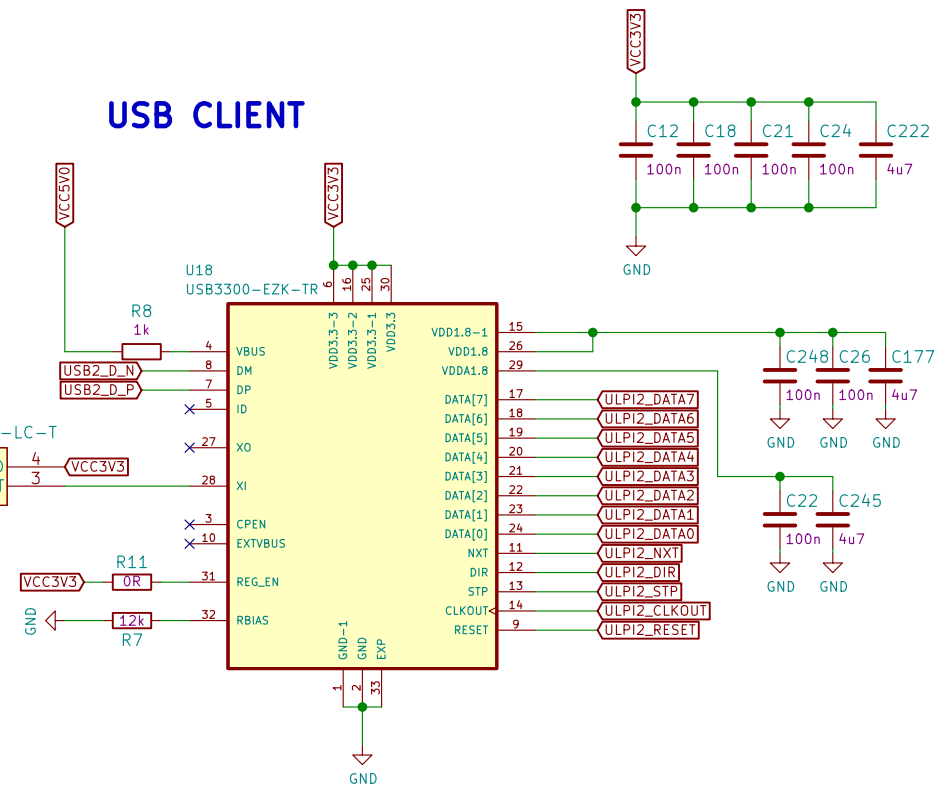


HPM SPI

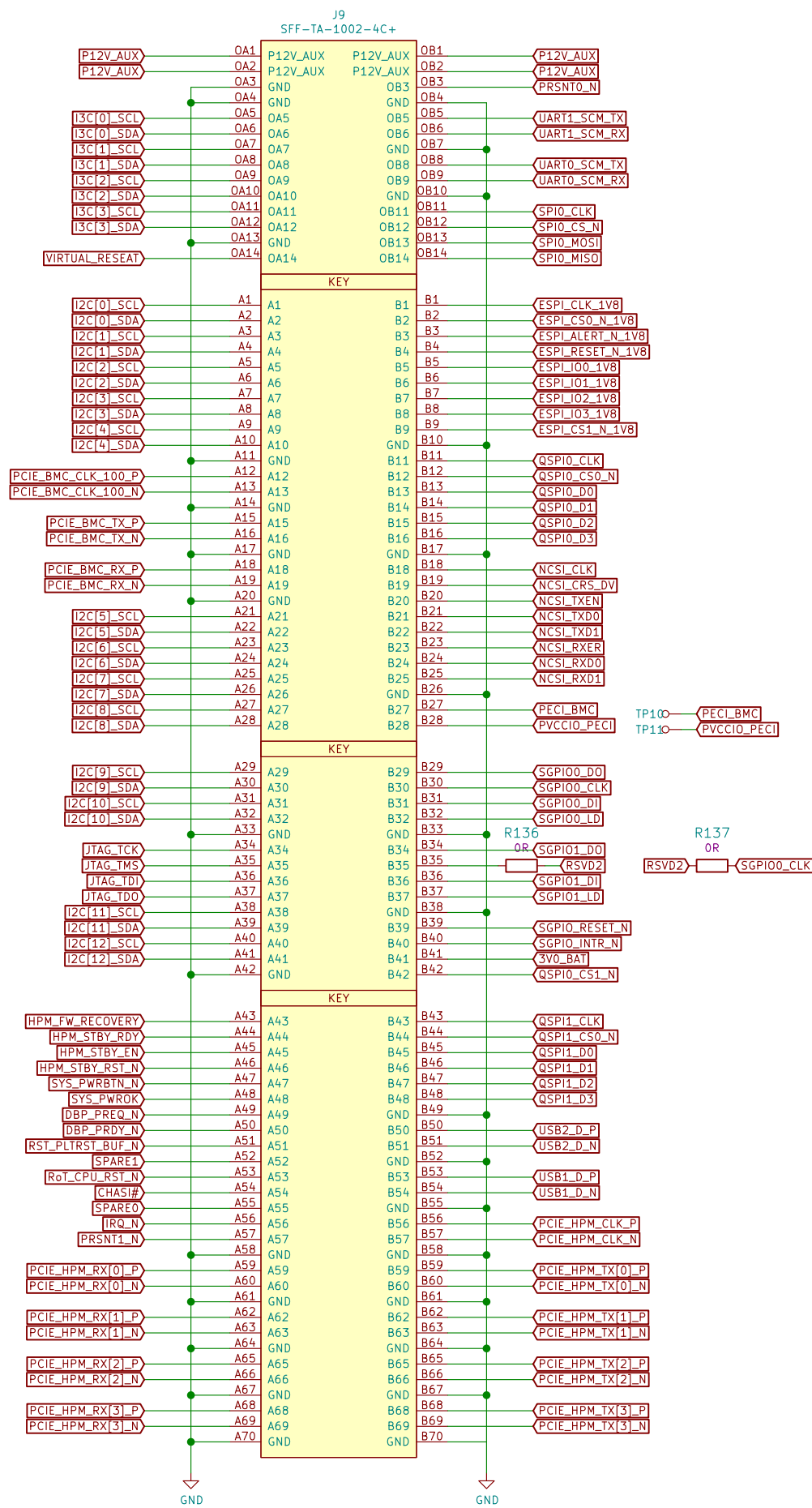
reserved for future use (as of DC-SCI OPC specification)



USB CLIENT

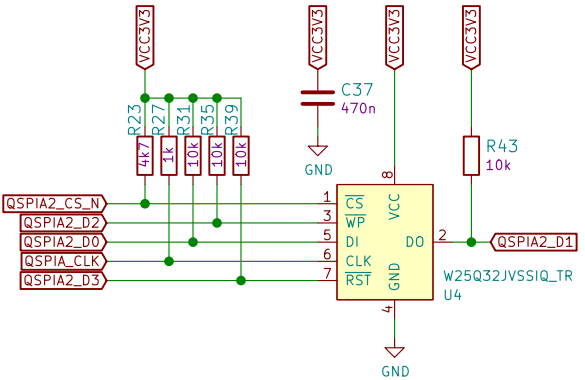
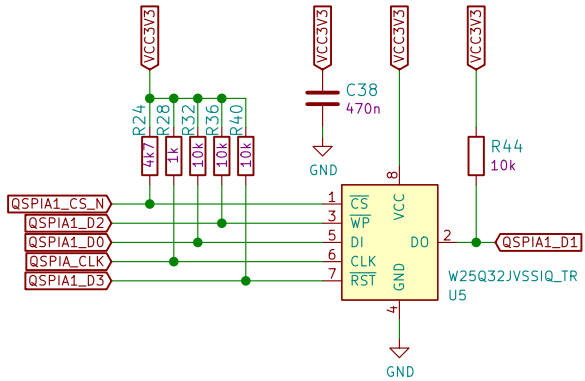


Edge connector



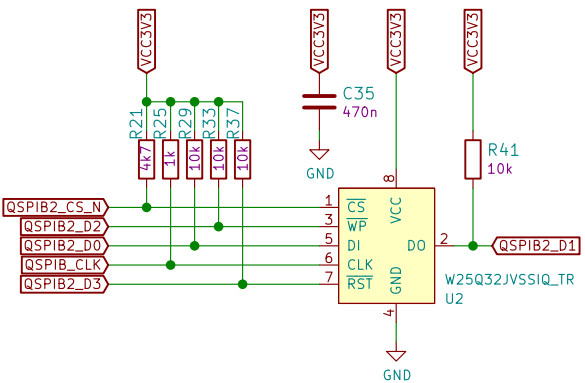
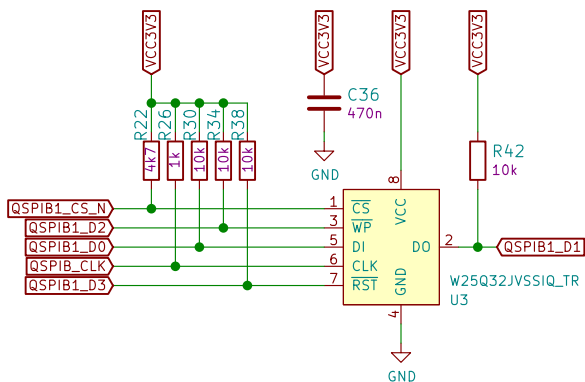
BIOS flash

One or typically two flash devices used to contain the BIOS firmware image

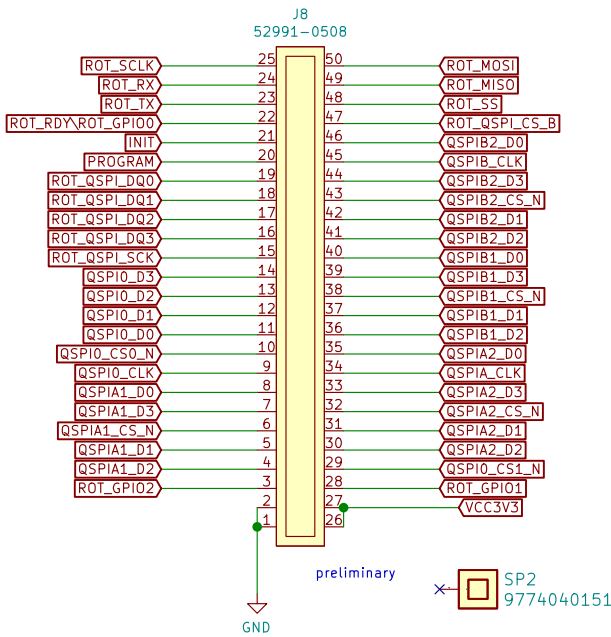


BMC flash

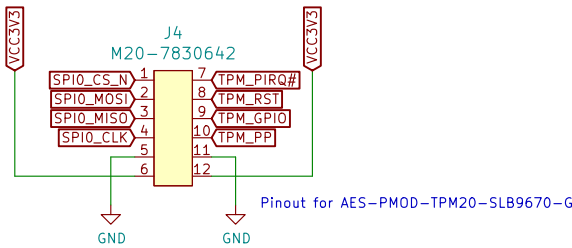
One or typically two flash devices used to contain the BMC firmware image



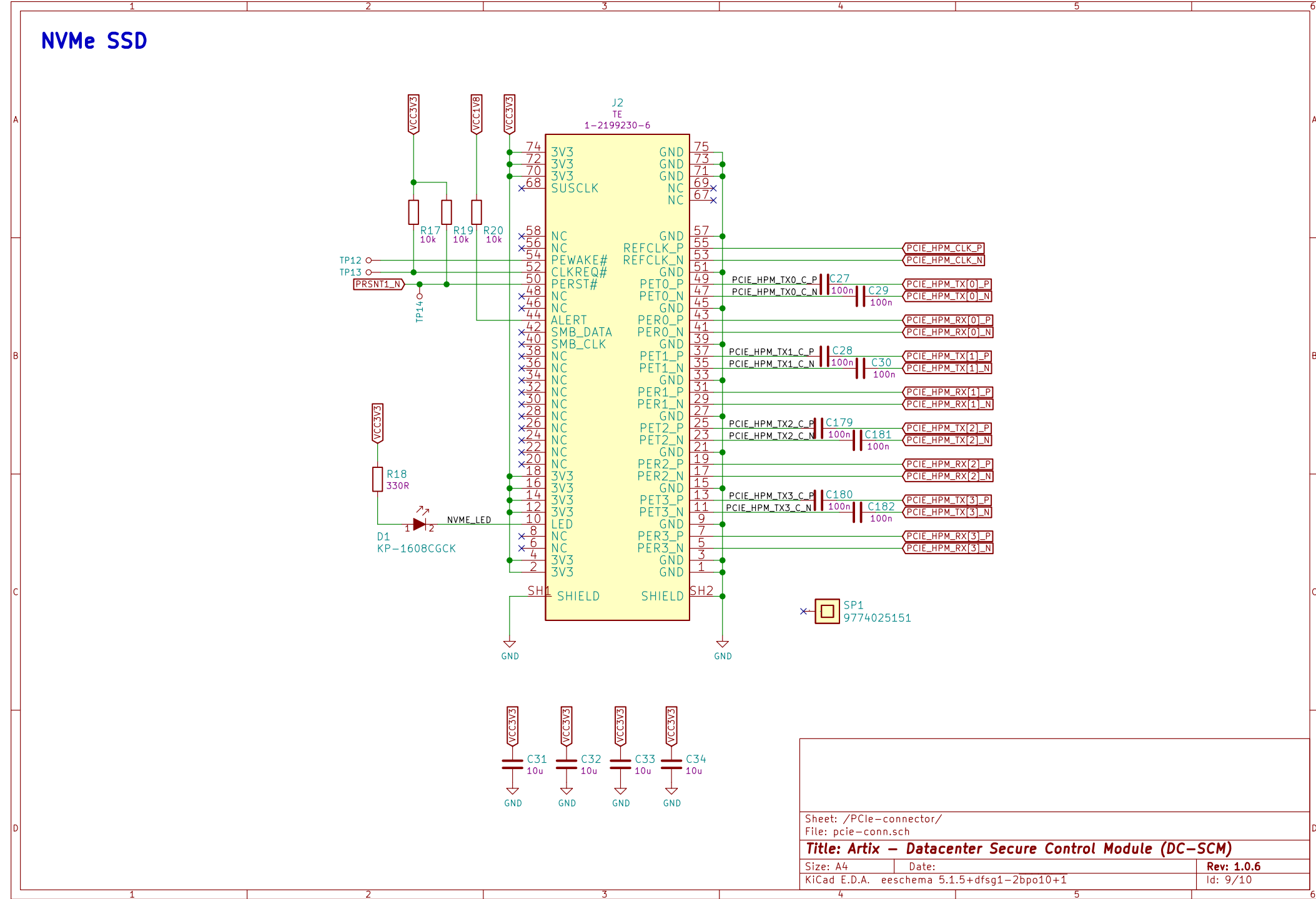
RoT module connector

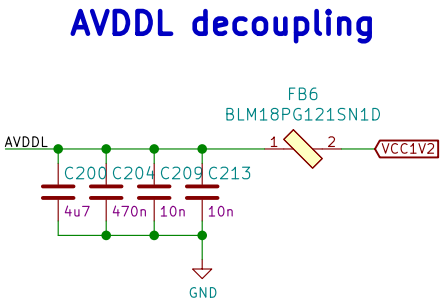
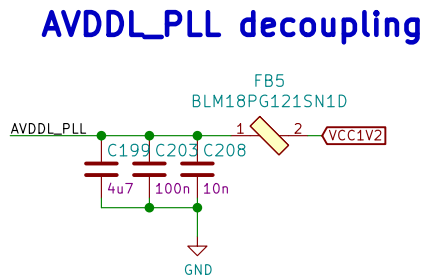
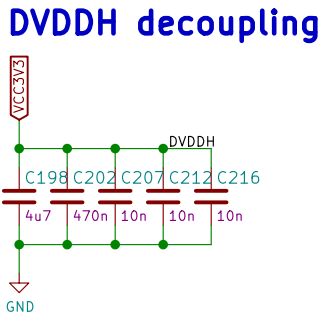
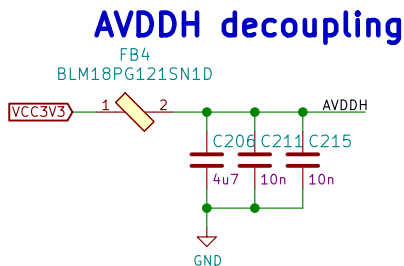
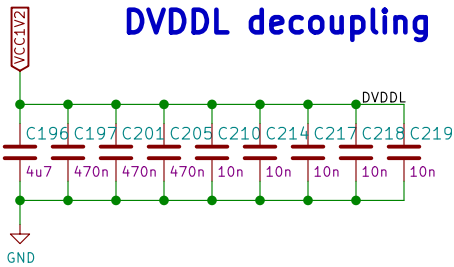


TPM connector

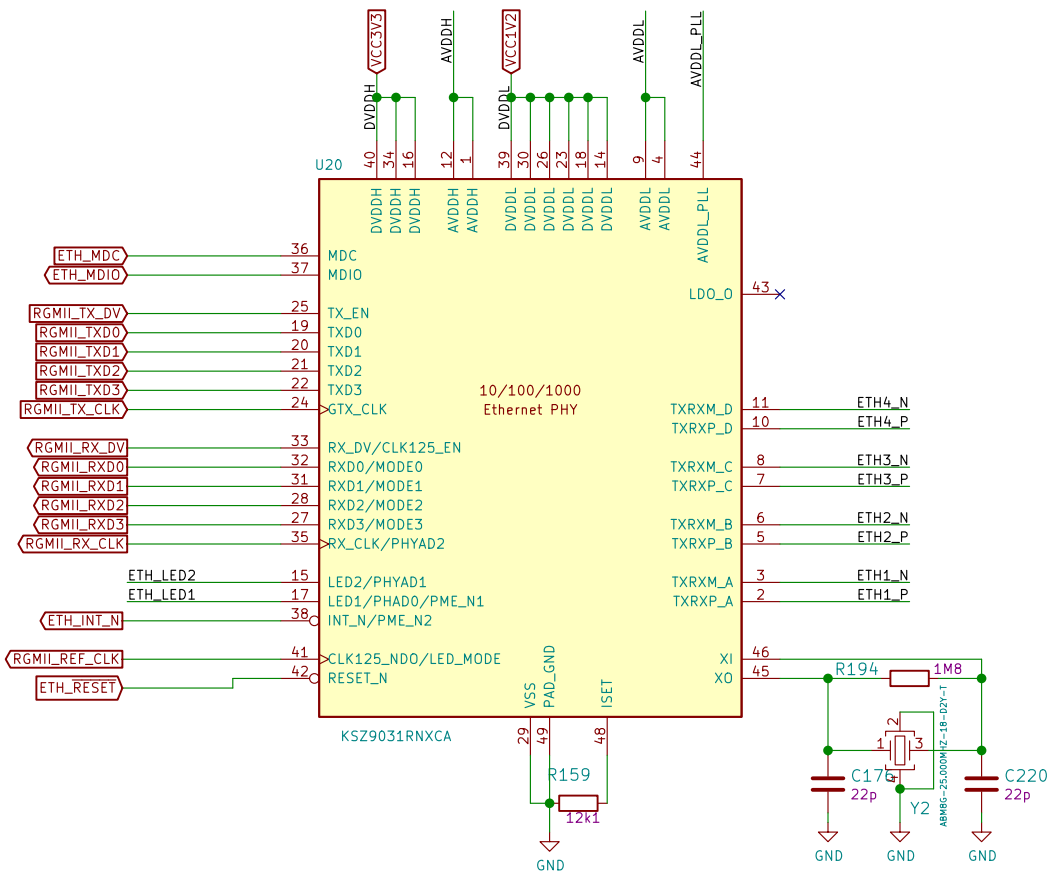


NVMe SSD

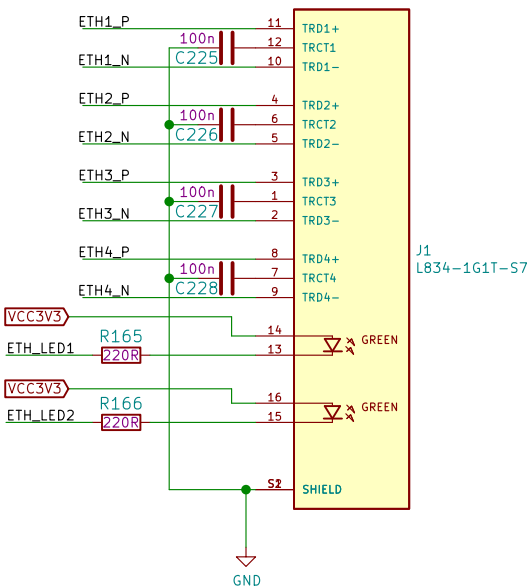




PHY



RJ45 Connector



Pull up resistors

