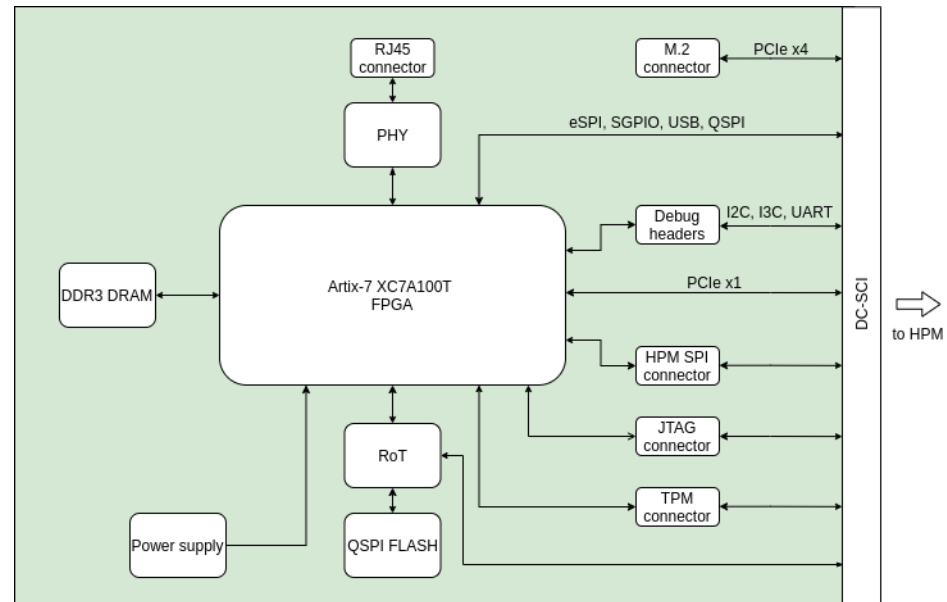


Artix – Datacenter Secure Control Module (DC-SCM)

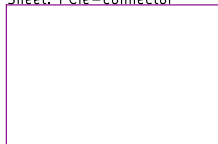


Sheet: Ethernet



File: ethernet.sch

Sheet: PCIe-connector



File: pcie-conn.sch

Sheet: RoT



File: rot.sch

Sheet: Edge connector



File: edge-connector.sch

Sheet: Interfaces



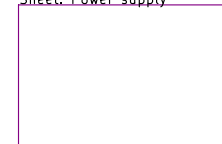
File: interfaces.sch

Sheet: DDR3



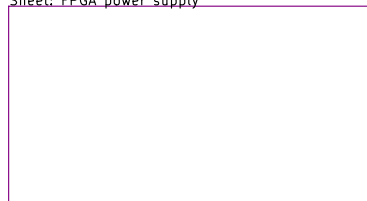
File: ddr3.sch

Sheet: Power supply



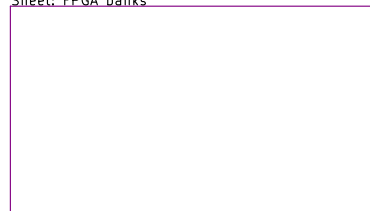
File: power-supply.sch

Sheet: FPGA power supply



File: fpga-power-supply.sch

Sheet: FPGA banks



File: fpga-banks.sch

Sheet: /

File: artix-dc-scm.sch

Title: Artix – Datacenter Secure Control Module (DC-SCM)

Size: A4

Date:

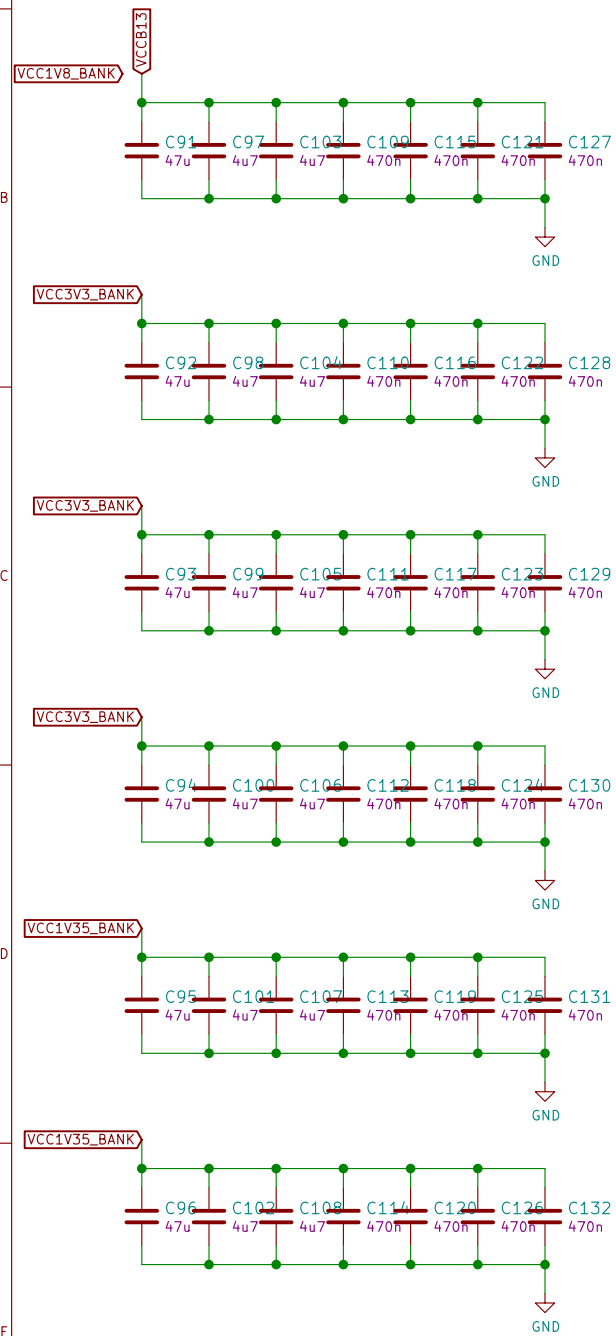
Rev: 1.0.0

KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1

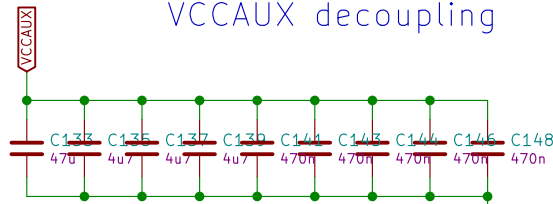
Id: 1/10

FPGA power supply

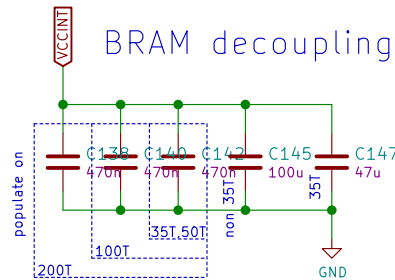
Banks decoupling



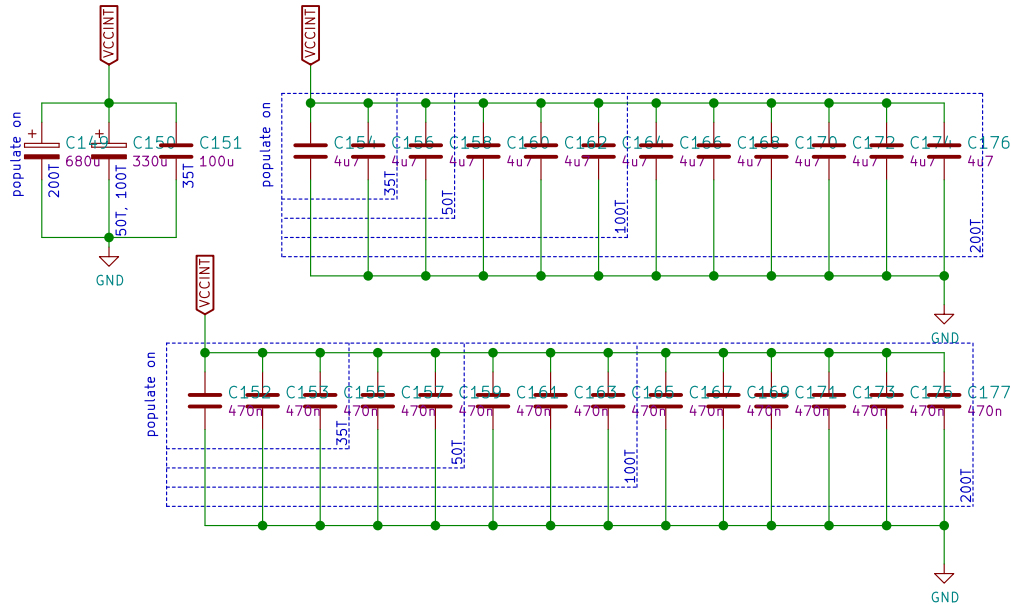
VCCAUX decoupling



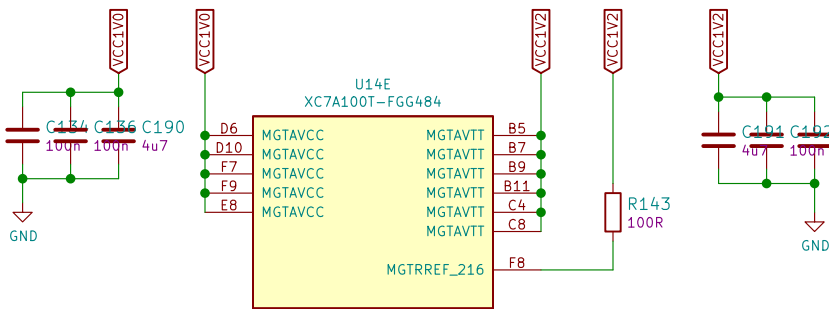
BRAM decoupling



VCCINT decoupling



Transceiver supply



External 12V supply

MainSupply (5V 5A)

Power sequencer

PWR_LED Indicators

3V3 supply

1V8 supply

1V35 supply

1V0 supply

Battery connector

Power Sequencing Table:

STEP	DESCRIPTION
STEP1:	VRs start and RoT boots (HPM_STBY_EN when both are done)
STEP2:	HPM starts its VRs and sets HPM_STBY_RDY when done
STEP3:	FPGA VCCINT (1.0V)
STEP4:	FPGA VCCAUX + DDR3 (1.8V, 1.35V)
STEP5:	FPGA VCCIO + DDR3 (3.3V, DDRVTT), HPM reset is de-asserted
STEP6:	HPM boots

Notes:

- TODO: decide which DC-SCI pin connected to FPGA does this

Sheet: /Power supply/
File: power-supply.sch
Title: Artix - Datacenter Secure Control Module (DC-SCM)
Size: A3 **Date:** **Rev: 1.0.0**
KiCad E.D.A. kiCad 5.1.5+dfsg1-2bpo10+1 **Id: 4/10**

External 12V supply

MainSupply (5V 5A)

PWR_LED Indicators

3V3 supply

1V8 supply

1V35 supply

1V0 supply

Battery connector

Power sequencer

STEP1: VRs start and RoT boots (HPM_STBY_EN when both are done)
STEP2: HPM starts its VRs and sets HPM_STBY_RDY when done
STEP3: FPGA VCCINT (1.0V)
STEP4: FPGA VCCAUX + DDR3 (1.8V, 1.35V)
STEP5: FPGA VCCIO + DDR3 (3.3V, DDRVTT), HPM reset is de-asserted
STEP6: HPM boots
 * TODO: decide which DC-SCI pin connected to FPGA does this

Sheet: /Power supply/
 File: power-supply.sch
Title: Artix - Datacenter Secure Control Module (DC-SCM)
 Size: A3 Date: Rev: 1.0.0
 KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1 Id: 4/10

External 12V supply

MainSupply (5V 5A)

Power sequencer

PWR_LED Indicators

3V3 supply

1V8 supply

1V35 supply

1V0 supply

Battery connector

Power Sequencing Table:

STEP	DESCRIPTION
STEP1:	VRs start and RoT boots (HPM_STBY_EN when both are done)
STEP2:	HPM starts its VRs and sets HPM_STBY_RDY when done
STEP3:	FPGA VCCINT (1.0V)
STEP4:	FPGA VCCAUX + DDR3 (1.8V, 1.35V)
STEP5:	FPGA VCCIO + DDR3 (3.3V, DDRVTT), HPM reset is de-asserted
STEP6:	HPM boots

Notes:

- TODO: decide which DC-SCI pin connected to FPGA does this

Sheet Information:

Sheet: /Power supply/
File: power-supply.sch
Title: Artix - Datacenter Secure Control Module (DC-SCM)
Size: A3 Date: Rev: 1.0.0
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1 Id: 4/10

External 12V supply

MainSupply (5V 5A)

3V3 supply

1V8 supply

1V35 supply

1V0 supply

Power sequencer

PWR_LED Indicators

Battery connector

STEP1: VRs start and RoT boots (HPM_STBY_EN when both are done)
STEP2: HPM starts its VRs and sets HPM_STBY_RDY when done
STEP3: FPGA VCCINT (1.0V)
STEP4: FPGA VCCAUX + DDR3 (1.8V, 1.35V)
STEP5: FPGA VCCIO + DDR3 (3.3V, DDRVTT), HPM reset is de-asserted
STEP6: HPM boots

TODO: decide which DC-SCI pin connected to FPGA does this

Sheet: /Power supply/
File: power-supply.sch
Title: Artix - Datacenter Secure Control Module (DC-SCM)
Size: A3 Date: Rev: 1.0.0
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1 Id: 4/10

External 12V supply

MainSupply (5V 5A)

3V3 supply

1V8 supply

1V35 supply

1V0 supply

Power sequencer

PWR_LED Indicators

Battery connector

STEP1: VRs start and RoT boots (HPM_STBY_EN when both are done)
STEP2: HPM starts its VRs and sets HPM_STBY_RDY when done
STEP3: FPGA VCCINT (1.0V)
STEP4: FPGA VCCAUX + DDR3 (1.8V, 1.35V)
STEP5: FPGA VCCIO + DDR3 (3.3V, DDRVTT), HPM reset is de-asserted
STEP6: HPM boots

TODO: decide which DC-SCI pin connected to FPGA does this

Sheet: /Power supply/
File: power-supply.sch
Title: Artix - Datacenter Secure Control Module (DC-SCM)
Size: A3 Date: Rev: 1.0.0
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1 Id: 4/10

External 12V supply

MainSupply (5V 5A)

3V3 supply

1V8 supply

1V35 supply

1V0 supply

Power sequencer

PWR_LED Indicators

Battery connector

STEP1: VRs start and RoT boots (HPM_STBY_EN when both are done)
STEP2: HPM starts its VRs and sets HPM_STBY_RDY when done
STEP3: FPGA VCCINT (1.0V)
STEP4: FPGA VCCAUX + DDR3 (1.8V, 1.35V)
STEP5: FPGA VCCIO + DDR3 (3.3V, DDRVTT), HPM reset is de-asserted
STEP6: HPM boots

TODO: decide which DC-SCI pin connected to FPGA does this

Sheet: /Power supply/
File: power-supply.sch
Title: Artix - Datacenter Secure Control Module (DC-SCM)
Size: A3 Date: Rev: 1.0.0
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1 Id: 4/10

External 12V supply

MainSupply (5V 5A)

3V3 supply

1V8 supply

1V35 supply

1V0 supply

Power sequencer

PWR_LED Indicators

Battery connector

STEP1: VRs start and RoT boots (HPM_STBY_EN when both are done)
STEP2: HPM starts its VRs and sets HPM_STBY_RDY when done
STEP3: FPGA VCCINT (1.0V)
STEP4: FPGA VCCAUX + DDR3 (1.8V, 1.35V)
STEP5: FPGA VCCIO + DDR3 (3.3V, DDRVTT), HPM reset is de-asserted
STEP6: HPM boots

TODO: decide which DC-SCI pin connected to FPGA does this

Sheet: /Power supply/
File: power-supply.sch
Title: Artix - Datacenter Secure Control Module (DC-SCM)
Size: A3 Date: Rev: 1.0.0
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1 Id: 4/10

External 12V supply

MainSupply (5V 5A)

Power sequencer

PWR_LED Indicators

3V3 supply

1V8 supply

1V35 supply

1V0 supply

Battery connector

Power Sequencing Table:

STEP	DESCRIPTION
STEP1:	VRs start and RoT boots (HPM_STBY_EN when both are done)
STEP2:	HPM starts its VRs and sets HPM_STBY_RDY when done
STEP3:	FPGA VCCINT (1.0V)
STEP4:	FPGA VCCAUX + DDR3 (1.8V, 1.35V)
STEP5:	FPGA VCCIO + DDR3 (3.3V, DDRVTT), HPM reset is de-asserted
STEP6:	HPM boots

Notes:

- TODO: decide which DC-SCI pin connected to FPGA does this

Sheet Information:

Sheet: /Power supply/
File: power-supply.sch
Title: Artix - Datacenter Secure Control Module (DC-SCM)
Size: A3 Date: Rev: 1.0.0
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1 Id: 4/10

External 12V supply

MainSupply (5V 5A)

Power sequencer

PWR_LED Indicators

3V3 supply

1V8 supply

1V35 supply

1V0 supply

Battery connector

Power Sequencing Table:

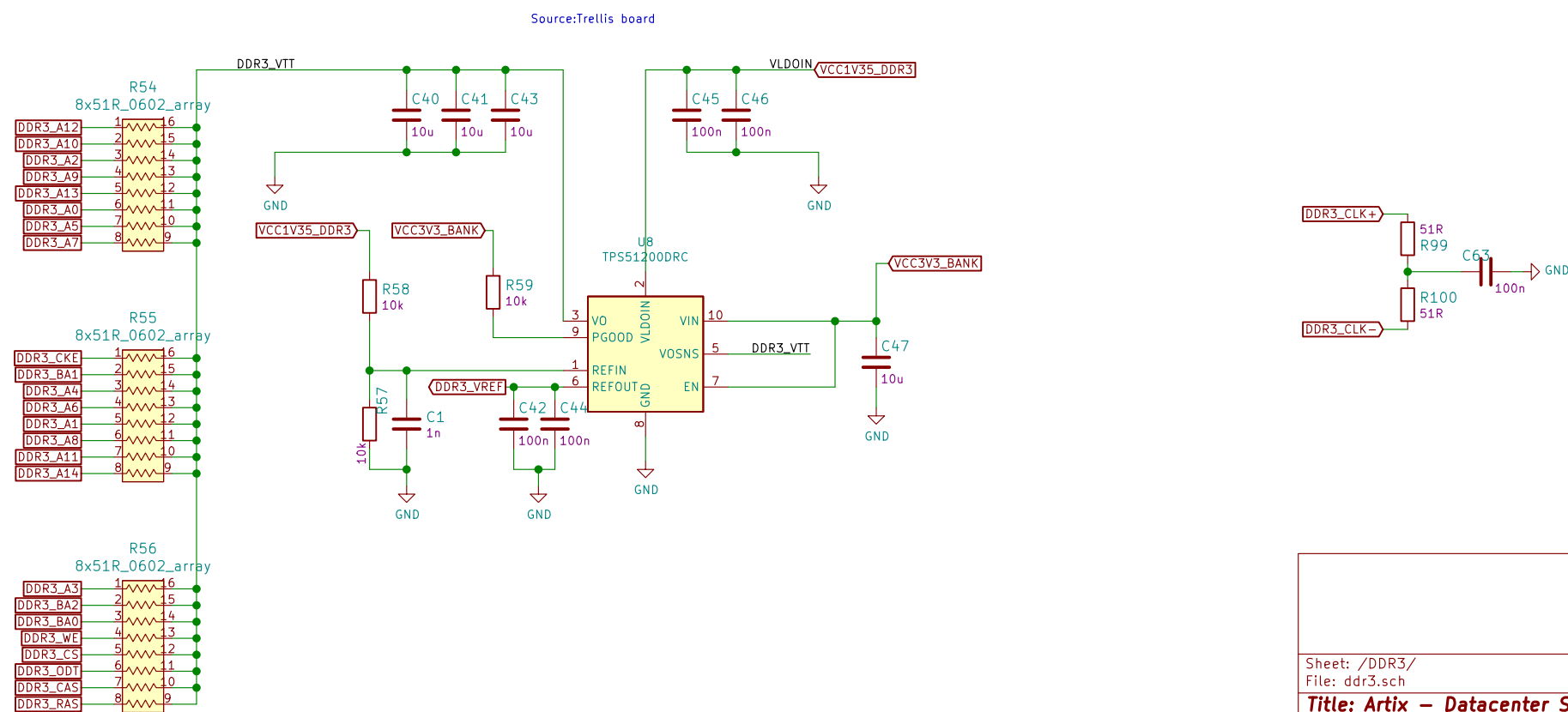
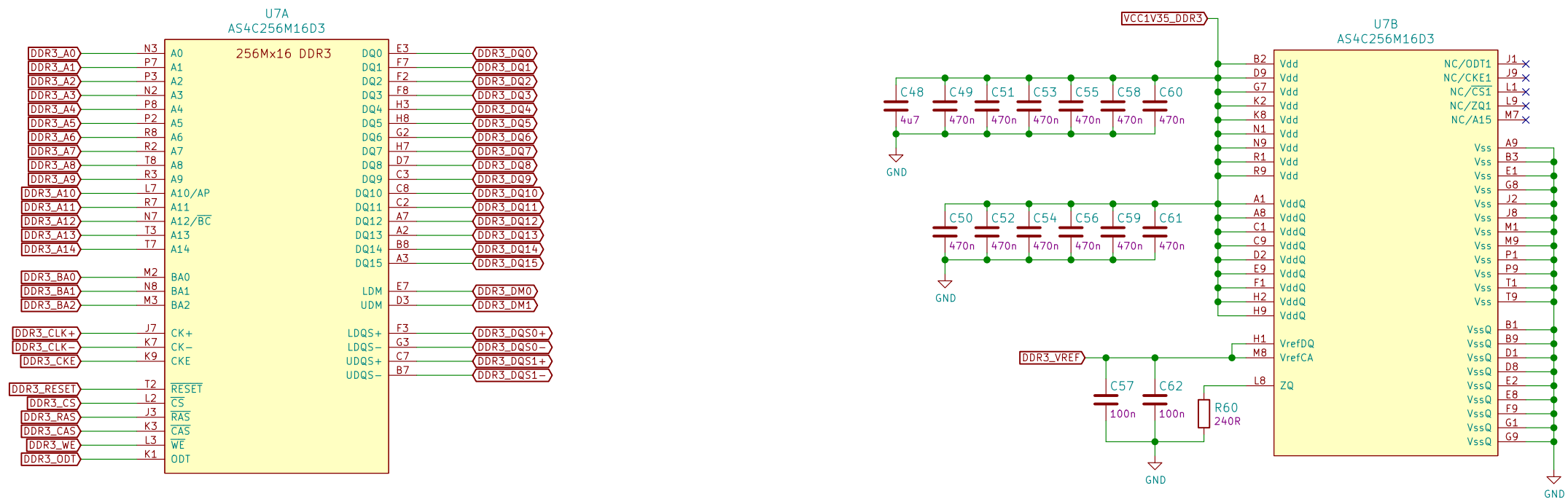
STEP	DESCRIPTION
STEP1:	VRs start and RoT boots (HPM_STBY_EN when both are done)
STEP2:	HPM starts its VRs and sets HPM_STBY_RDY when done
STEP3:	FPGA VCCINT (1.0V)
STEP4:	FPGA VCCAUX + DDR3 (1.8V, 1.35V)
STEP5:	FPGA VCCIO + DDR3 (3.3V, DDRVTT), HPM reset is de-asserted
STEP6:	HPM boots

Notes:

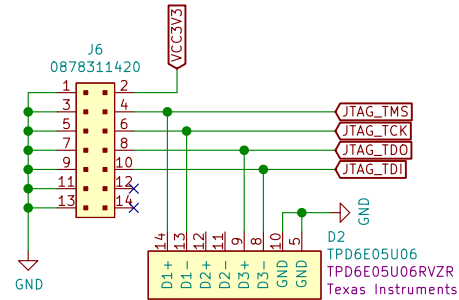
- TODO: decide which DC-SCI pin connected to FPGA does this

Sheet Information:

Sheet: /Power supply/
File: power-supply.sch
Title: Artix - Datacenter Secure Control Module (DC-SCM)
Size: A3 Date: Rev: 1.0.0
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1 Id: 4/10



Compatible with Xilinx Platform Cable

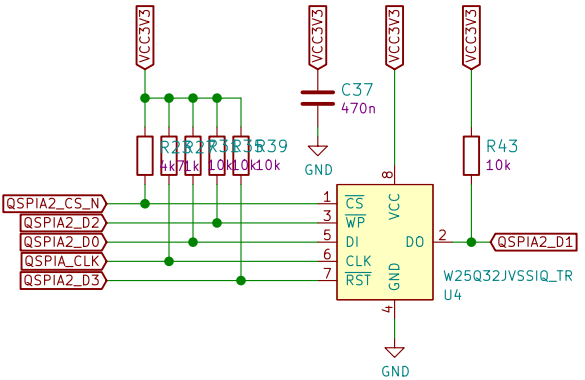
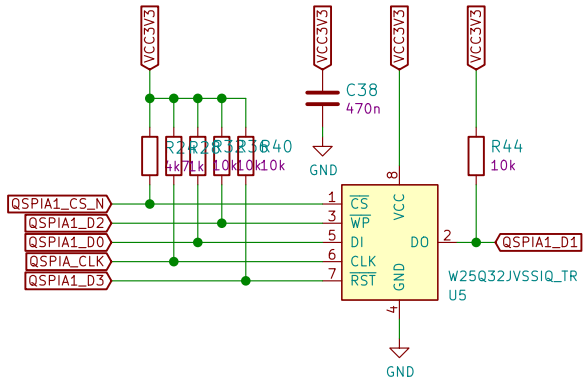


U140
XC7A100T-FGG484

Title: Artix – Datacenter Secure Control Module (DC-SCM)		
Size: A3	Date:	Rev: 1.0.0
KICad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 7/10

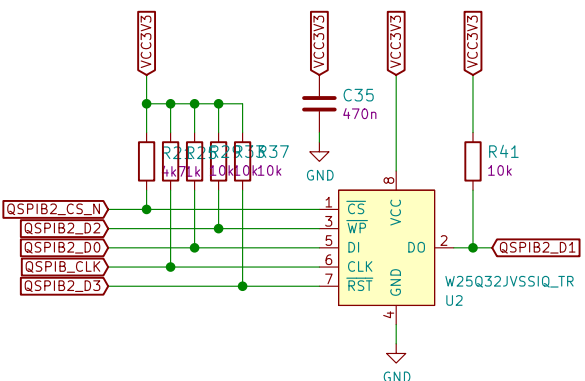
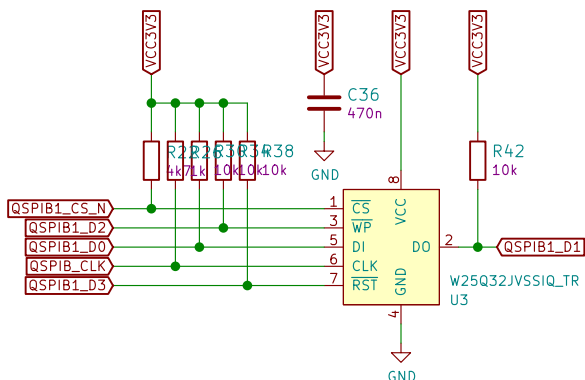
BIOS flash

One or typically two flash devices used to contain the BIOS firmware image

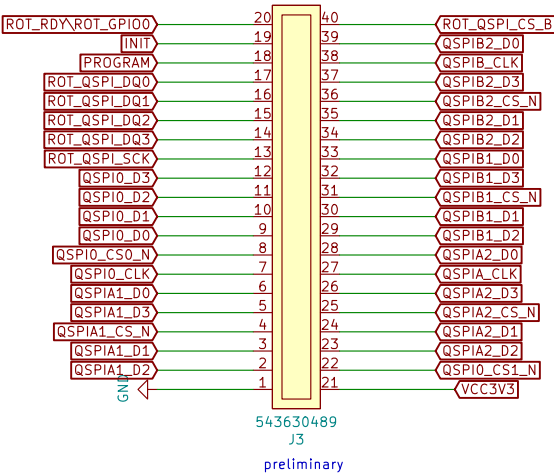


BMC flash

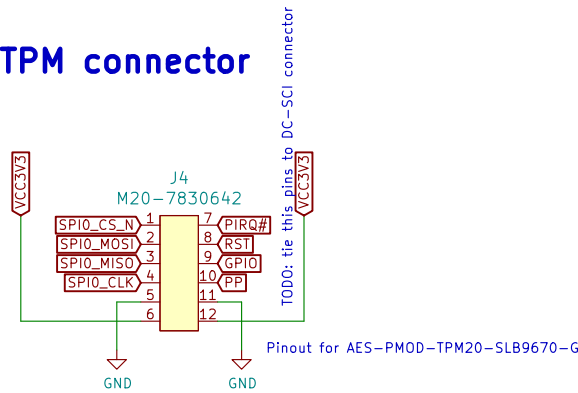
One or typically two flash devices used to contain the BMC firmware image



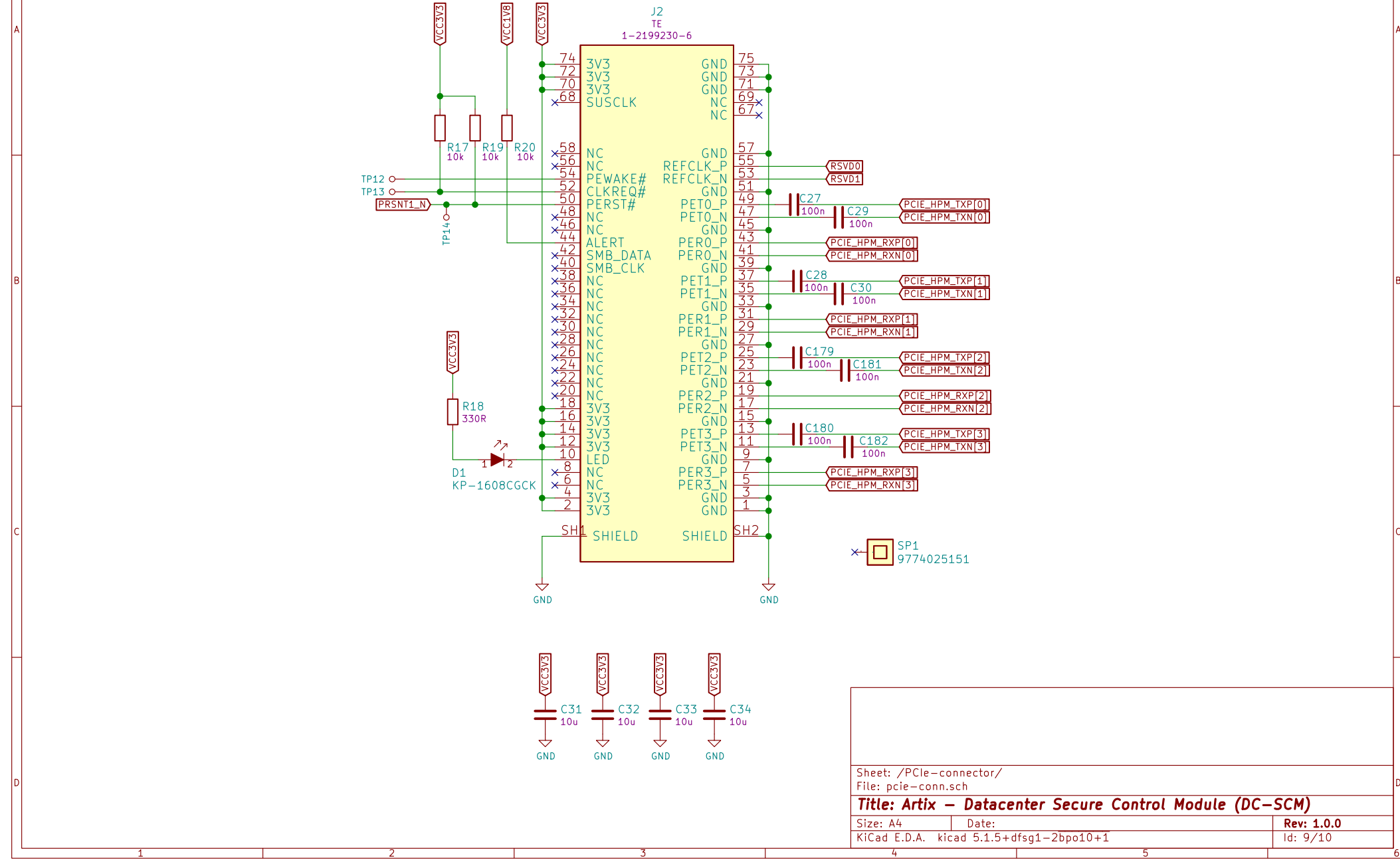
RoT module connector



TPM connector



NVMe SSD



Ethernet transceiver

RJ45 Connector

