

Data Center RDIMM DDR4 Tester



HyperRAM



File: hyperram.kicad_sch

DDR4



File: DDR4.kicad_sch

Interfaces



File: interfaces.kicad_sch

Ethernet



File: ethernet.kicad_sch

Supply



File: supply.kicad_sch

FMC_HPC



File: fmc_hpc.kicad_sch

Config SPI flash



File: config-spi.kicad_sch

FPGA power



File: fpga-power.kicad_sch

FPGA banks 12–15



File: fpga-banks-12-15.kicad_sch

FPGA banks 16–34



File: fpga-banks-16-34.kicad_sch

FPGA banks 115–116



File: pcie.kicad_sch

A

A

B

B

C

C

D

D

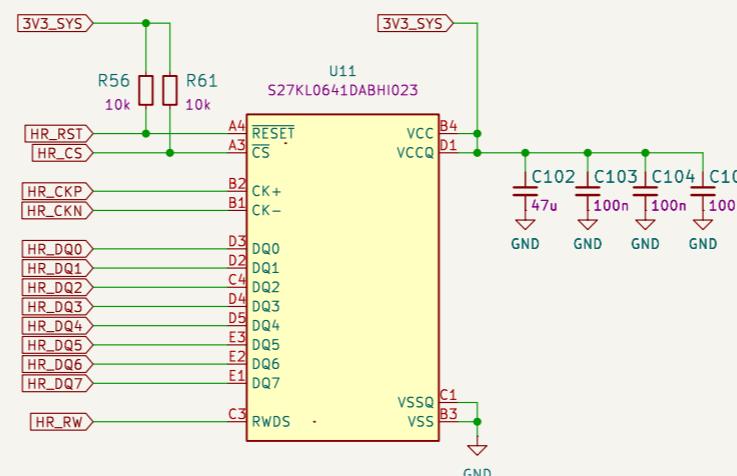
E

E

F

F

HyperRAM

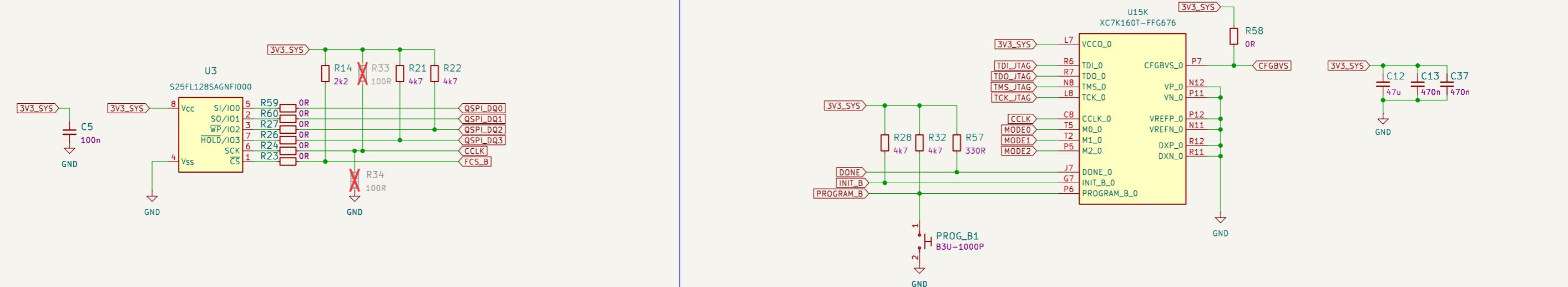


1 2 3 4 5 6 7 8

Master SPI Quad (x4) configuration scheme

Follows Figure 2-14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

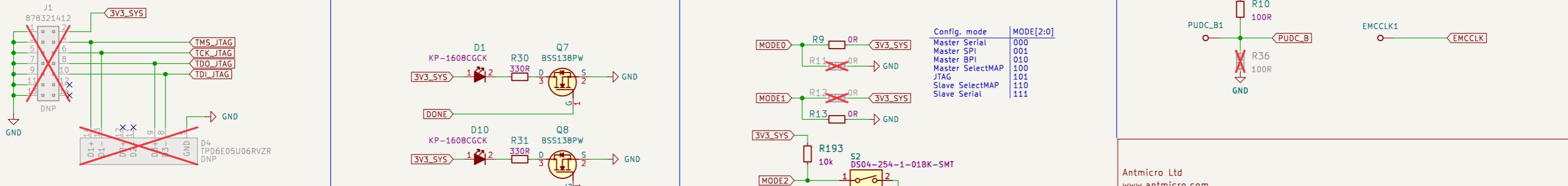
(Q)SPI flash



FPGA BANK 0

JTAG Connector

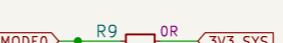
Compatible with Xilinx Platform Cable



STATUS LEDs

Configuration Modes

For details, see UG470 p. 21



Config. mode	MODE[2:0]
Master Serial	000
Master SPI	001
Master BPI	010
Master SelectMAP	100
JTAG	101
Slave SelectMAP	110
Slave Serial	111

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Sheet: /Config SPI flash/
File: config-spi.kicad_sch

Title: Data Center RDIMM DDR4 Tester

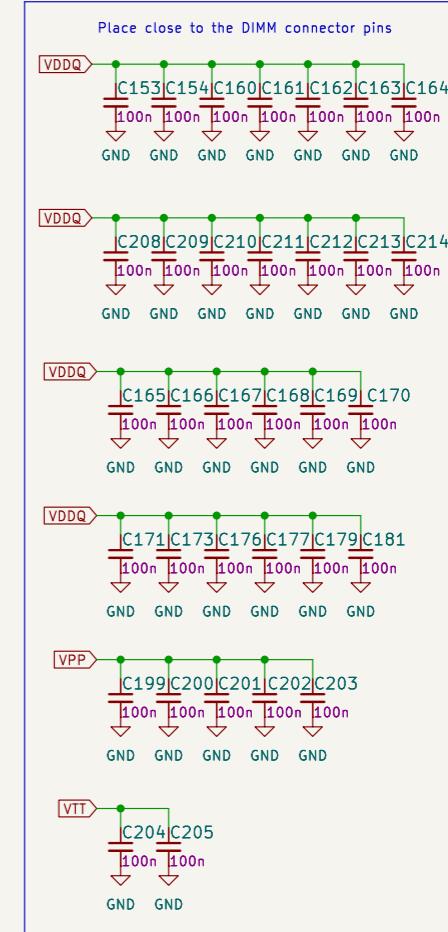
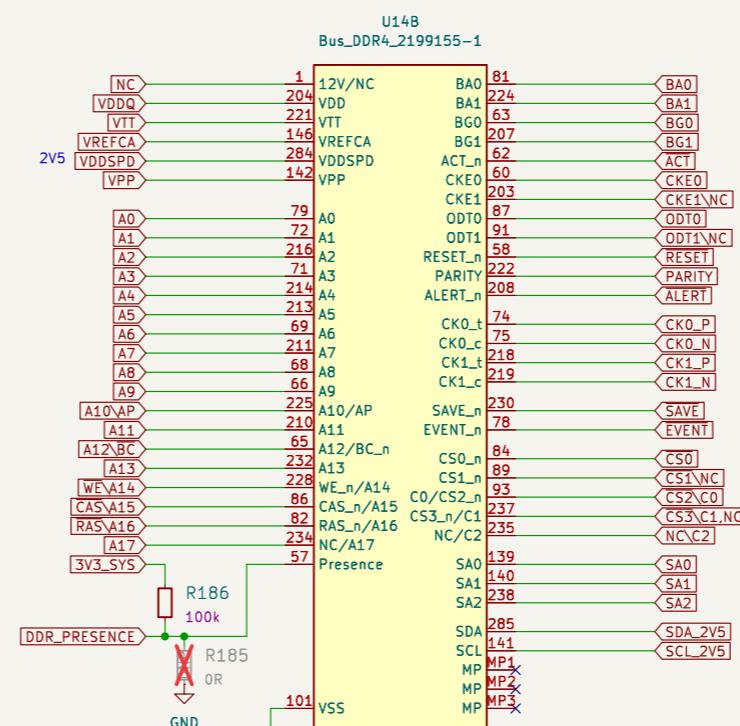
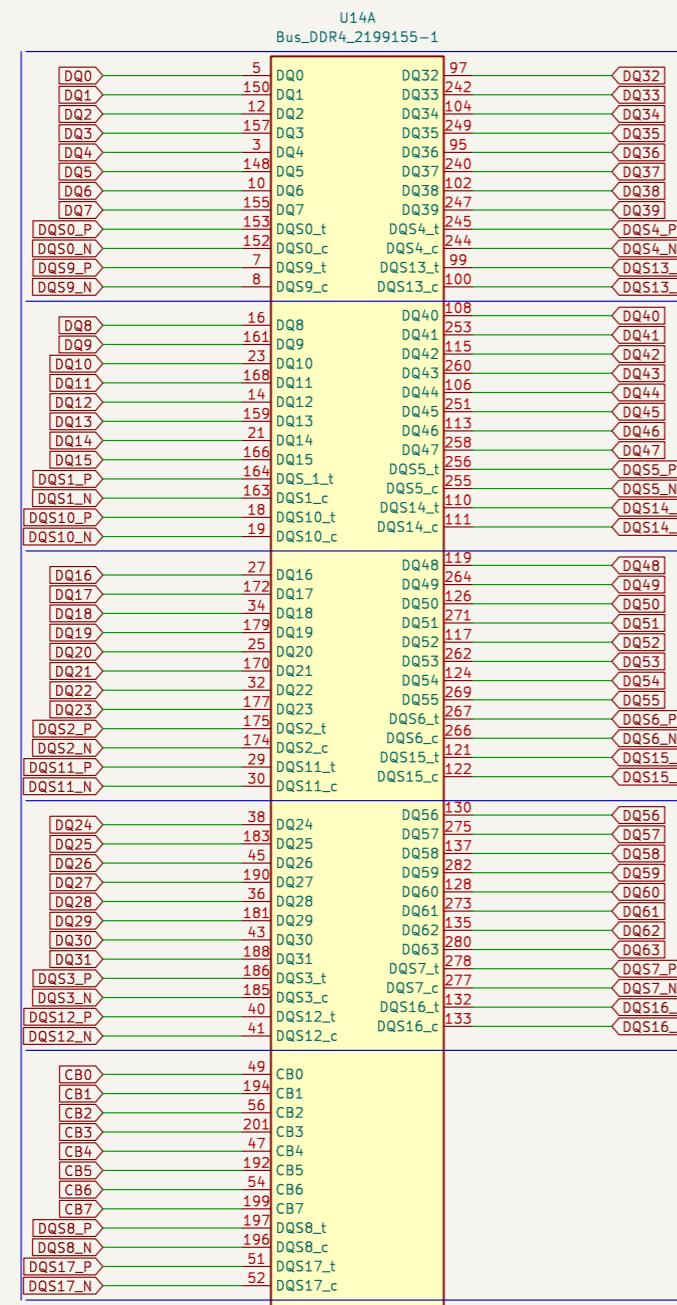
Size: A3 | Date: 2024-02-12
KiCad E.D.A. kicad-cli 7.0.10+1

Rev: 1.2.3:3f1c9
Id: 3/12



DDR4 RDIMM connector

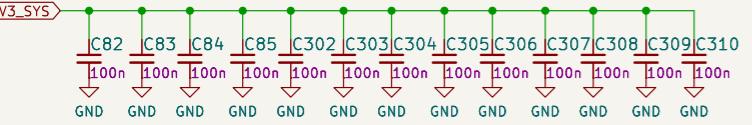
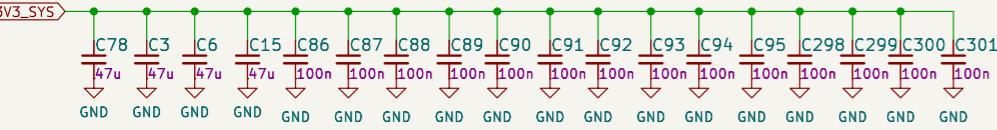
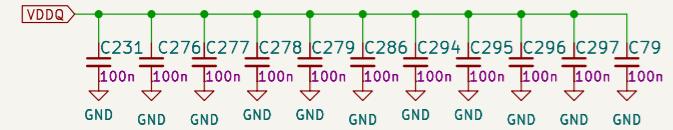
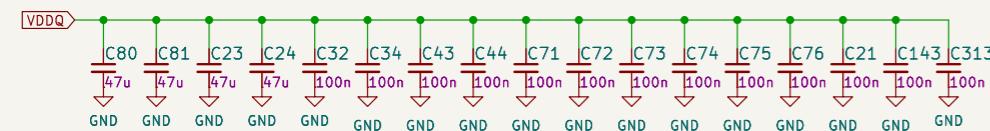
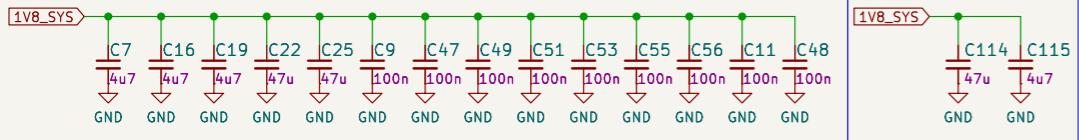
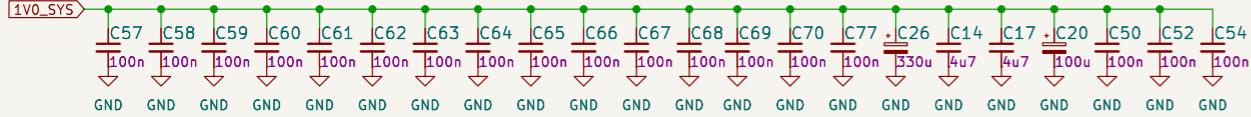
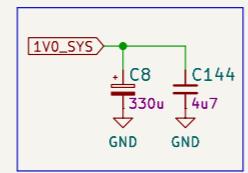
A



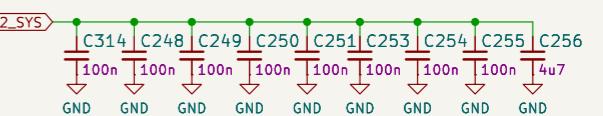
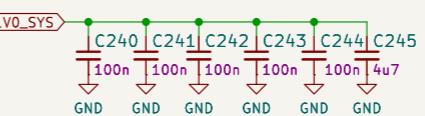
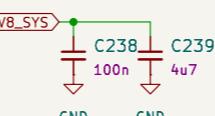
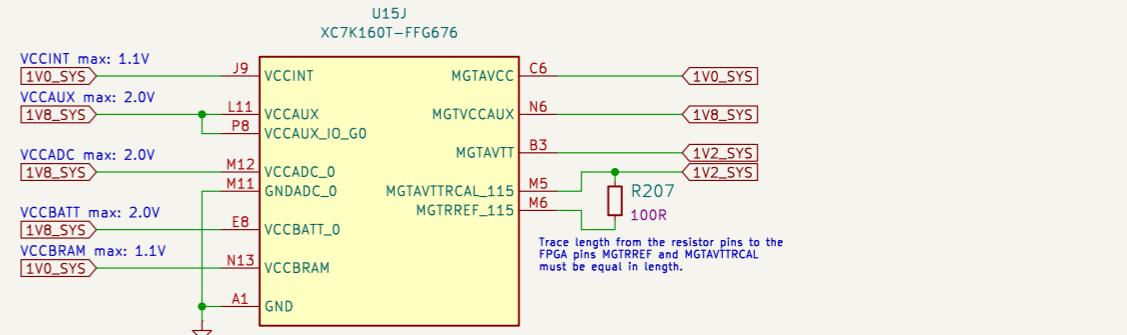
1 2 3 4 5 6 7 8

A

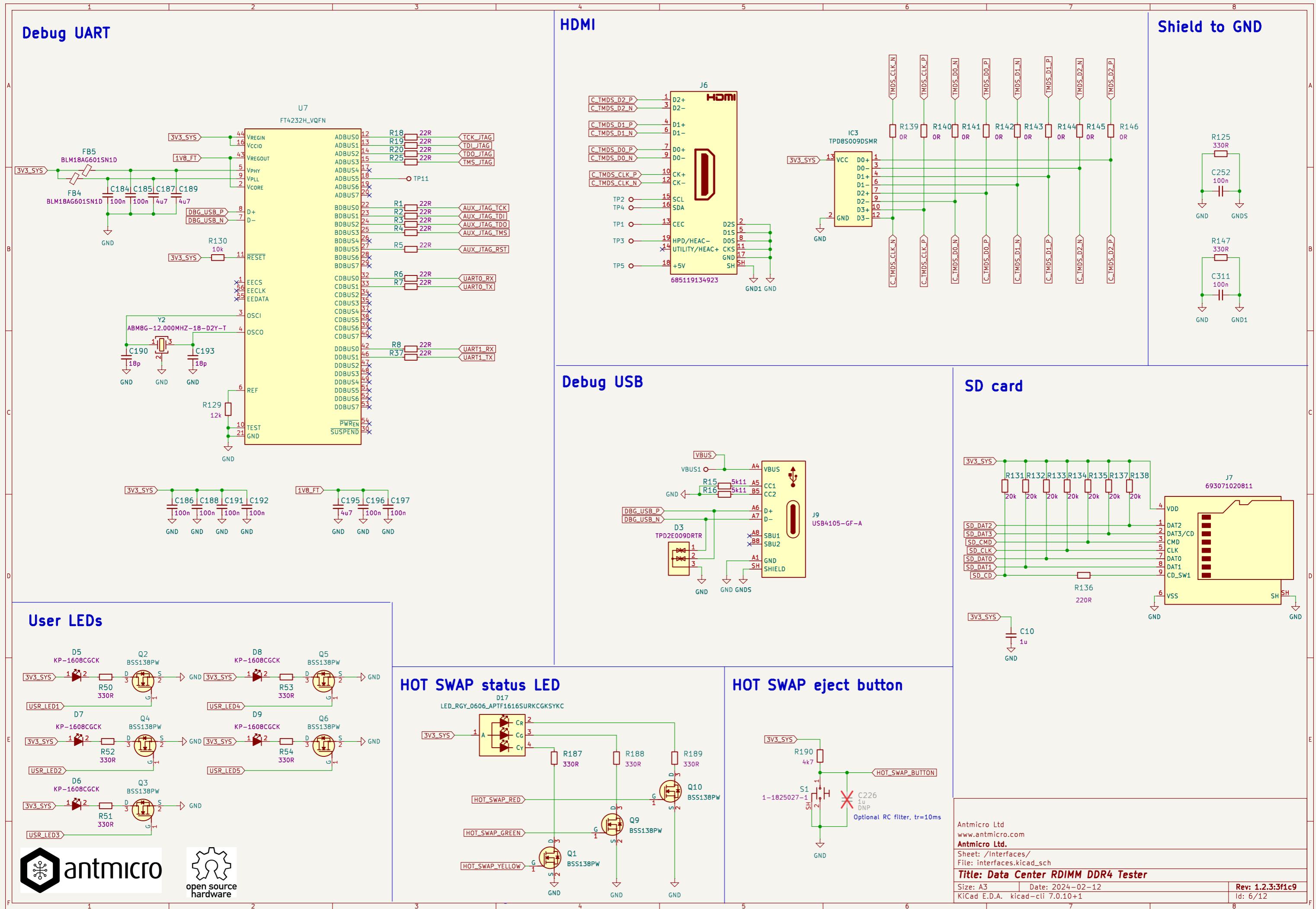
Added capacitors corresponding to PCB Design Guide UG483

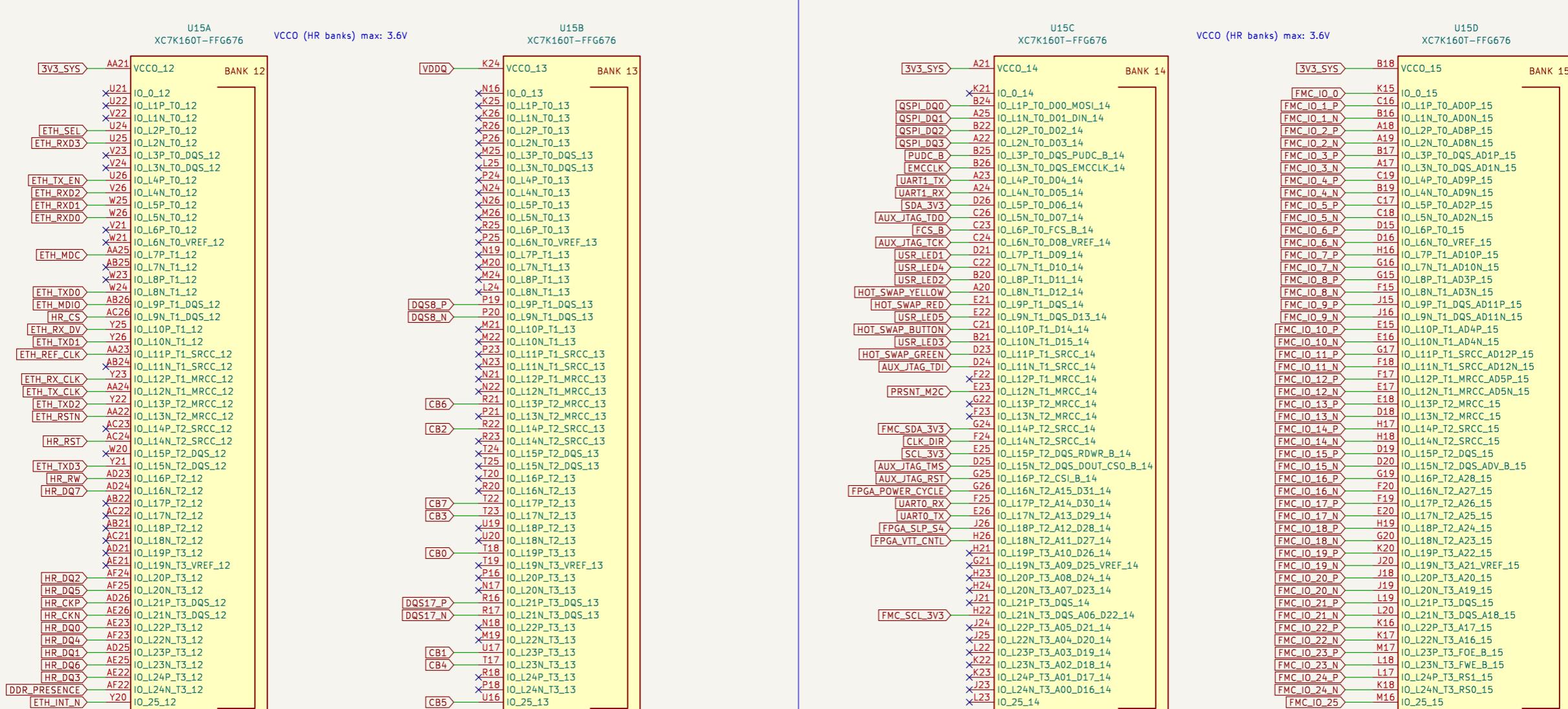


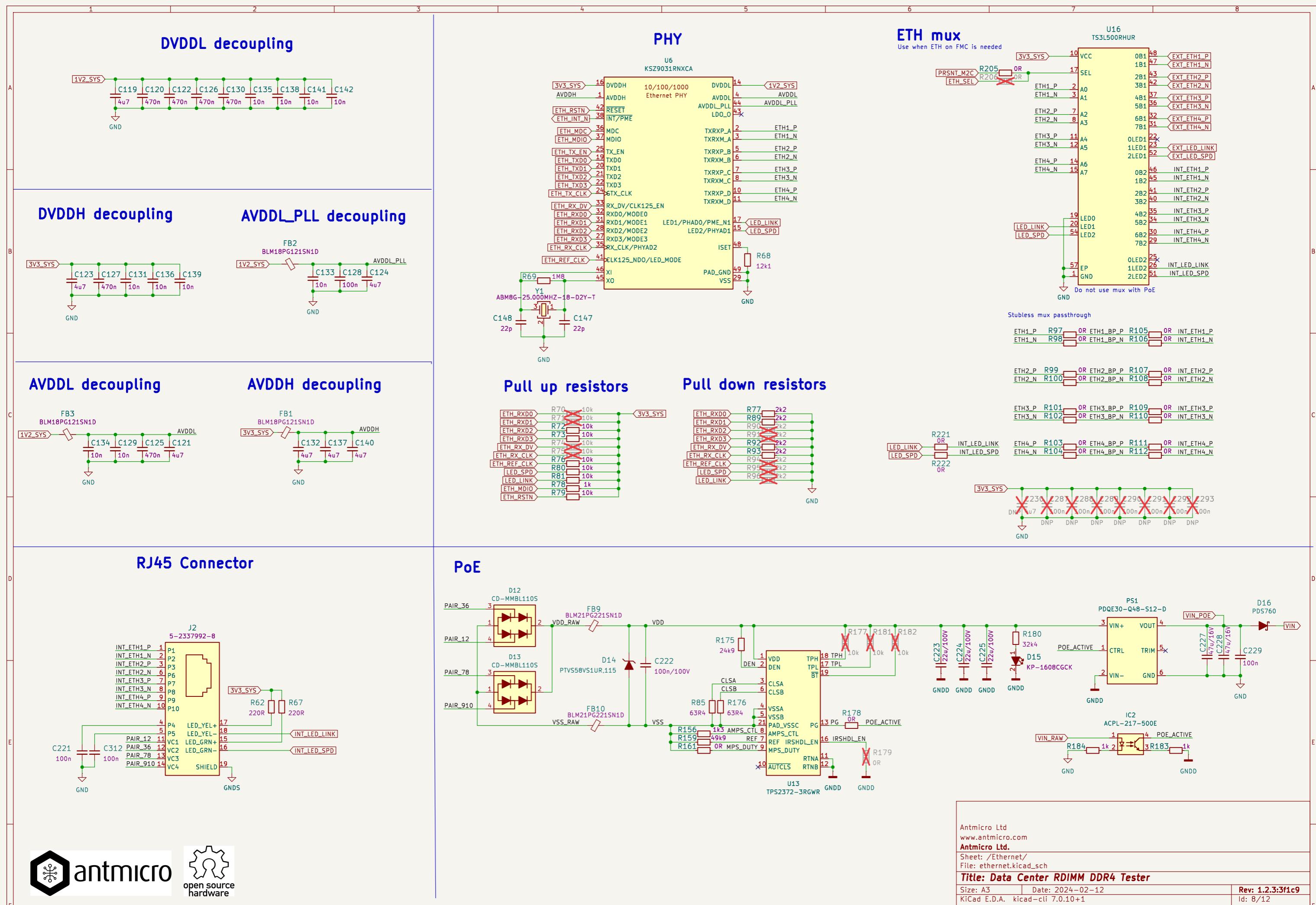
POWER RAILS
Decoupling referenced from 7 Series FPGAs
PCB Design Guide UG483
TODO: verify!



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Title: Data Center RDIMM DDR4 Tester	
Size: A3 Date: 2024-02-12	
KiCad E.D.A. kicad-cli 7.0.10+1	
Rev: 1.2.3:3f1c9	
Id: 5/12	

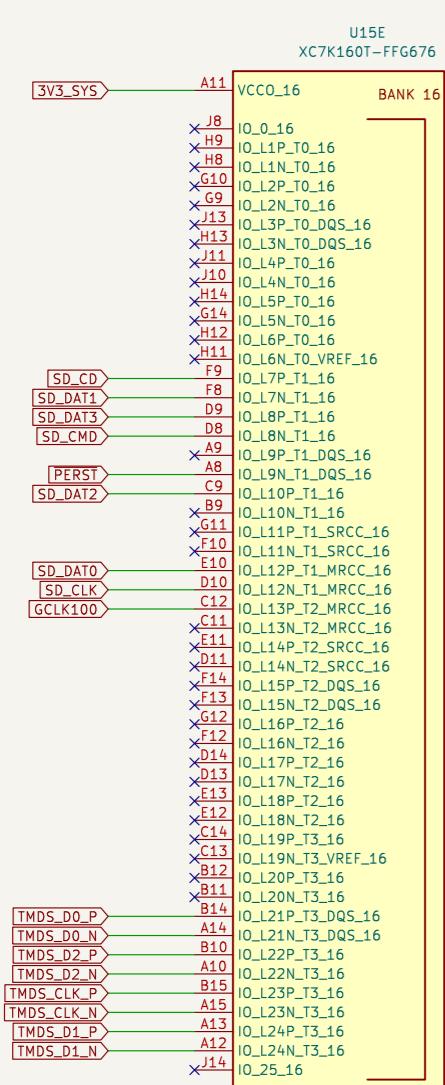
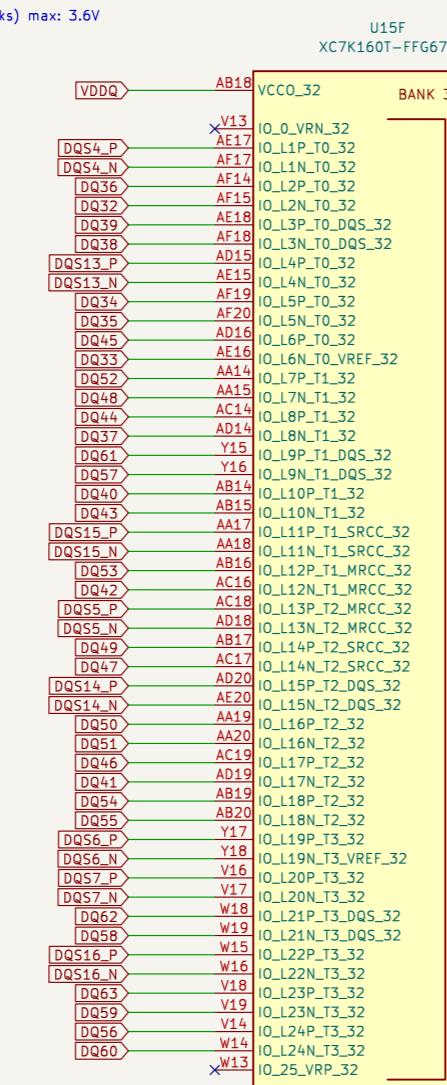
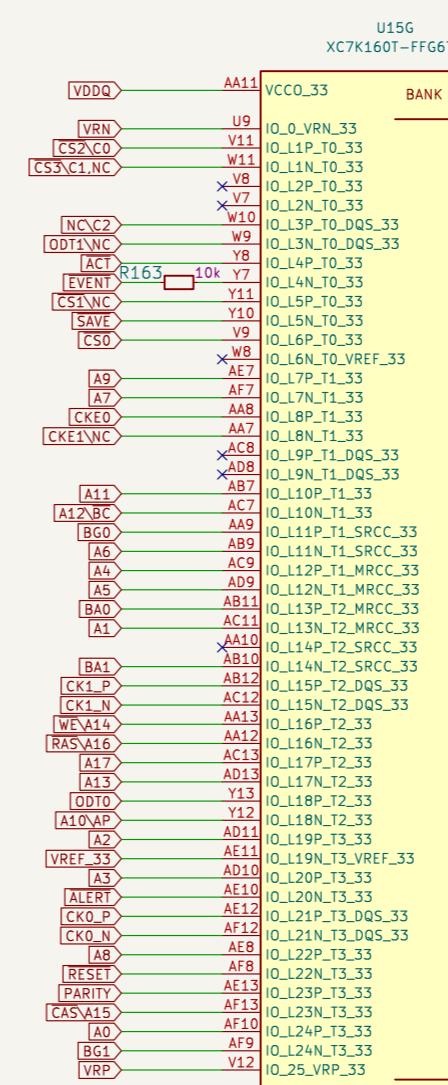
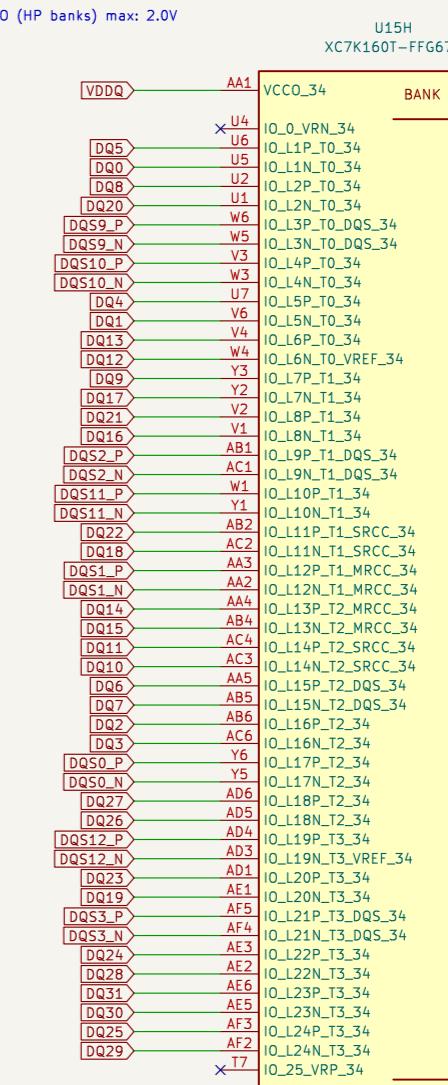




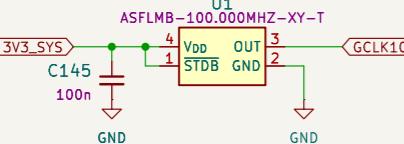
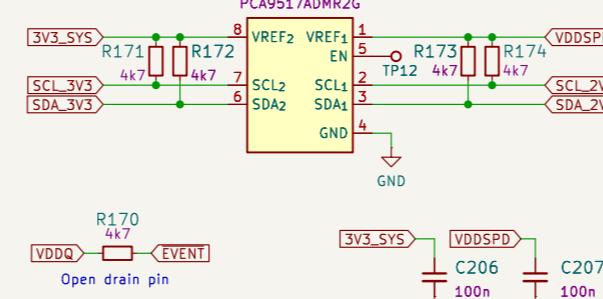
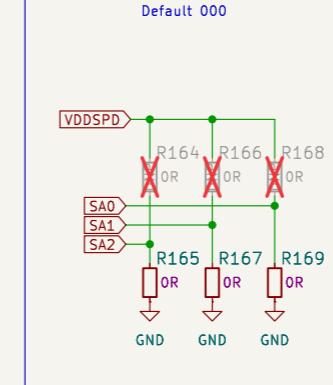
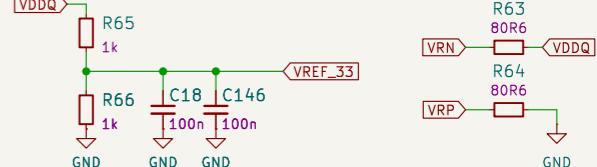


1 2 3 4 5 6 7 8

A

BANK 16**BANK 32****BANK 33****BANK 34**

HDMI

Clock source**I2C logic translator****Serial adress select****VREF**Antmicro Ltd
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Sheet: /FPGA banks 16-34/
File: fpga-banks-16-34.kicad_sch**Title: Data Center RDIMM DDR4 Tester**Size: A3 | Date: 2024-02-12
KiCad E.D.A. kicad-cl 7.0.10+1Rev: 1.2.3:3f1c9
Id: 9/12

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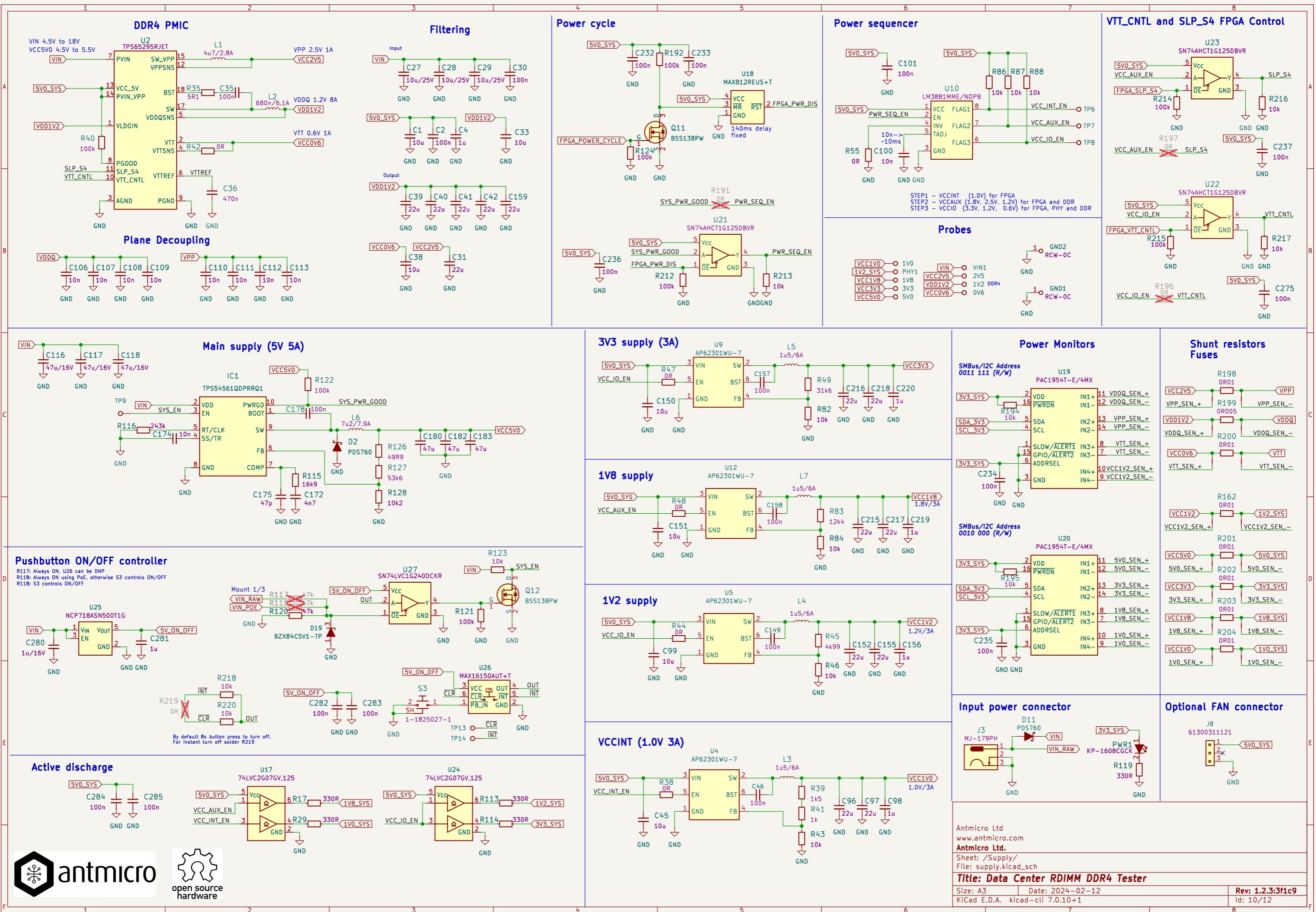
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A

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A

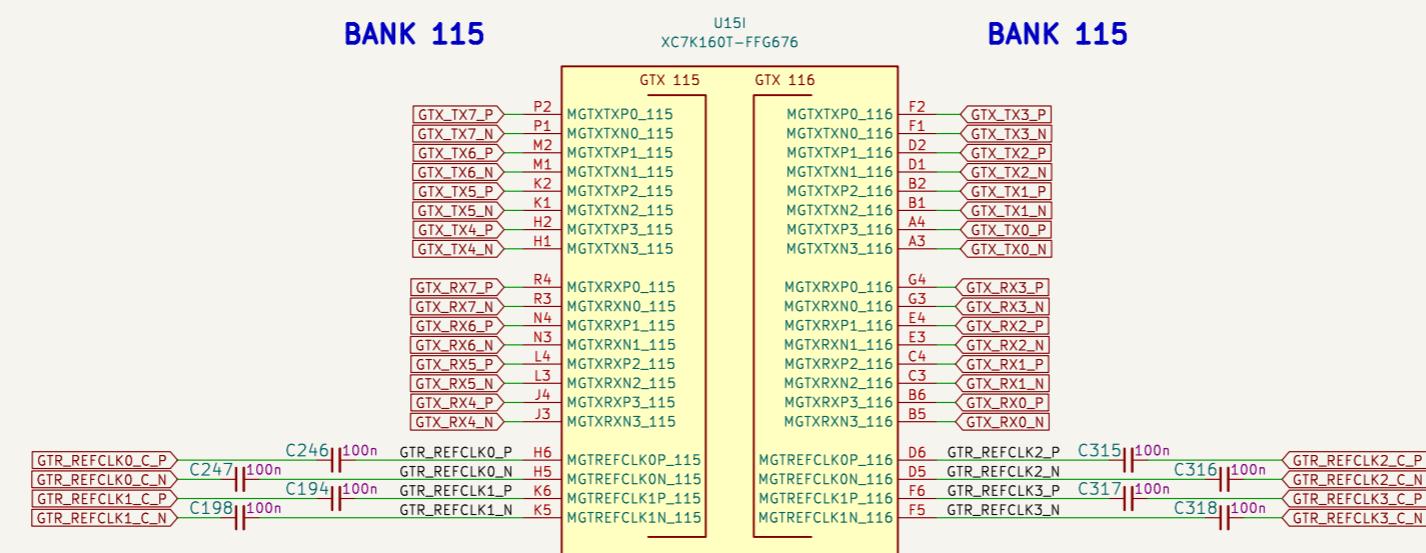
B

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Sheet: /FPGA banks 115-116/
File: pcie.kicad_sch

Title: Data Center RDIMM DDR4 Tester

Size: A3 | Date: 2024-02-12
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Id: 11/12

FMC HPC

