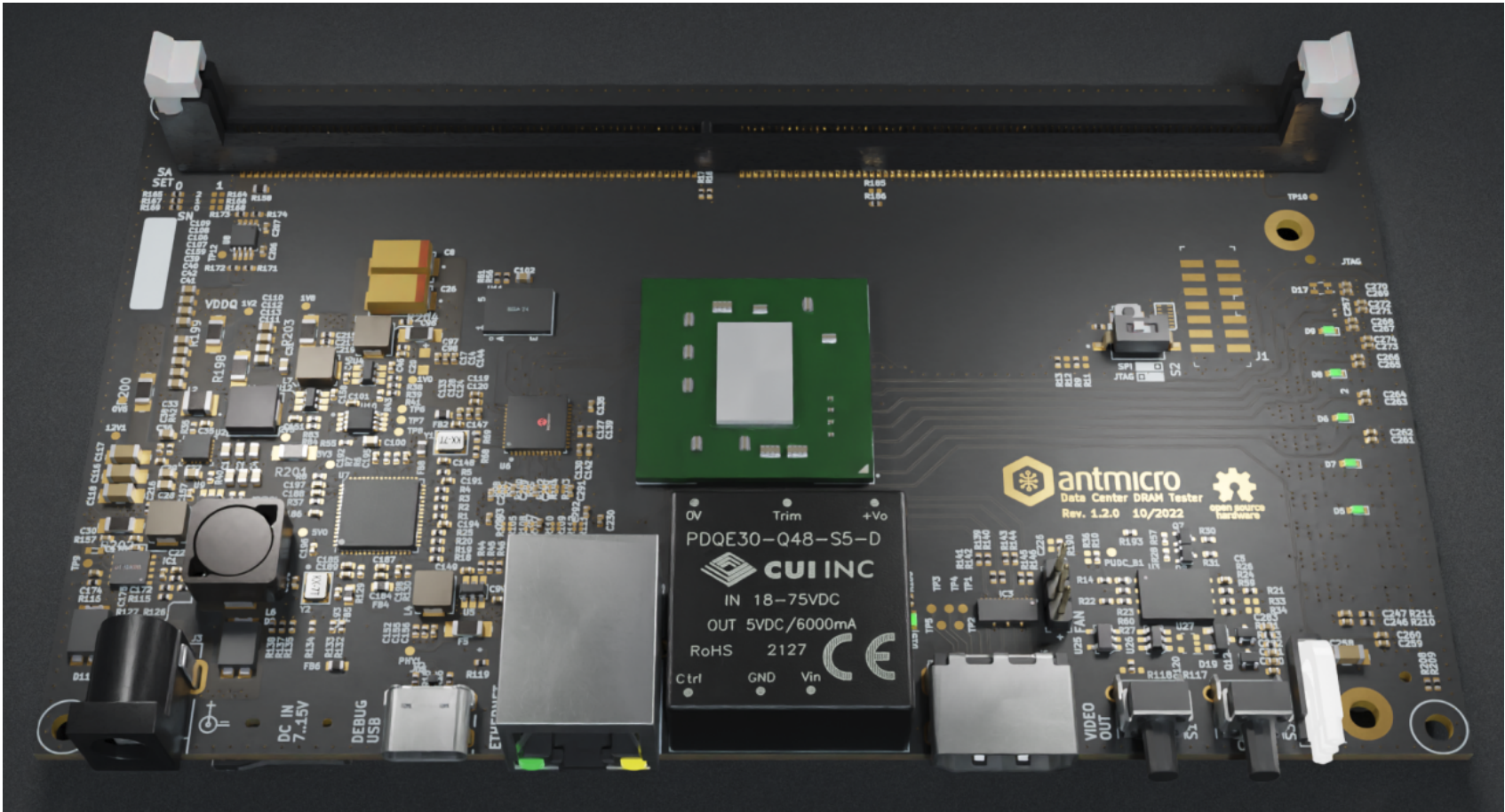


Data Center DRAM Tester



HyperRAM



File: hyperram.kicad_sch

DDR4



File: DDR4.kicad_sch

Interfaces



File: interfaces.kicad_sch

Ethernet



File: ethernet.kicad_sch

Supply



File: supply.kicad_sch

FMC HPC



File: fmc_hpc.kicad_sch

Config SPI flash



File: config-spi.kicad_sch

FPGA power



File: fpga-power.kicad_sch

FPGA banks 12–15



File: fpga-banks-12-15.kicad_sch

FPGA banks 16–34

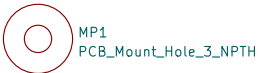


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FPGA banks 115–116



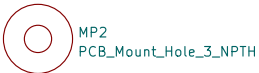
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MP1
PCB_Mount_Hole_3_NPTH



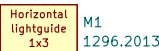
MP3
PCB_Mount_Hole_3_NPTH



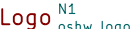
MP2
PCB_Mount_Hole_3_NPTH



MP4
PCB_Mount_Hole_3_NPTH



M1
1296.2013



N1
oshw_logo



N2
antmicro_logo

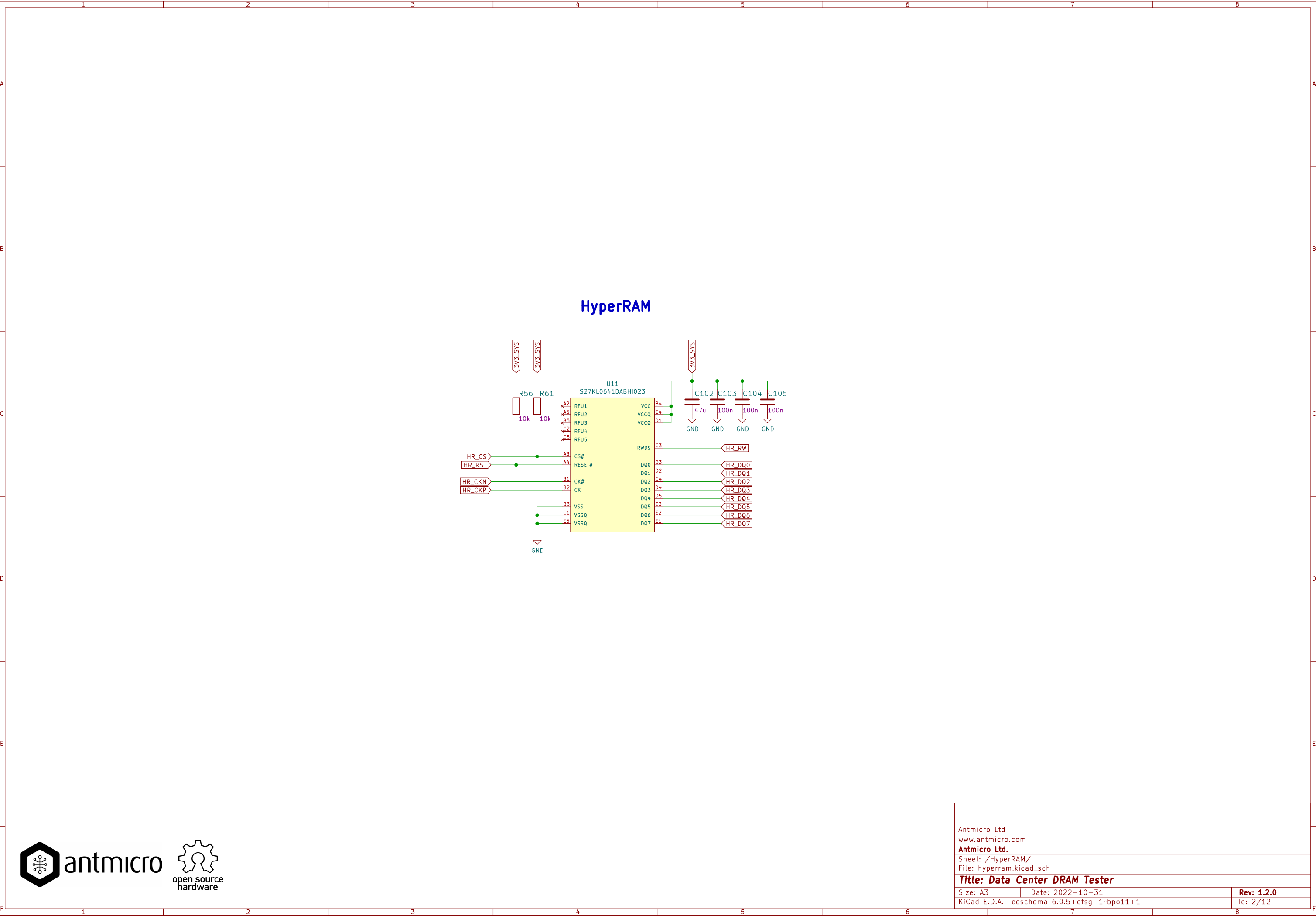
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Sheet: /
File: data-center-dram-tester.kicad_sch

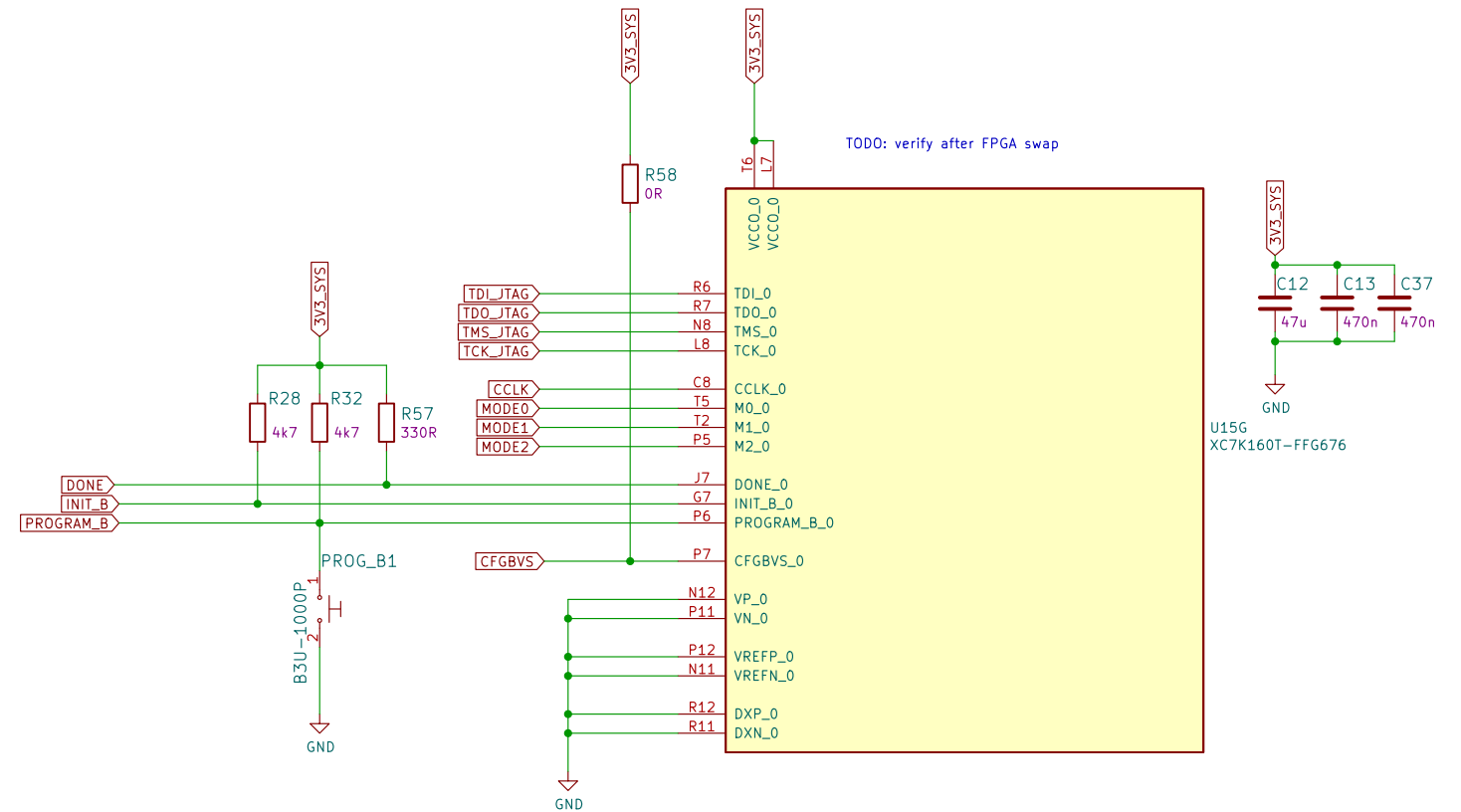
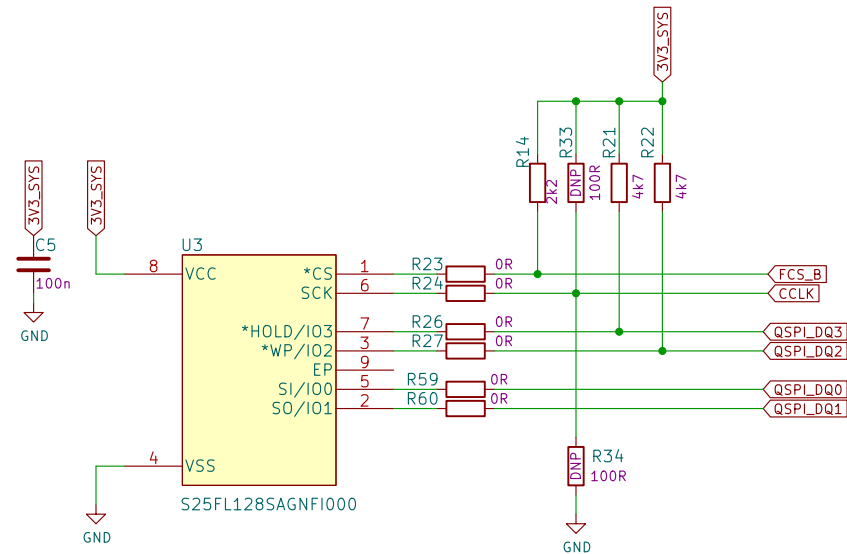
Title: Data Center DRAM Tester

Size: A3 Date: 2022-10-31
KiCad E.D.A. eeschema 6.0.5+dfsg-1-bpo11+1

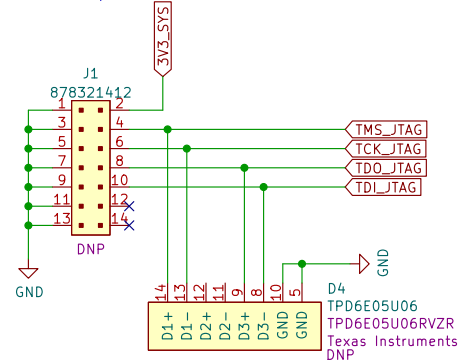
Rev: 1.2.0
Id: 1/12



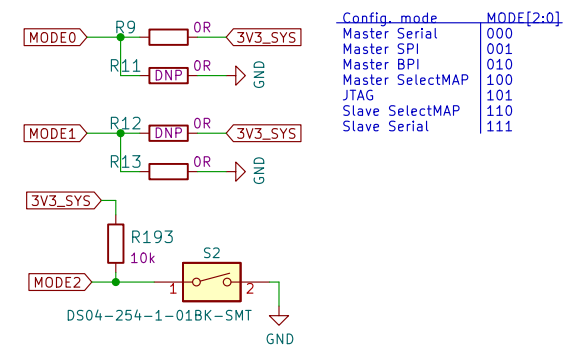
Follows Figure 2–14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)



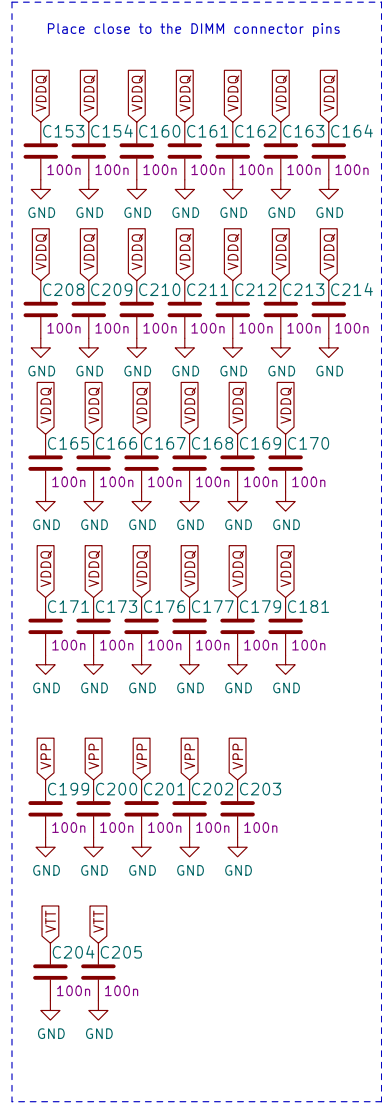
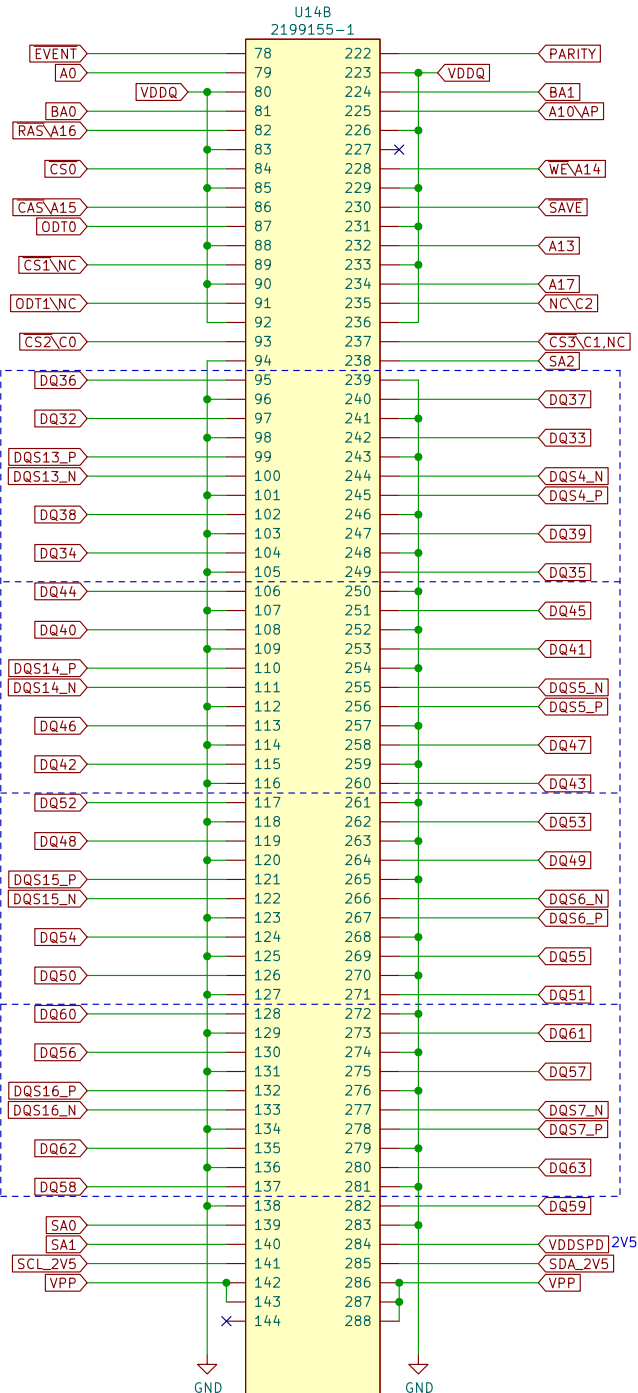
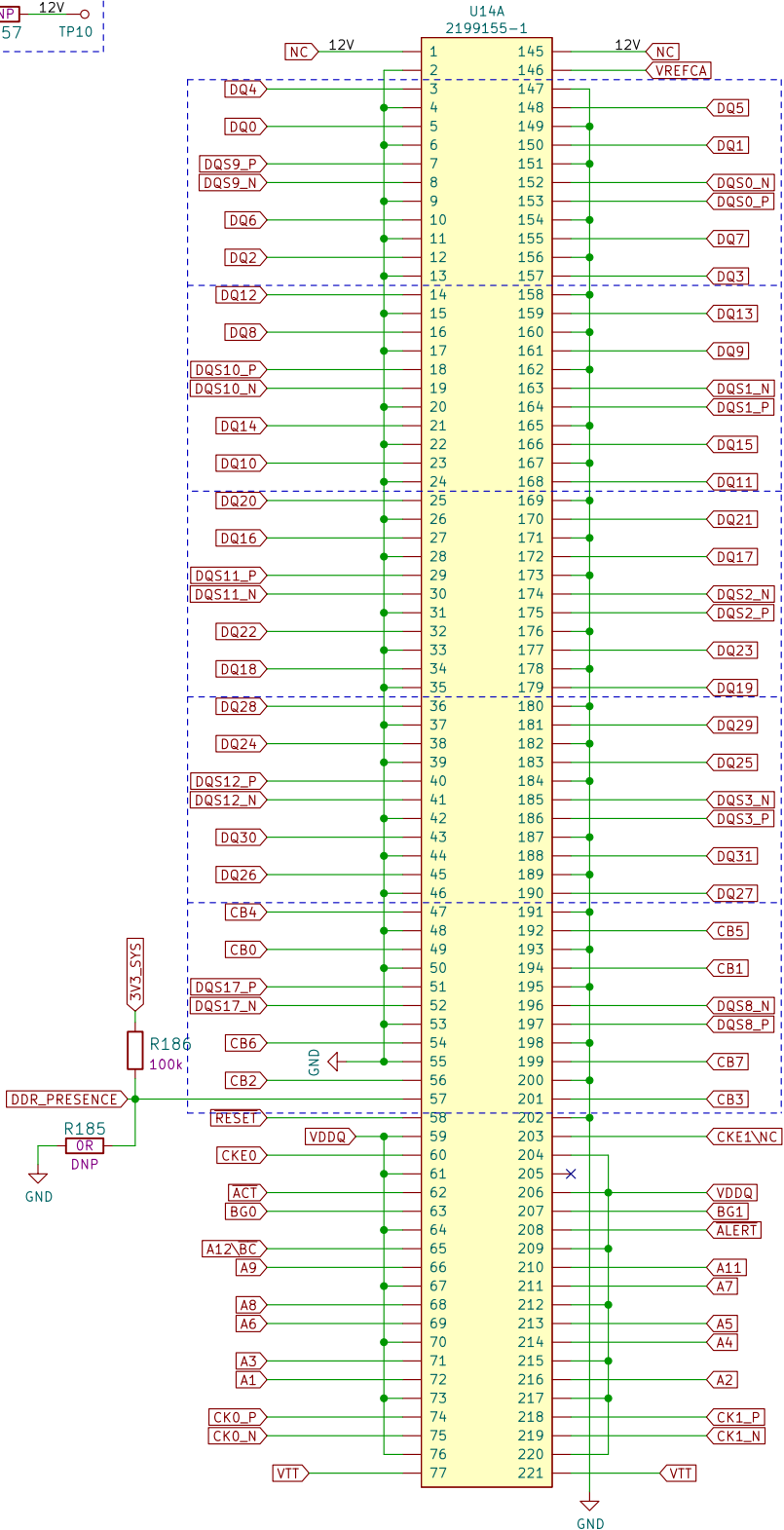
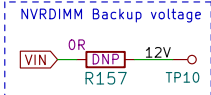
Compatible with Xilinx Platform Cable



For details, see UG470 p. 21

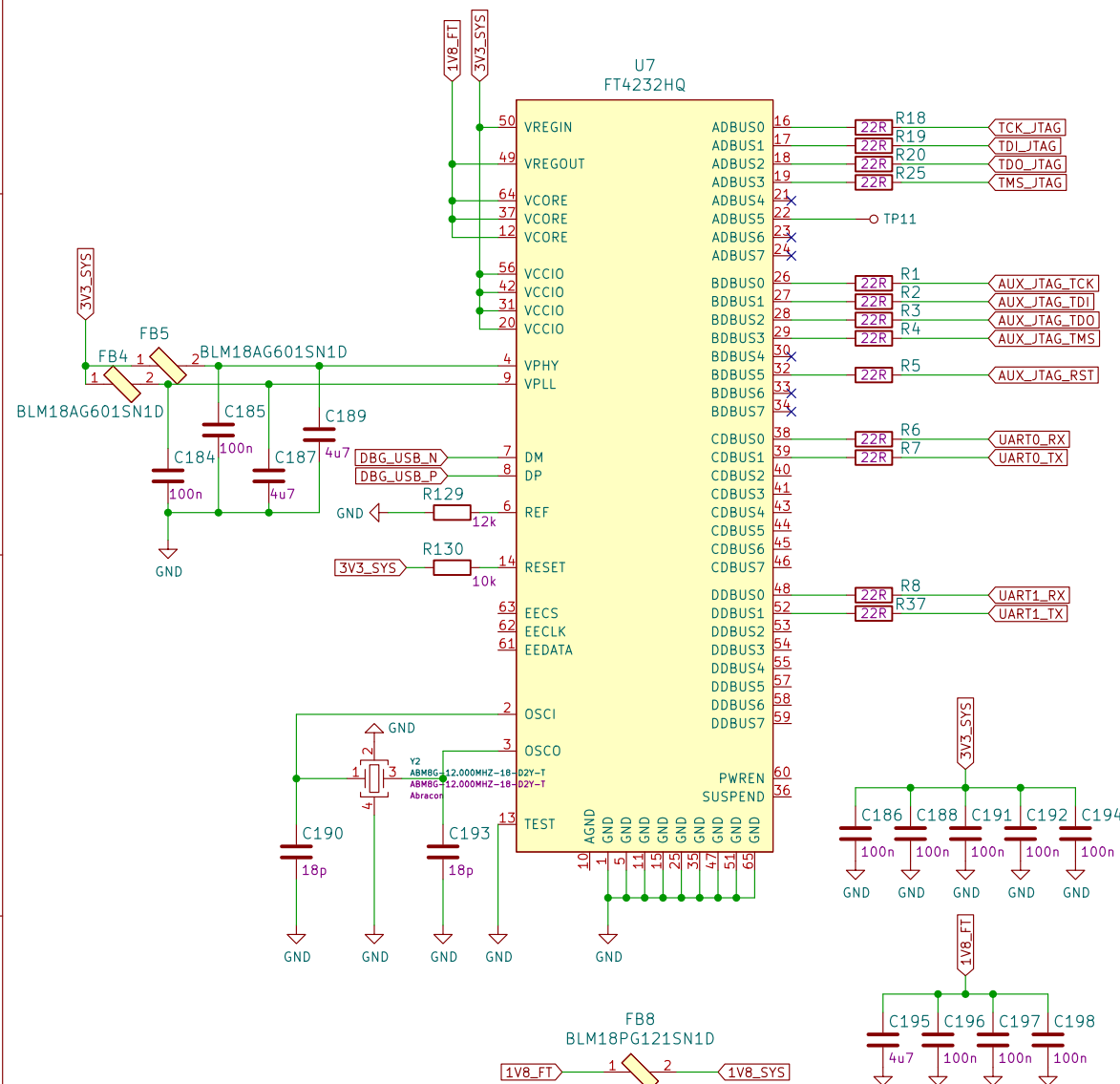


DDR4 RDIMM connector

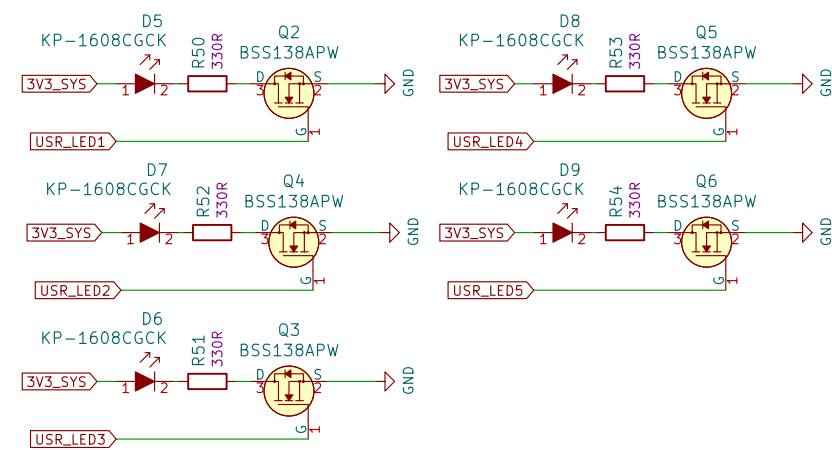




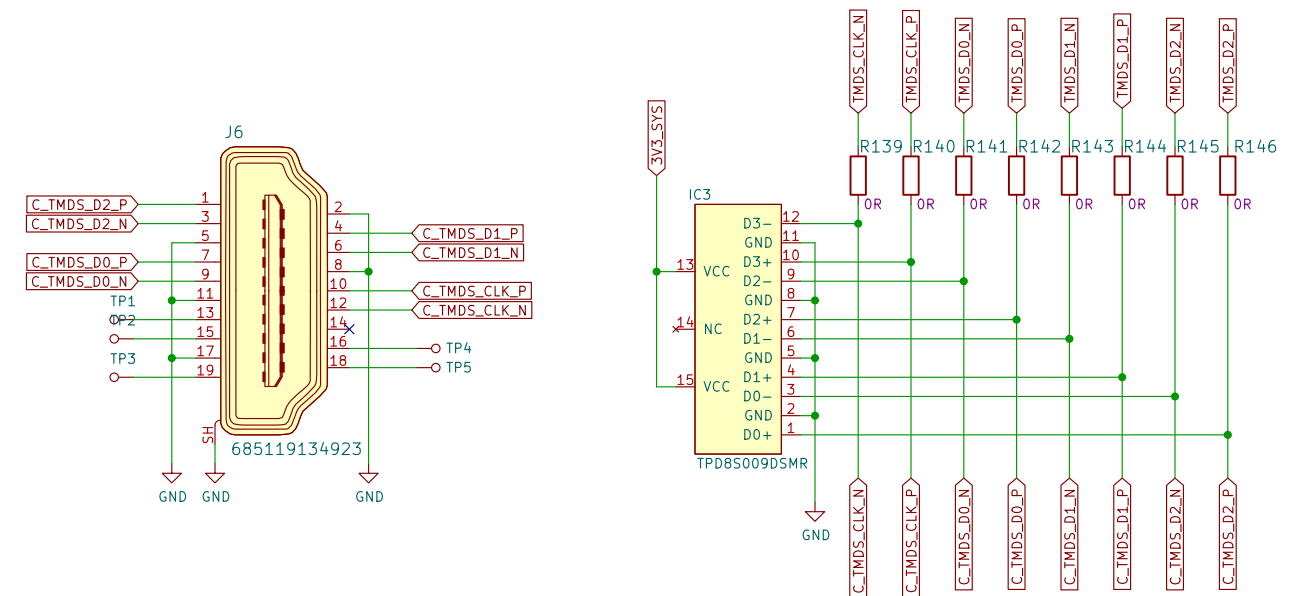
Debug UART



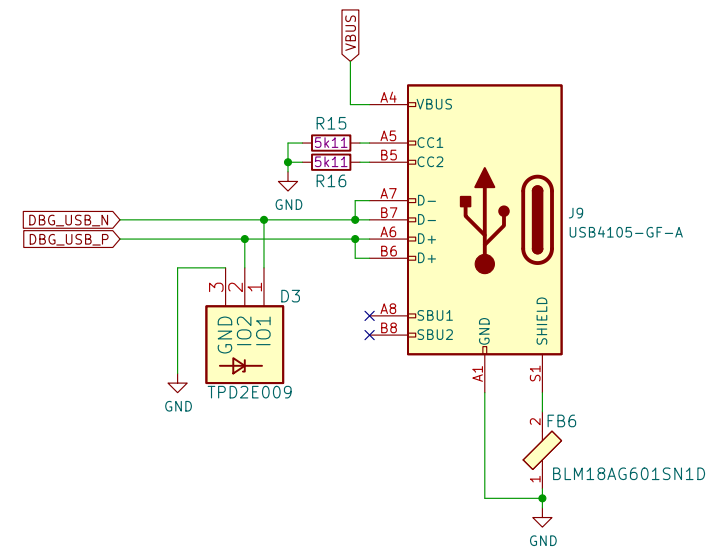
User LEDs



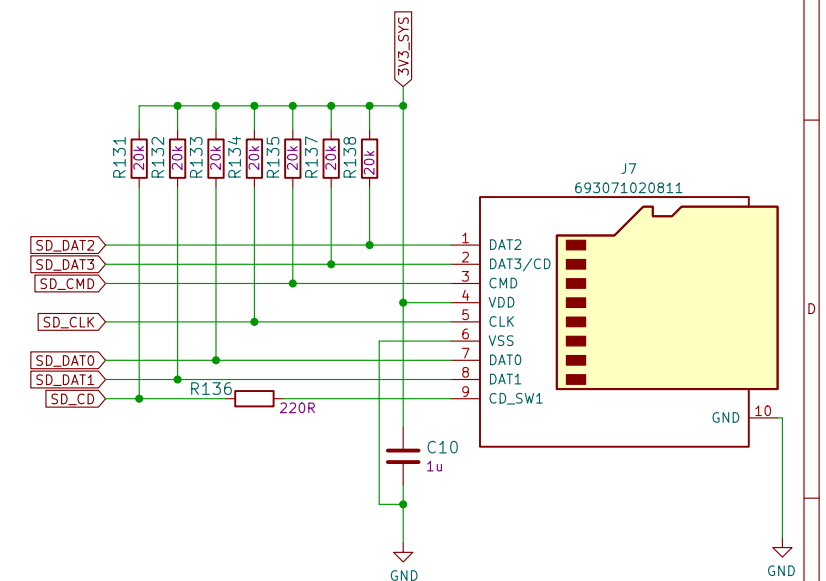
HDMI



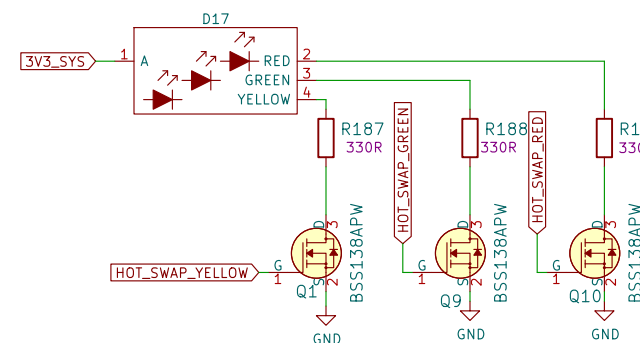
Debug USB



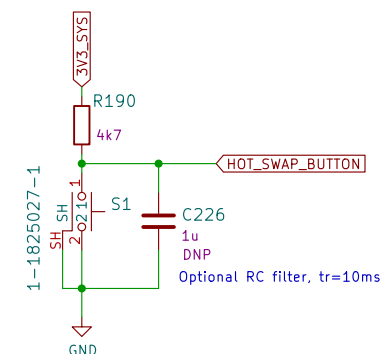
SD card



HOT SWAP status LED



HOT SWAP eject button



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Sheet: /Interfaces/
File: interfaces.kicad_sch

Title: Data Center DRAM Tester

Size: A3	Date: 2022-10-31
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Size: A3	Date: 2022-10-31
KiCad E.D.A. eeschema 6.0.5+dfsg-1~bpo11+1	

Rev: 1.2.0

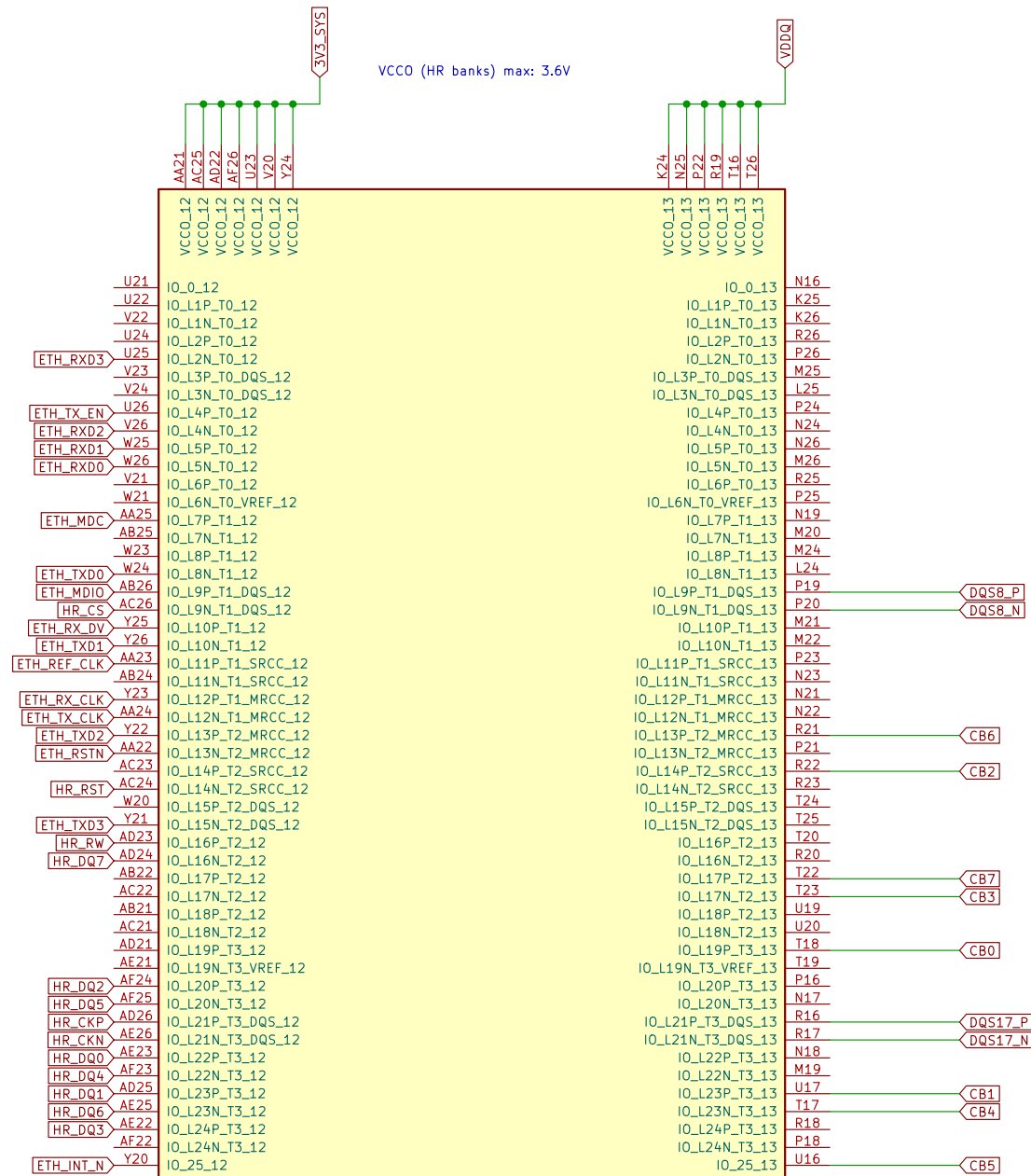
Id: 6/12

BANK 12

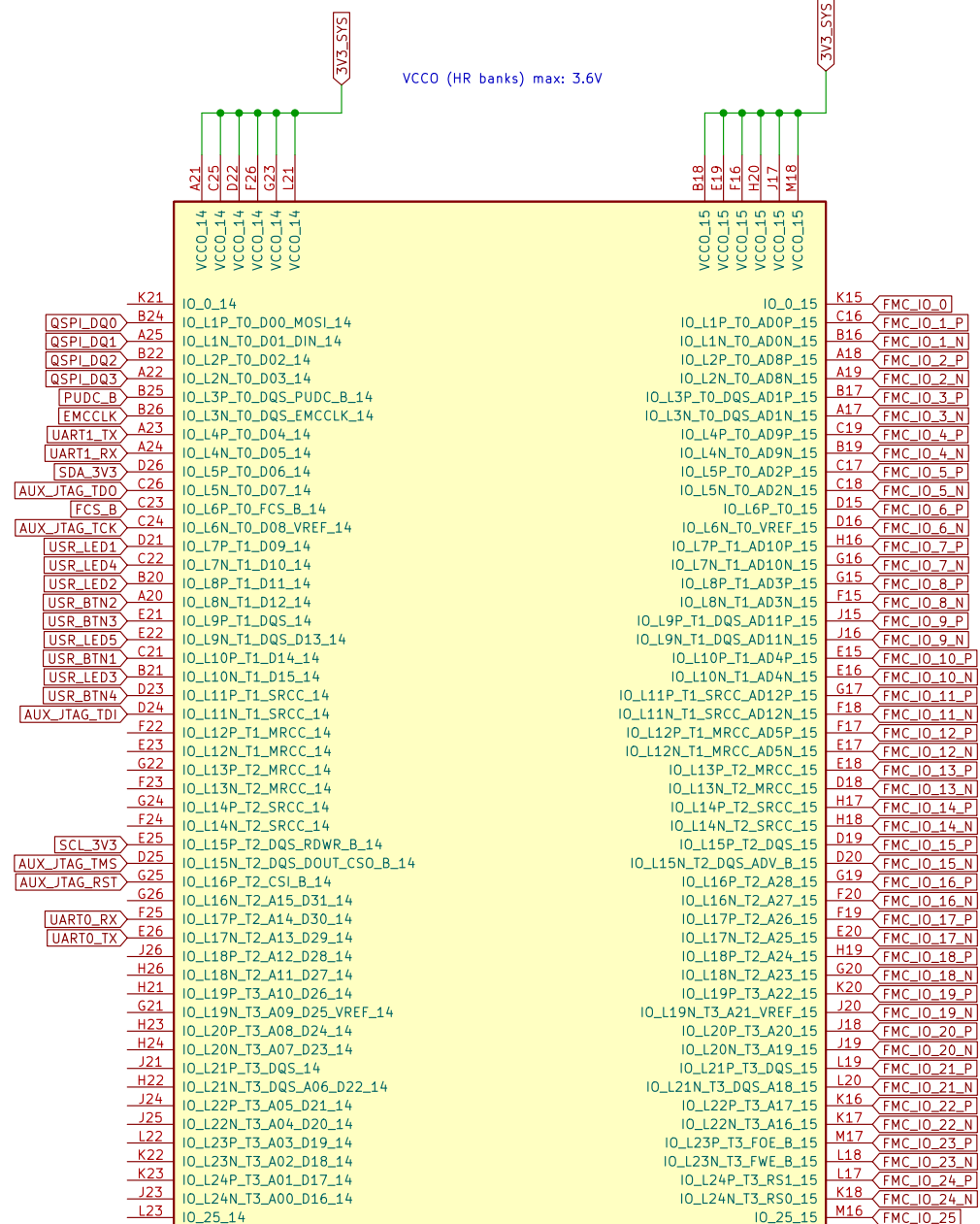
BANK 13

BANK 14

BANK 15



U15A
XC7K160T-FFG676
antmicro-footprints:xc7k160tfg676



U15B
XC7K160T-FFG676
antmicro-footprints:xc7k160tfg676



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Sheet: /FPGA banks 12-15/

File: fpga-banks-12-15.kicad_sch

Title: Data Center DRAM Tester

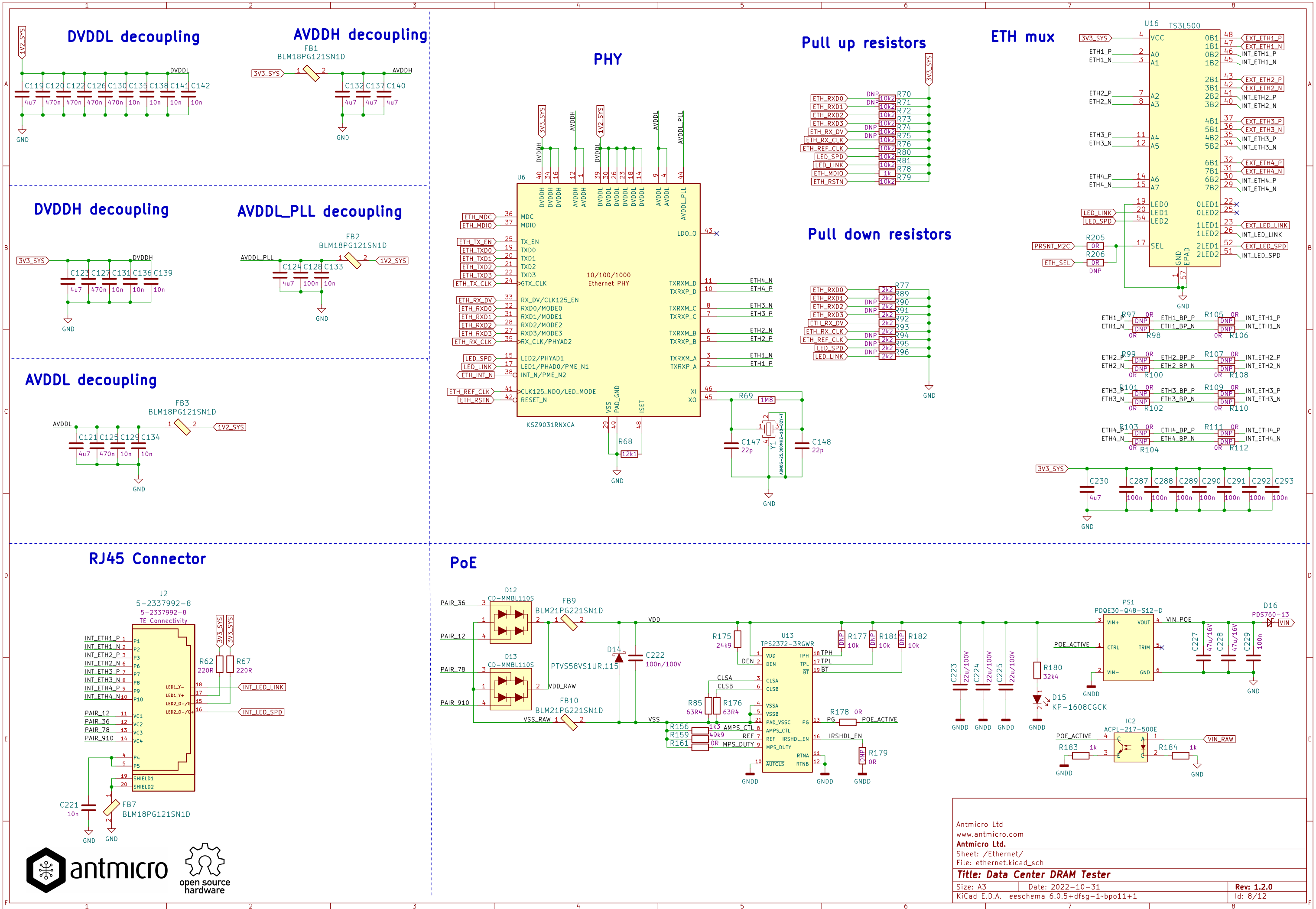
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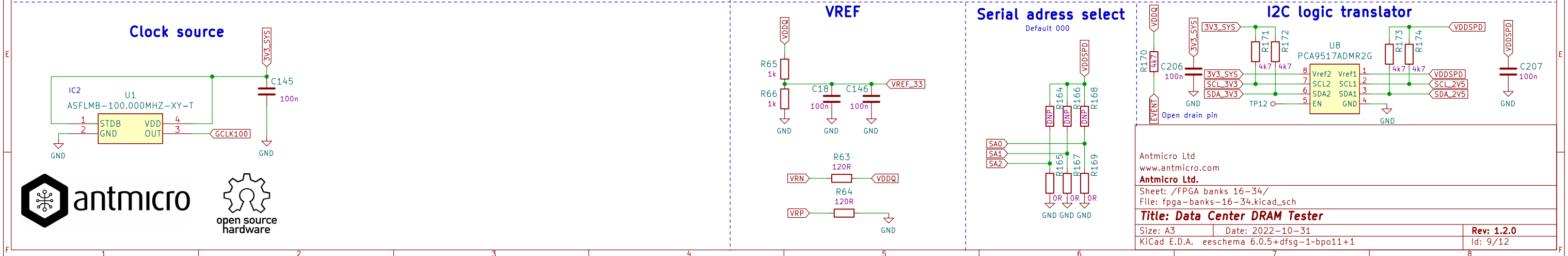
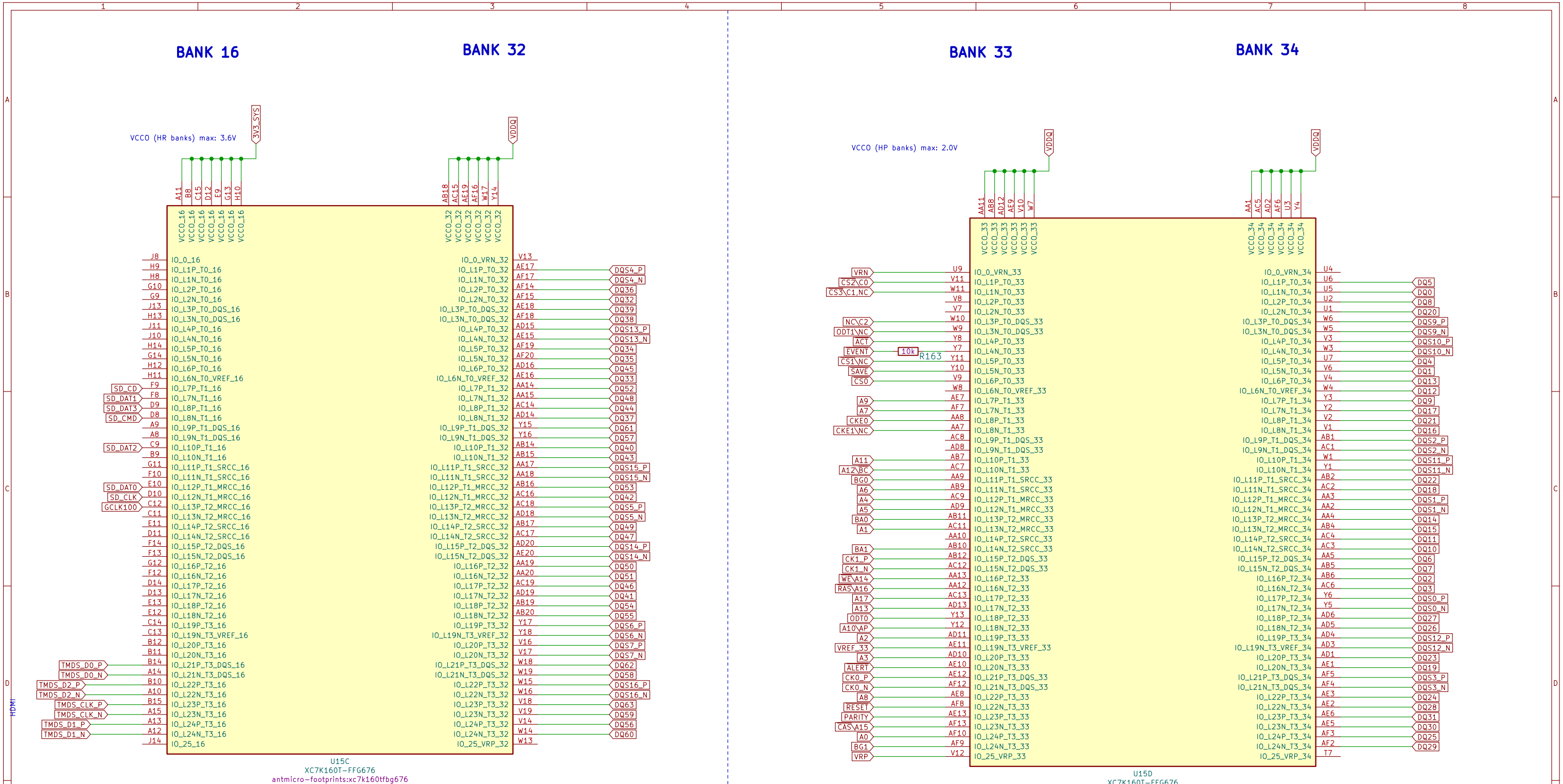
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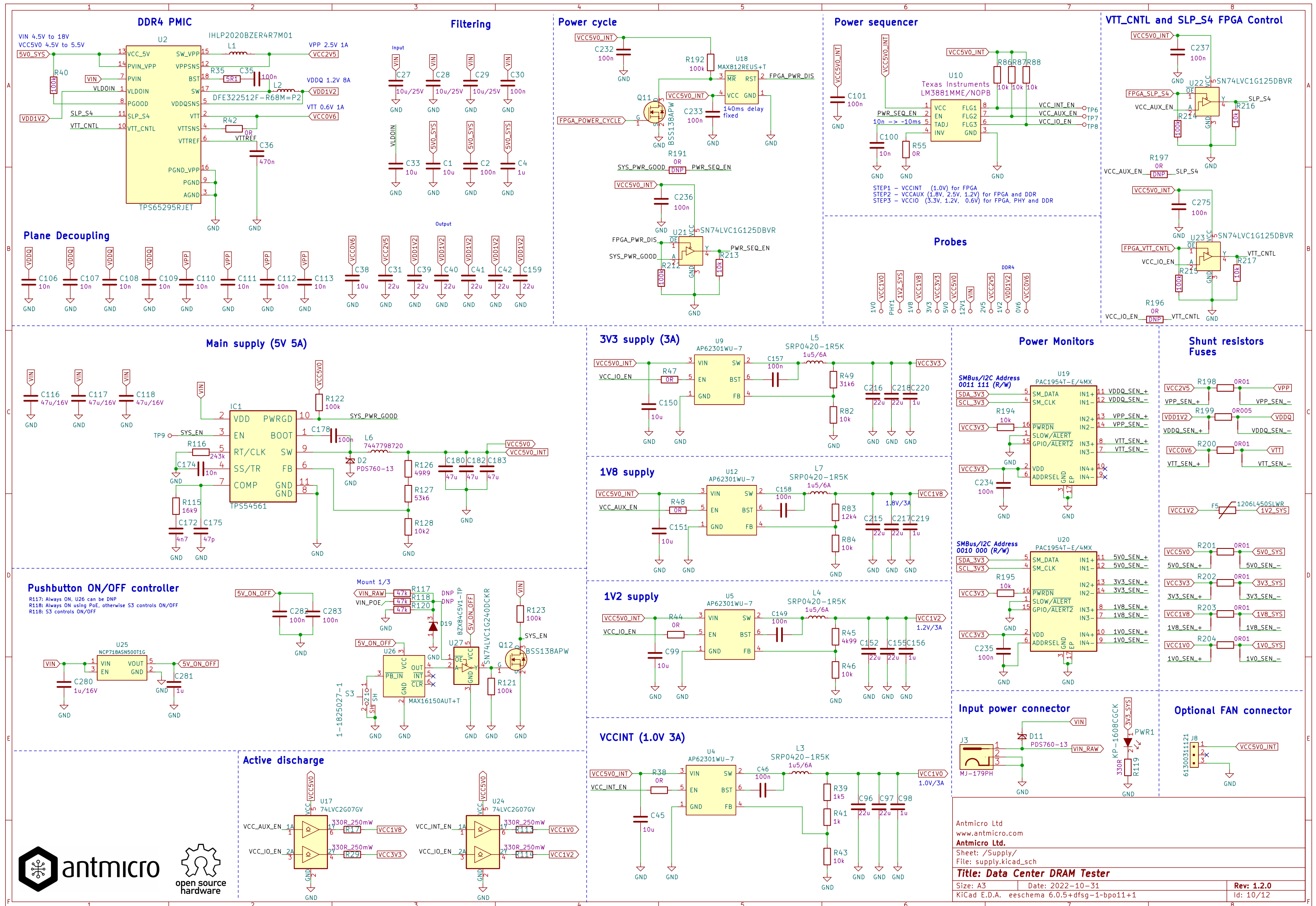
Rev: 1.2.0

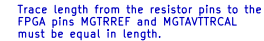
KiCad E.D.A. eeschema 6.0.5+dfsg-1-bpo11+1

Id: 7/12

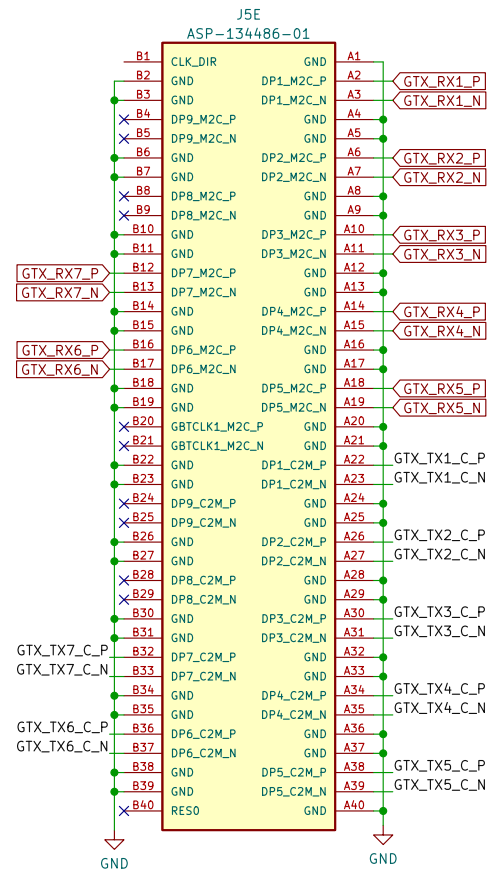
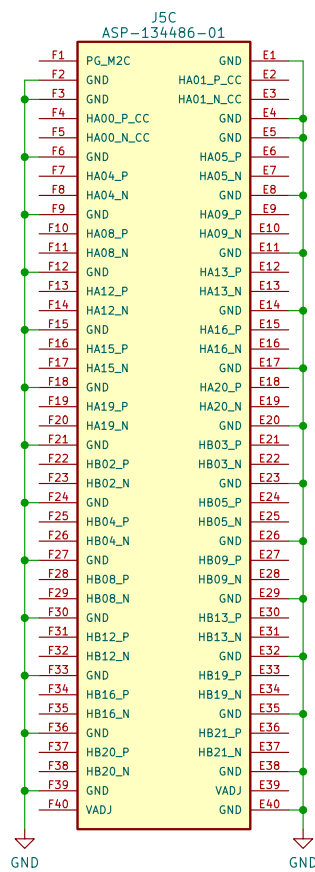
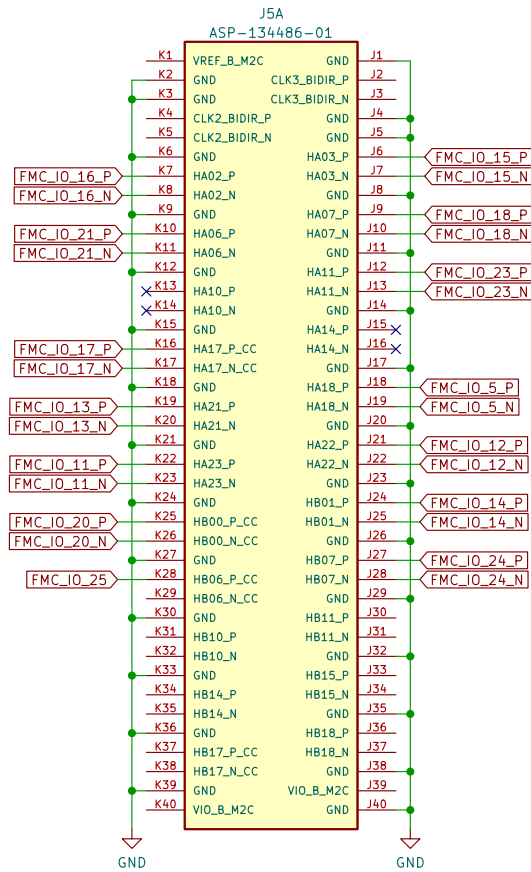






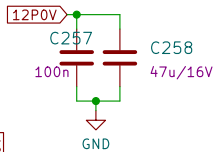
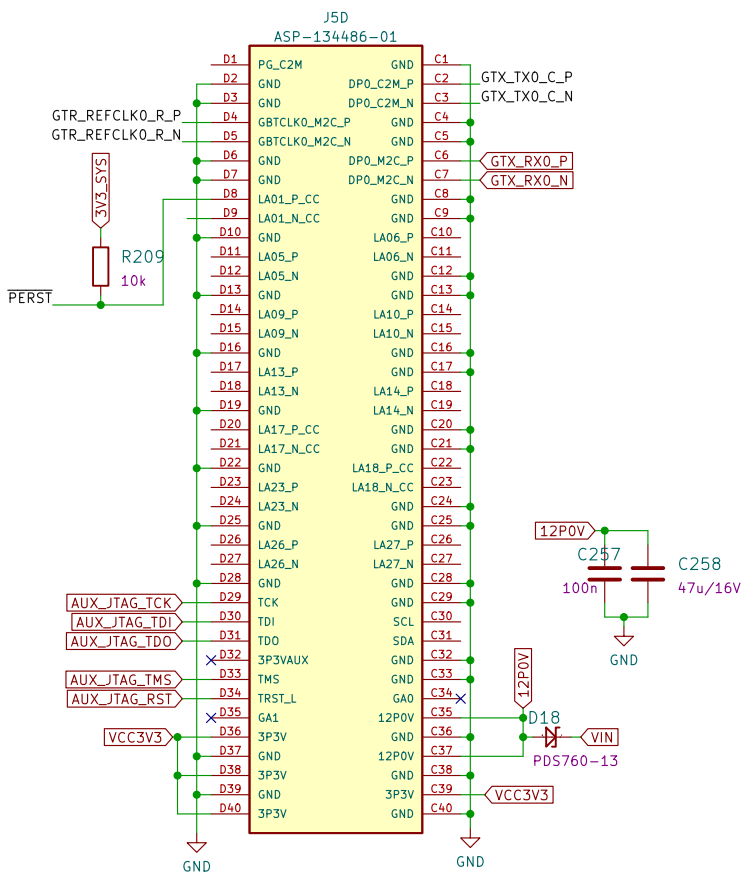
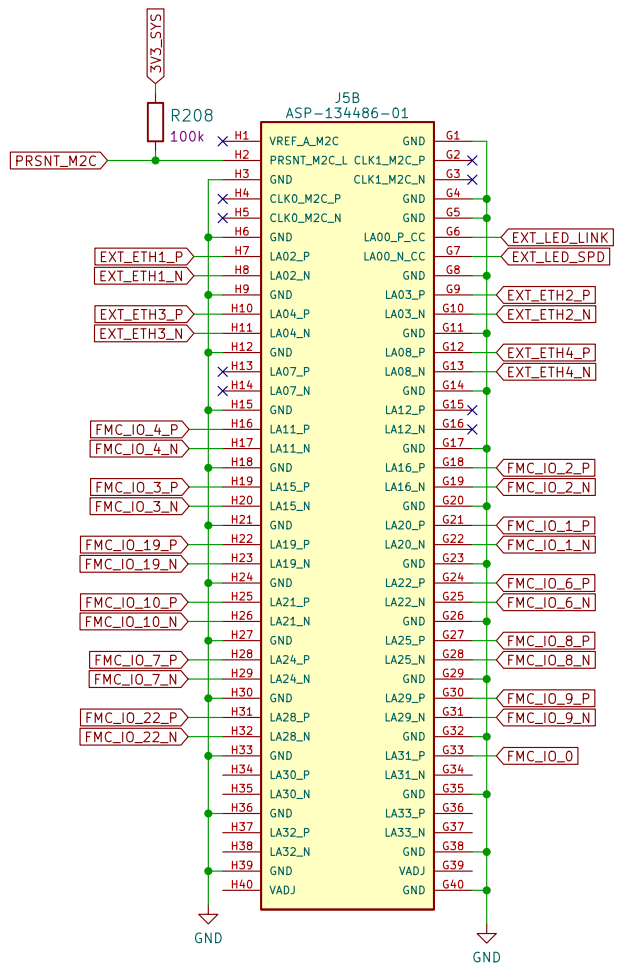
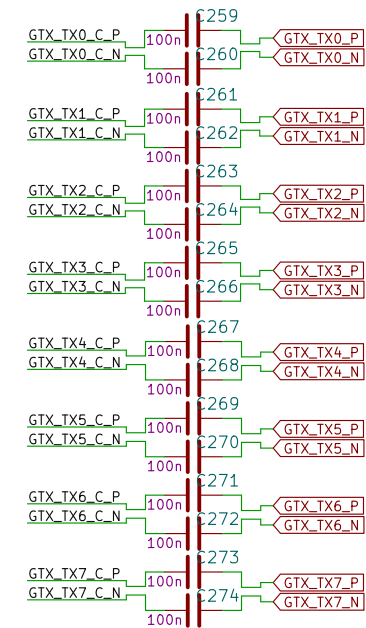


FMC HPC



R210
GTR_REFCLK0_R_P
R211
GTR_REFCLK0_R_N
GTR_REFCLK0_C_P
GTR_REFCLK0_C_N
Resistors needed to comply with standard HCSL PCIe clock.
Route REFCLK as 50 Ohm SE (or 100 Ohm diff)

Place close to connector



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Sheet: /FMC HPC/
File: fmc_hpc.kicad_sch

Title: Data Center DRAM Tester

Size: A3
KiCad E.D.A. eeschema 6.0.5+dfsg-1-bpo11+1

Date: 2022-10-31

Rev: 1.2.0

Id: 12/12