Data Center DRAM Tester

Sheet: HyperRAM
File: hyperram.sch

Sheet: DDR4
File: DDR4.sch

Sheet: Interfaces
File: interfaces.sch

Sheet: Ethernet
File: ethernet.sch

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File: supply.sch

Sheet: Config SPI flash
File: config-spi.sch

Sheet: FPGA power
File: fpga-power.sch

Sheet: FPGA banks 12-15
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Sheet: FPGA banks 16-34
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Logo N1
oshw_logo

Logo N2
antmicro_logo

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Sheet: /
File: data-center-dram-tester.sch

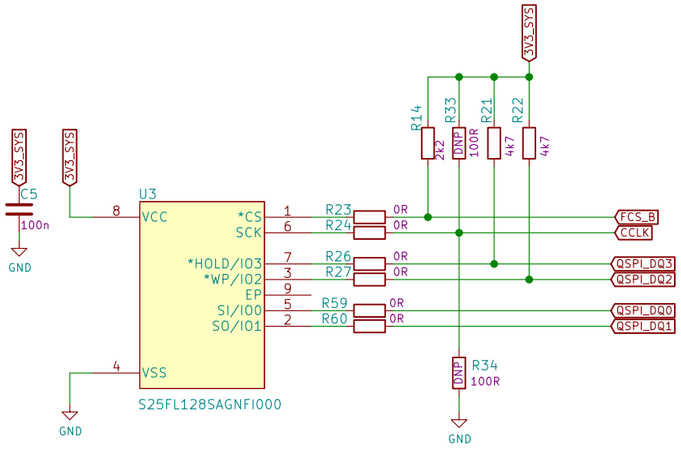
Title: Data Center DRAM Tester

Size: A3	Date: 2021-08	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 1/10

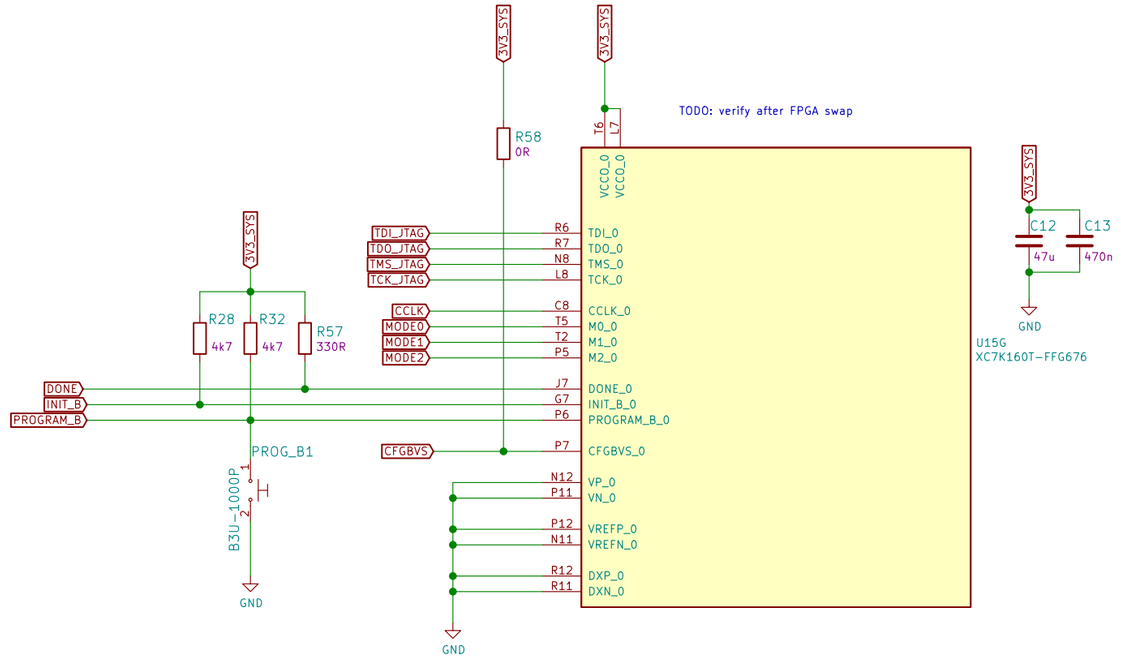
Master SPI Quad (x4) configuration scheme

Follows Figure 2–14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

(Q)SPI flash

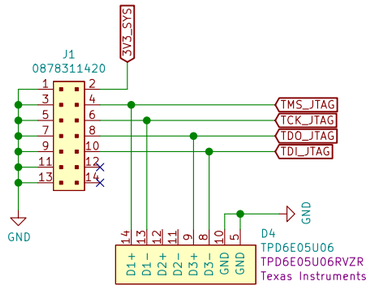


FPGA BANK 0

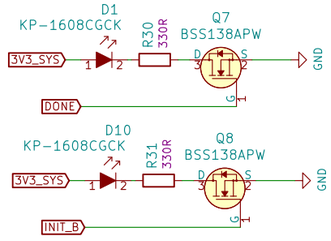


JTAG Connector

Compatible with Xilinx Platform Cable

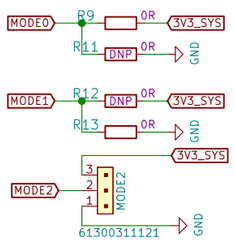


STATUS LEDs



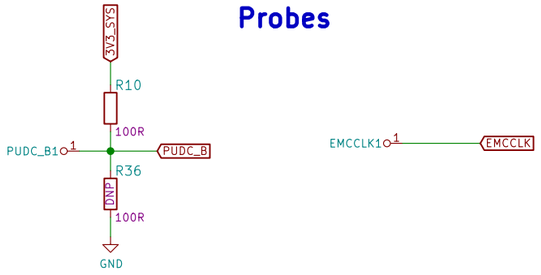
Configuration Modes

For details, see UG470 p. 21



Config. mode	MODE[2:0]
Master Serial	000
Master SPI	001
Master BPI	010
Master SelectMAP	100
JTAG	101
Slave SelectMAP	110
Slave Serial	111

Probes



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Sheet: /Config SPI flash/
File: config-spi.sch

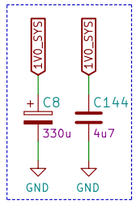
Title: Data Center DRAM Tester

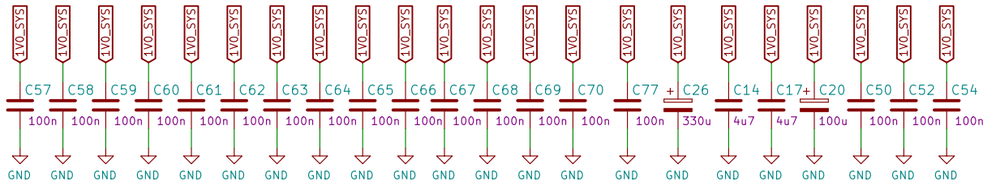
Size: A3	Date: 2021-08	**Rev: 1.0.0**
KiCad E.D.A.	kicad 5.1.5+dfsg1-2bpo10+1	Id: 2/10

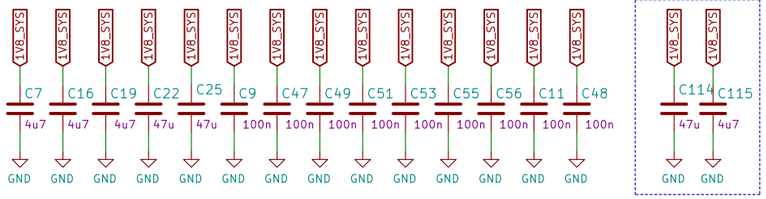
POWER RAILS

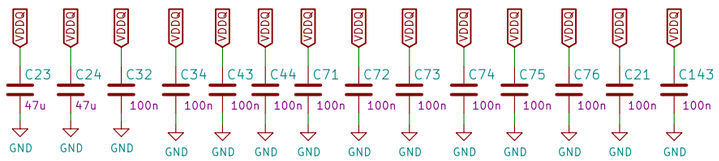
Decoupling referenced from 7 Series FPGAs
PCB Design Guide UG483
TODO: verify!

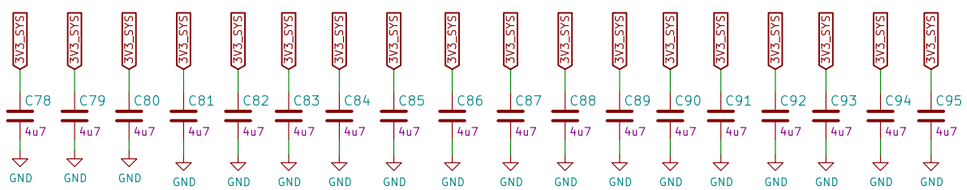
Added capacitors coresponding to PCB Design Guide UG483

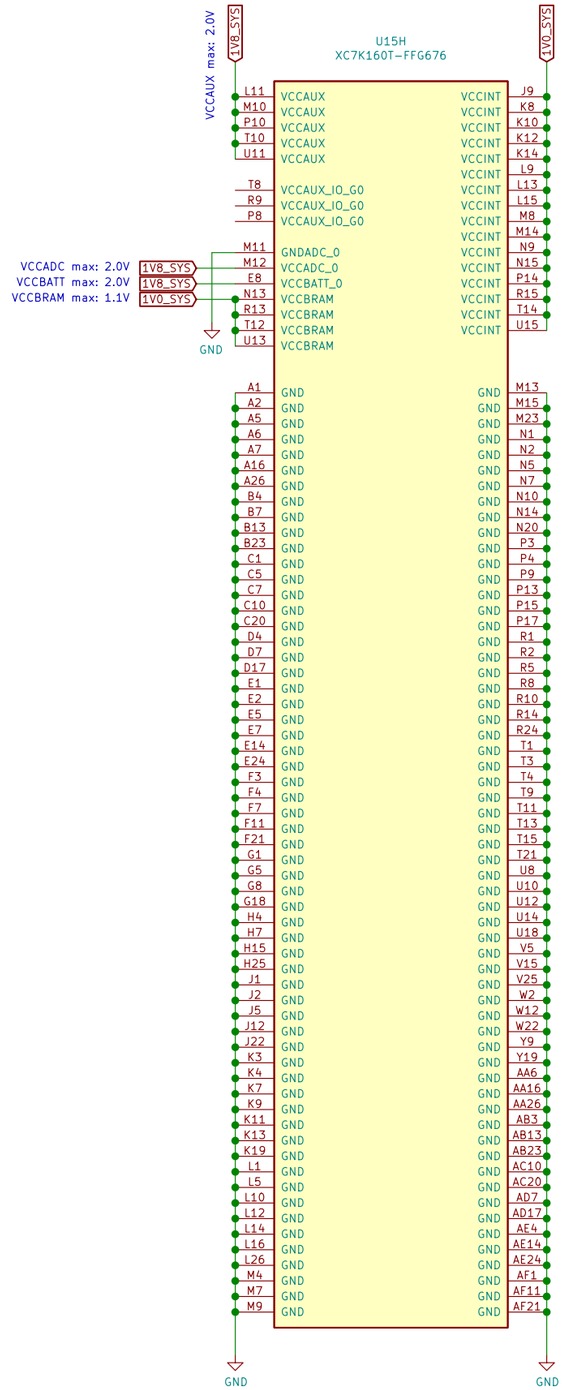


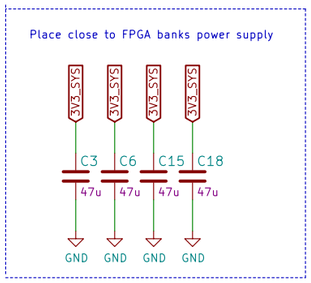




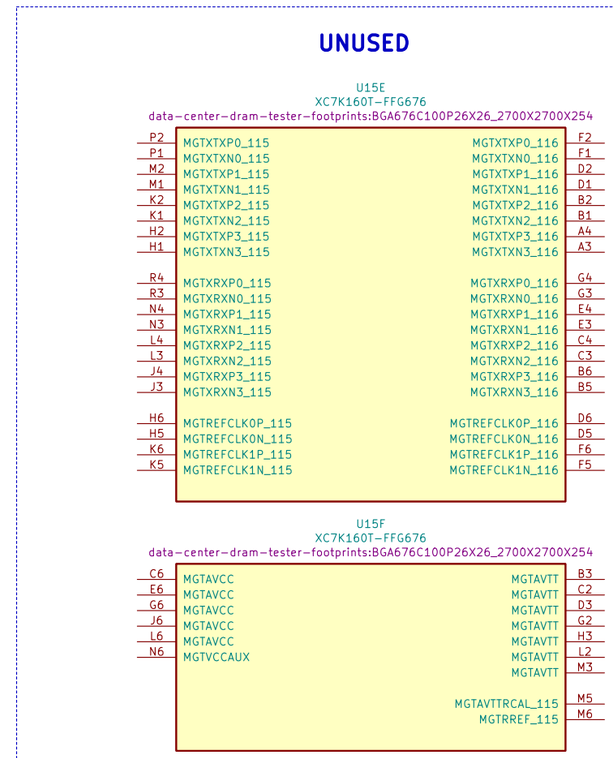








UNUSED



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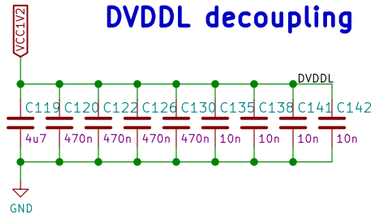
Sheet: /FPGA power/
File: fpga-power.sch

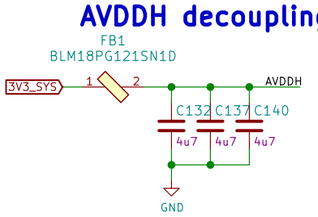
Title: Data Center DRAM Tester

Size: A3	Date: 2021-08	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 3/10

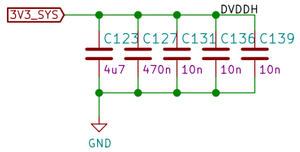
DVDDL decoupling



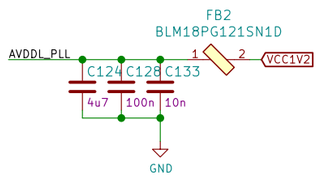
AVDDH decoupling



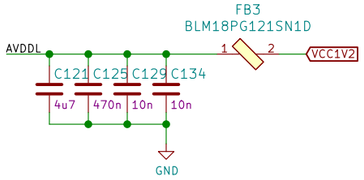
DVDDH decoupling



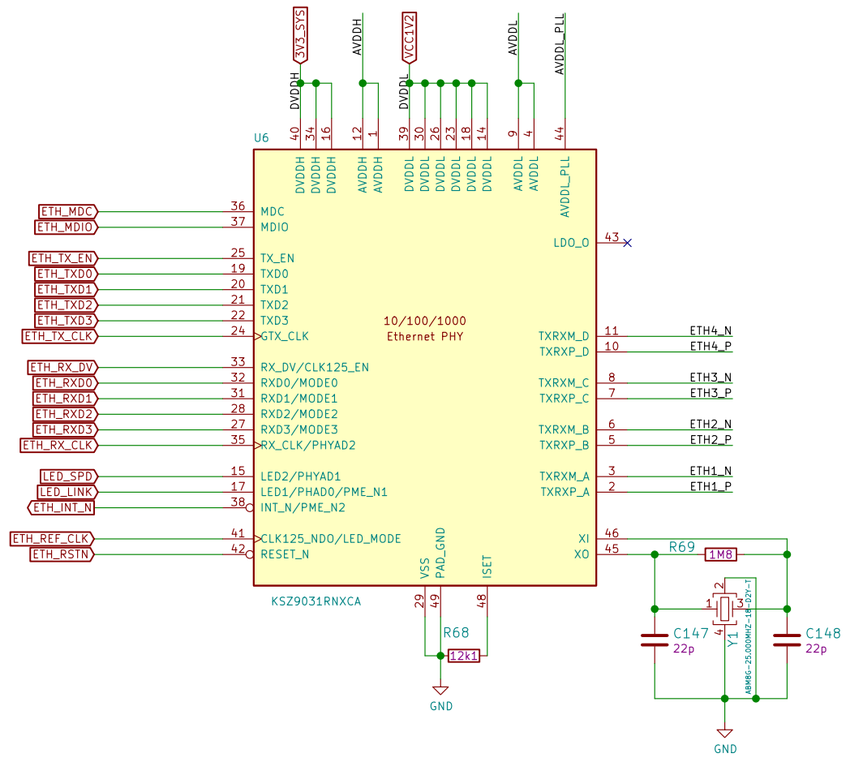
AVDDL_PLL decoupling



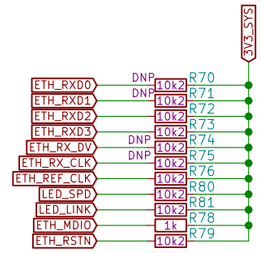
AVDDL decoupling



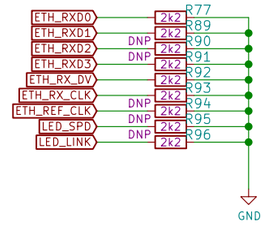
PHY



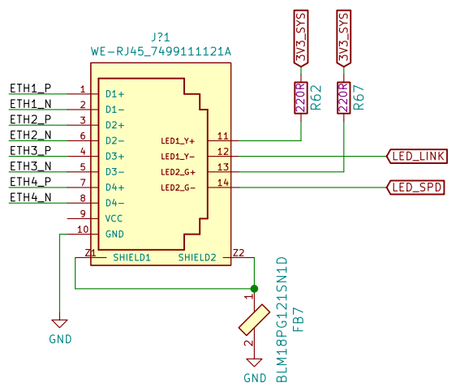
Pull up resistors



Pull down resistors



RJ45 Connector



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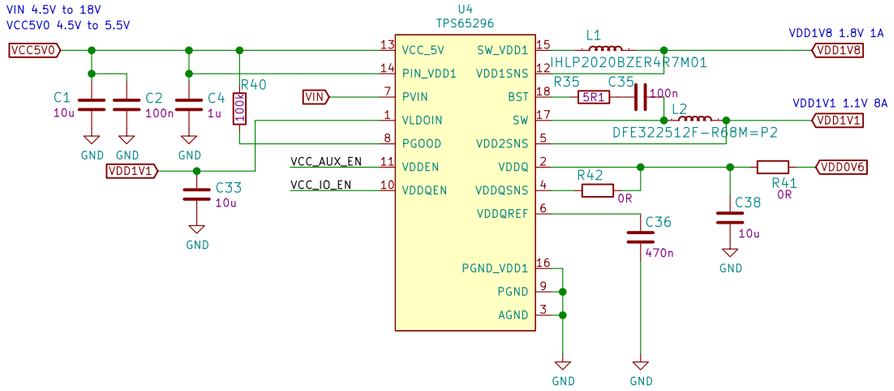
Sheet: /Ethernet/
File: ethernet.sch

Title: Data Center DRAM Tester

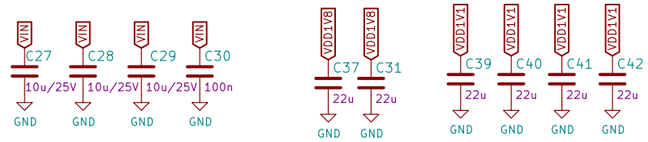
Size: A3	Date: 2021-08	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 4/10

DDR4 PMIC

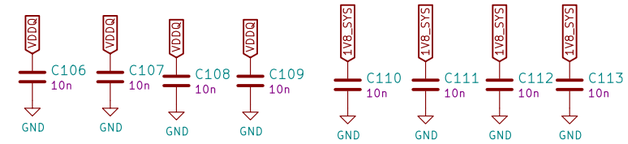
TODO: Replace with TPS65295



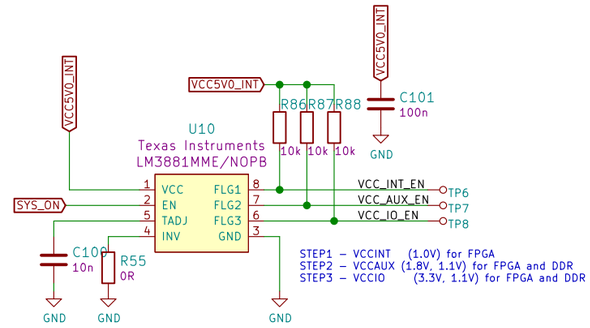
Filtering



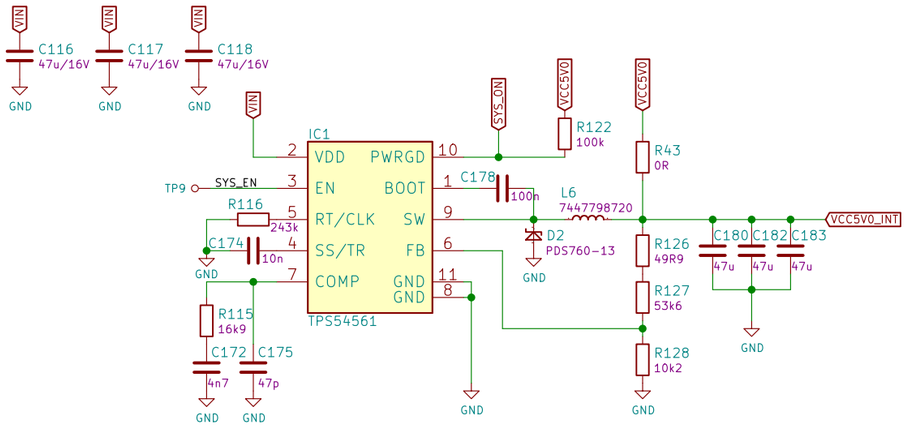
Plane Decoupling



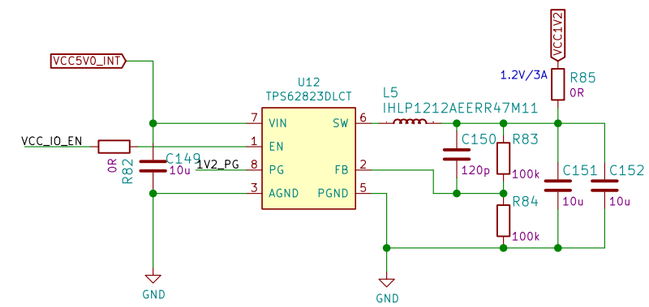
Power sequencer



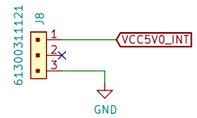
Main supply (5V 5A)



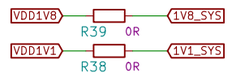
1V2 supply



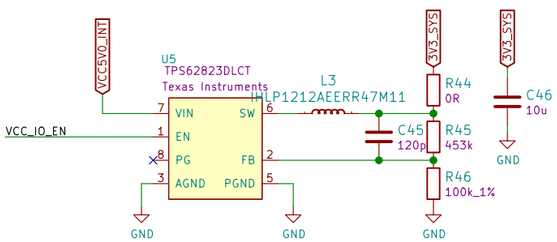
Optional FAN connector



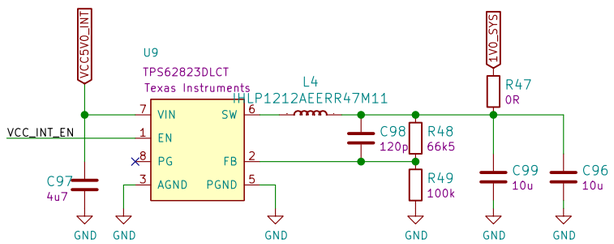
Shunt resistors



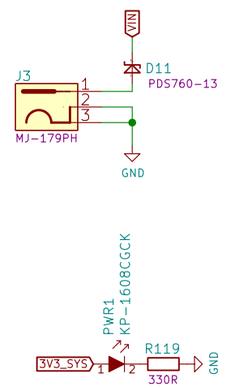
3V3 supply (2A)



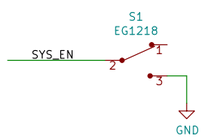
VCCINT (1.0V 2A)



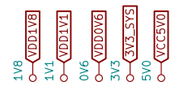
Input power connector



Power switch



Probes



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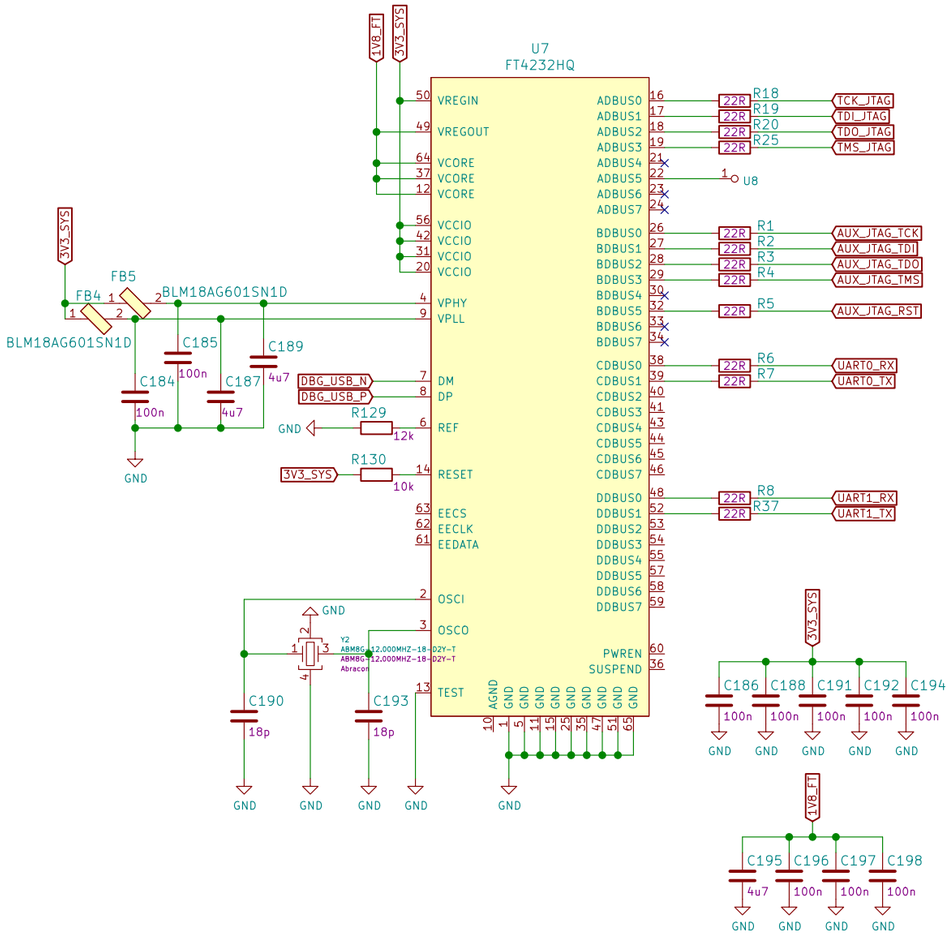
Sheet: /Supply/
File: supply.sch

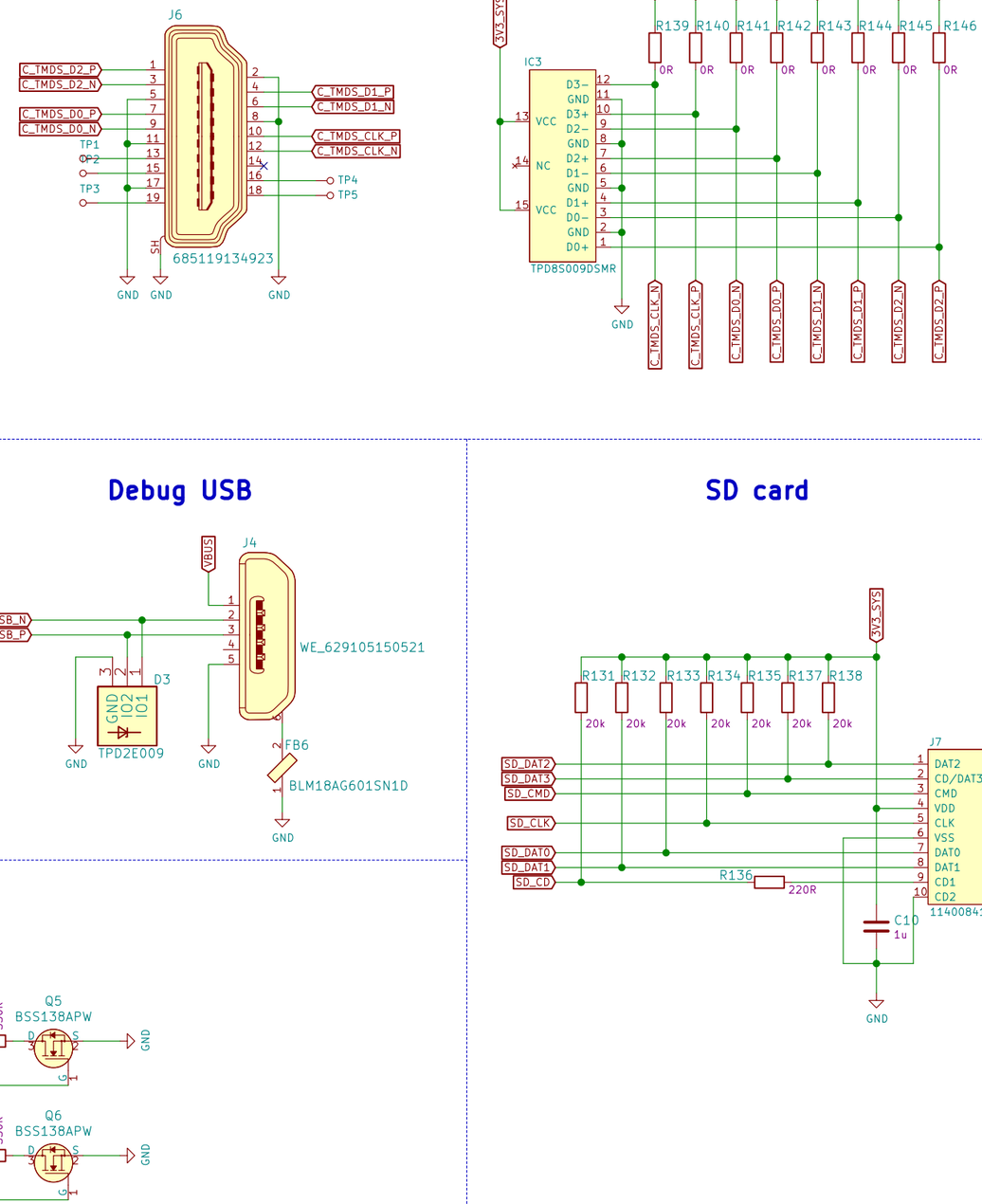
Title: Data Center DRAM Tester

Size: A3	Date: 2021-08	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 5/10

Debug UART



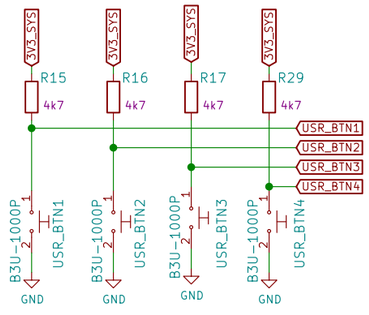
HDMI



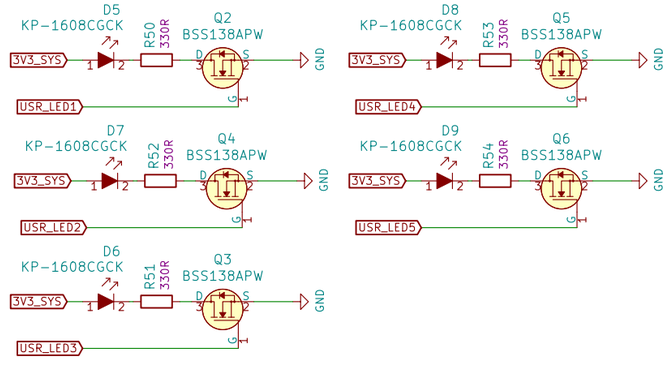
Debug USB

SD card

User buttons



User LEDs



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Sheet: /Interfaces/
File: interfaces.sch

Title: Data Center DRAM Tester

Size: A3	Date: 2021-08	**Rev: 1.0.0**
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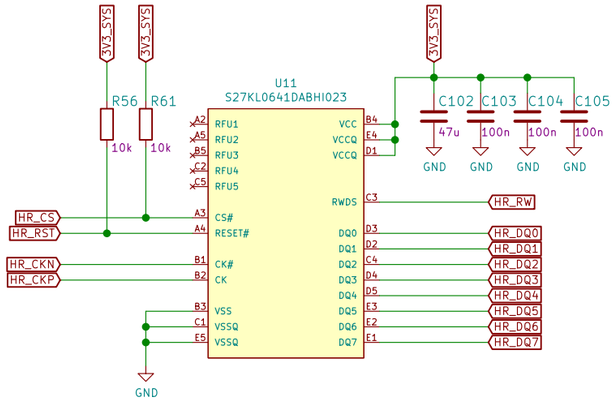
HyperRAM



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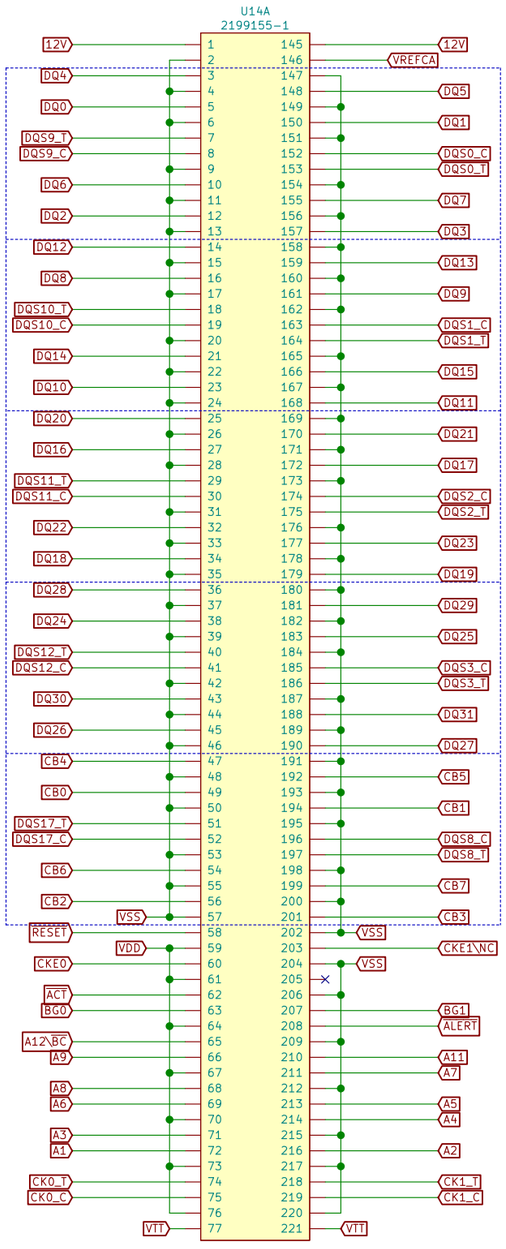
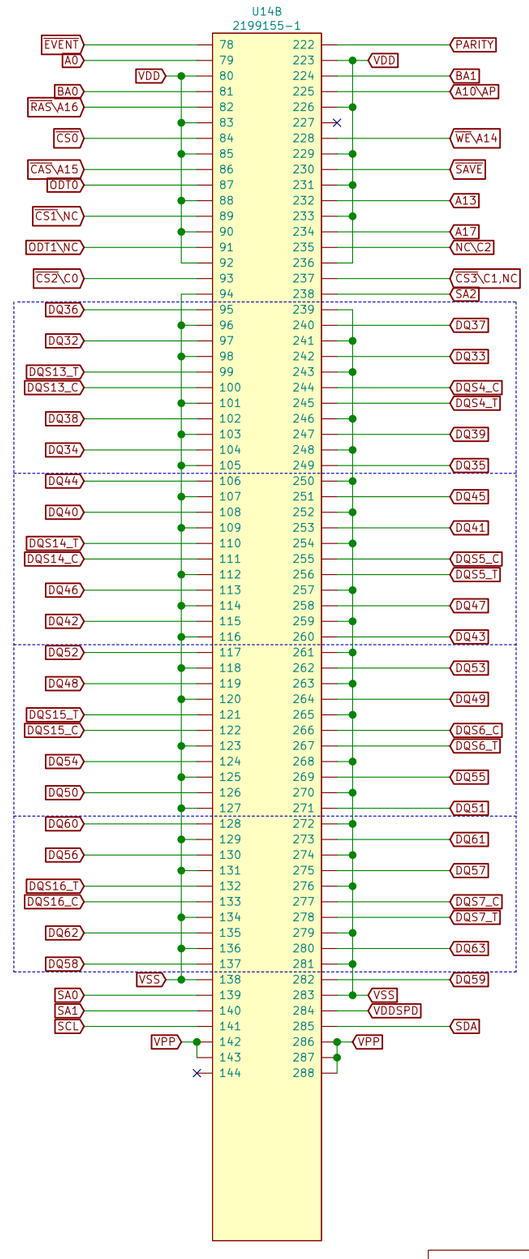
Sheet: /HyperRAM/
File: hyperram.sch

Title: Data Center DRAM Tester

Size: A3	Date: 2021-08	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 7/10

DDR4 RDIMM connector





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Sheet: /DDR4/
File: DDR4.sch

Title: Data Center DRAM Tester

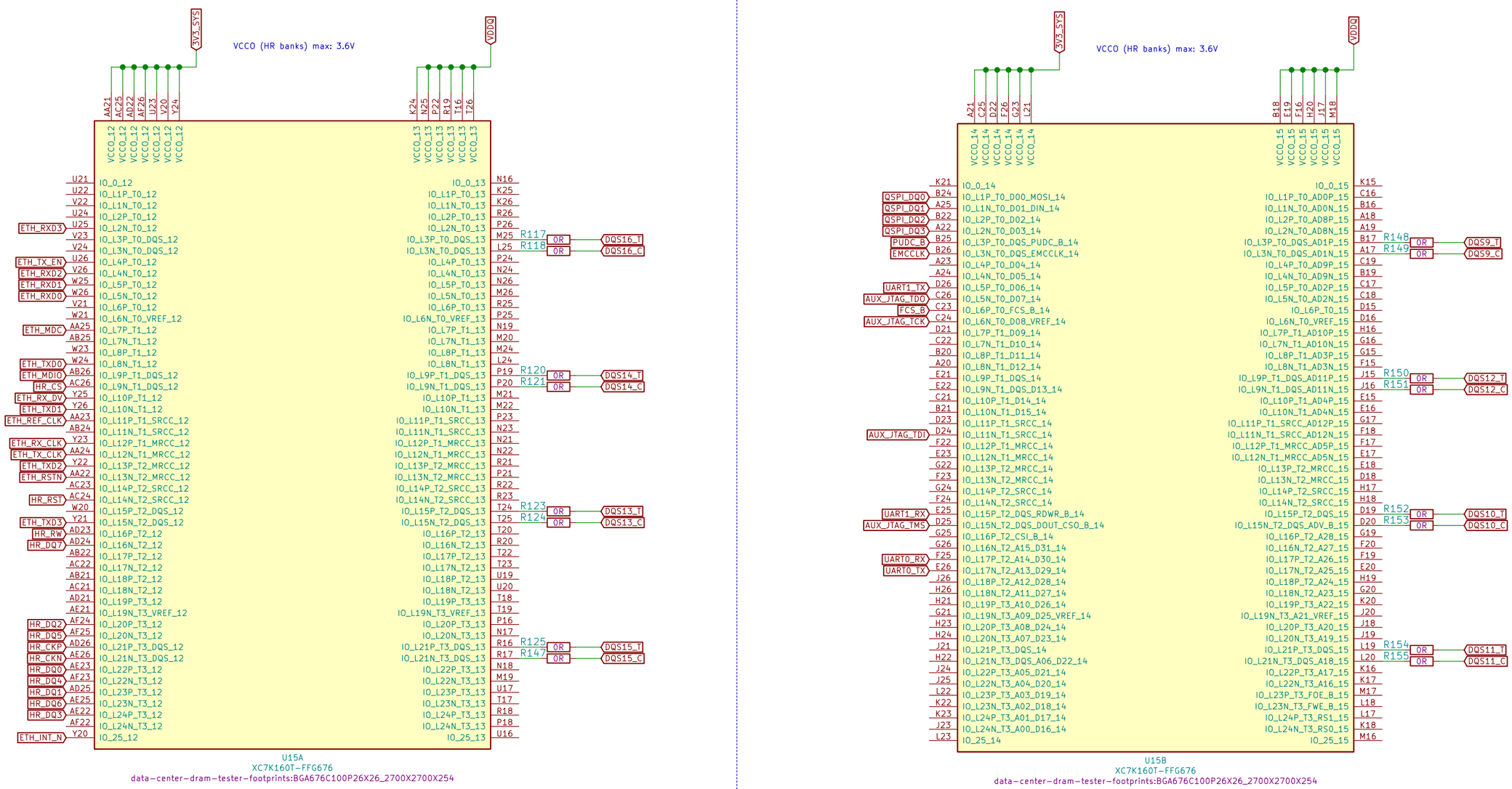
Size: A3	Date: 2021-08	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 8/10

BANK 12

BANK 13

BANK 14

BANK 15



TODO: Connect these signals

AUX_JTAG_RST
GCLK100
USR_BTN1
USR_BTN3
USR_LED5
USR_LED1
USR_LED2
USR_BTN4
USR_BTN2
USR_LED4
USR_LED3

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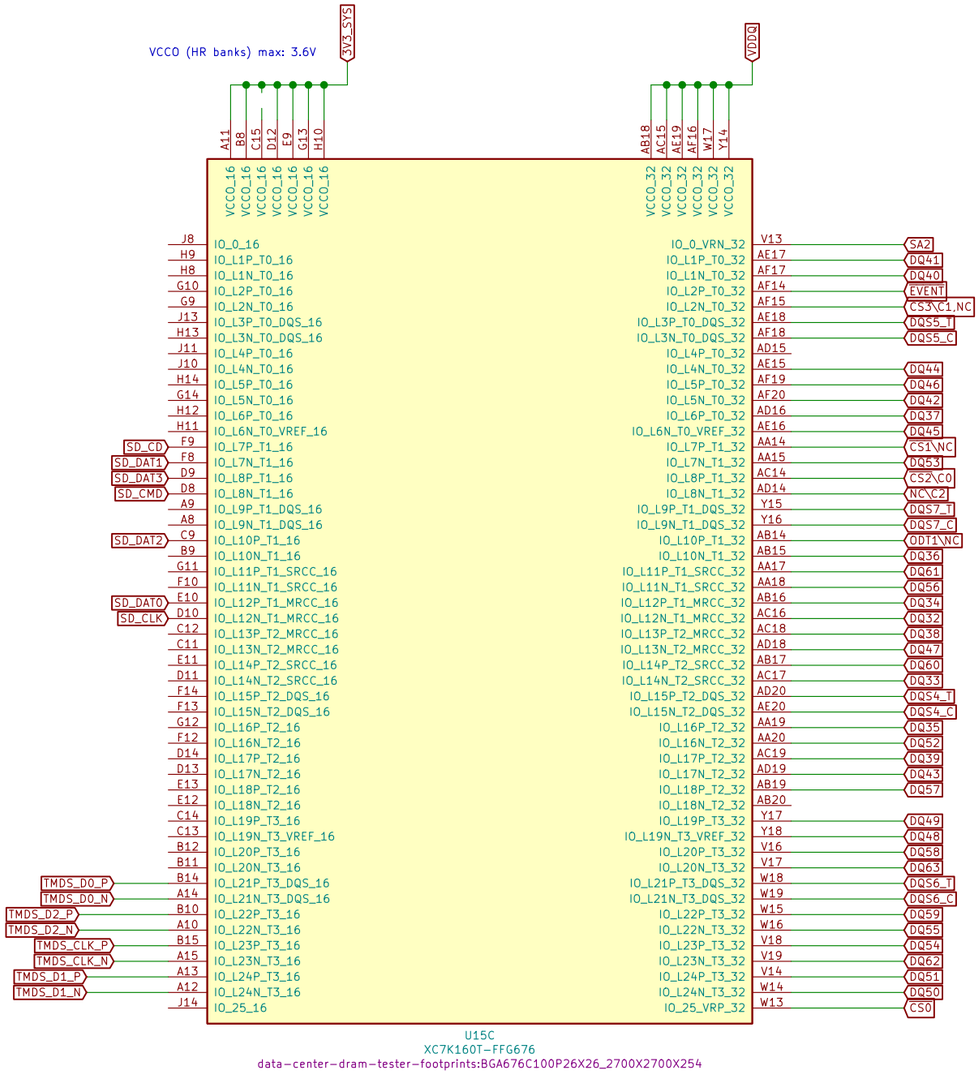
Sheet: /FPGA banks 12-15/
File: fpga-banks-12-15.sch

Title: Data Center DRAM Tester

Size: A3	Date: 2021-08	**Rev: 1.0.0**
KiCad E.D.A.	kicad 5.1.5+dfsg1-2bpo10+1	Id: 9/10

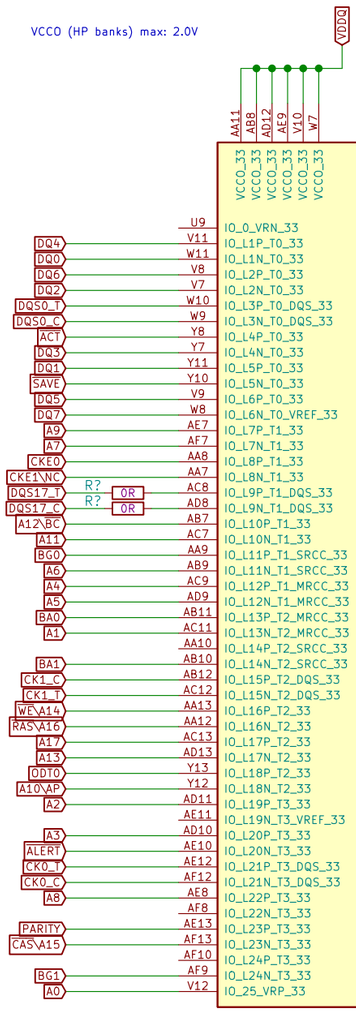
BANK 16



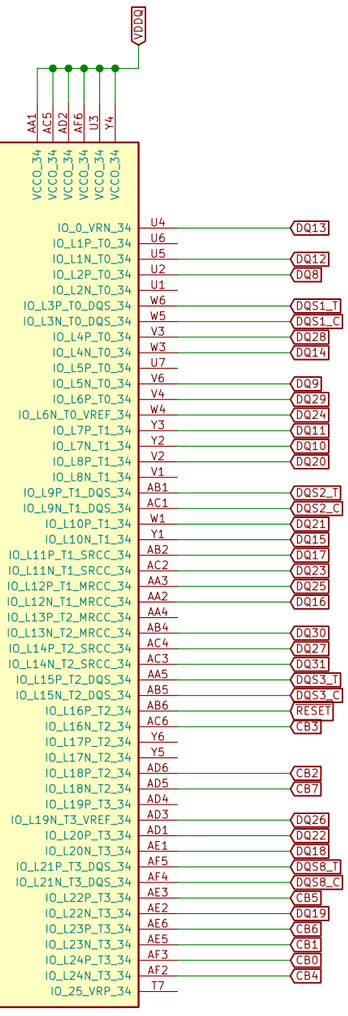
BANK 32

U15C
XC7K160T-FFG676
data-center-dram-tester-footprints:BGA676C100P26X26_2700X2700X254

BANK 33



BANK 34



U15D
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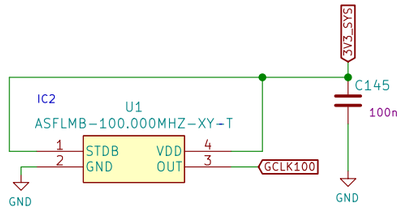
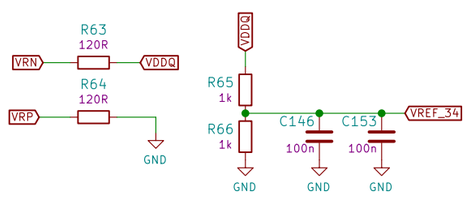
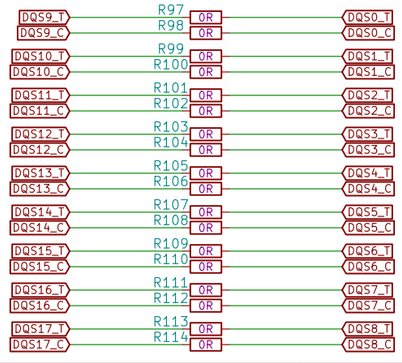
Clock source

TODO: Verify with the new design

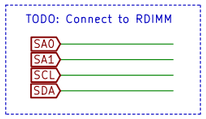


LPDDR VREF





TODO: Connect to RDIMM



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File: fpga-banks-16-34.sch

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Size: A3	Date: 2021-08	**Rev: 1.0.0**
KiCad E.D.A. kicad 5.1.5+dfsg1-2bpo10+1		Id: 10/10