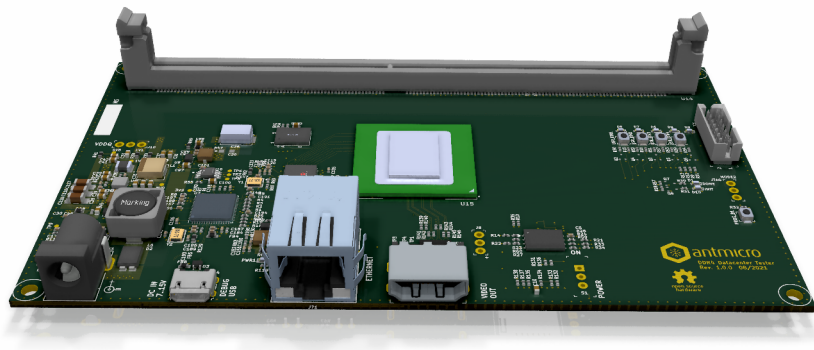


Data Center DRAM Tester



Sheet: HyperRAM	Sheet: DDR4	Sheet: Interfaces	Sheet: Ethernet	Sheet: Supply
File: hyperram.sch	File: DDR4.sch	File: interfaces.sch	File: ethernet.sch	File: supply.sch
Sheet: Config SPI flash	Sheet: FPGA power	Sheet: FPGA banks 12-15	Sheet: FPGA banks 16-34	
File: config-spi.sch	File: fpga-power.sch	File: fpga-banks-12-15.sch	File: fpga-banks-16-34.sch	

Logo N1 oshw_logo
Logo N2 antmicro_logo

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Sheet: /
File: data-center-dram-tester.sch

Title: Data Center DRAM Tester

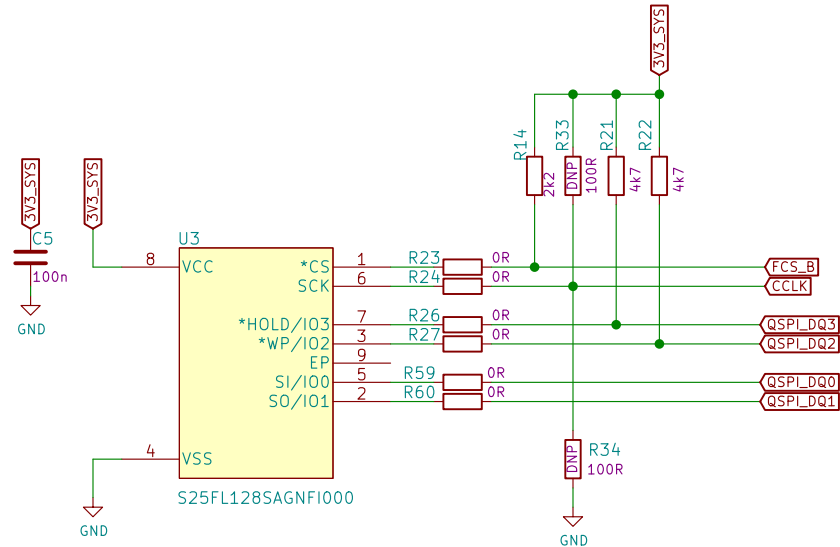
Size: A3 Date: 2021-08
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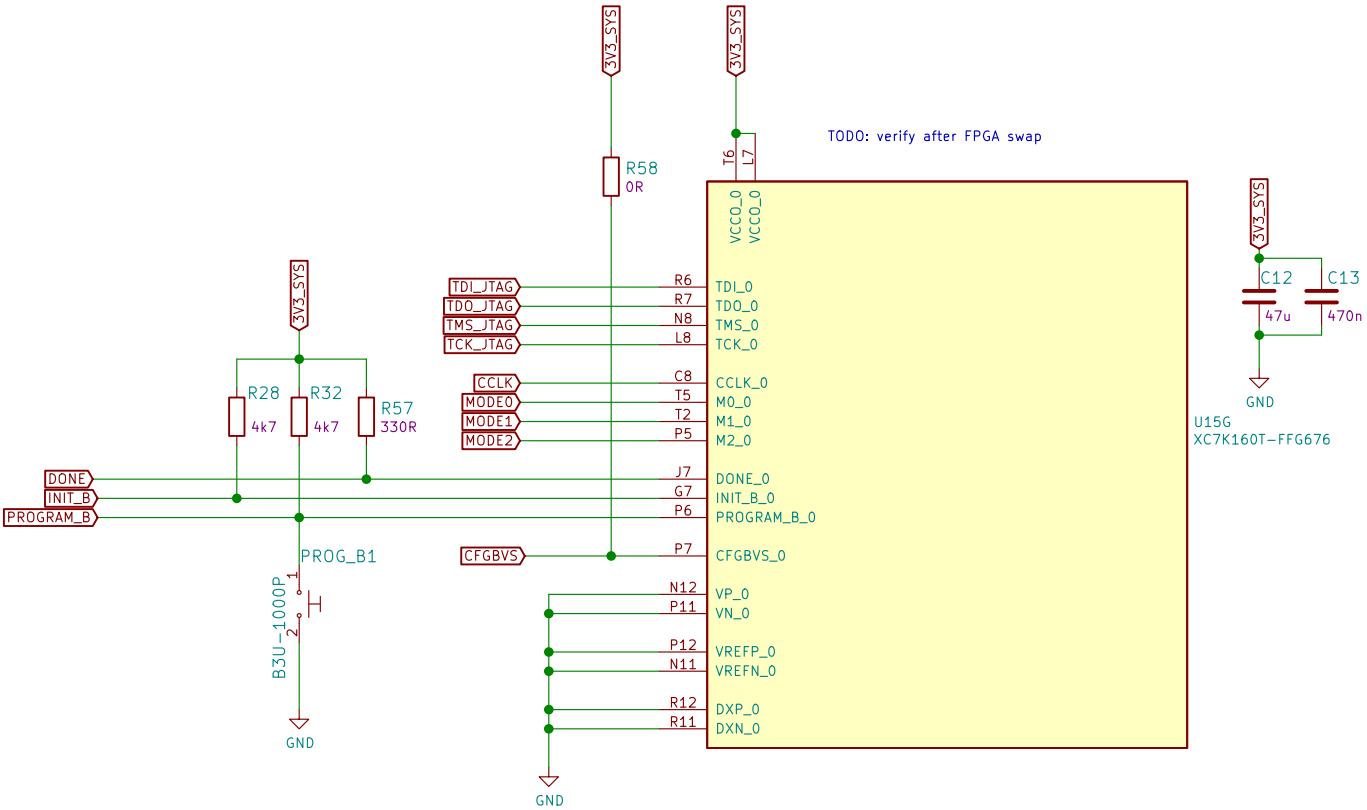
Master SPI Quad (x4) configuration scheme

Follows Figure 2-14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

(Q)SPI flash

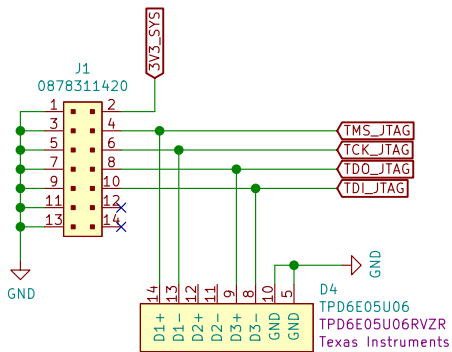


FPGA BANK 0

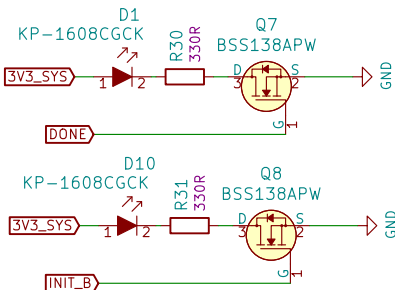


JTAG Connector

Compatible with Xilinx Platform Cable

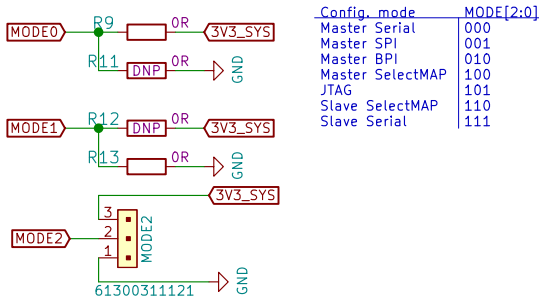


STATUS LEDs

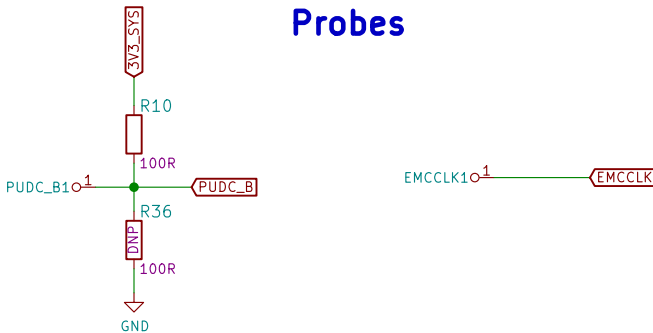


Configuration Modes

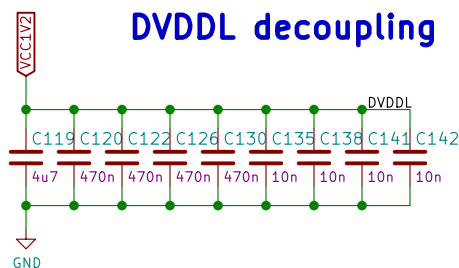
For details, see UG470 p. 21



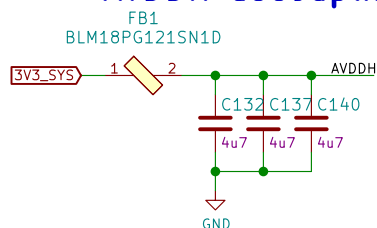
Probes



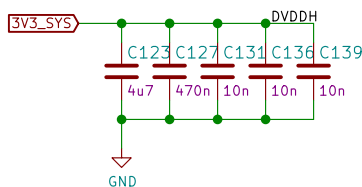
DVDDL decoupling



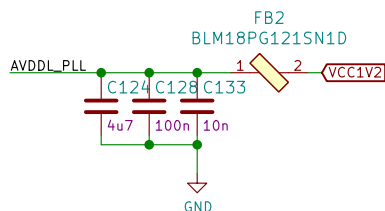
AVDDH decoupling



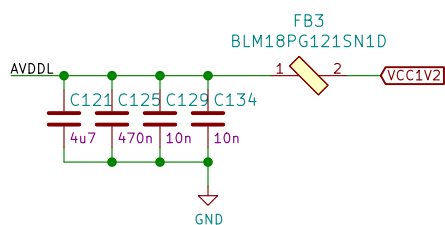
DVDDH decoupling



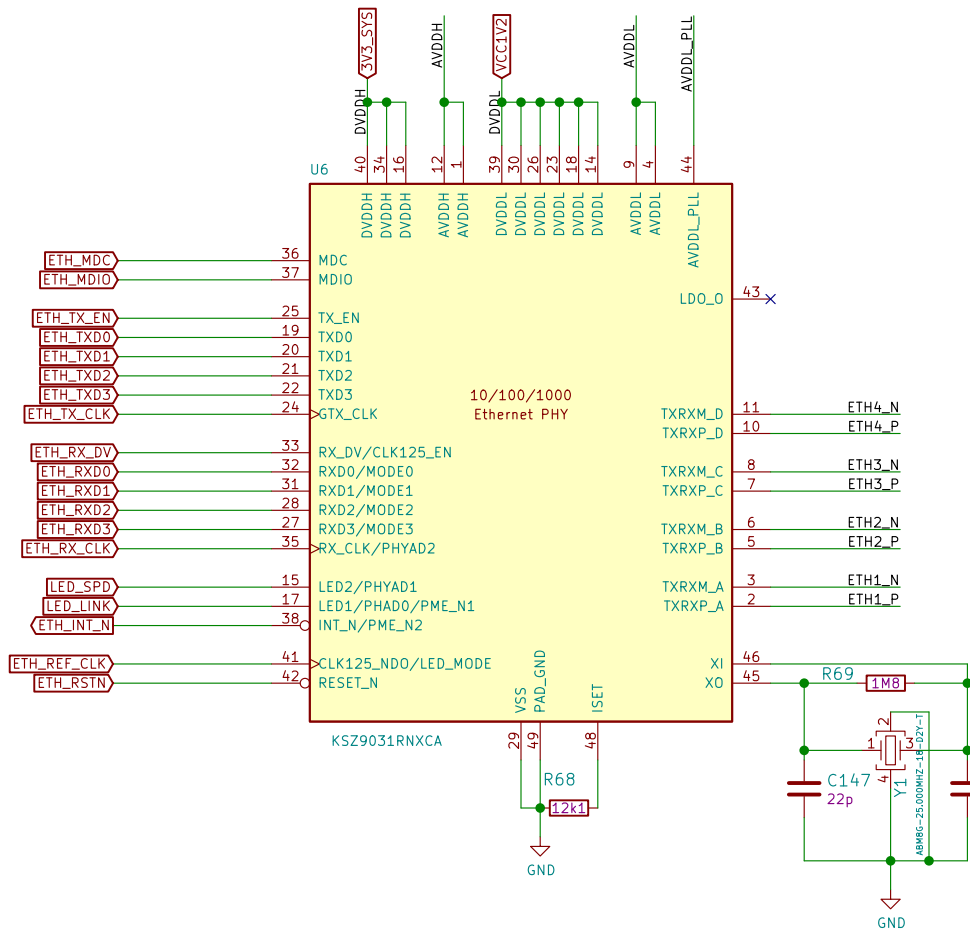
AVDDL_PLL decoupling



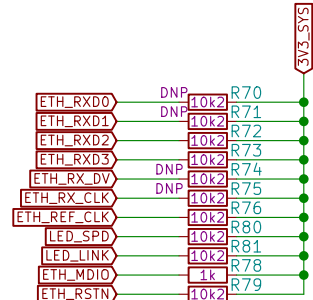
AVDDL decoupling



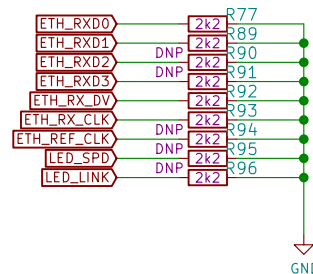
PHY



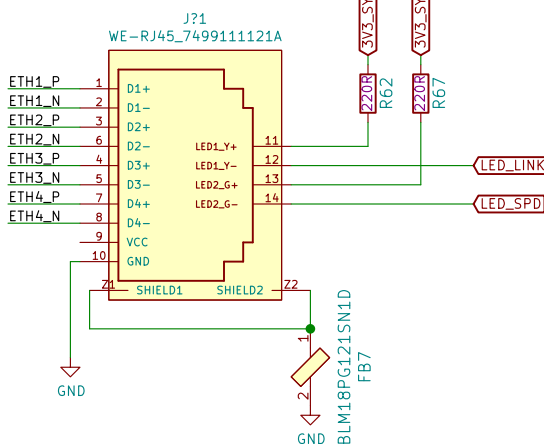
Pull up resistors



Pull down resistors



RJ45 Connector



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Debug USB

The diagram illustrates the wiring for a Debug USB connection. A USB connector J4 is shown with the following connections:

- Pin 1 (VBUS) is connected to GND.
- Pin 2 is connected to DBG_USB_N.
- Pin 3 is connected to DBG_USB_P.
- Pin 4 is connected to GND.
- Pin 5 is connected to a diode (TPD2E009) which is also connected to GND.
- A 10k resistor (FB6, BLM18AG6015N10) is connected between pin 5 and GND.

SD card

The diagram illustrates the electrical connections for an SD card. The card, labeled 'microSD CARD' and 'Shell', has a pinout as follows:

- Pin 1: DAT2
- Pin 2: CD/DAT3
- Pin 3: CMD
- Pin 4: VDD
- Pin 5: VSS
- Pin 6: CLK
- Pin 7: DAT0
- Pin 8: DAT1
- Pin 9: CD1
- Pin 10: CD2

The connections are as follows:

- 3V3_SYS** is connected to the VDD pin (Pin 4).
- SD_DAT2** is connected to Pin 1 (DAT2).
- SD_DAT3** is connected to Pin 2 (CD/DAT3).
- SD_CMD** is connected to Pin 3 (CMD).
- SD_CLK** is connected to Pin 6 (CLK).
- SD_DAT0** is connected to Pin 7 (DAT0).
- SD_DAT1** is connected to Pin 8 (DAT1).
- SD_CD** is connected to Pin 9 (CD1) and Pin 10 (CD2).
- A **220R** resistor (R136) is connected between Pin 10 (CD2) and ground.
- A **1uF** capacitor (C10) is connected between Pin 10 (CD2) and ground.

User buttons

The diagram shows four user buttons (USR_BTN1, USR_BTN2, USR_BTN3, USR_BTN4) connected to a 3V3-SYS supply and a common ground. Each button is connected to a 4k7 resistor (R15, R16, R17, R29) which is then connected to a common green line leading to GND. Each button is also connected to a 1000P capacitor (B3U-1000P) which is connected to GND.

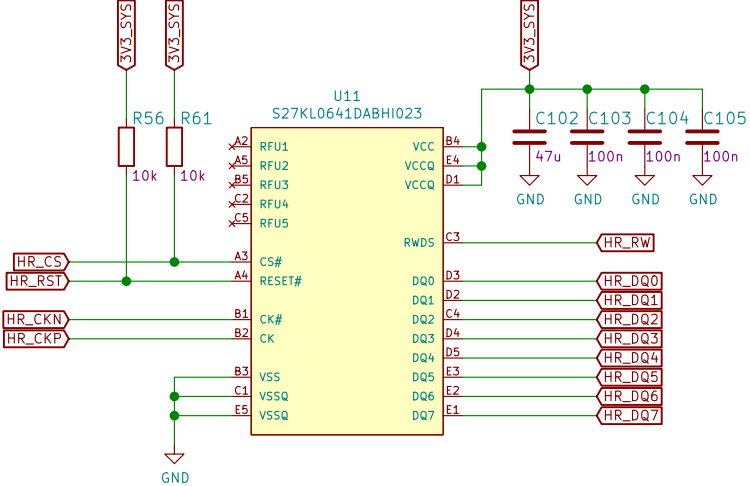
User LEDs

Diagram showing three LED driver circuits (USR_LED1, USR_LED2, USR_LED3) connected to a 3V3_SYS supply. Each circuit uses a diode (D5, D7, D6), a 330R resistor (R50, R52, R51), and a BSS138APW MOSFET (Q2, Q4, Q3) to drive the LED.

Diagram showing two LED driver circuits (USR_LED4, USR_LED5) connected to a 3V3_SYS supply. Each circuit uses a diode (D8, D9), a 330R resistor (R53, R54), and a BSS138APW MOSFET (Q5, Q6) to drive the LED.

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HyperRAM



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Sheet: /HyperRAM/
File: hyperram.sch

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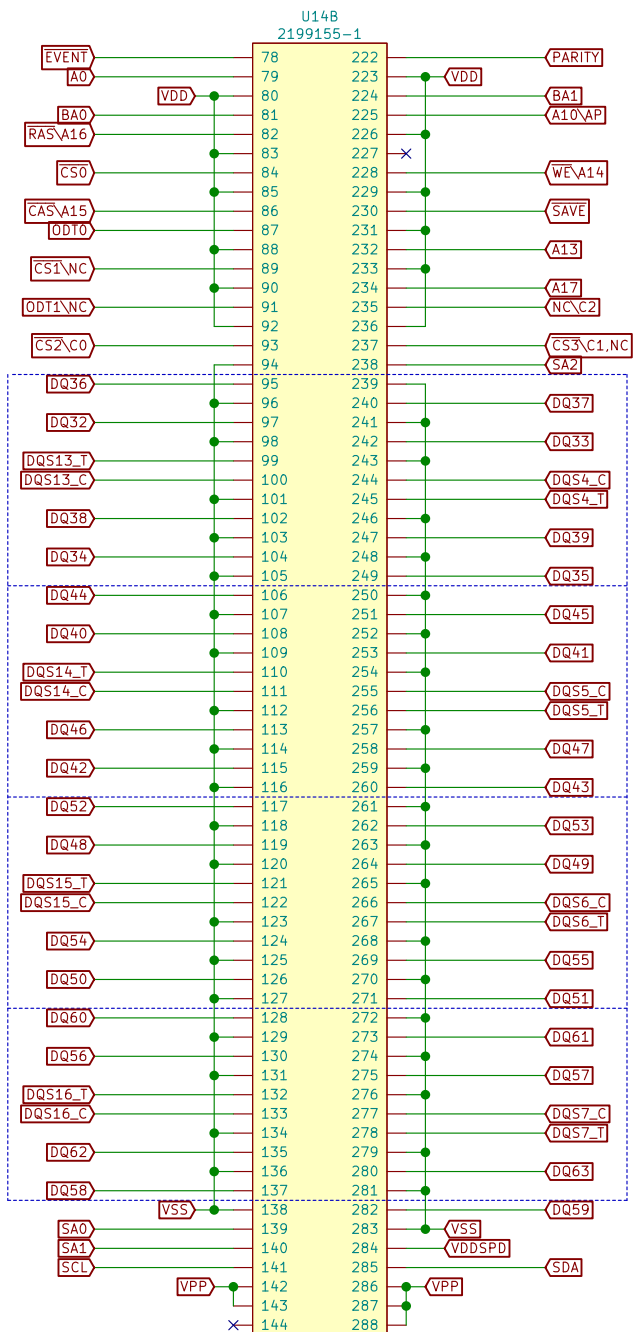
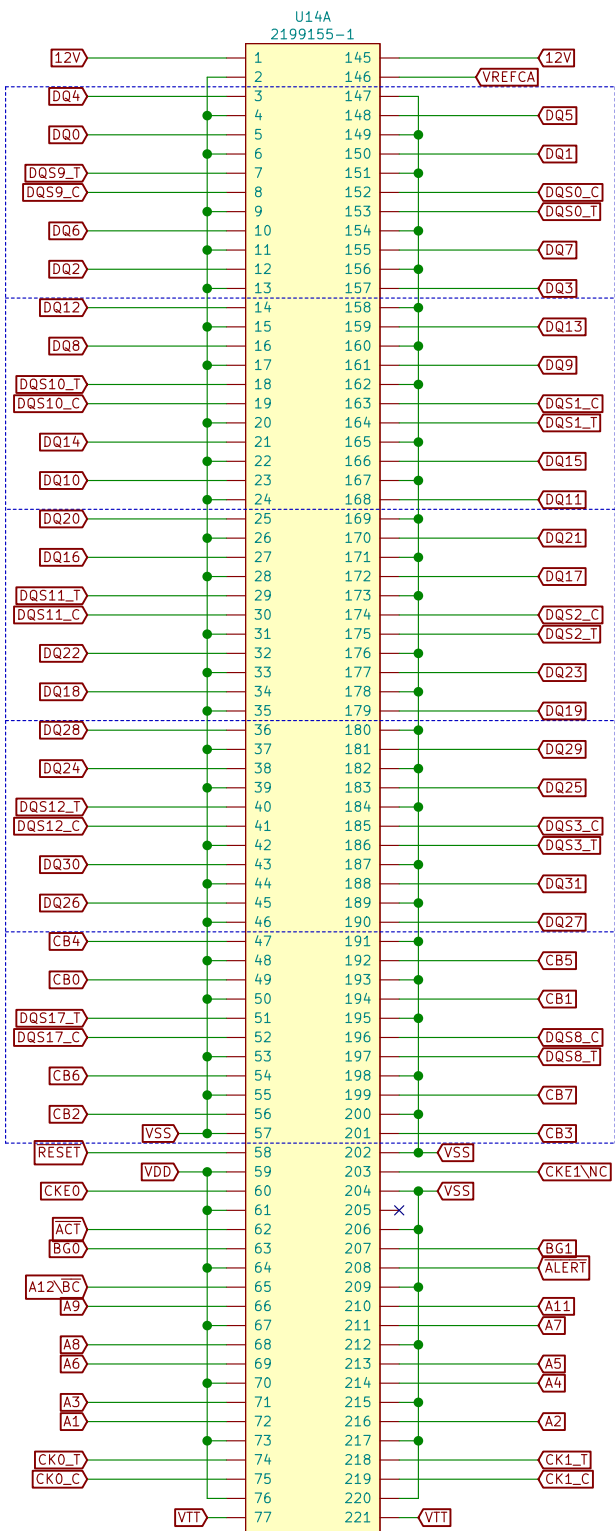
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DDR4 RDIMM connector



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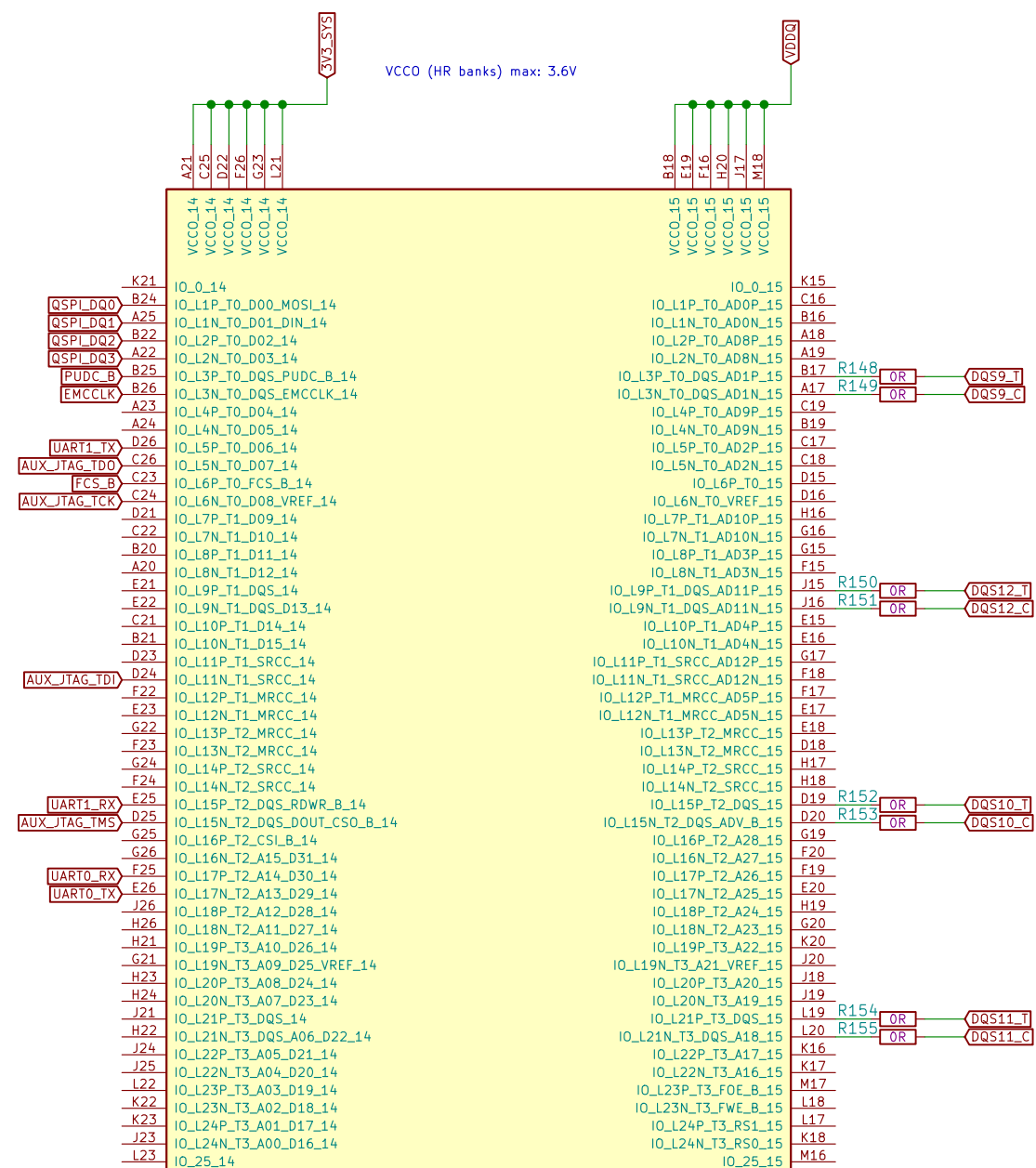
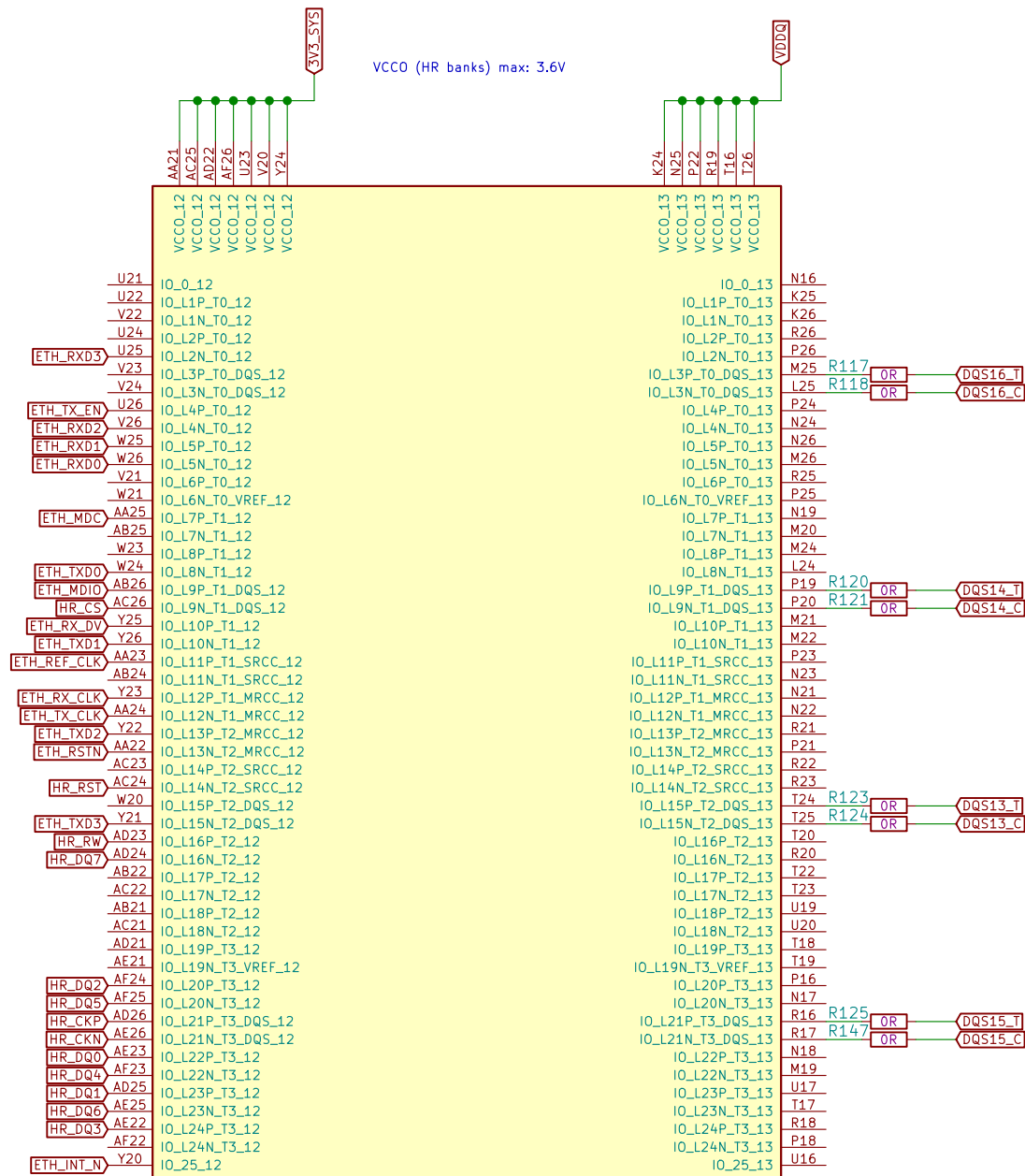
Id: 8/10

BANK 12

BANK 13

BANK 14

BANK 15



TODO: Connect these signals

AUX_JTAG_RST
[GCLK100]

USR_BTN1
USR_BTN3
USR_LED5
USR_LED1
USR_LED2
USR_BTN4
USR_BTN2
USR_LED4
USR_LED3

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File: fpga-banks-12-15.sch

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