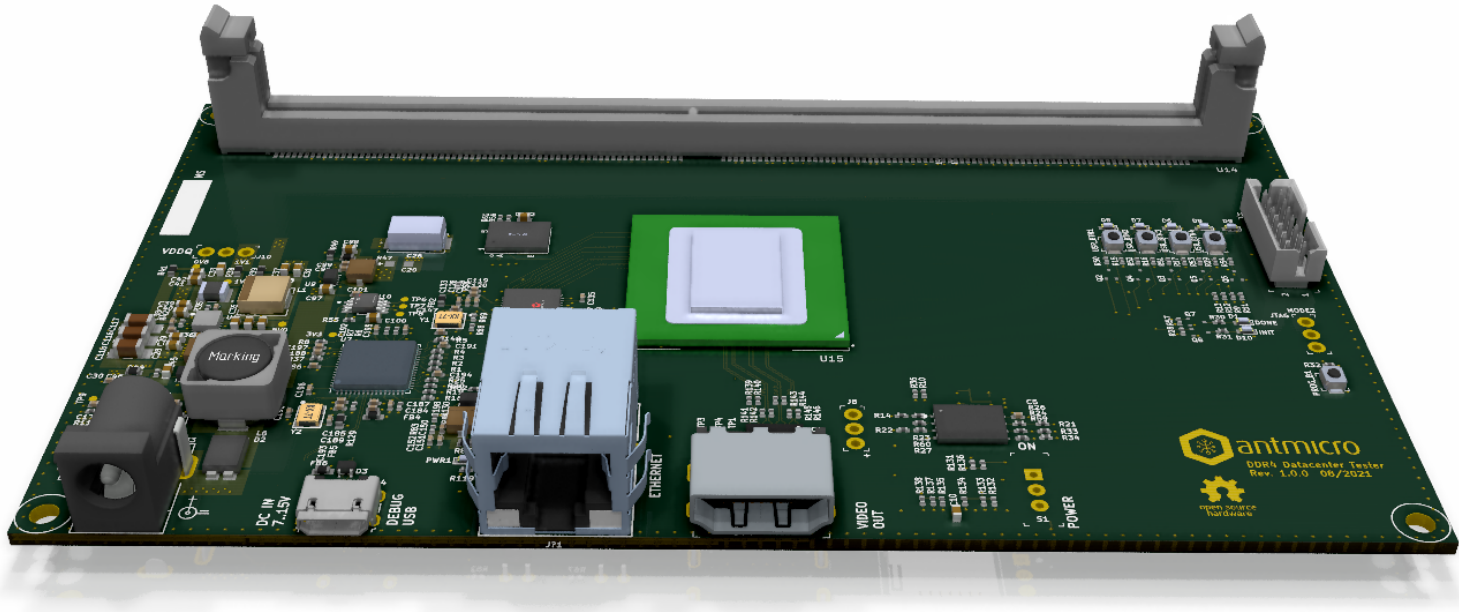


Data Center DRAM Tester



Sheet: HyperRAM



File: hyperram.sch

Sheet: DDR4



File: DDR4.sch

Sheet: Interfaces



File: interfaces.sch

Sheet: Ethernet



File: ethernet.sch

Sheet: Supply



File: supply.sch

Sheet: Config SPI flash



File: config-spi.sch

Sheet: FPGA power



File: fpga-power.sch

Sheet: FPGA banks 12-15



File: fpga-banks-12-15.sch

Sheet: FPGA banks 16-34



File: fpga-banks-16-34.sch

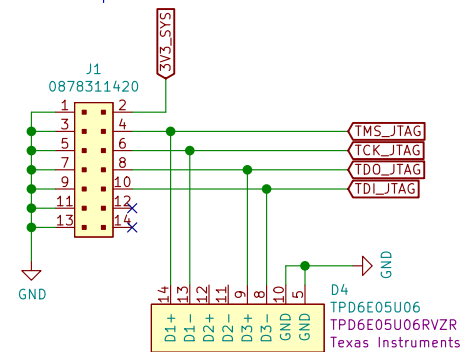
Logo ^{N1} oshw_logo
Logo ^{N2} antmicro_logo

Follows Figure 2-14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

The schematic diagram illustrates the power and signal connections for the XC7K160T-FFG676 FPGA. The FPGA is represented by a large yellow block with various pins labeled on the right side. The connections are as follows:

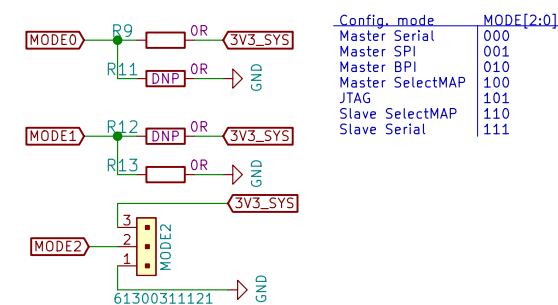
- Power Connections:**
 - VCC0_0 and VCC0_1:** Connected to a 3V3_SYS supply through a 16 ohm resistor (R58) and a 17 ohm resistor (L7).
 - VP_0 and VN_0:** Connected to a 3V3_SYS supply through a 12 ohm resistor (N12) and a 11 ohm resistor (P11).
 - VREFP_0 and VREFN_0:** Connected to a 3V3_SYS supply through a 12 ohm resistor (P12) and a 11 ohm resistor (N11).
 - DXP_0 and DXN_0:** Connected to a 3V3_SYS supply through a 12 ohm resistor (R12) and a 11 ohm resistor (R11).
- Signal Connections:**
 - JTAG Interface:** TDI_0, TDO_0, TMS_0, and TCK_0 are connected to a 3V3_SYS supply through resistors R6, R7, N8, and L8. TDI_0 is also connected to a 3V3_SYS supply through a 16 ohm resistor (R58).
 - Configuration:** CCLK_0, M0_0, M1_0, and M2_0 are connected to a 3V3_SYS supply through resistors C8, T5, T2, and P5. DONE_0, INIT_B_0, and PROGRAM_B_0 are connected to a 3V3_SYS supply through resistors J7, G7, and P6. CFGBVS_0 is connected to a 3V3_SYS supply through a 16 ohm resistor (P7).
 - Other Signals:** VP_0, VN_0, VREFP_0, VREFN_0, DXP_0, and DXN_0 are connected to a 3V3_SYS supply through resistors N12, P11, P12, N11, R12, and R11.
- Power Regulation:**
 - A 3V3_SYS supply is connected to a 3V3_SYS supply through a 16 ohm resistor (R58) and a 17 ohm resistor (L7).
 - A 3V3_SYS supply is connected to a 3V3_SYS supply through a 16 ohm resistor (R58) and a 17 ohm resistor (L7).
- Other Components:**
 - U15G:** XC7K160T-FFG676
 - C12:** 47uF capacitor
 - C13:** 470nF capacitor
 - C37:** 470nF capacitor
 - B3U-1000P:** 1000pF capacitor

Compatible with Xilinx Platform Cable



The diagram shows two identical circuit blocks. The top block contains an inverter D1 (KP-1608CGCK) with its input (pin 1) connected to 3V3_SYS and its output (pin 2) connected to the DONE pin of the AD9232. A 330R resistor (R30) is connected between the output of the inverter and the DONE pin. A Schottky diode Q7 (BSS138APW) is connected with its anode to the output of the inverter and its cathode to GND. The bottom block contains an inverter D10 (KP-1608CGCK) with its input (pin 1) connected to 3V3_SYS and its output (pin 2) connected to the INIT_B pin of the AD9232. A 330R resistor (R31) is connected between the output of the inverter and the INIT_B pin. A Schottky diode Q8 (BSS138APW) is connected with its anode to the output of the inverter and its cathode to GND.

For details, see UG470 p. 21



Probes

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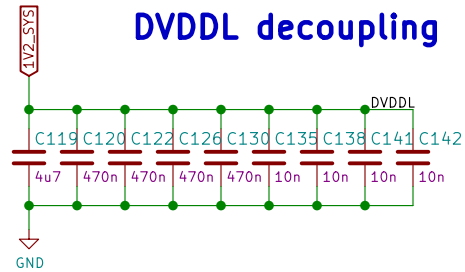
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Rev: 1.1.0
Id: 2/10

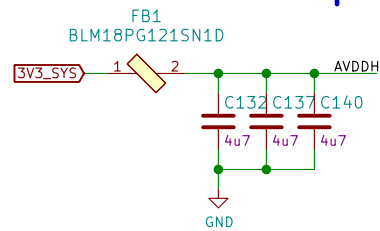




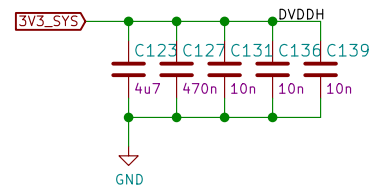
DVDDL decoupling



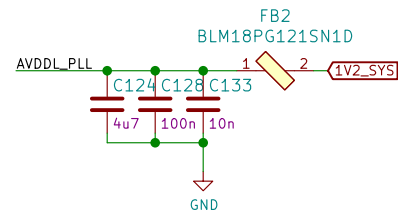
AVDDH decoupling



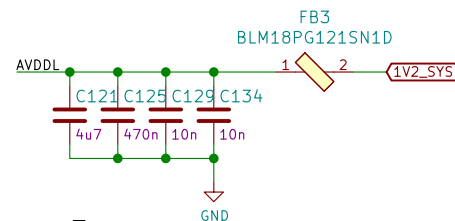
DVDDH decoupling



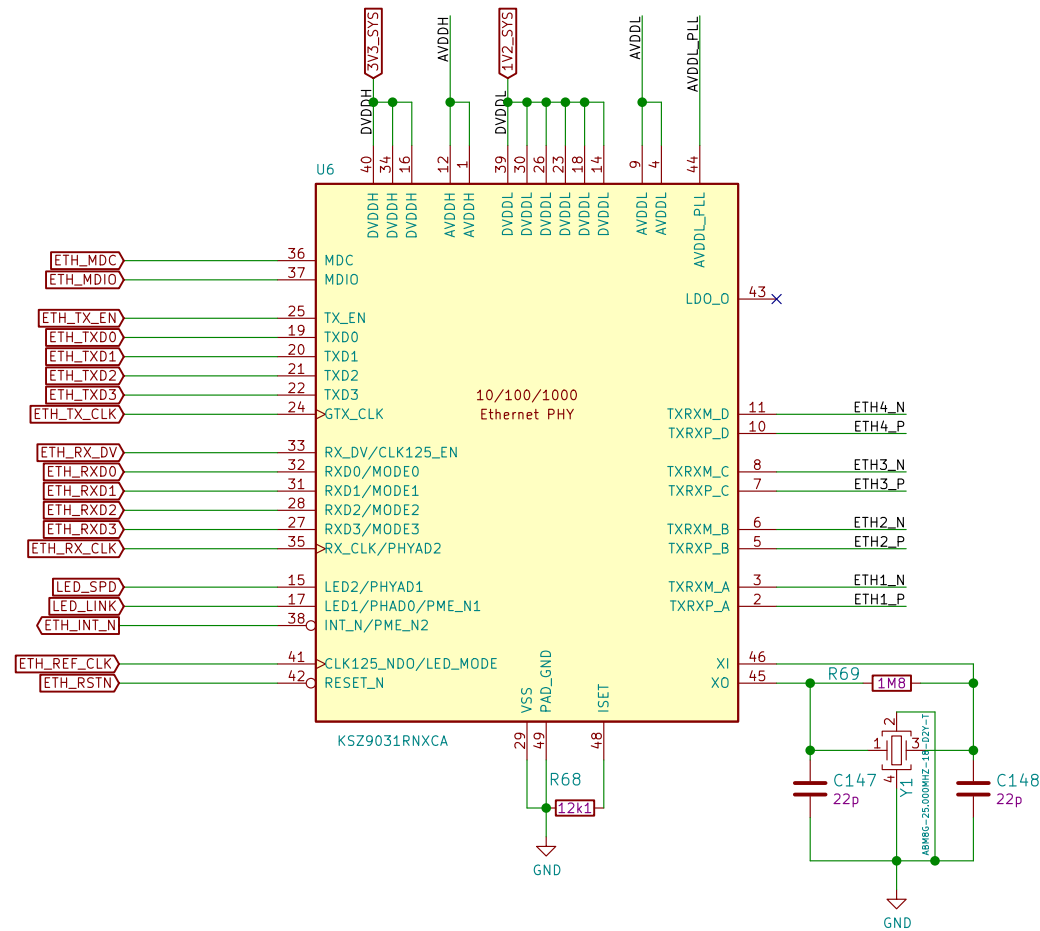
AVDDL_PLL decoupling



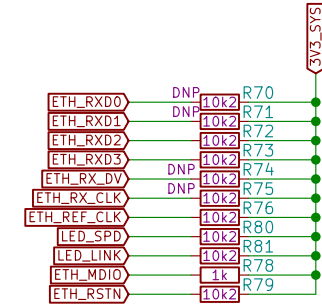
AVDDL decoupling



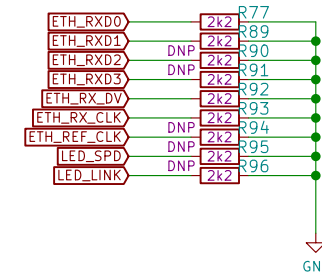
PHY



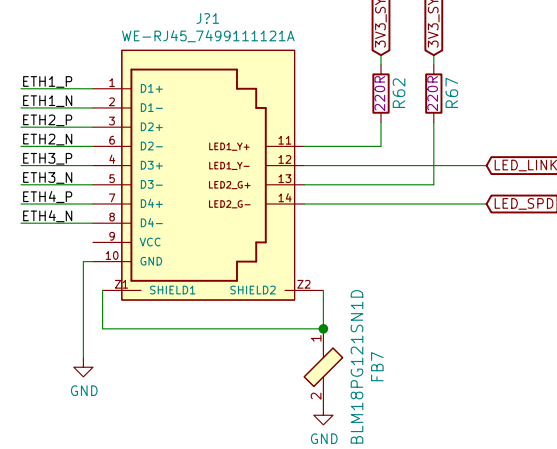
Pull up resistors



Pull down resistors



RJ45 Connector



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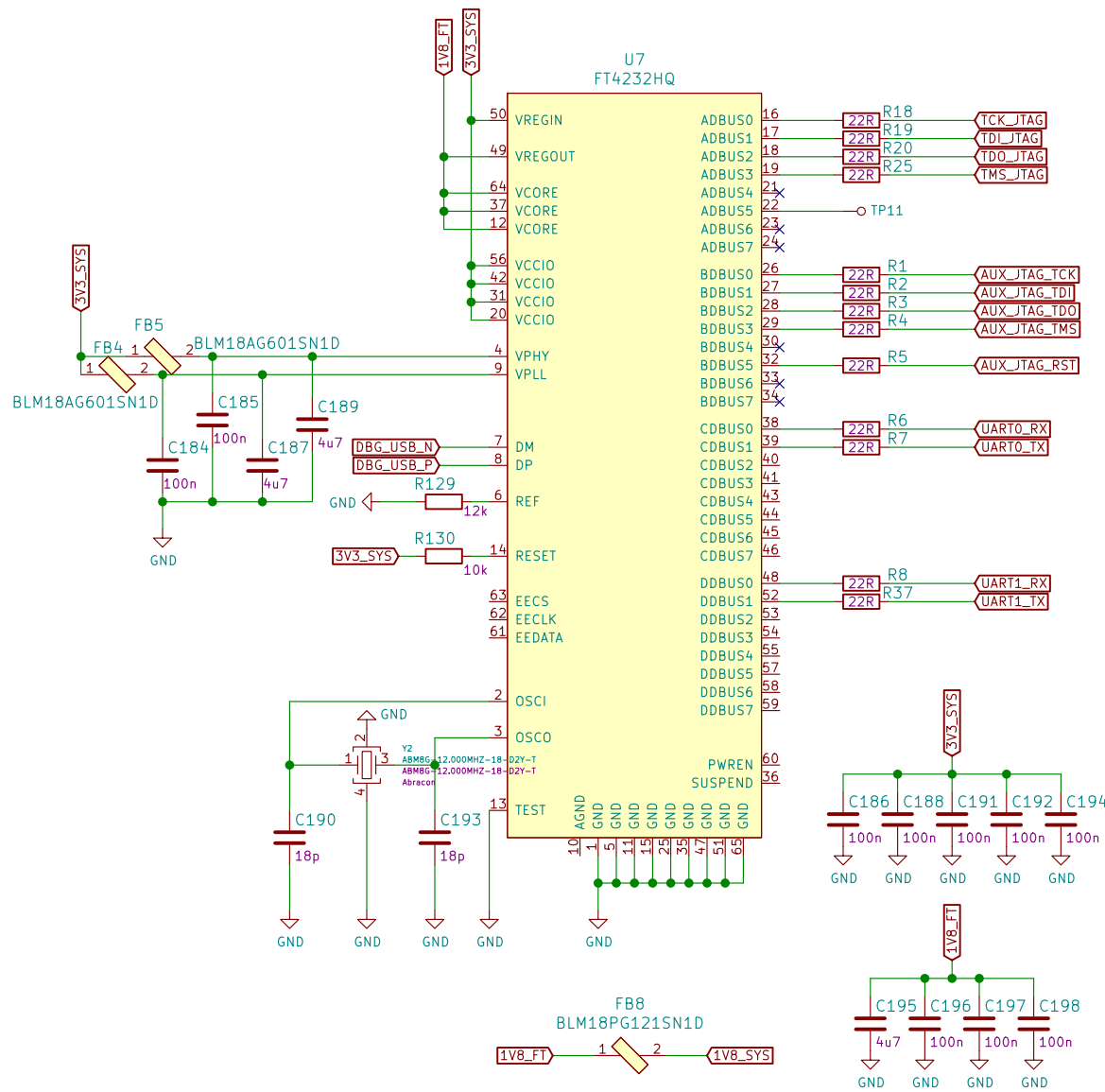
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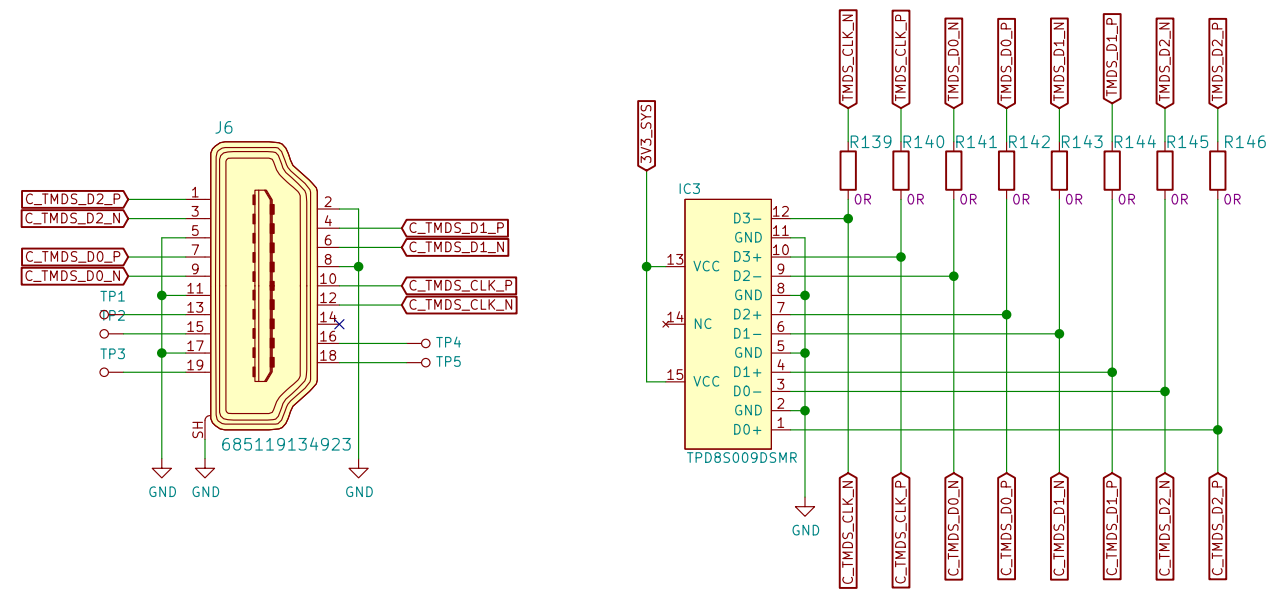
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Rev: 1.1.0
Id: 4/10

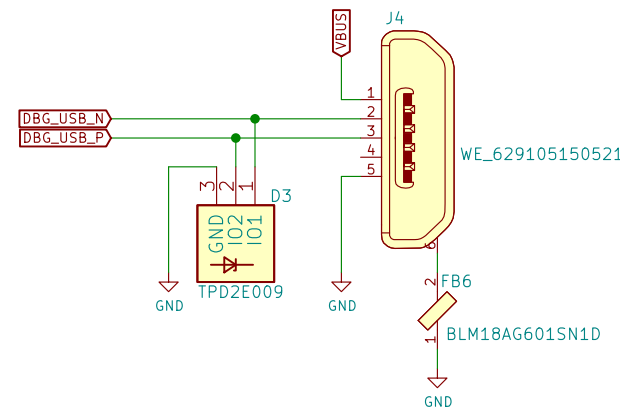
Debug UART



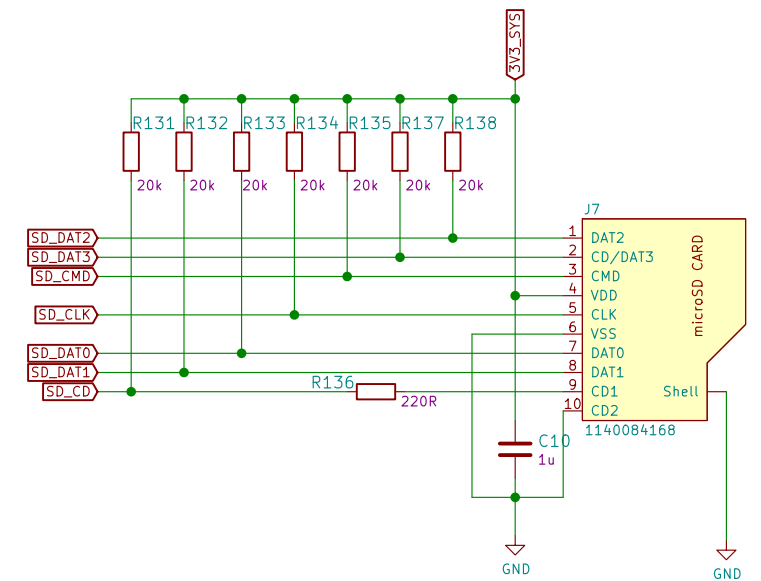
HDMI



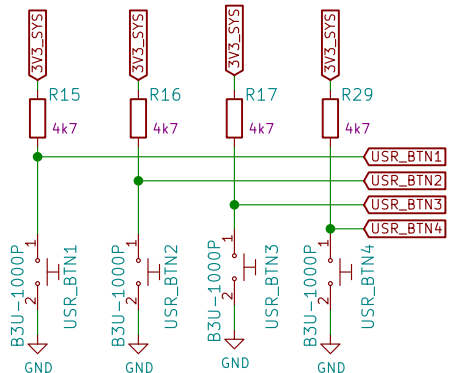
Debug USB



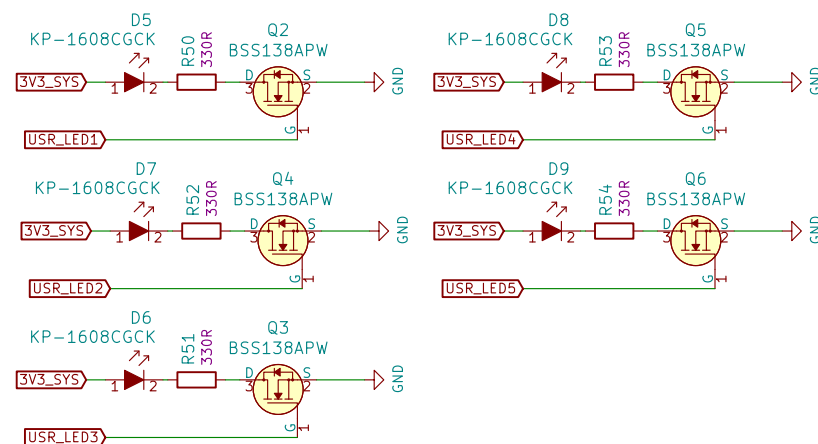
SD card

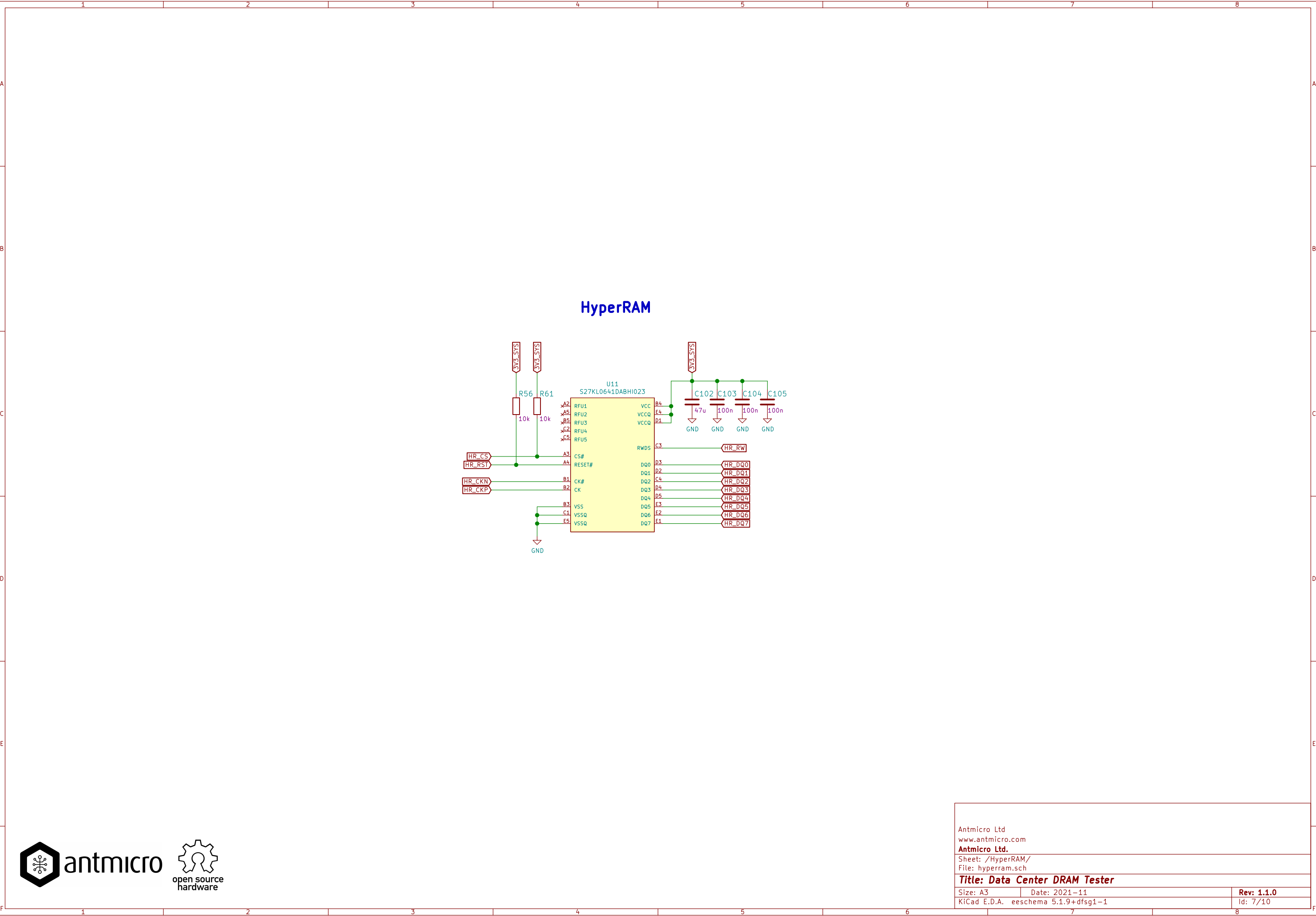


User buttons

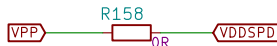
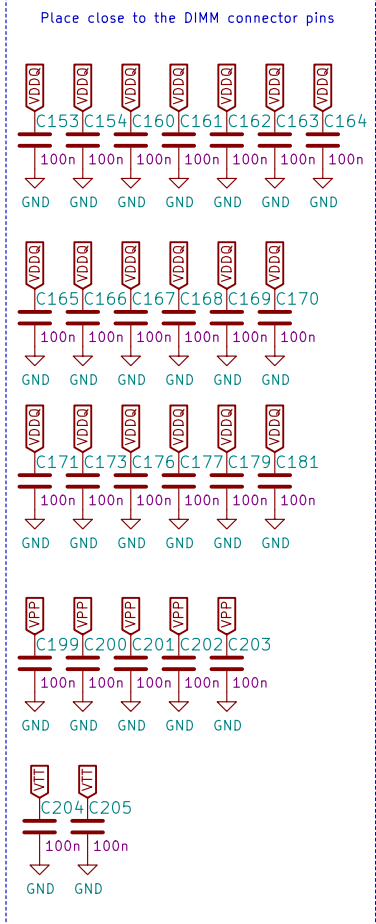
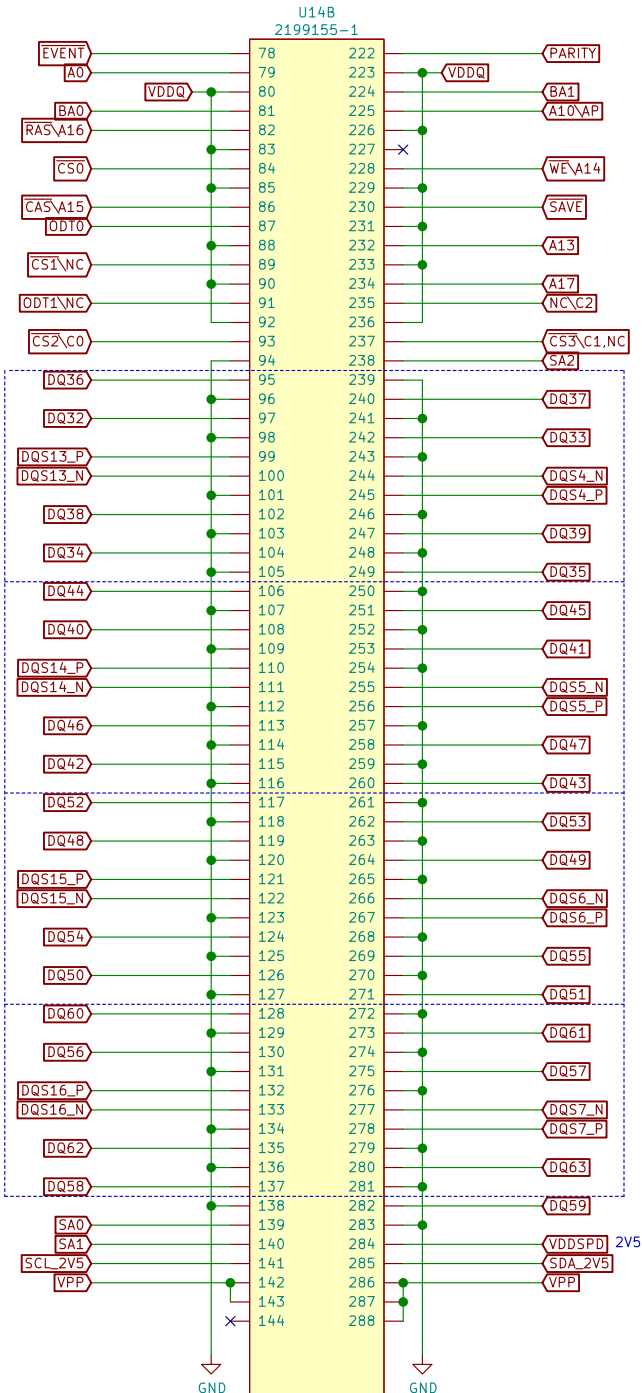
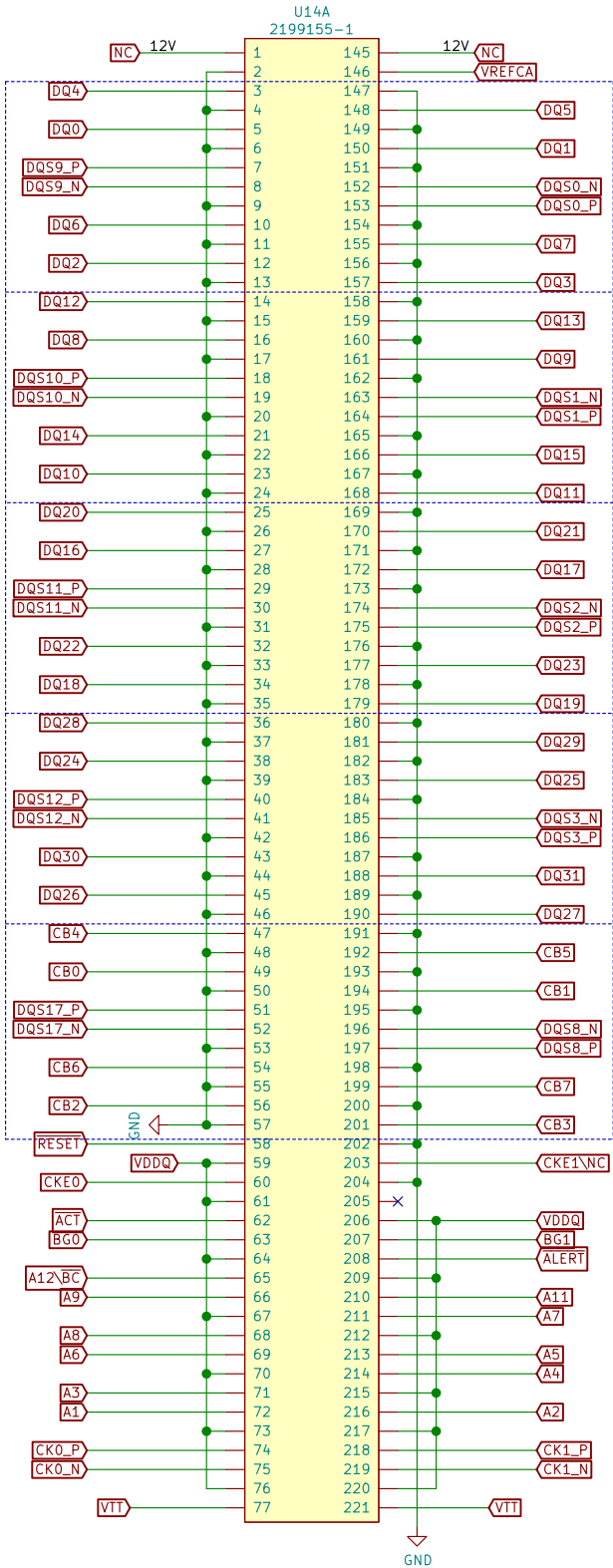
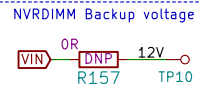


User LEDs





DDR4 RDIMM connector

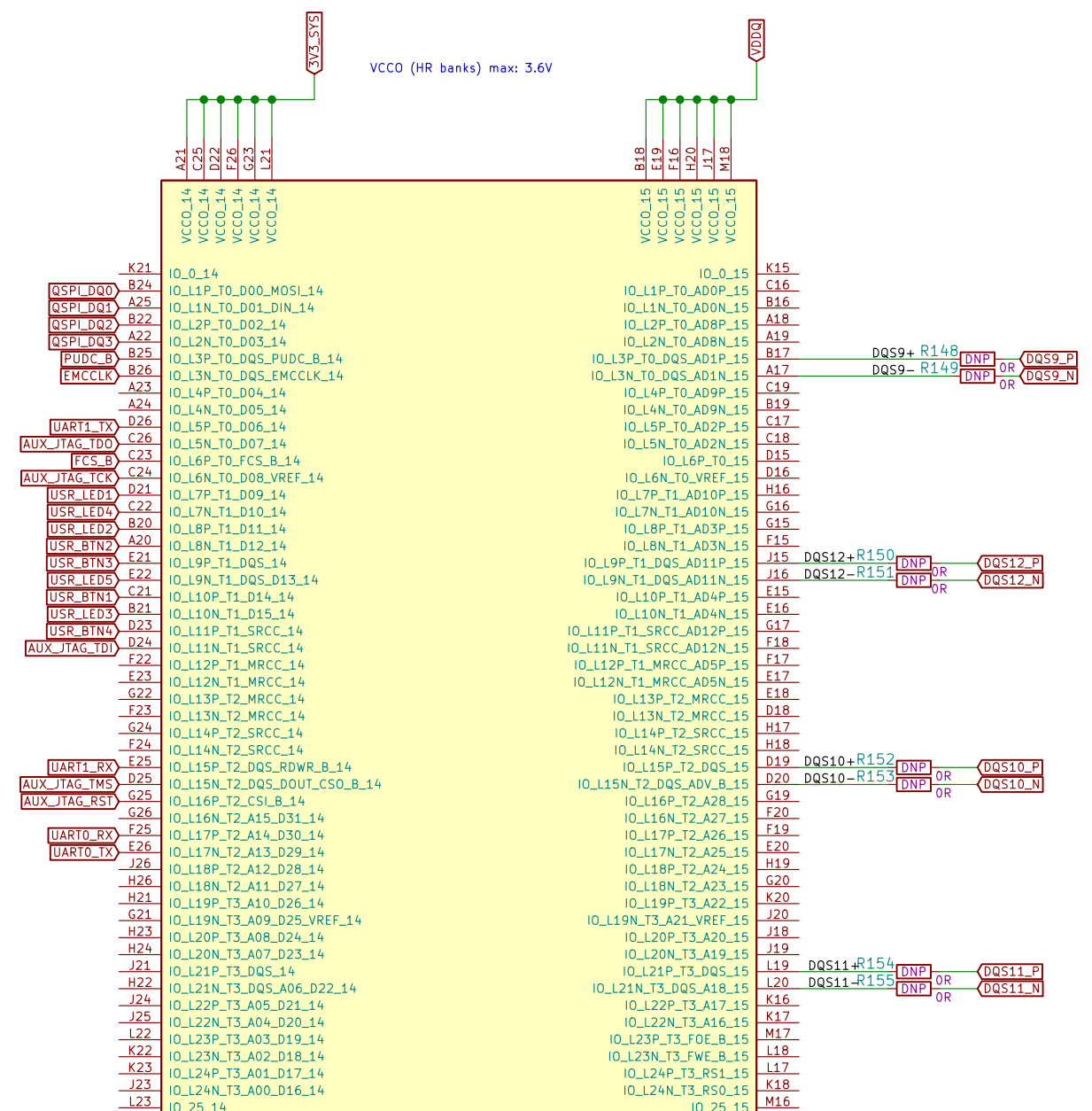
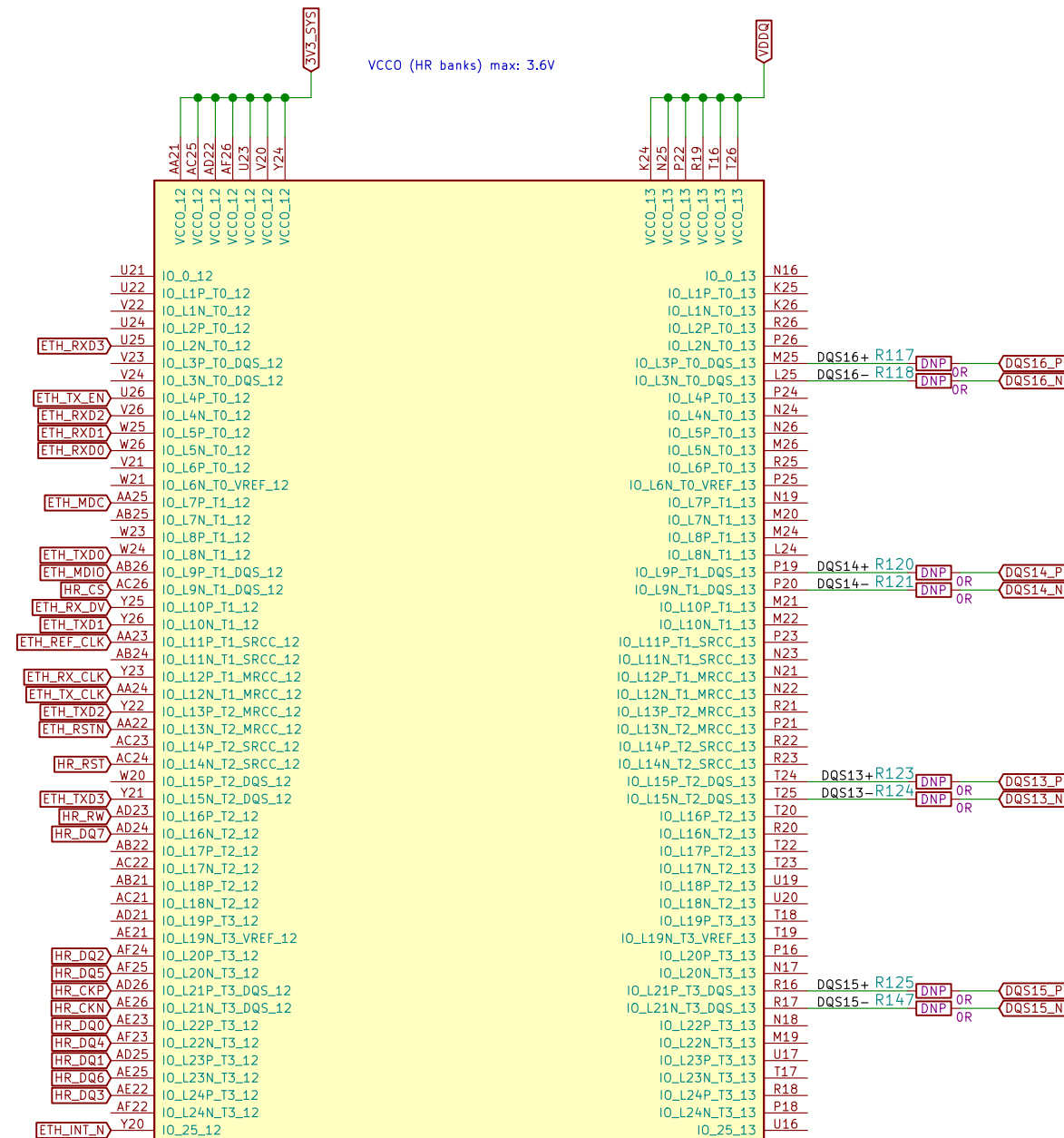


BANK 12

BANK 13

BANK 14

BANK 15



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Sheet: /FPGA banks 12-15/
File: fpga-banks-12-15.sch

Title: Data Center DRAM Tester

Size: A3

Date: 2021-11

Rev: 1.1.0

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Id: 9/10

