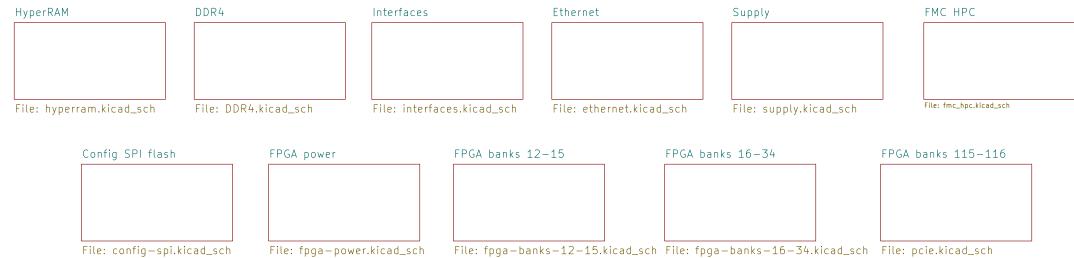
# Data Center DRAM Tester













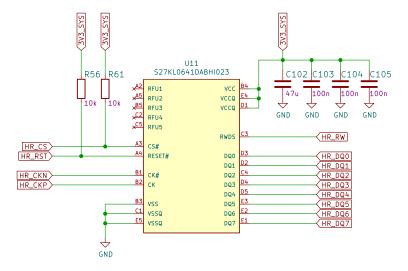


Logo N1 oshw\_logo

Antmicro Ltd www.antmicro.com Sheet: /
File: data-center-dram-tester.kicad\_sch

Title: Data Center DRAM Tester

# HyperRAM





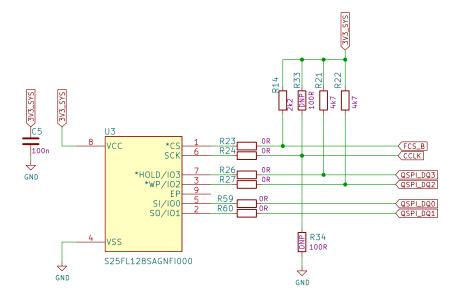
Antmicro Ltd www.antmicro.com
Antmicro Ltd. Sheet: /HyperRAM/ File: hyperram.kicad\_sch

Title: Data Center DRAM Tester Size: A3 Date: 2022-10-31 KiCad E.D.A. eeschema 6.0.5+dfsg-1~bpo11+1

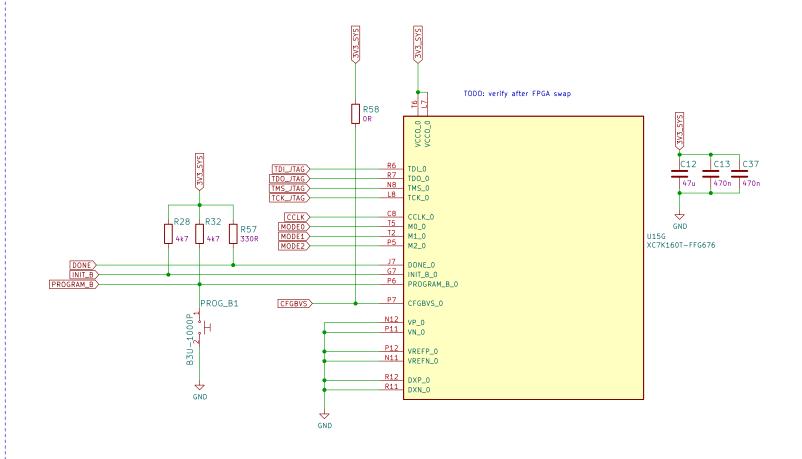
## Master SPI Quad (x4) configuration scheme

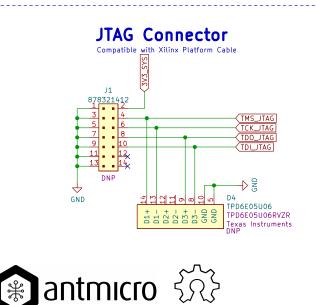
Follows Figure 2–14 7 Series FPGAs Configuration User Guide UG470 (v1.13.1)

## (Q)SPI flash

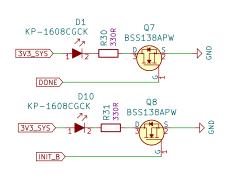


#### FPGA BANK 0



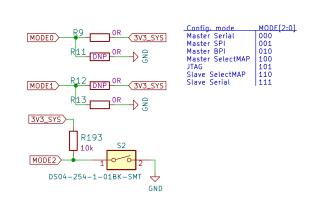


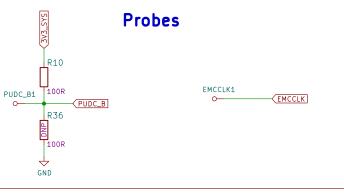
### STATUS LEDs



### **Configuration Modes**

For details, see UG470 p. 21





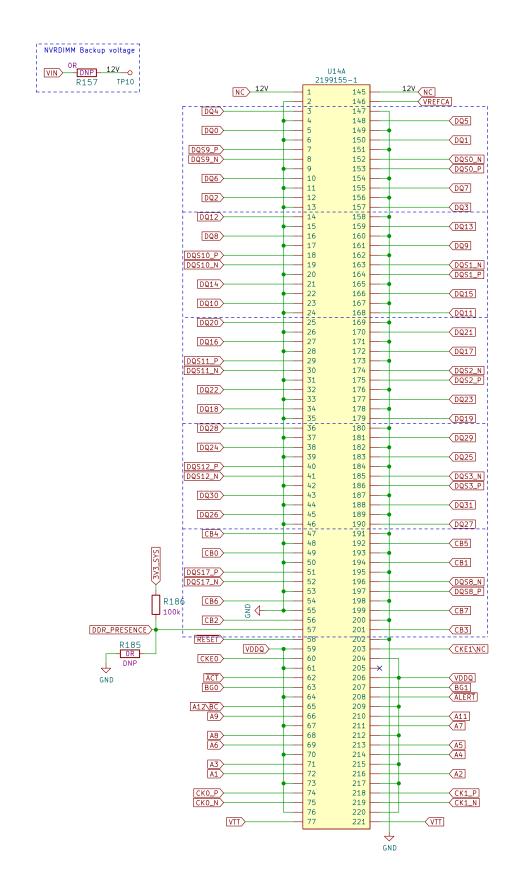
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File: config-spi.kicad\_sch

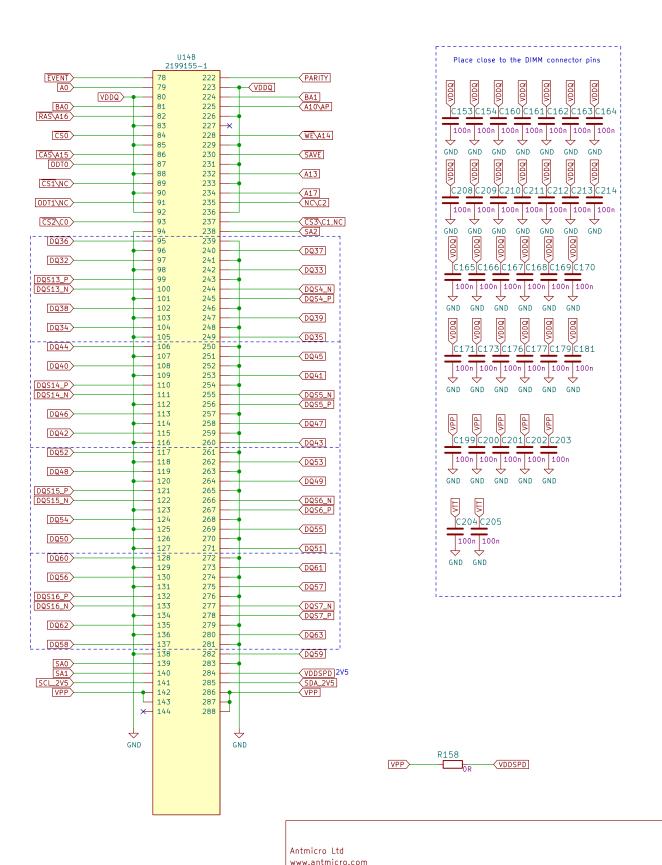
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 Size: A3
 Date: 2022-10-31
 Rev: 1.2.0

 KiCad E.D.A. eeschema 6.0.5+dfsg-1-bpo11+1
 Id: 3/12

#### DDR4 RDIMM connector





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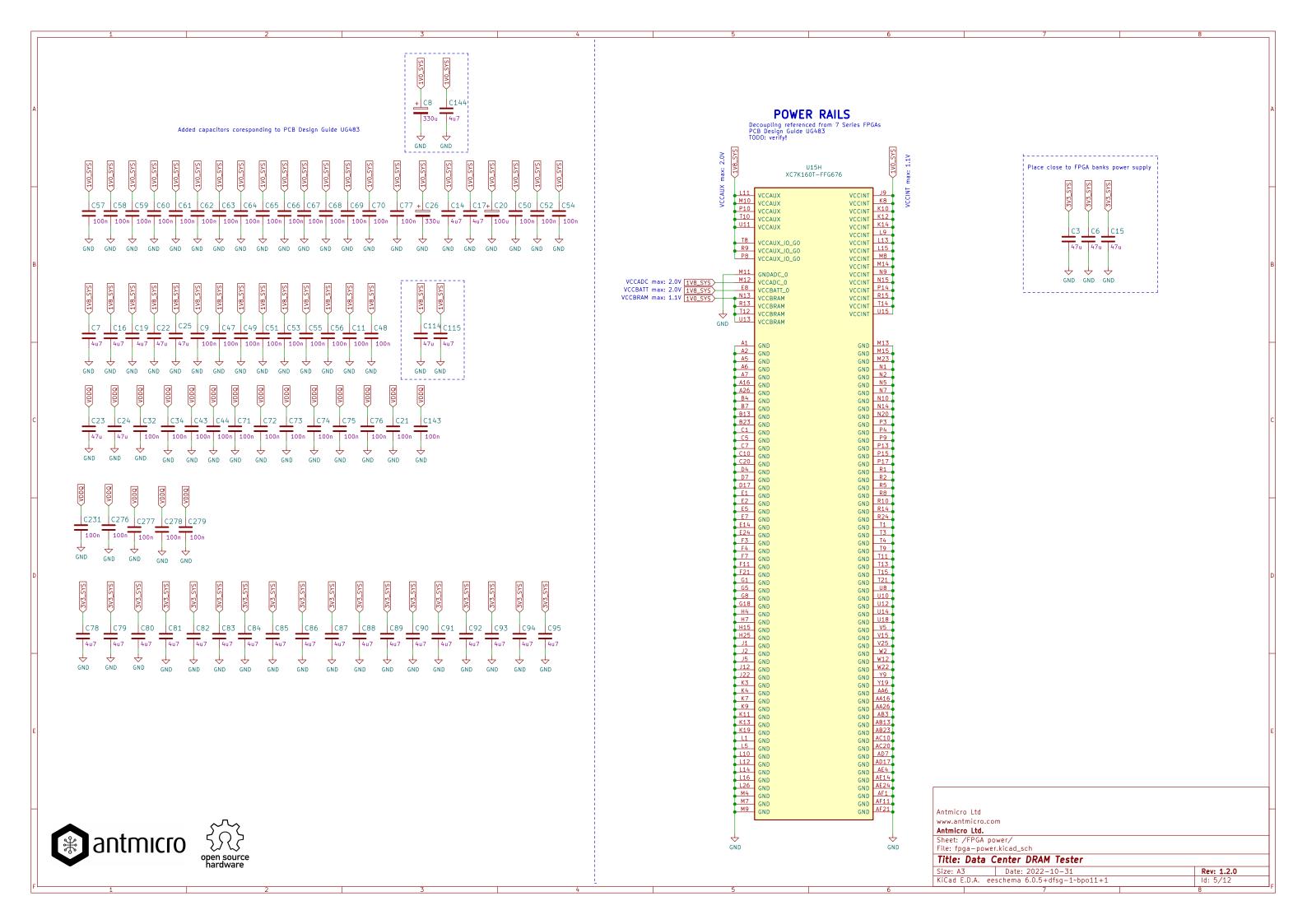
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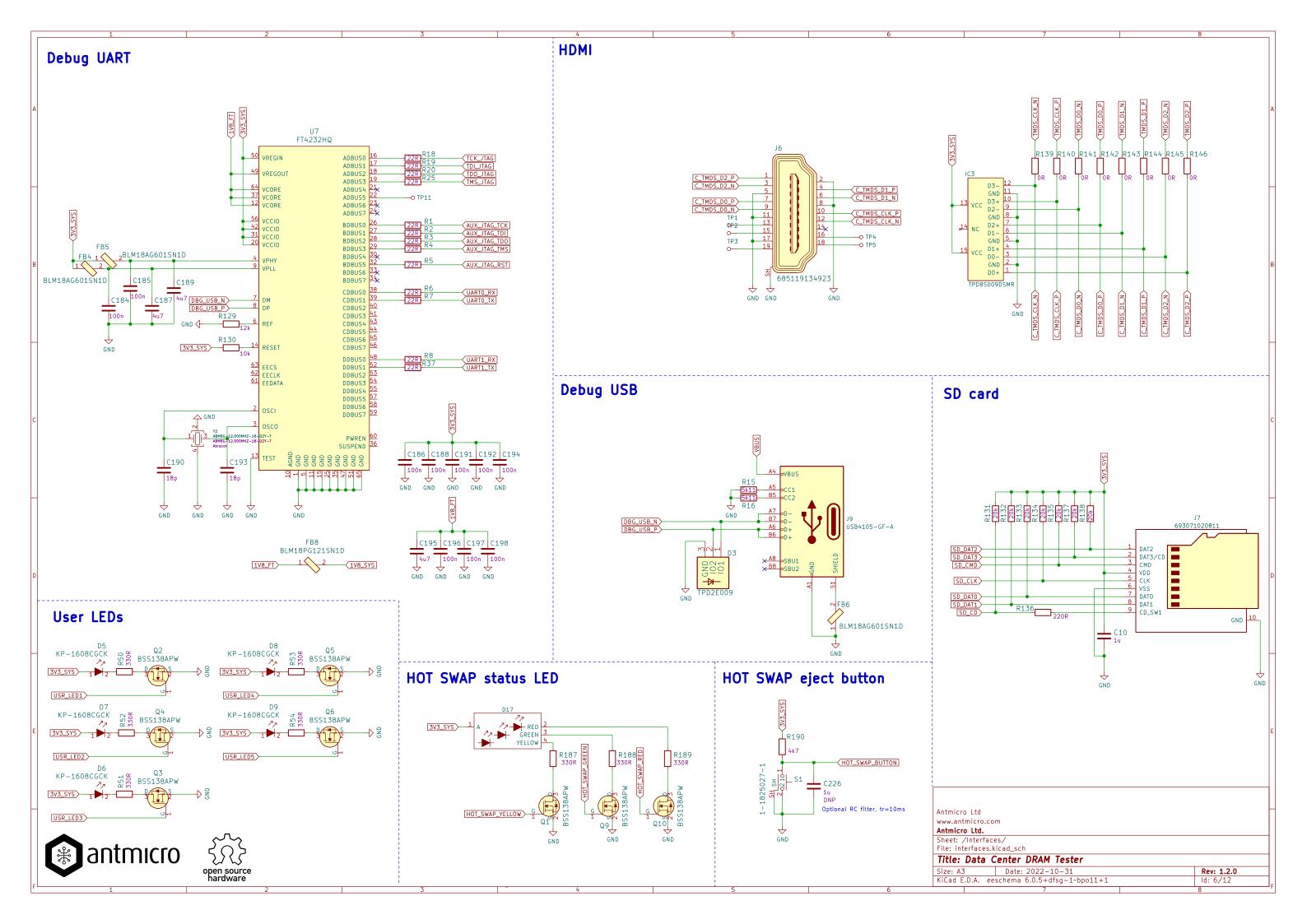
 Title:
 Data
 Center
 DRAM
 Tester

 Size:
 A3
 Date:
 2022-10-31

 KiCad
 E.D.A.
 eeschema
 6.0.5+dfsg-1-bpo11+1







BANK 12 **BANK 13** 

VCCO (HR banks) max: 3.6V IO\_0\_13 IO\_L1P\_T0\_13 U22 V22 K25 K26 0\_L1P\_T0\_12 O\_L1N\_T0\_12 IO\_L1N\_T0\_13 IO\_L2P\_T0\_12 IO\_L2N\_T0\_12 IO L2P TO 13 ETH\_RXD3 U25 V23 IO\_L2N\_T0\_13 P26 IO\_L3P\_T0\_DQS\_12
IO\_L3N\_T0\_DQS\_12 IO\_L3P\_T0\_DQS\_13 IO\_L3N\_T0\_DQS\_13 ETH\_TX\_EN U26 L25 P24 O\_L4P\_T0\_12 ETH\_RXD2 V26 ETH\_RXD1 W25 0 L4N T0 12 IO L4N TO 13 N26 D\_L5P\_T0\_12 IO\_L5P\_T0\_13 0 L5N T0 12 IO\_L5N\_T0\_13 D\_L6P\_T0\_12 IO\_L6P\_T0\_13 R25 W21 IO\_L6N\_T0\_VREF\_12 IO\_L7P\_T1\_12 IO\_L6N\_T0\_VREF\_13 IO\_L7P\_T1\_13 ETH\_MDC AA25 AB25 N19 M20 IO\_L7N\_T1\_12 IO\_L8P\_T1\_12 IO\_L7N\_T1\_13 IO\_L8P\_T1\_13 <u>W23</u> M24 D\_L8N\_T1\_12 IO\_L8N\_T1\_13 L24 P19 IO\_L9P\_T1\_DQS\_12 IO\_L9N\_T1\_DQS\_12 IO\_L9P\_T1\_DQS\_13 IO\_L9N\_T1\_DQS\_13 P20 O\_L10P\_T1\_12 O\_L10N\_T1\_12 IO\_L10P\_T1\_13 IO\_L10N\_T1\_13 M22 ETH\_TXD1 AA23
ETH\_REF\_CLK AB24
ETH\_TX\_CLK Y23
ETH\_TX\_CLK AA24
ETH\_TX\_CLK AA24
ETH\_TX\_CLX AA22
AC23
ETH\_RSTN AA22
AC23 O\_L11P\_T1\_SRCC\_12 O\_L11N\_T1\_SRCC\_12 IO\_L11P\_T1\_SRCC\_13 IO\_L11N\_T1\_SRCC\_13 N23 N21 \_L12P\_T1\_MRCC\_12 IO\_L12P\_T1\_MRCC\_13 IO\_L12N\_T1\_MRCC\_12 IO L12N T1 MRCC 13 D\_L13P\_T2\_MRCC\_12 IO\_L13P\_T2\_MRCC\_13 R21 CB6 IO\_L13N\_T2\_MRCC\_12 IO\_L14P\_T2\_SRCC\_12 IO L13N T2 MRCC 13 IO\_L14P\_T2\_SRCC\_13 R22 CB2 HR\_RST AC24 W20 ETH\_TXD3 Y21 HR\_RW AD23 HR\_DQ7 AD24 AB22 R23 IO\_L14N\_T2\_SRCC\_12 IO\_L15P\_T2\_DQS\_12 IO\_L14N\_T2\_SRCC\_13 IO\_L15P\_T2\_DQS\_13 T25 D\_L15N\_T2\_DQS\_12 IO\_L15N\_T2\_DQS\_13 T20 R20 IO L16P T2 12 IO L16P T2 13 D\_L16N\_T2\_12 IO\_L16N\_T2\_13 CB7 IO\_L17P\_T2\_12 IO\_L17N\_T2\_12 IO\_L17P\_T2\_13 AC22 T23 IO\_L17N\_T2\_13 AB21 U19 IO\_L18P\_T2\_12 IO\_L18N\_T2\_12 IO 118P T2 13 AC21 U20 T18 IO\_L18N\_T2\_13 AD21 IO\_L19P\_T3\_12 IO\_L19N\_T3\_VREF\_12 IO\_L19P\_T3\_13 CB0 HR\_DQ2 AF24
HR\_DQ5 AF25
HR\_CKP AD26 T19 P16 IO 119N T3 VRFF 13 IO\_L20P\_T3\_12 0\_L20N\_T3\_12 IO\_L20N\_T3\_13 O\_L21P\_T3\_DQS\_12 IO\_L21P\_T3\_DQS\_13 R16 HR\_CKP AB26
HR\_CKN AE26
HR\_DQ0 AE23
HR\_DQ4 AF23
HR\_DQ1 AD25
HR\_DQ6 AE25 IO\_L21N\_T3\_DQS\_12 IO\_L22P\_T3\_12 IO\_L21N\_T3\_DQS\_13 IO\_L22P\_T3\_13 N18 M19 IO\_L22N\_T3\_12 IO\_L23P\_T3\_12 IO\_L22N\_T3\_13 U17 IO\_L23P\_T3\_13 CB1 CB4 D\_L23N\_T3\_12 IO\_L23N\_T3\_13 AE22 R18 IO\_L24P\_T3\_12 IO\_L24N\_T3\_12

> U15A XC7K160T-FFG676 antmicro-footprints:xc7k160tfbg676

IO\_L24P\_T3\_13

IO\_L24N\_T3\_13

10\_25\_13

P18

CB5

**BANK 14** 

**BANK 15** 

VCCO (HR banks) max: 3.6V O\_L1P\_T0\_D00\_M0SI\_14 IO\_L1P\_TO\_ADOP\_15 O\_L1N\_T0\_D01\_DIN\_14 O\_L2P\_T0\_D02\_14 IO\_L1N\_TO\_ADON\_15 \_L2N\_T0\_D03\_14 IO\_L2N\_T0\_AD8N\_15 O L3P TO DQS PUDC B 14 IO L3P TO DQS AD1P 15 \_L3N\_T0\_DQS\_EMCCLK\_14 IO\_L3N\_TO\_DQS\_AD1N\_15 O L4P TO D04 14 IO L4P TO AD9P 15 O\_L4N\_T0\_D05\_14 IO\_L4N\_T0\_AD9N\_15 0 L5P T0 D06 14 IO L5P TO AD2P 15 0\_L5N\_T0\_D07\_14 IO\_L5N\_TO\_AD2N\_15 IO\_L6P\_T0\_15 IO\_L6N\_T0\_VREF\_15 O\_L6P\_T0\_FCS\_B\_14 O L6N TO D08 VREF 14 \_L7P\_T1\_D09\_14 IO\_L7P\_T1\_AD10P\_15 IO L7N T1 AD10N 15 O L7N T1 D10 14 O\_L8P\_T1\_D11\_14 IO\_L8P\_T1\_AD3P\_15 O\_L8N\_T1\_D12\_14 IO\_L8N\_T1\_AD3N\_15 O\_L9P\_T1\_DQS\_14 IO\_L9P\_T1\_DQS\_AD11P\_15 O\_L9N\_T1\_DQS\_D13\_14 O\_L10P\_T1\_D14\_14 IO\_L9N\_T1\_DQS\_AD11N\_15 IO\_L10P\_T1\_AD4P\_15 O\_L10N\_T1\_D15\_14 IO\_L10N\_T1\_AD4N\_15 IO 111P T1 SRCC AD12P 15 0 I 11P T1 SRCC 14 AUX\_JTAG\_TDI F22 \_L11N\_T1\_SRCC\_14 IO\_L11N\_T1\_SRCC\_AD12N\_15 0\_L12P\_T1\_MRCC\_14 IO\_L12P\_T1\_MRCC\_AD5P\_15 \_E23 0\_L12N\_T1\_MRCC\_14 IO\_L12N\_T1\_MRCC\_AD5N\_15 \_G22 IO\_L13P\_T2\_MRCC\_14 IO\_L13N\_T2\_MRCC\_14 IO\_L13P\_T2\_MRCC\_15 IO\_L13N\_T2\_MRCC\_15 F23 G24 0\_L14P\_T2\_SRCC\_14 IO\_L14P\_T2\_SRCC\_15 F24 0\_L14N\_T2\_SRCC\_14 IO\_L14N\_T2\_SRCC\_15 SCL\_3V3 E25
AUX\_JTAG\_TMS D25
AUX\_JTAG\_RST G25
G26 O\_L15P\_T2\_DQS\_RDWR\_B\_14 IO\_L15P\_T2\_DQS\_15 IO\_L15N\_T2\_DQS\_DOUT\_CSO\_B\_14 IO\_L16P\_T2\_CSI\_B\_14 IO\_L15N\_T2\_DQS\_ADV\_B\_15 IO\_L16P\_T2\_A28\_15 O\_L16N\_T2\_A15\_D31\_14 O\_L17P\_T2\_A14\_D30\_14 IO\_L16N\_T2\_A27\_15 IO\_L17P\_T2\_A26\_15 UARTO\_RX F25 UARTO\_TX E26
UARTO\_TX J26
H26 O\_L17N\_T2\_A13\_D29\_14 O\_L18P\_T2\_A12\_D28\_14 O\_L18N\_T2\_A11\_D27\_14 IO\_L17N\_T2\_A25\_15 IO\_L18P\_T2\_A24\_15 IO\_L18N\_T2\_A23\_15 H21 G21 O\_L19P\_T3\_A10\_D26\_14 IO L19P T3 A22 15 O\_L19N\_T3\_A09\_D25\_VREF\_14 IO\_L19N\_T3\_A21\_VREF\_15 H23 O\_L20P\_T3\_A08\_D24\_14 IO\_L20P\_T3\_A20\_15 H24 O\_L20N\_T3\_A07\_D23\_14 IO\_L20N\_T3\_A19\_15 J19 J21 O\_L21P\_T3\_DQS\_14 O\_L21N\_T3\_DQS\_A06\_D22\_14 IO\_L21P\_T3\_DQS\_15 IO\_L21N\_T3\_DQS\_A18\_15 H22 J24 IO\_L22P\_T3\_A17\_15 IO\_L22N\_T3\_A16\_15 O\_L22P\_T3\_A05\_D21\_14 \_\_<u>J25</u> \_\_<u>L22</u> 0 122N T3 A04 D20 14 )\_L23P\_T3\_A03\_D19\_14 IO\_L23P\_T3\_F0E\_B\_15 K22 K23 O\_L23N\_T3\_A02\_D18\_14 IO\_L23N\_T3\_FWE\_B\_15 IO\_L24P\_T3\_RS1\_15 O\_L24P\_T3\_A01\_D17\_14 J23 O\_L24N\_T3\_A00\_D16\_14 O\_25\_14 IO\_L24N\_T3\_RS0\_15

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ETH\_INT\_N Y20

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Sheet: /FPGA banks 12-15/ File: fpga-banks-12-15.kicad\_sch

Title: Data Center DRAM Tester

Size: A3 Date: 2022-10-31
KiCad E.D.A. eeschema 6.0.5+dfsg-1~bpo11+1

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