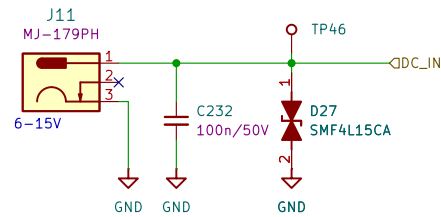
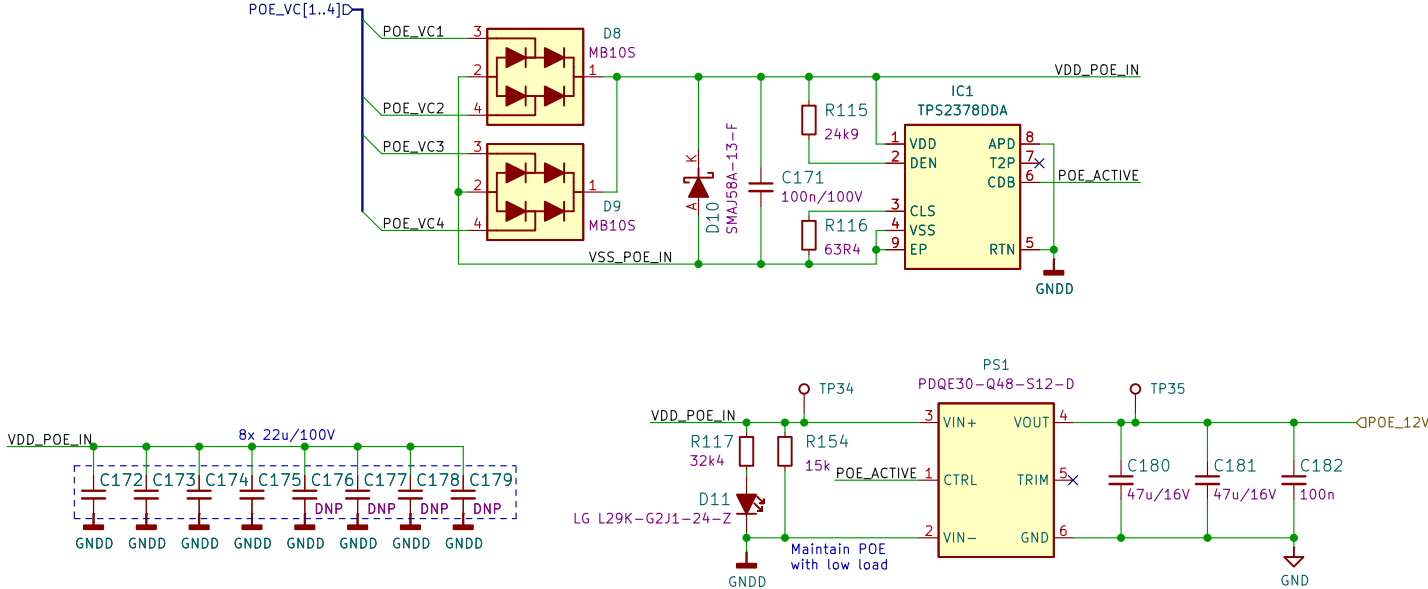


Id: 3/19



PoE PD



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Sheet: /Power Supply/PoE/
File: PoE.kicad_sch

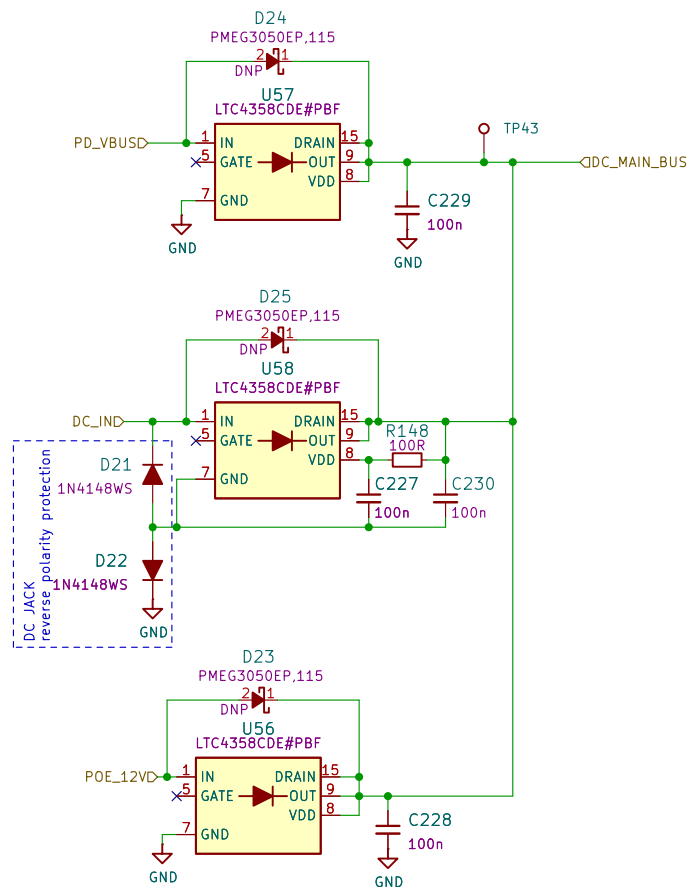
Title: Kria K26 Devboard

Size: A4 Date: 2023-07-27

KiCad E.D.A. kicad 6.0.11+dfsg-1

Rev: 1.2.1

Id: 5/19



The image displays a detailed PCB layout for three power domains: SOM 5V, PS domain, and PL domain. Each domain is represented by a yellow-shaded area containing a buck converter circuit.

- SOM 5V Domain:** Features two buck converters, U47 and U48, both using the RT6236AHGQUF IC. U47 converts DC_MAIN_BUSD to USB_5V, and U48 converts DC_MAIN_BUSD to SOM_5V. Both converters include input capacitors (C183, C185, C186, C187, C188, C189), feedback capacitors (C191, C192, C193, C194), and output capacitors (C195, C197, C199, C196, C198, C200). Test points TP51 and TP50 are located at the outputs.
- PS domain:** Contains four buck converters, U49, U50, U51, and U52, all using the AP62301WU-7 IC. They convert VCCOEN_PS_M2CD to PS_3V3, PS_2V5, PS_1V8, and PS_1V2 respectively. Each converter includes input capacitors (C201, C202, C203, C204), feedback capacitors (C206, C207, C208, C209), and output capacitors (C211, C212, C213, C214, C215, C216, C217, C218). Test points TP36, TP37, TP38, and TP39 are located at the outputs.
- PL domain:** Contains two buck converters, U54 and U55, both using the AP62301WU-7 IC. They convert VCCOEN_PL_M2CD to PL_3V3 and PL_1V2 respectively. Each converter includes input capacitors (C219, C220), feedback capacitors (C221, C222), and output capacitors (C223, C224, C225, C226). Test points TP41 and TP42 are located at the outputs.

Additional components include resistors (R118, R119, R122, R123, R124, R125, R131, R132, R133, R134, R135, R136, R137, R138, R140, R144, R145, R146, R147, R156, R157, R158, R159, R160, R161, R162, R163, R164, R165, R166), inductors (L1, L2, L3, L4, L5, L6, L7, L8, L9), and diodes (D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, D32, D33, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, D49, D50, D51, D52, D53, D54, D55, D56, D57, D58, D59, D60, D61, D62, D63, D64, D65, D66, D67, D68, D69, D70, D71, D72, D73, D74, D75, D76, D77, D78, D79, D80, D81, D82, D83, D84, D85, D86, D87, D88, D89, D90, D91, D92, D93, D94, D95, D96, D97, D98, D99, D100). The layout also shows various test points (TP51, TP50, TP36, TP37, TP38, TP39, TP41, TP42) and output labels (USB_5V, SOM_5V, PS_3V3, PS_2V5, PS_1V8, PS_1V2, PL_3V3, PL_1V2).

Power indication

SOM_5V_OUT R120 2k2 D12 LG L29K-G2J1-24-Z

USB_5V_OUT R121 2k2 D13 LG L29K-G2J1-24-Z

PS_3V3_OUT R126 1k D14 LG L29K-G2J1-24-Z

PS_2V5_OUT R128 510R D15 LG L29K-G2J1-24-Z

PL_3V3_OUT R142 1k D19 LG L29K-G2J1-24-Z

PS_3V3_OUT R129 1k D16 LG L29K-G2J1-24-Z

PS_3V3_OUT R130 1k D17 LG L29K-G2J1-24-Z

PS_2V5_OUT R141 510R D18 LG L29K-G2J1-24-Z

PL_3V3_OUT R143 1k D20 LG L29K-G2J1-24-Z

PS_1V8_OUT B 1 10k Q18 DTC014TEBTL

PS_1V2_OUT B 1 10k Q13 DTC014TEBTL

PS_1V0_OUT B 1 10k Q14 DTC014TEBTL

PL_1V2_OUT B 1 10k Q15 DTC014TEBTL

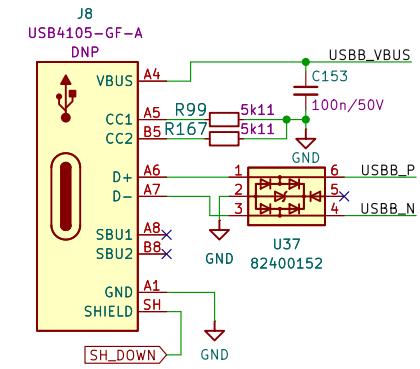
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Sheet: /Power Supply/DC/DC converters/
File: dc-dc-converters.kicad_sch

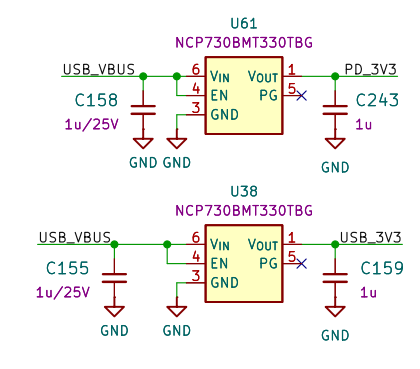
Title: Kria K26 Devboard

Size: A3	Date: 2023-07-27	Rev: 1.2.1
KiCad E.D.A. kicad 6.0.11+dfsg-1		Id: 7/19

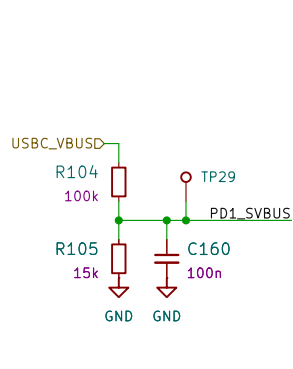
Optional debug USB



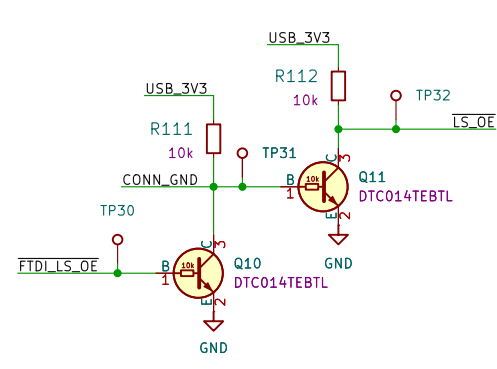
Supply



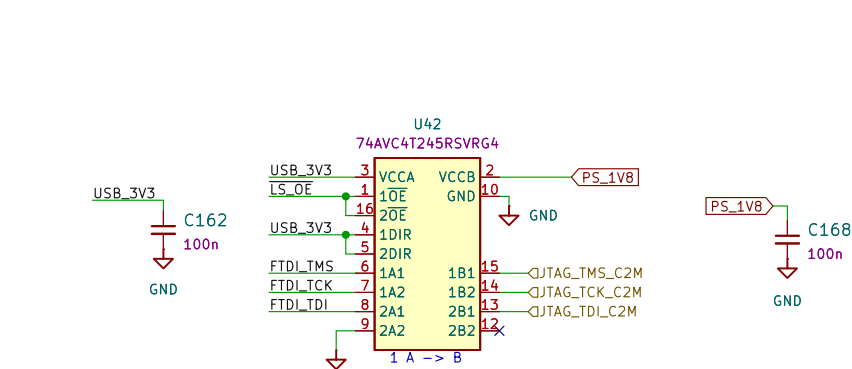
USB-C VBUS voltage divider



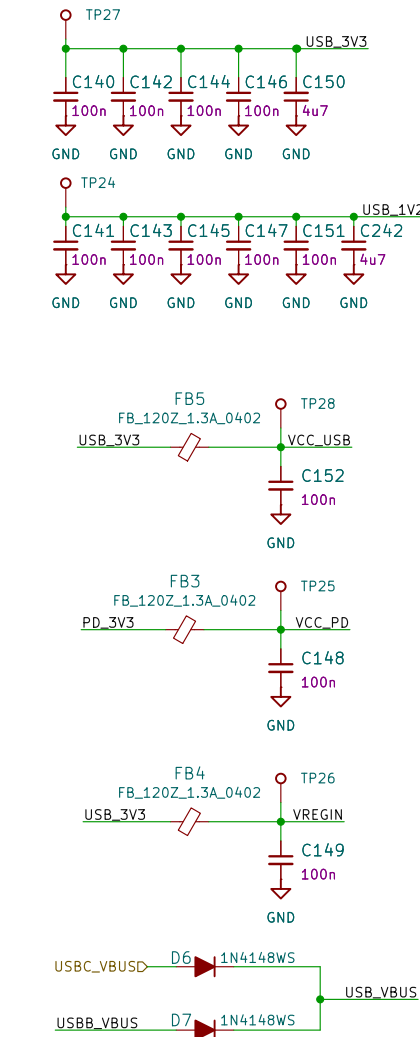
Logic level conversion enable



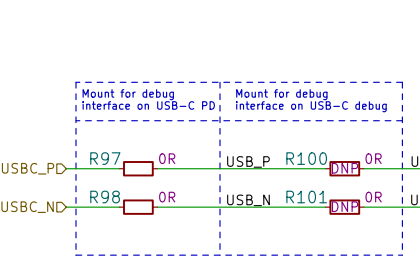
Logic level conversion



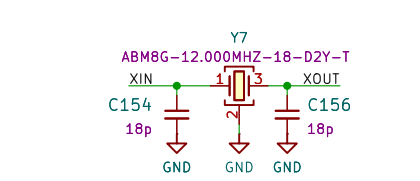
Decoupling and Filtering



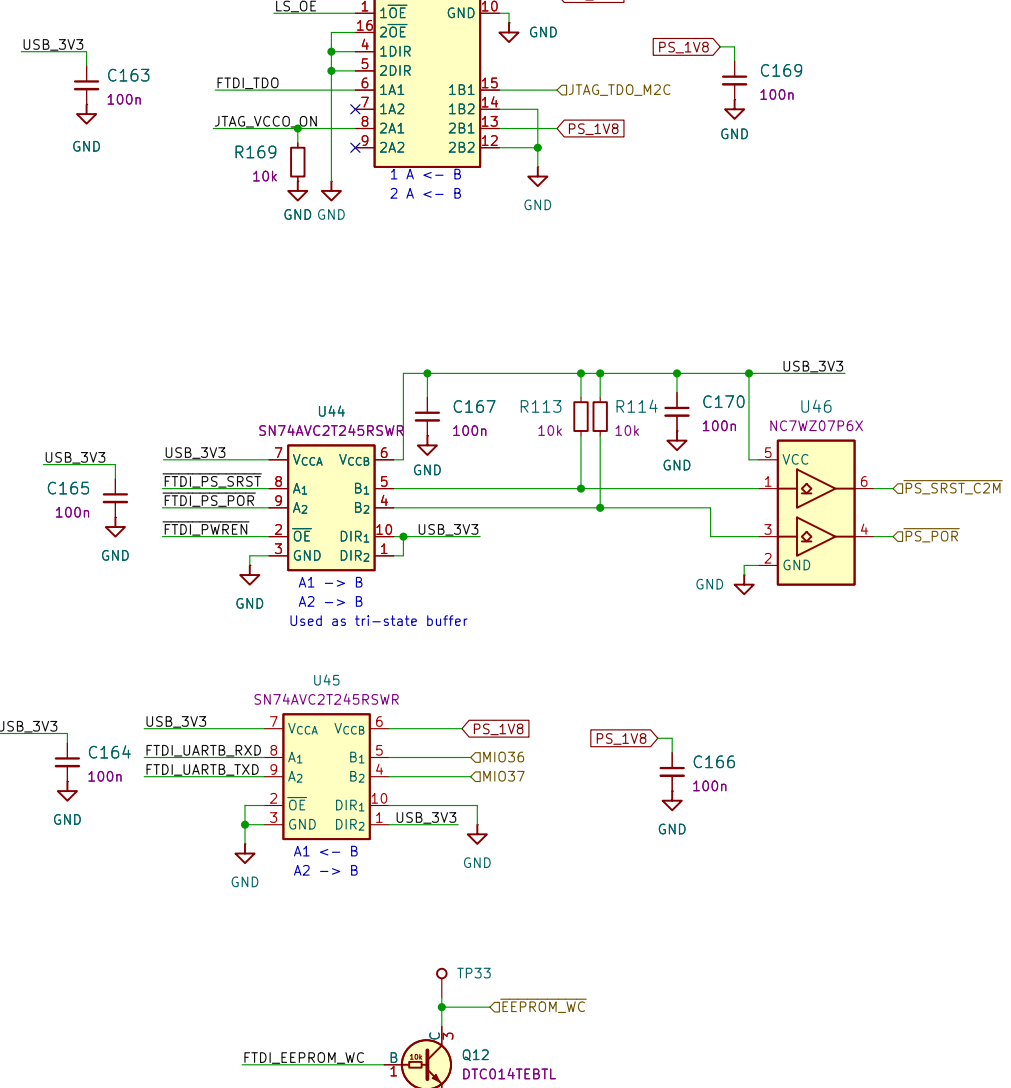
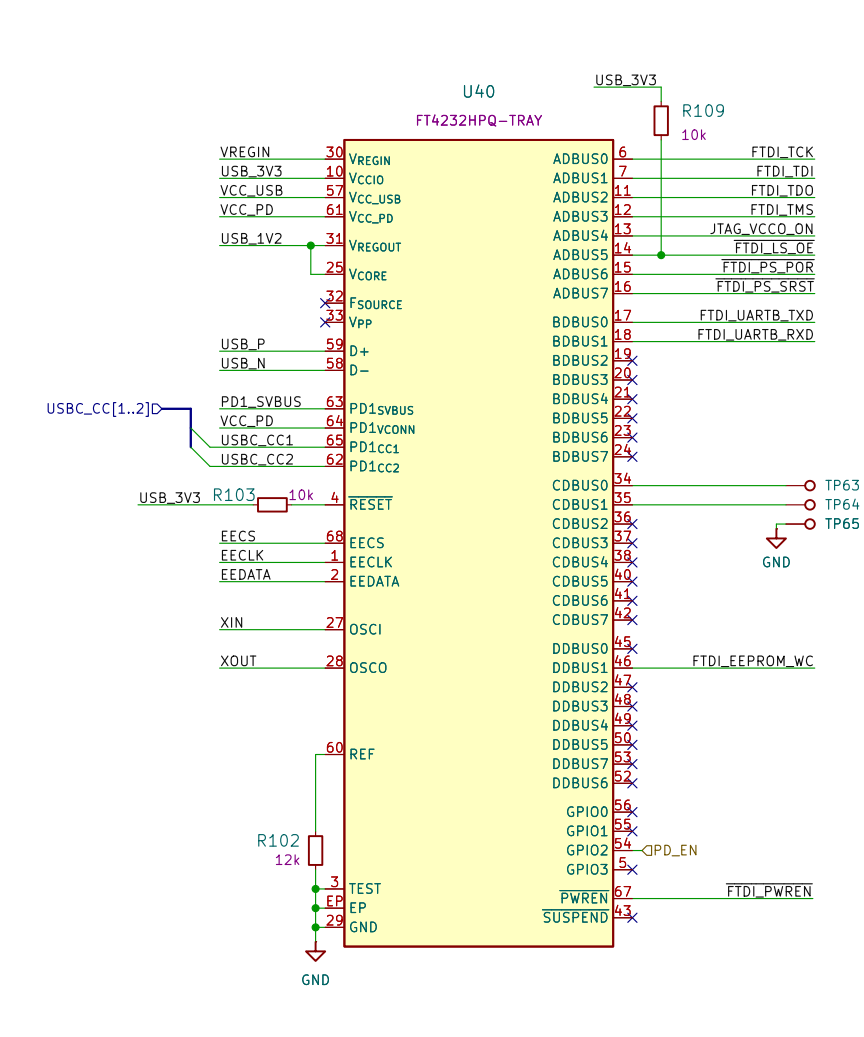
Connector configuration



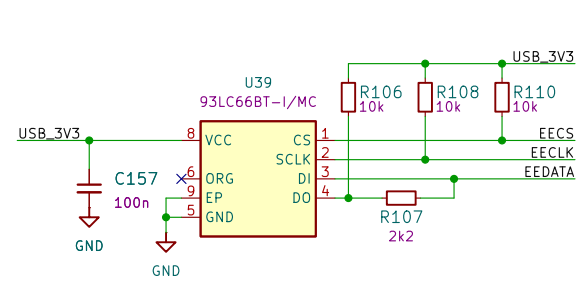
Crystal



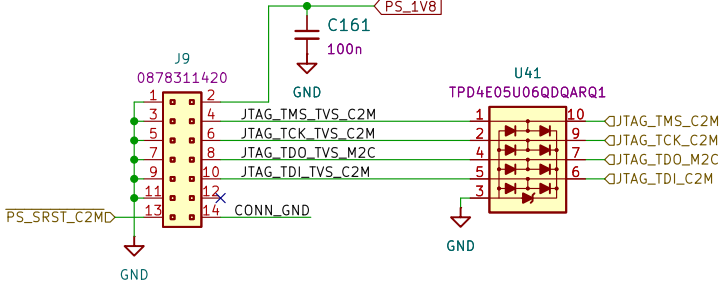
FTDI



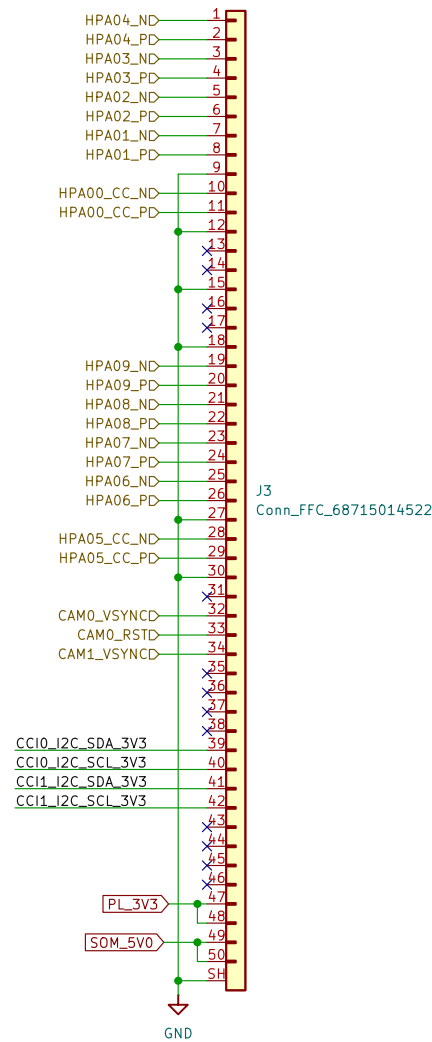
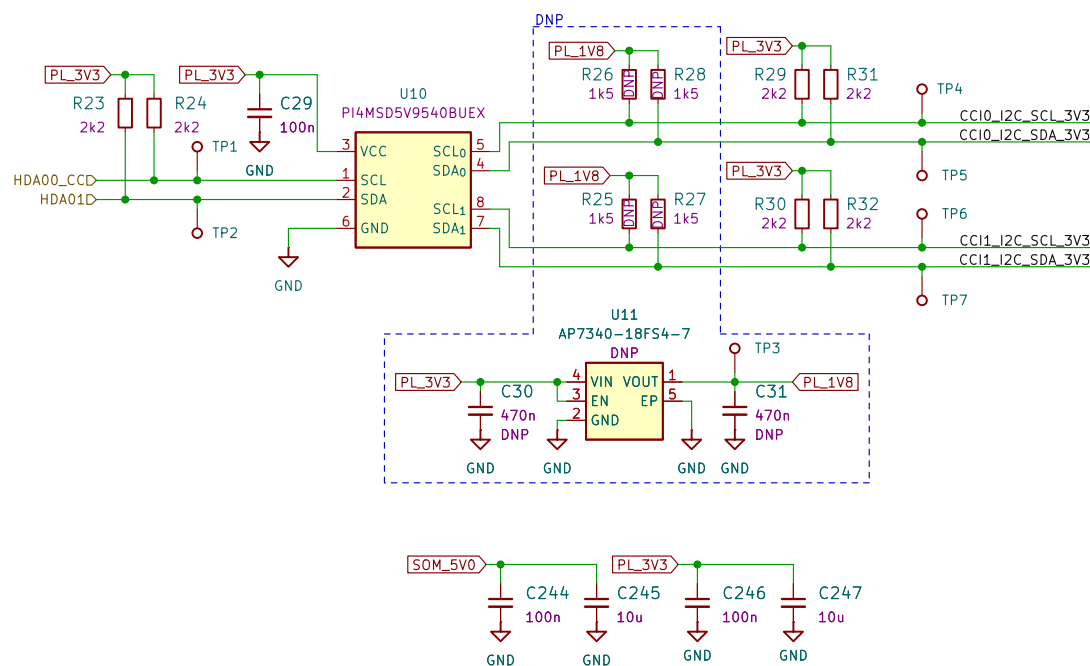
EEPROM



JTAG connector

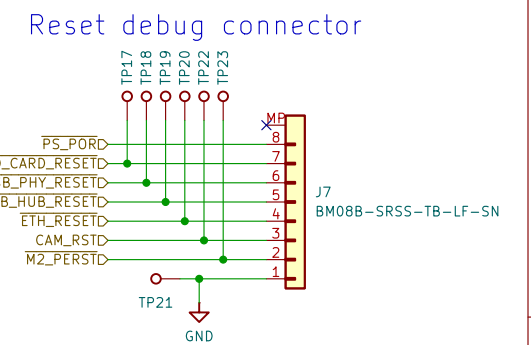
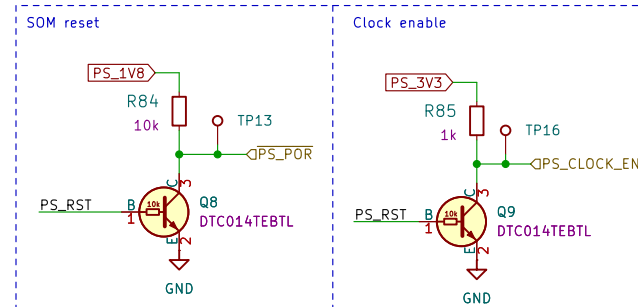
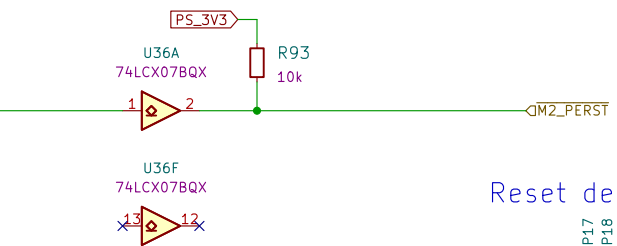
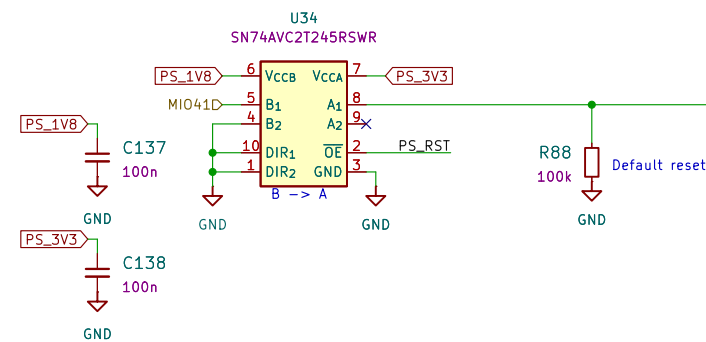
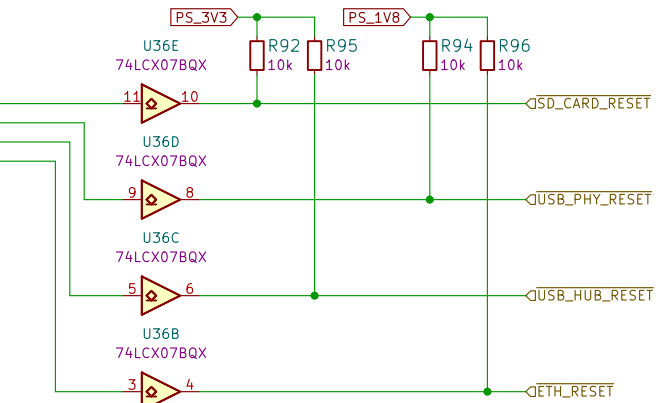
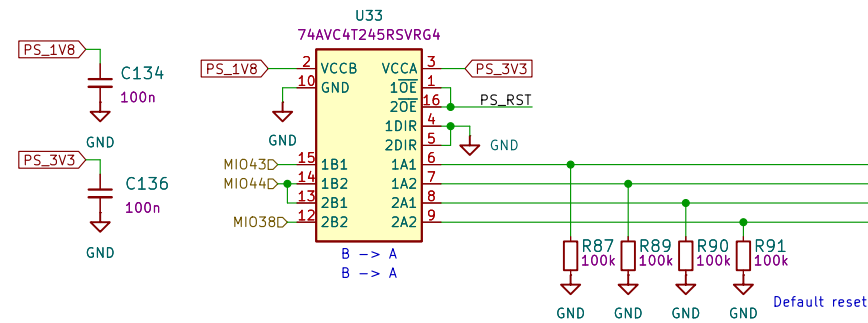


Camera interface

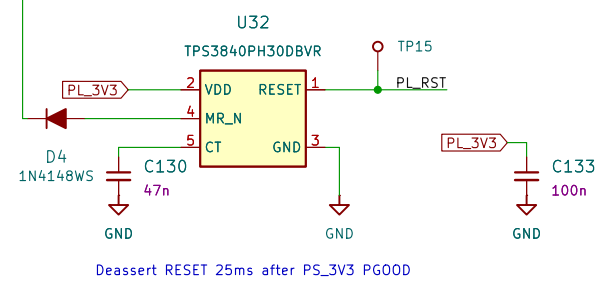
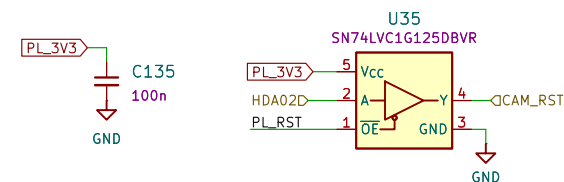


A
B
C
D
E
F

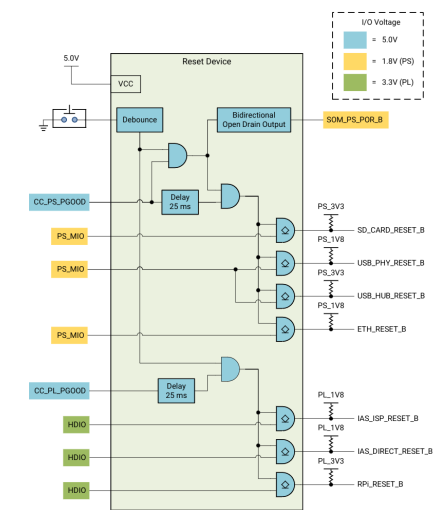
Logic level conversion enabled by voltage supervisor



Xilinx reference



R86
OR
HDA02D DNF CAM_RST

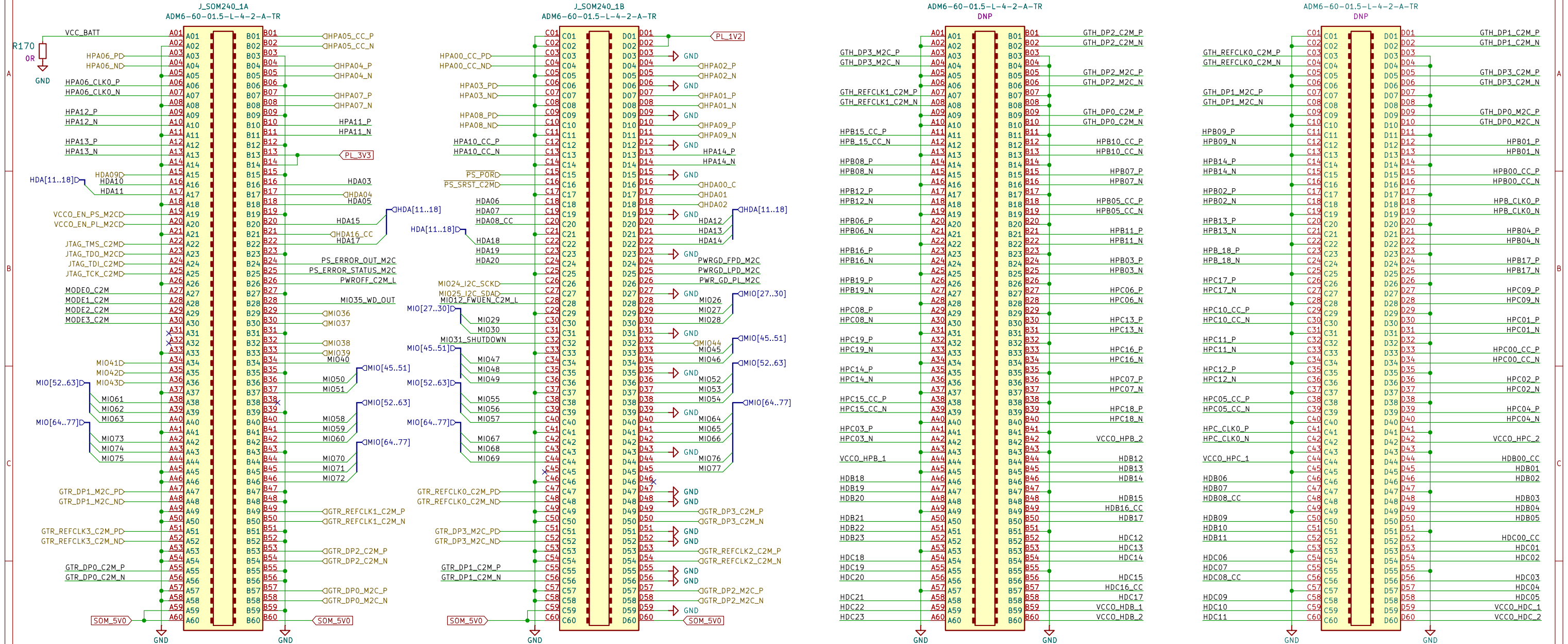


Rev: 1.2.1

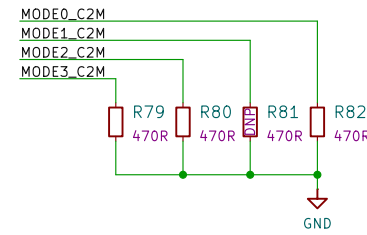
Id: 10/19



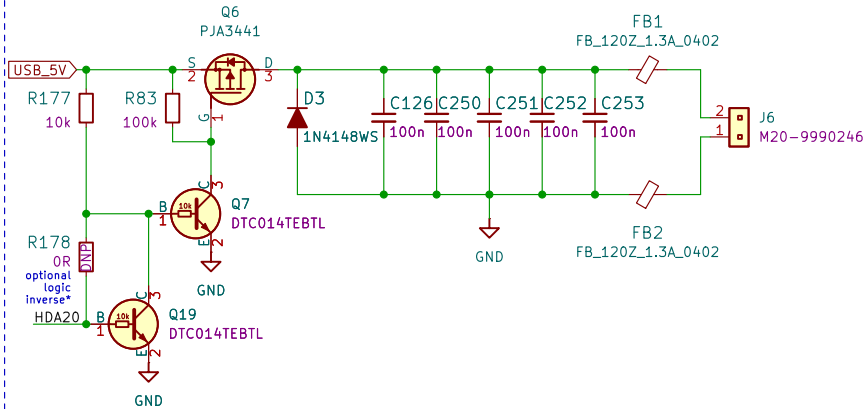
SOM K26 B2B connectors



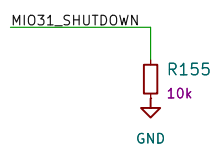
BOOT MODE: QUAD-SPI



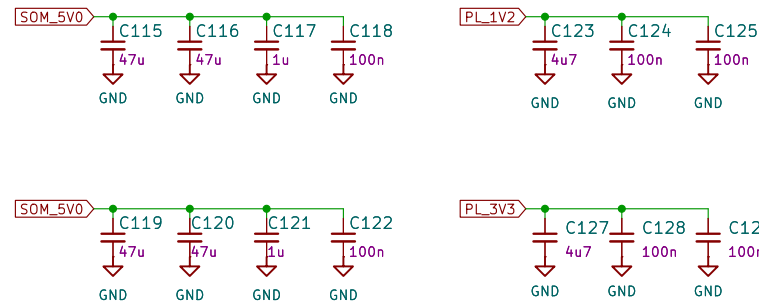
5V Fan header



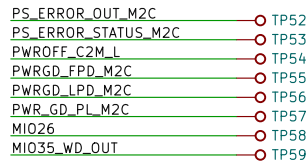
SHUTDOWN pull-down



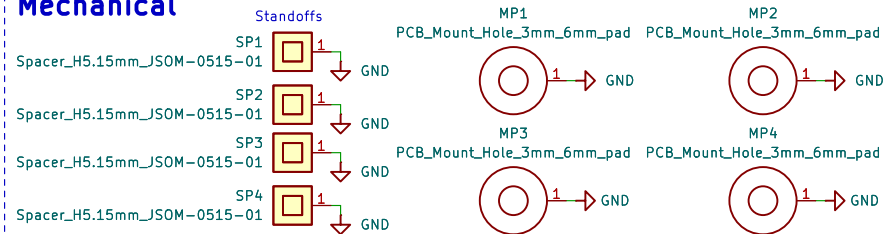
SOM decoupling



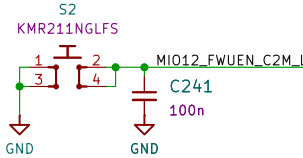
Test points



Mechanical



FWUEN Button



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Sheet: /Xilinx K26 SOM/
File: k26_som.kicad_sch

Title: Kria K26 Devboard

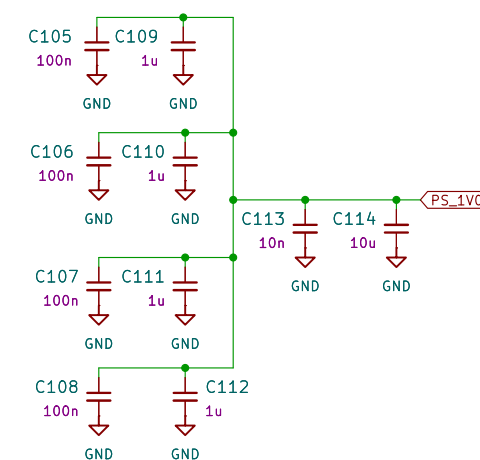
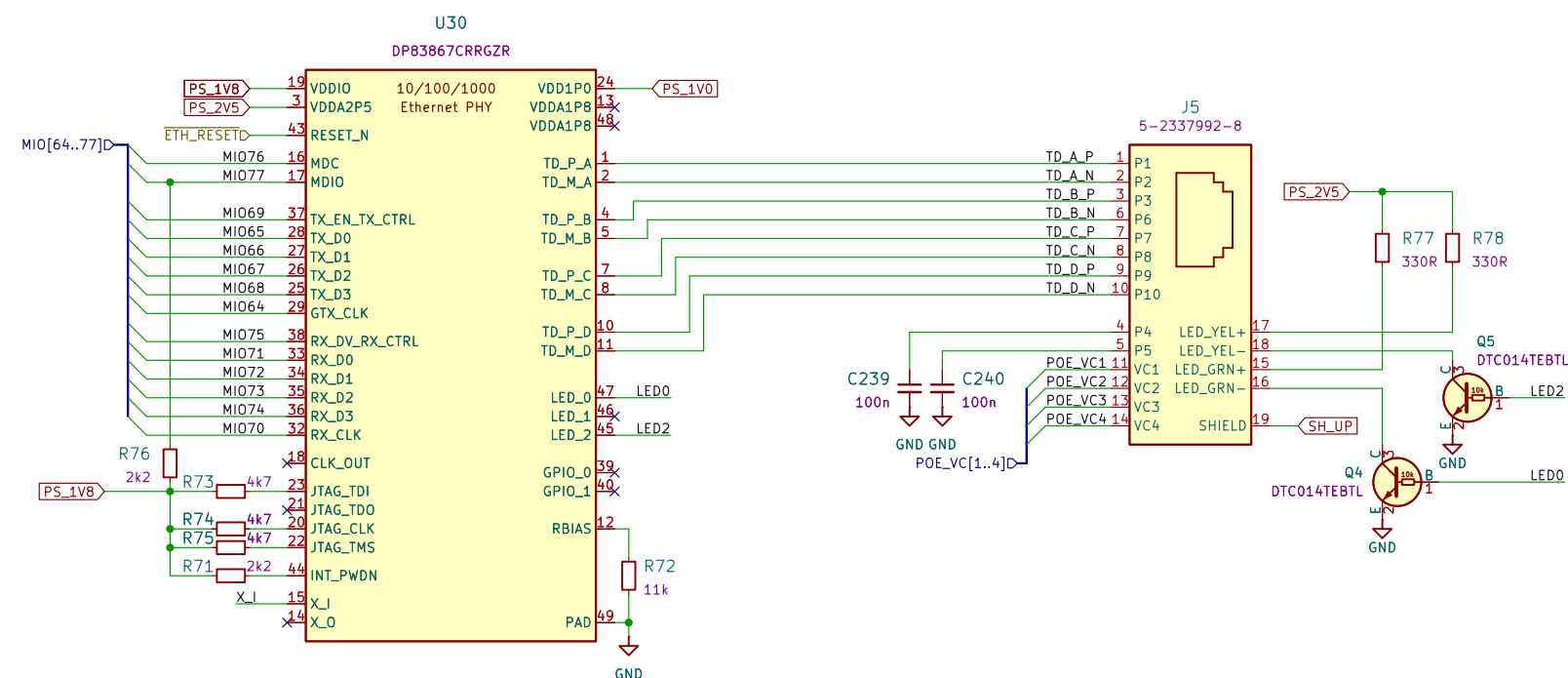
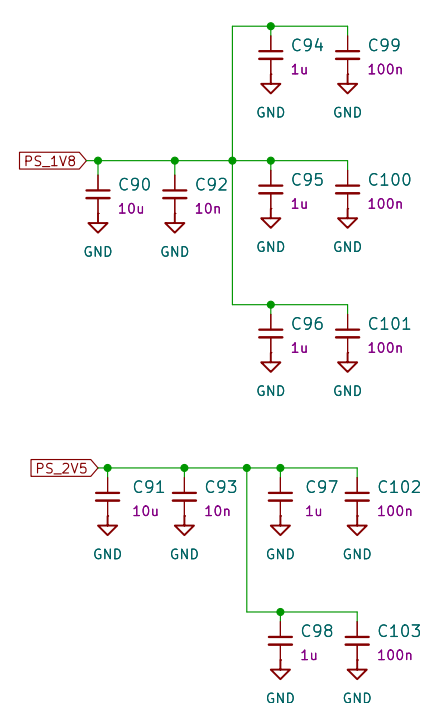
Size: A3 Date: 2023-07-27

KiCad E.D.A. kicad 6.0.11+dfsg-1

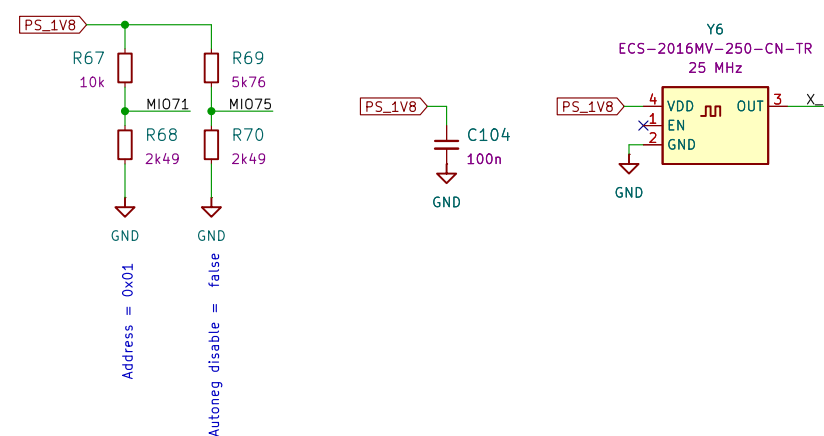
Rev: 1.2.1

Id: 11/19

ETH0 – PD PoE



Strap Configuration



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Sheet: /Ethernet/
File: eth.kicad_sch

Title: Kria K26 Devboard

Size: A3	Date: 2023-07-27
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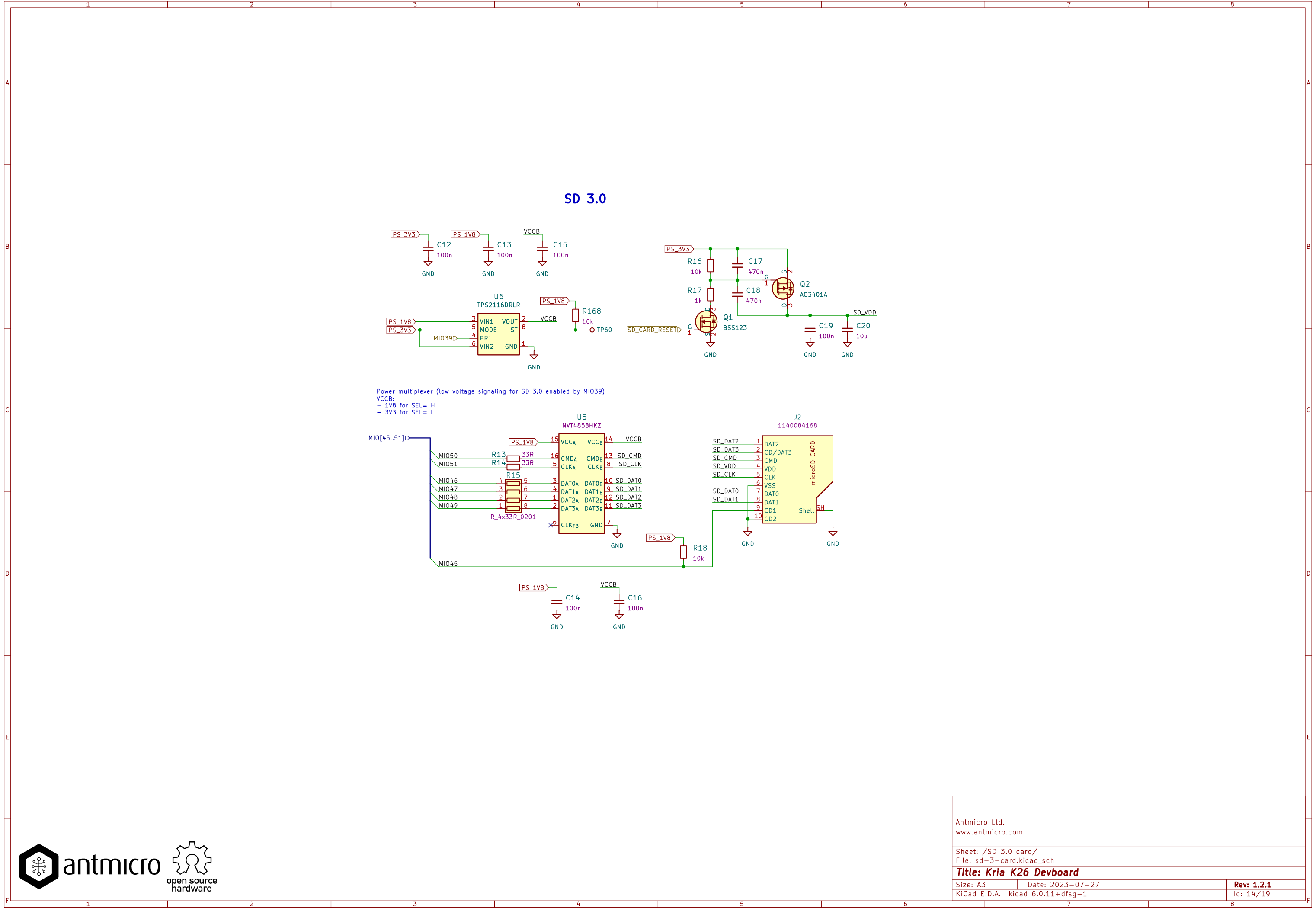
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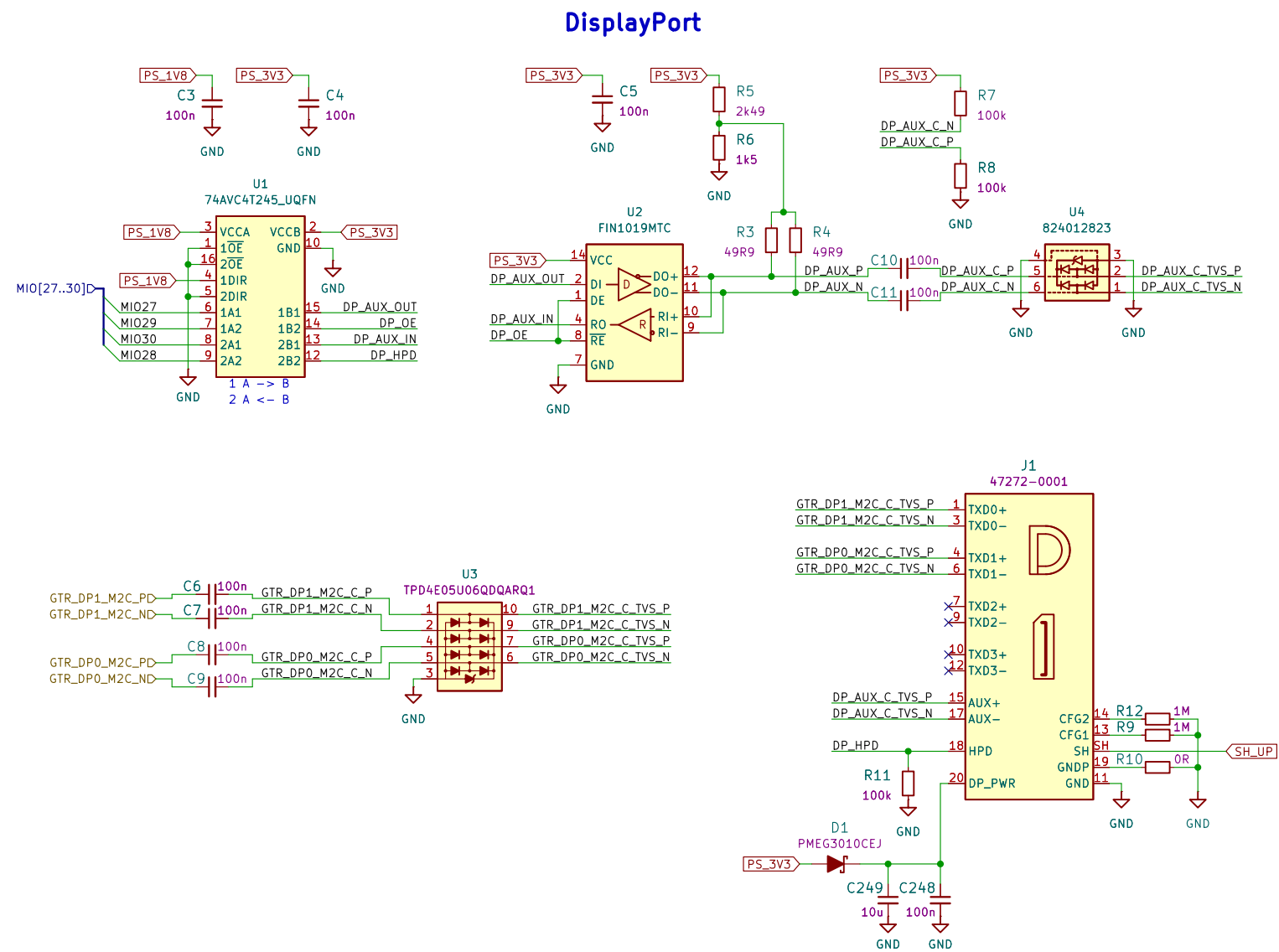
Rev: 1.2.1

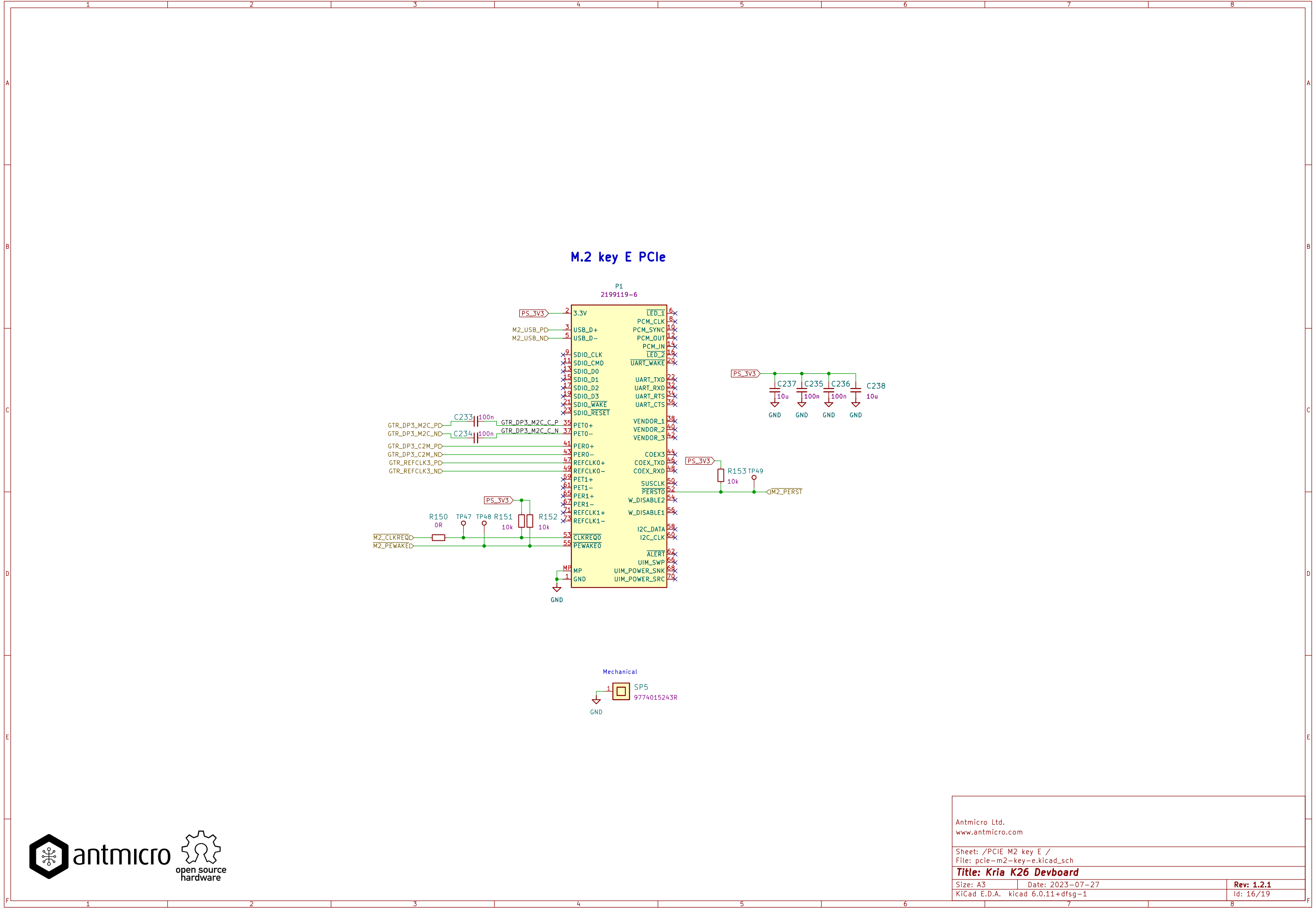
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NOTE:

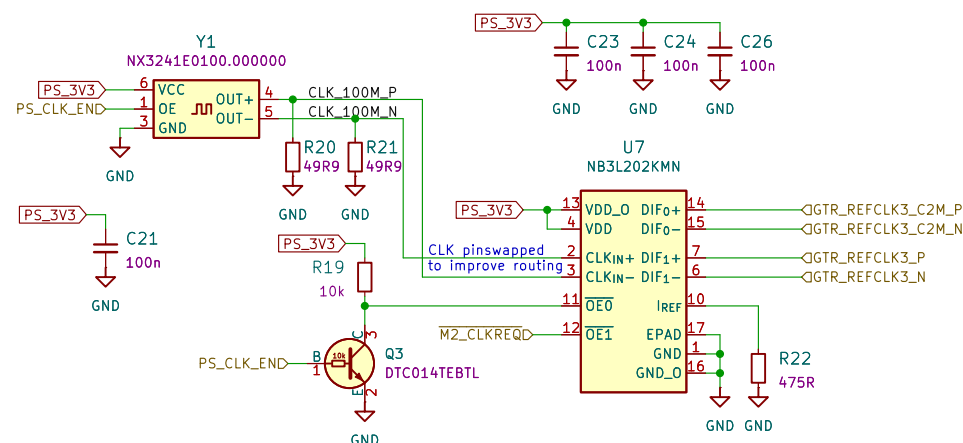
CLK is matched to data lanes, the device tree should use "rgmii-id"



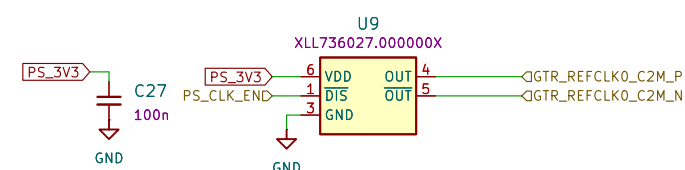




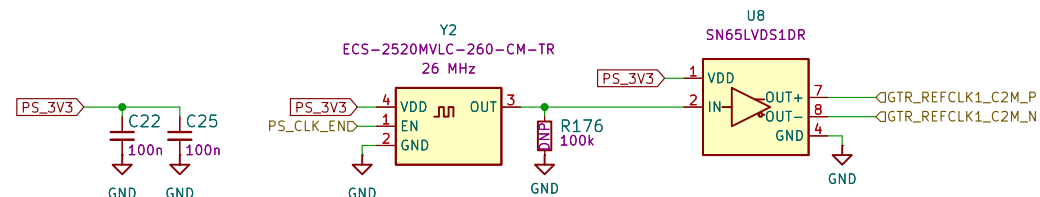
PCIe GTH REFCLK: 2x100MHz HCSL



DisplayPort GTH REFCLK: 27MHz LVDS



USB GTH REFCLK: 26MHz LVDS



ETH GTH REFCLK: 125MHz LVDS

