

A

A

B

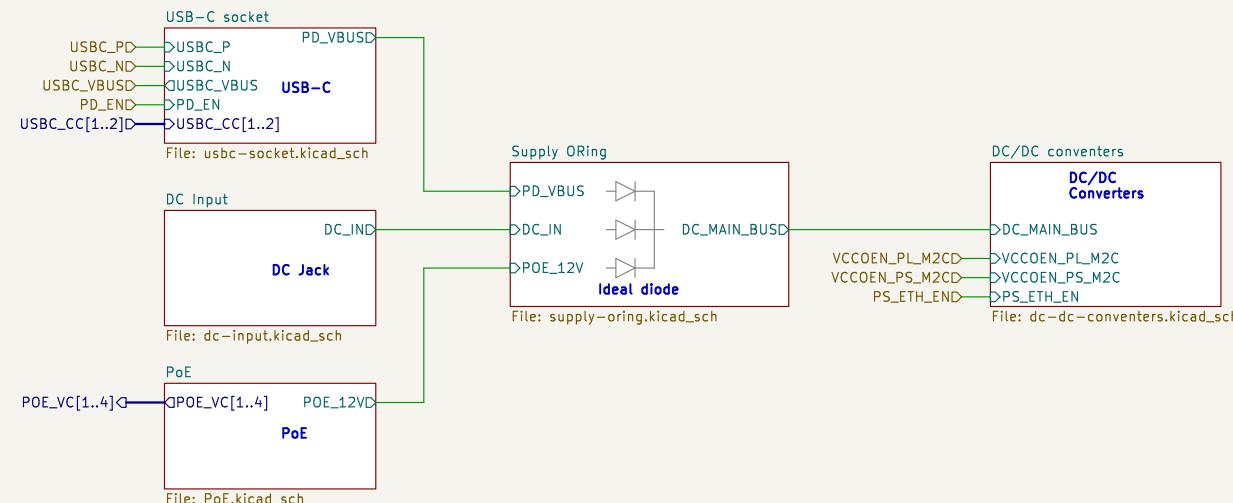
B

C

C

D

D



Antmicro Ltd.  
www.antmicro.com

Sheet: /Power Supply/  
File: supply.kicad\_sch

**Title: Kria K26 Devboard**

Size: A4 | Date: 2023-11-02  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 1.2.4:b5051  
Id: 2/19

A

A

B

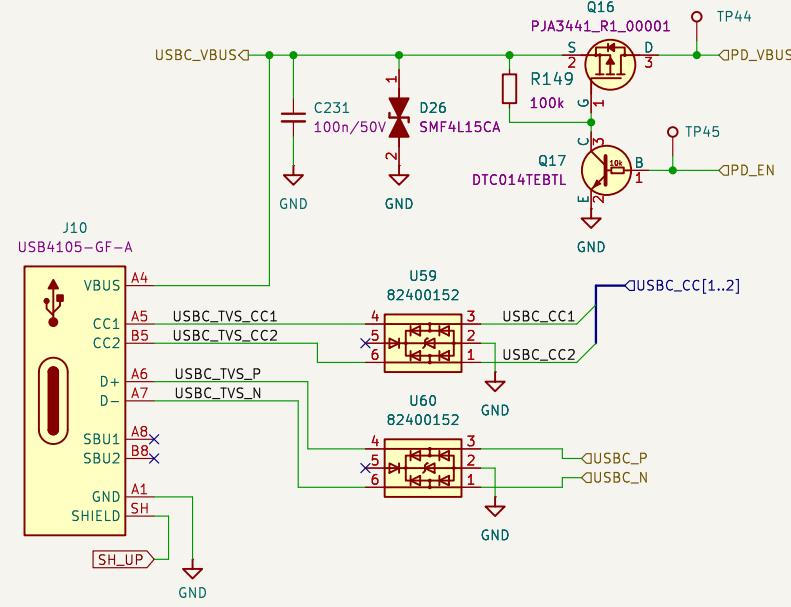
B

C

C

D

D



Antmicro Ltd.  
www.antmicro.com

Sheet: /Power Supply/USB-C socket/  
File: usbc-socket.kicad\_sch

**Title: Kria K26 Devboard**

Size: A4 Date: 2023-11-02  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 1.2.4:b5051  
Id: 3/19

A

A

B

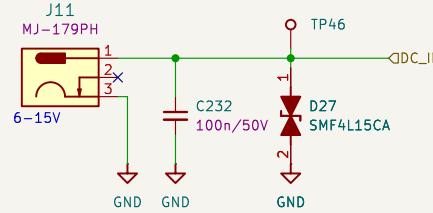
B

C

C

D

D



Antmicro Ltd.  
[www.antmicro.com](http://www.antmicro.com)

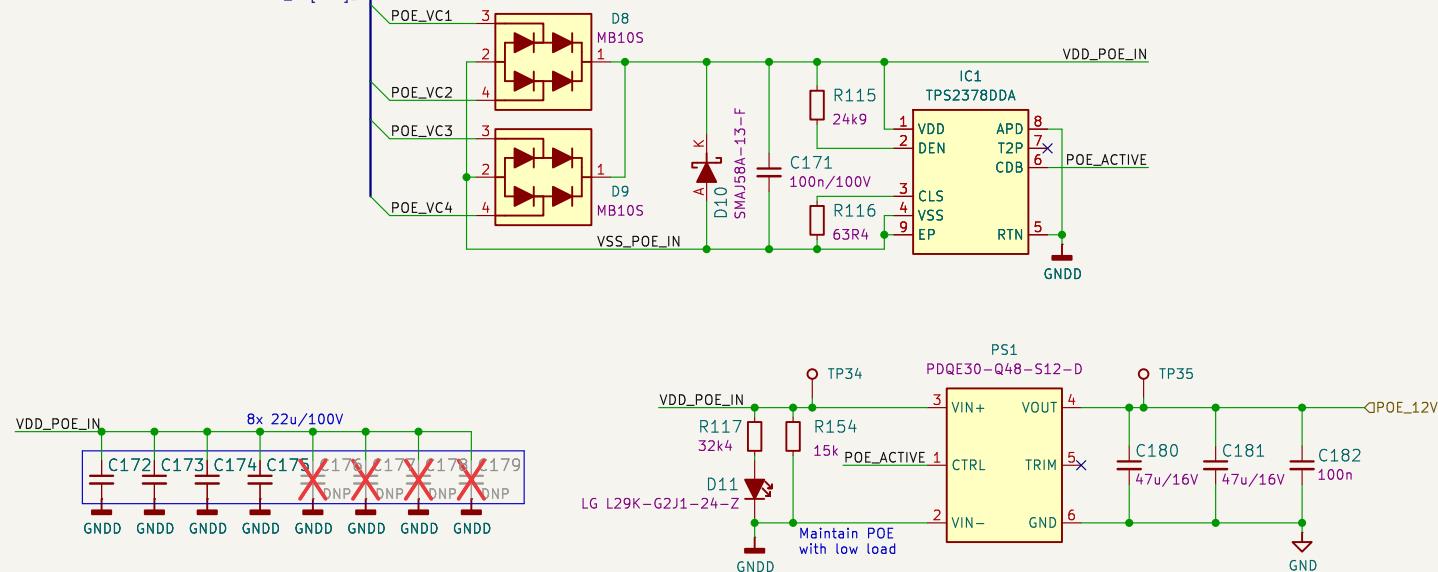
Sheet: /Power Supply/DC Input/  
File: dc-input.kicad\_sch

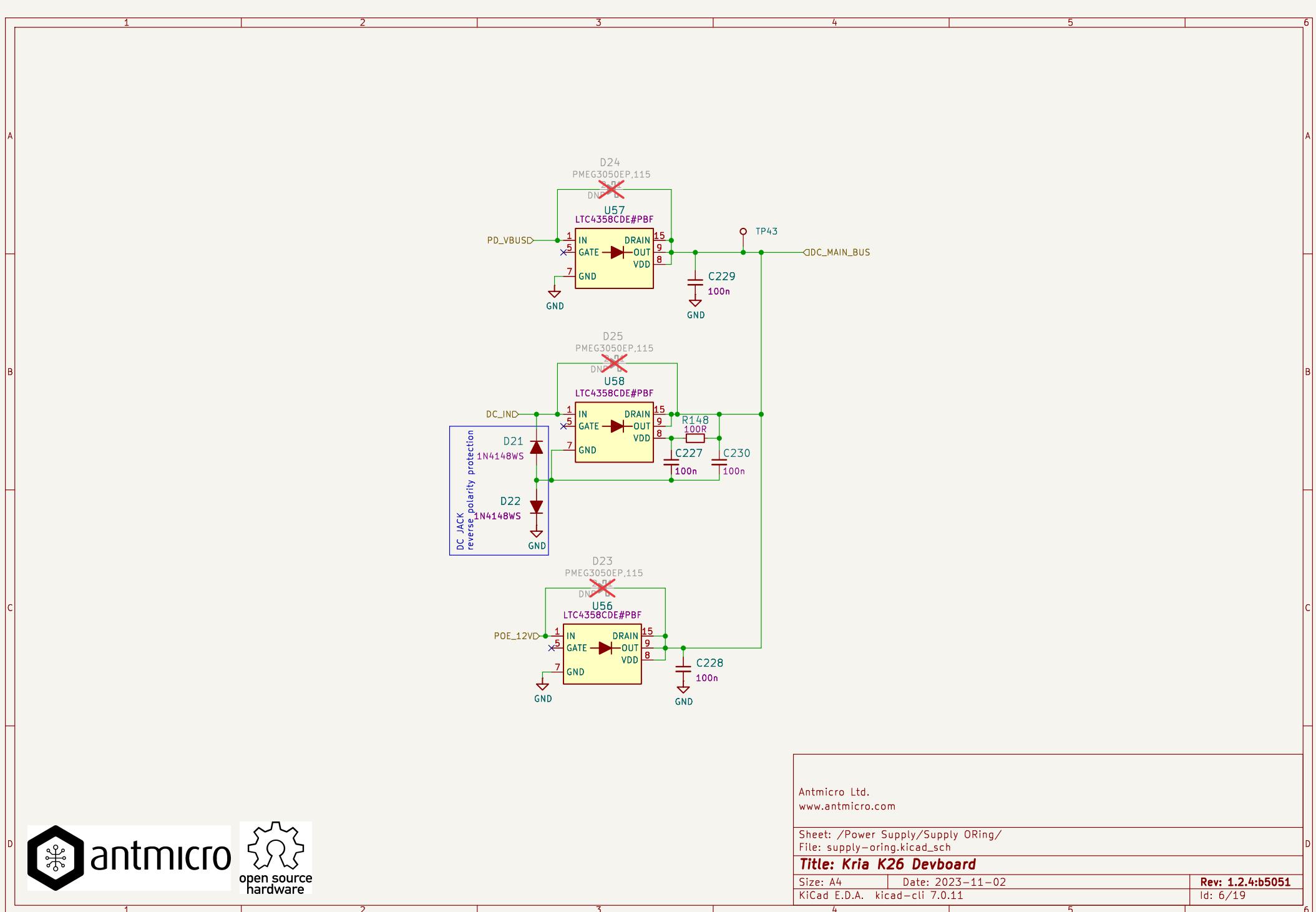
**Title: Kria K26 Devboard**

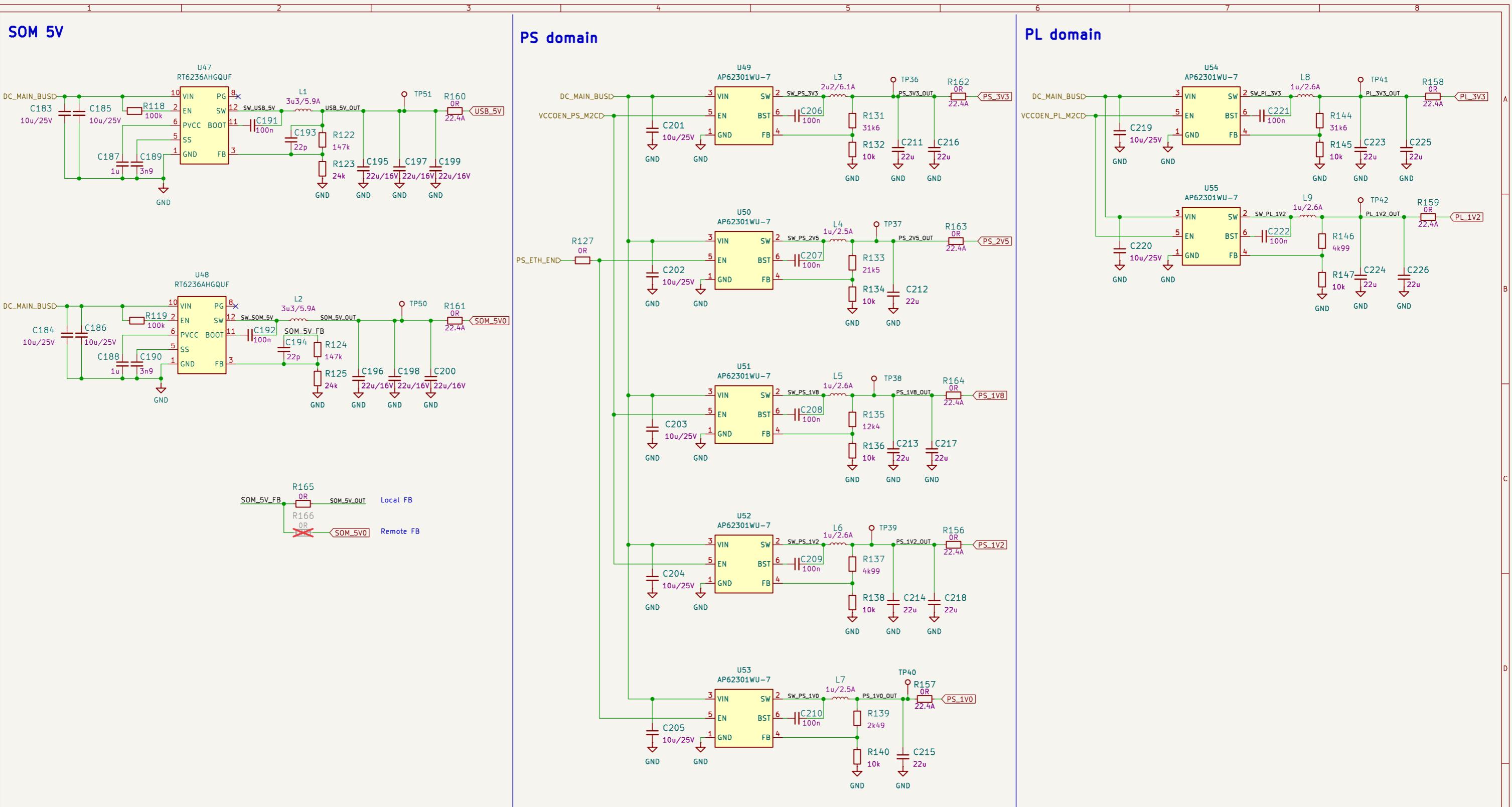
Size: A4 | Date: 2023-11-02  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 1.2.4:b5051  
Id: 4/19

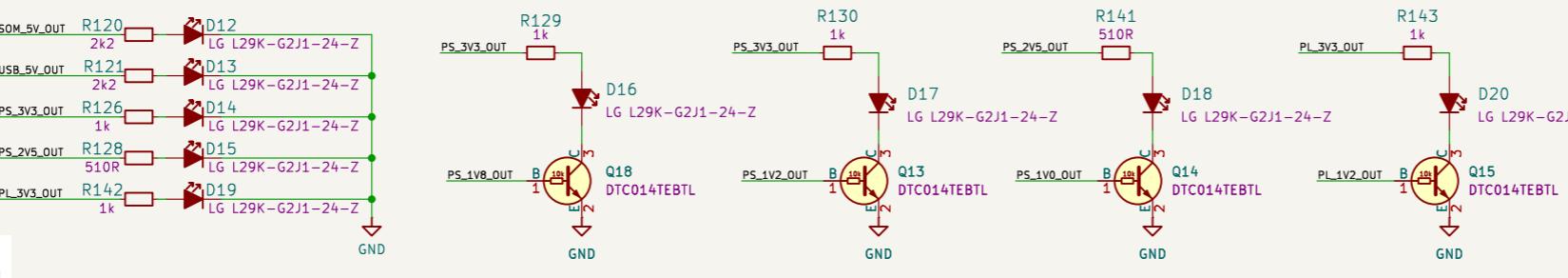
## PoE PD







### Power indication



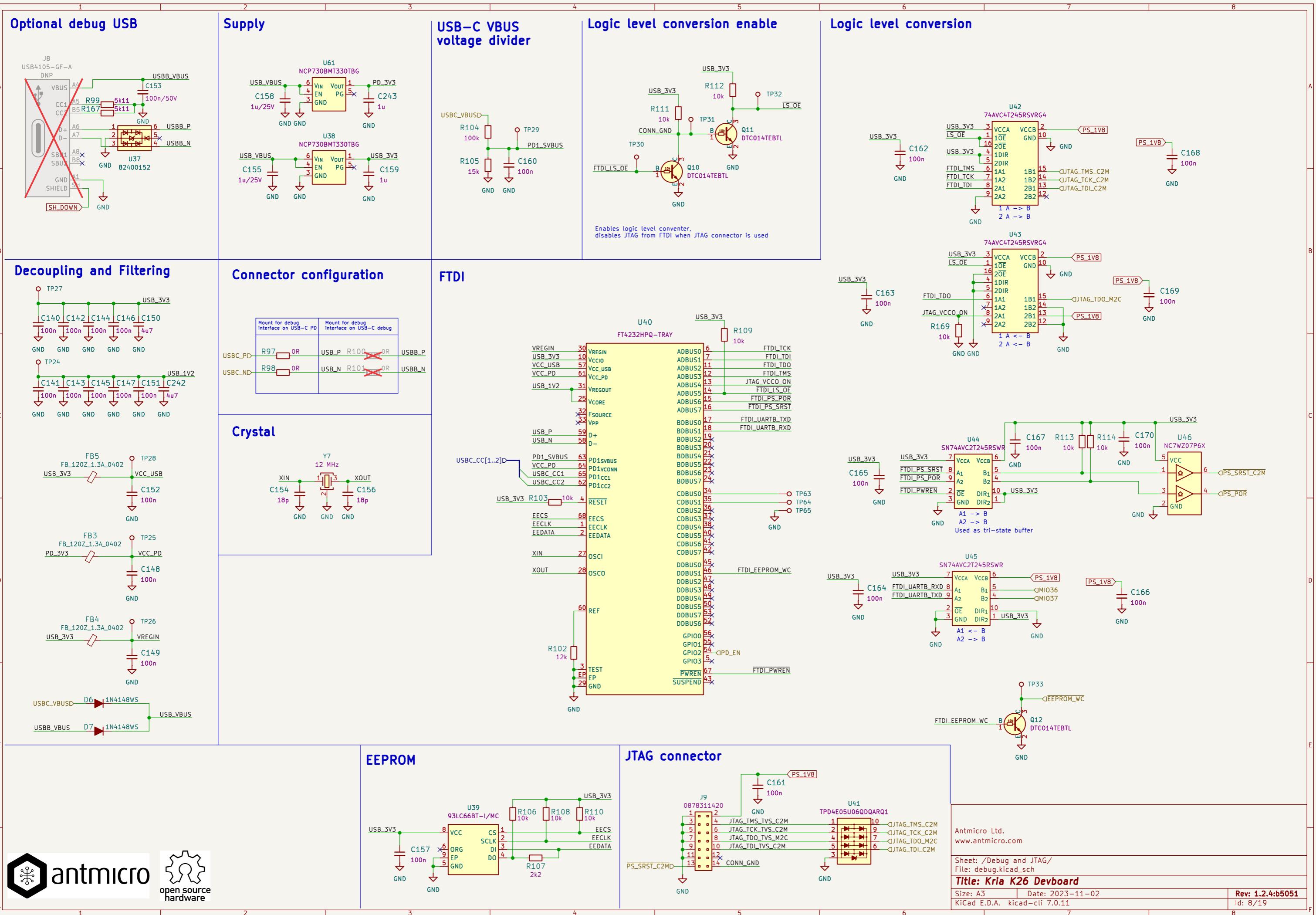
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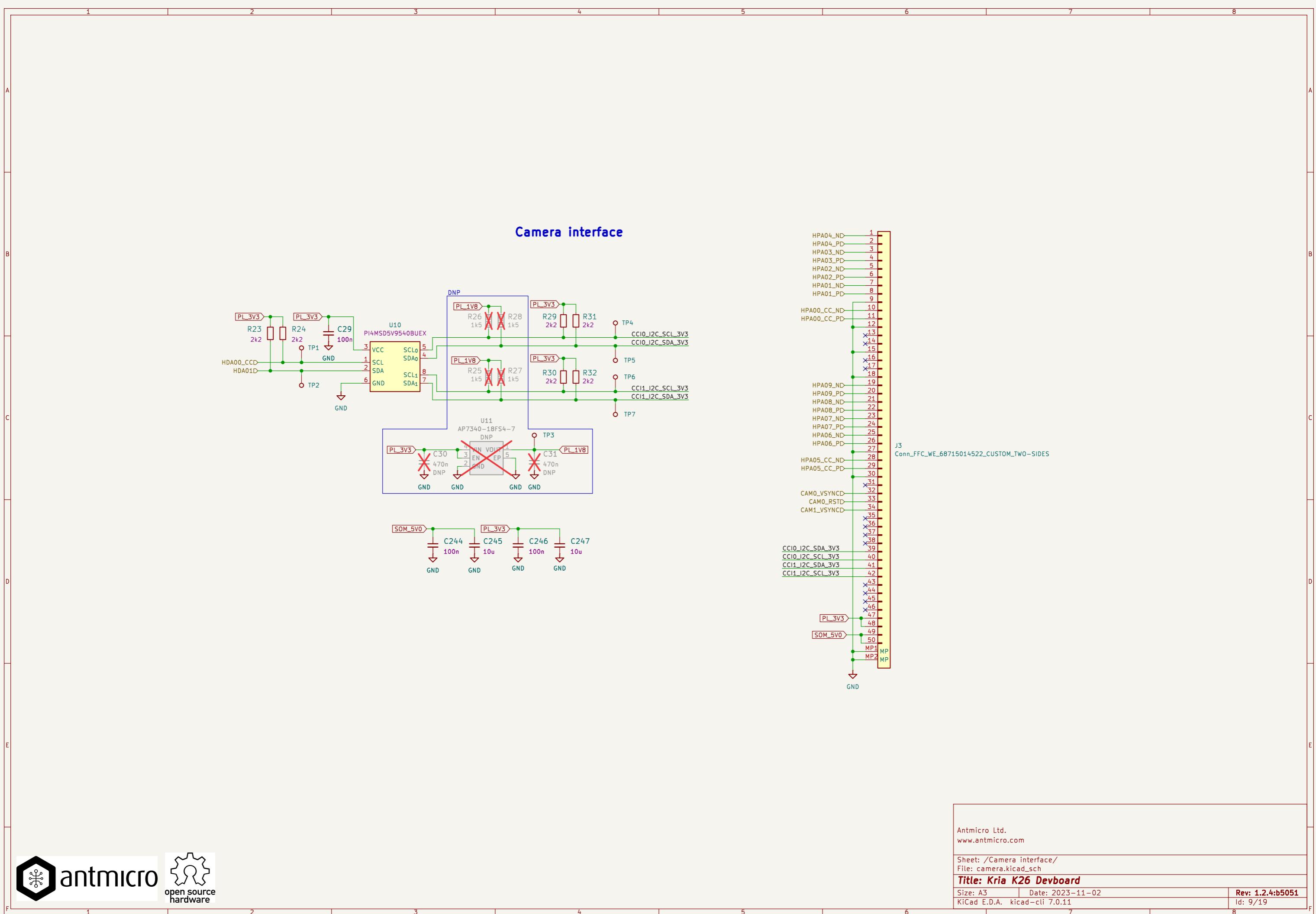
Sheet: /Power Supply/DC/DC converters/  
File: dc-dc-converters.kicad\_sch

**Title: Kria K26 Devboard**

Size: A3 Date: 2023-11-02  
KiCad E.D.A. kicad-cli 7.0.11

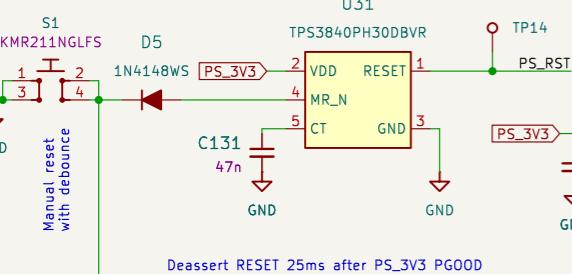
Rev: 1.2.4:b5051  
Id: 7/19





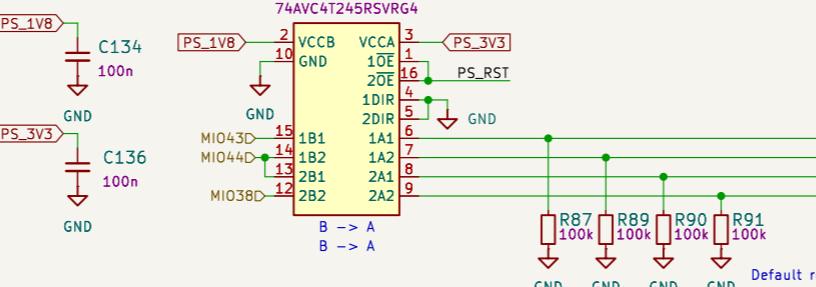
## PS domain

PS voltage supervisor (3V0 threshold) with manual reset



Deassert RESET 25ms after PS\_3V3 PGOOD

Logic level conversion enabled by voltage supervisor



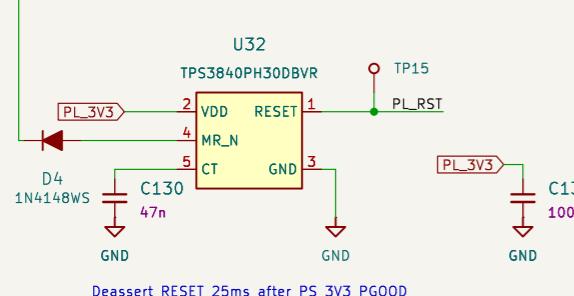
A

B

C

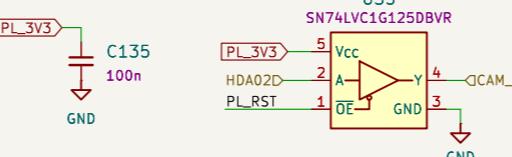
## PL domain

PL voltage supervisor (3V0 threshold) with manual reset

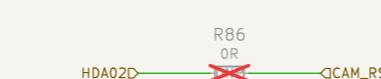


Deassert RESET 25ms after PS\_3V3 PGOOD

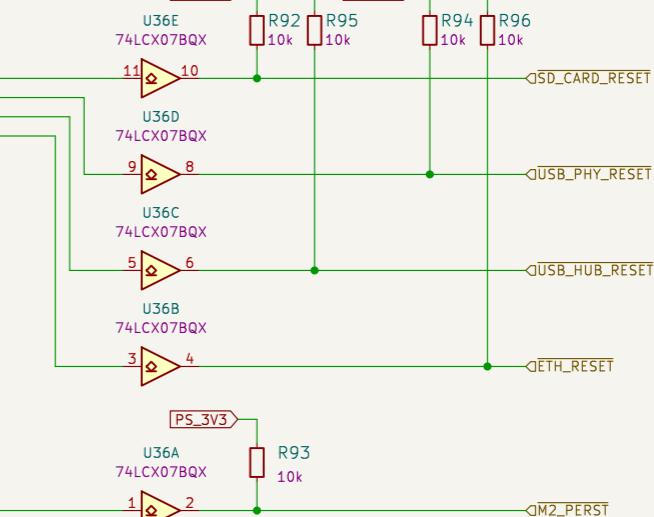
Reset OE controlled by voltage supervisor



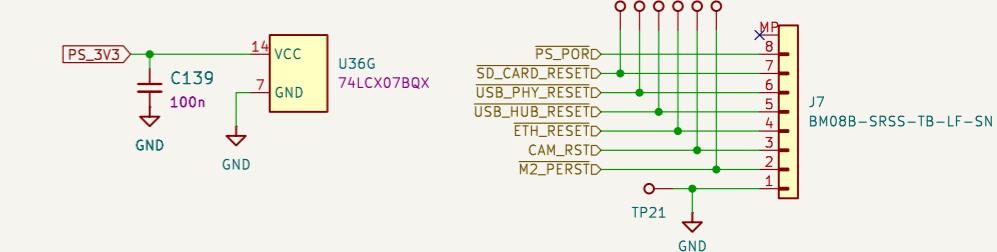
Optional PL bypass  
(when using DNP other PL reset circuitry)



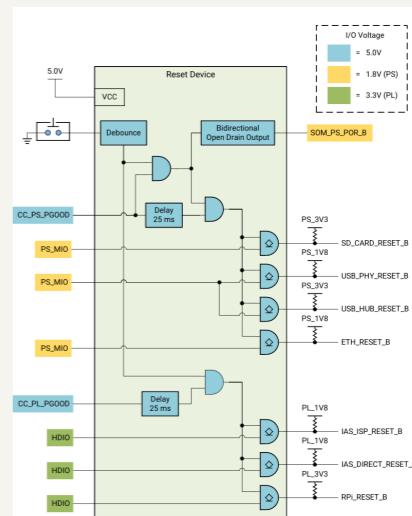
OD reset buffer



Reset debug connector



## Xilinx reference



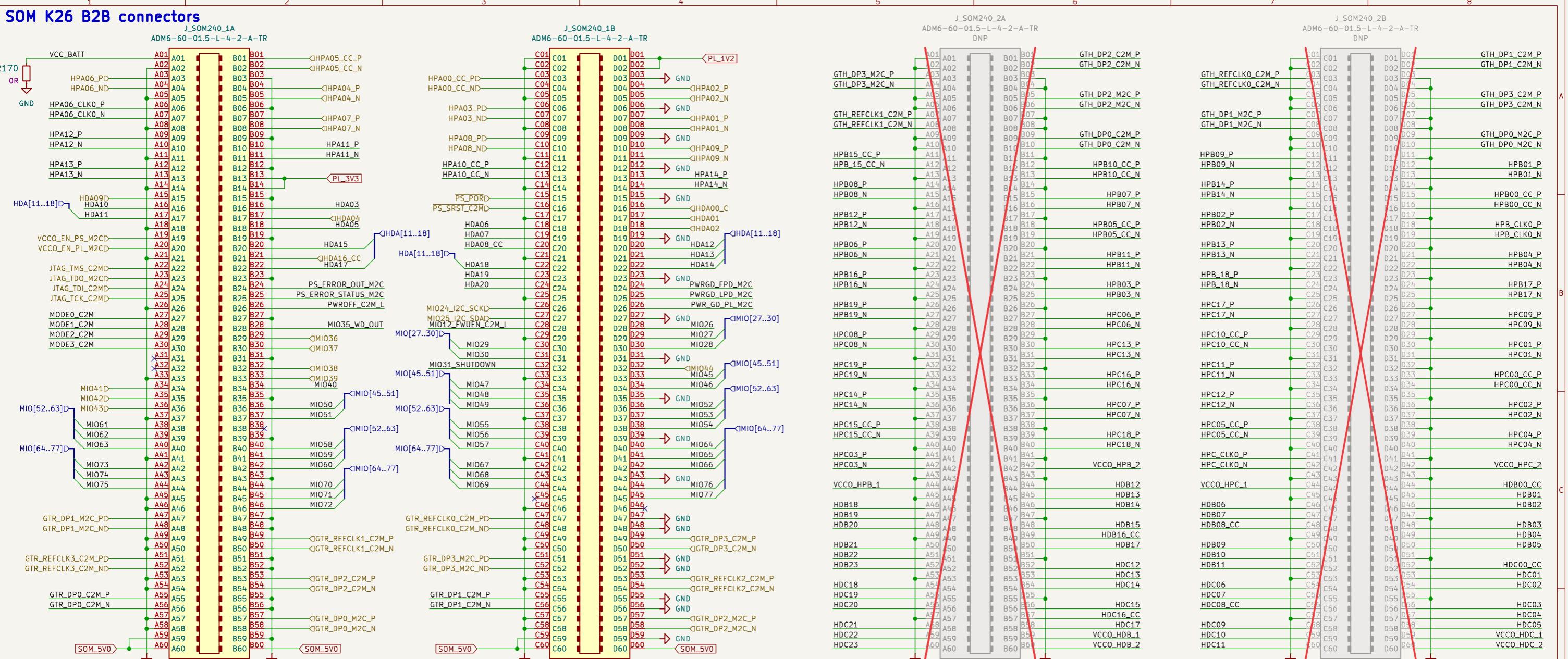
Antmicro Ltd.  
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Sheet: /Reset logic/  
File: reset.kicad\_sch

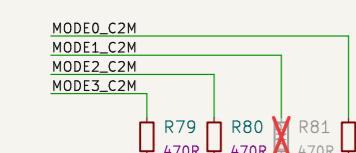
Title: Kria K26 Devboard

Size: A3 Date: 2023-11-02  
KiCad E.D.A. kicad-cl 7.0.11

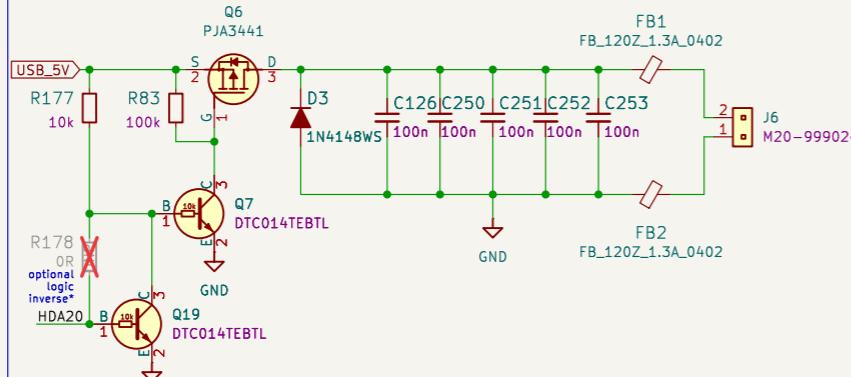
Rev: 1.2.4:b5051  
Id: 10/19



#### BOOT MODE: QUAD-SPI



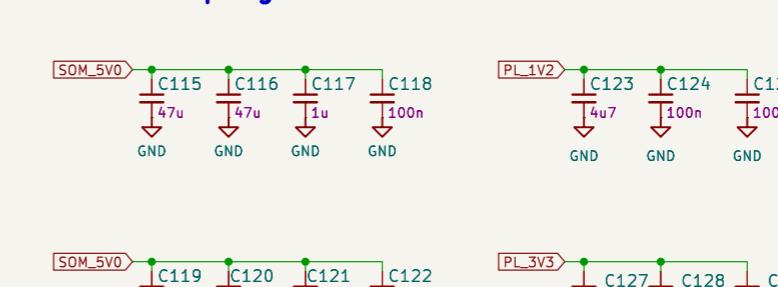
#### 5V Fan header



#### SHUTDOWN pull-down



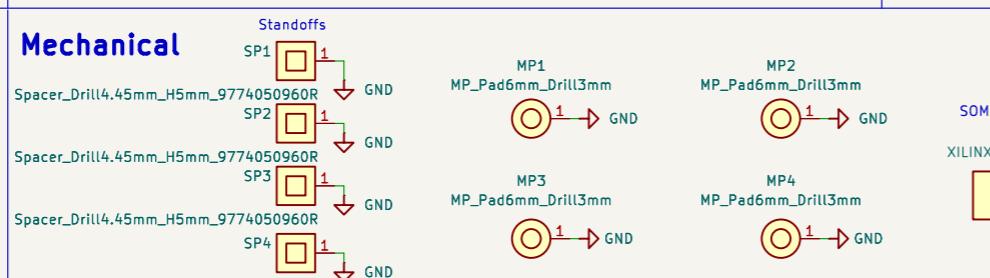
#### SOM decoupling



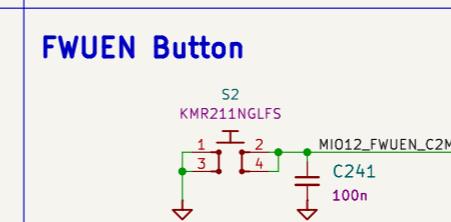
#### Test points

PS_ERROR_OUT_M2C	TP52
PS_ERROR_STATUS_M2C	TP53
PWRGD_FPD_M2C	TP54
PWRGD_LPD_M2C	TP55
PWR_GD_PL_M2C	TP56
MIO26	TP57
MIO35_WD_OUT	TP58
MIO35_WD_OUT	TP59

#### Mechanical



#### FWUEN Button



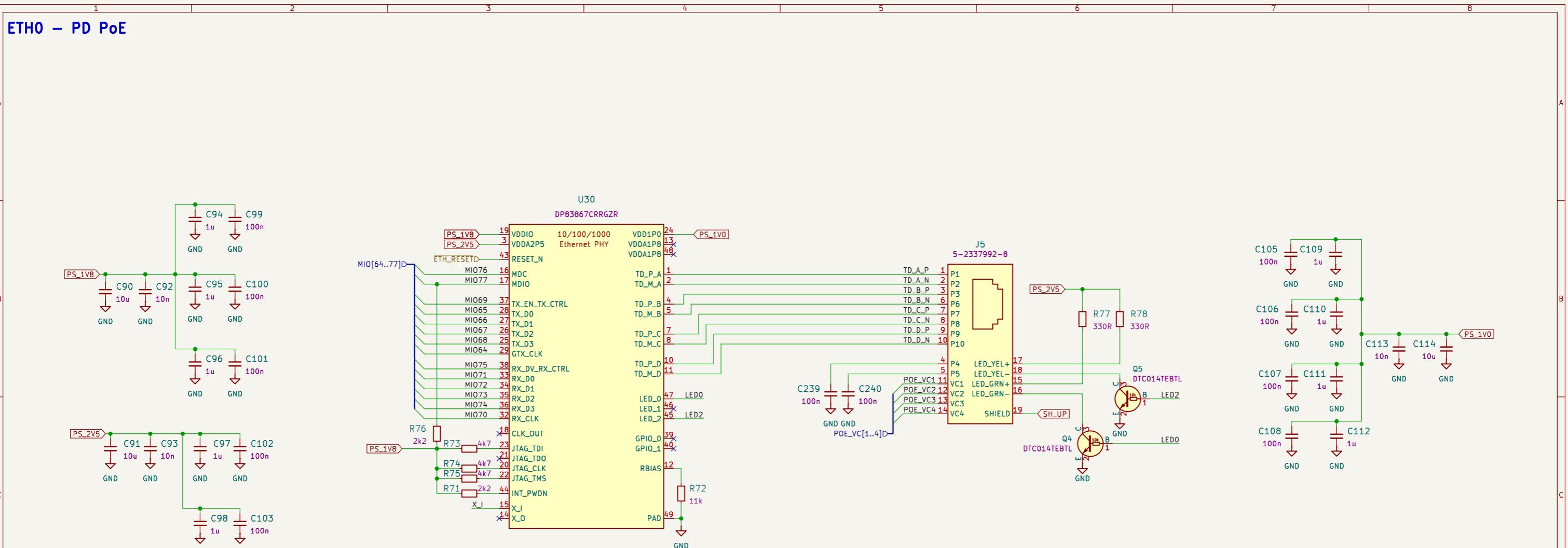
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**Antmicro**

Sheet: /Xilinx K26 SOM/  
File: k26\_som.kicad\_sch

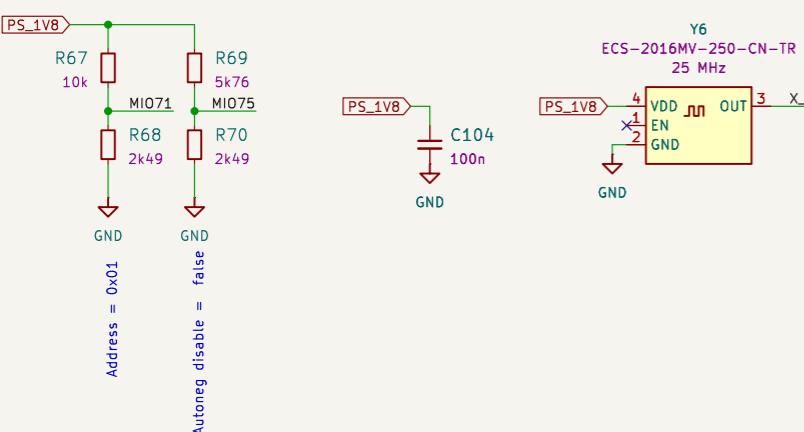
**Title: Kria K26 Devboard**

Size: A3 Date: 2023-11-02  
KiCad E.D.A. kicad-cl 7.0.11

Rev: 1.2.4:b5051  
Id: 11/19



## Strap Configuration



**NOTE:** CLK is matched to data lanes, the device tree should use "rgmii-id"

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Sheet: /Ethernet/  
File: eth.kicad\_sch

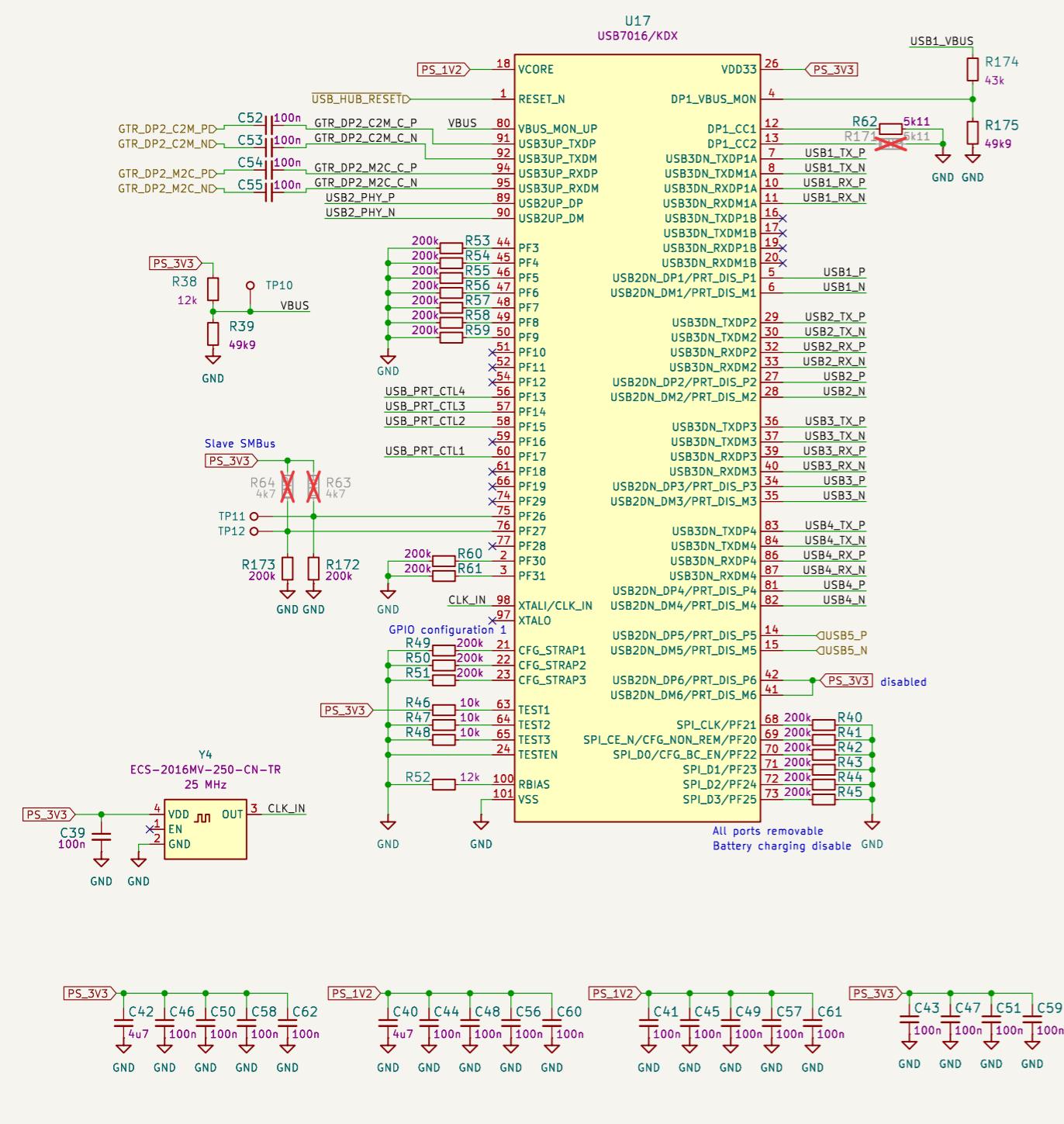
## Title: Kria K26 Devboard

Size: A3 Date: 2023-11-02  
KiCad E.D.A. kicad-cli 7.0.11

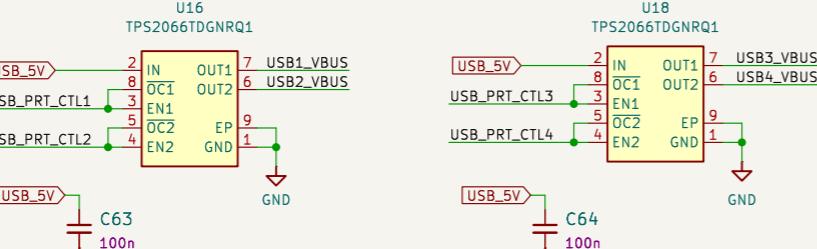
Rev: 1.2.4:b5051  
Id: 12/19



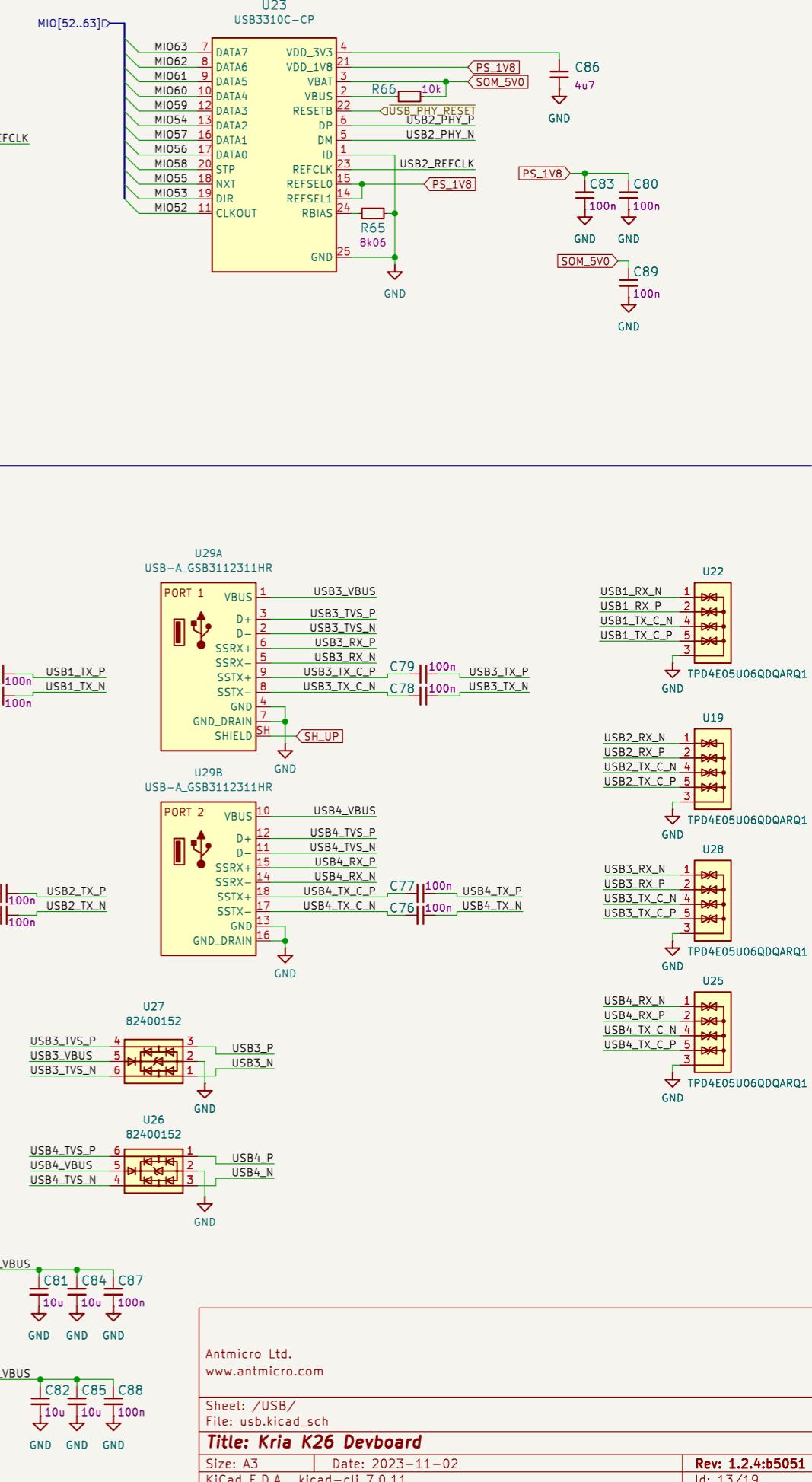
6 port USB hub

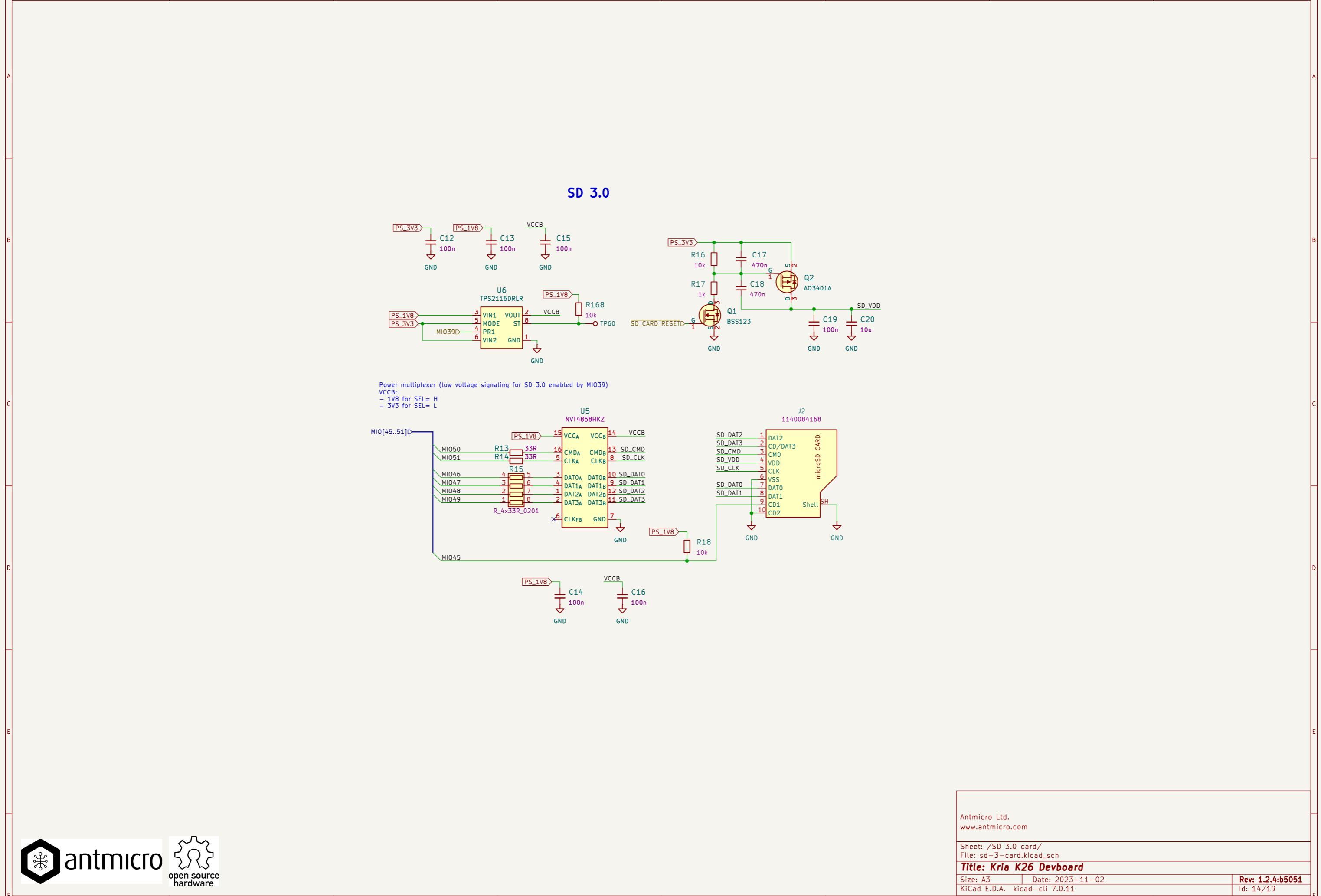


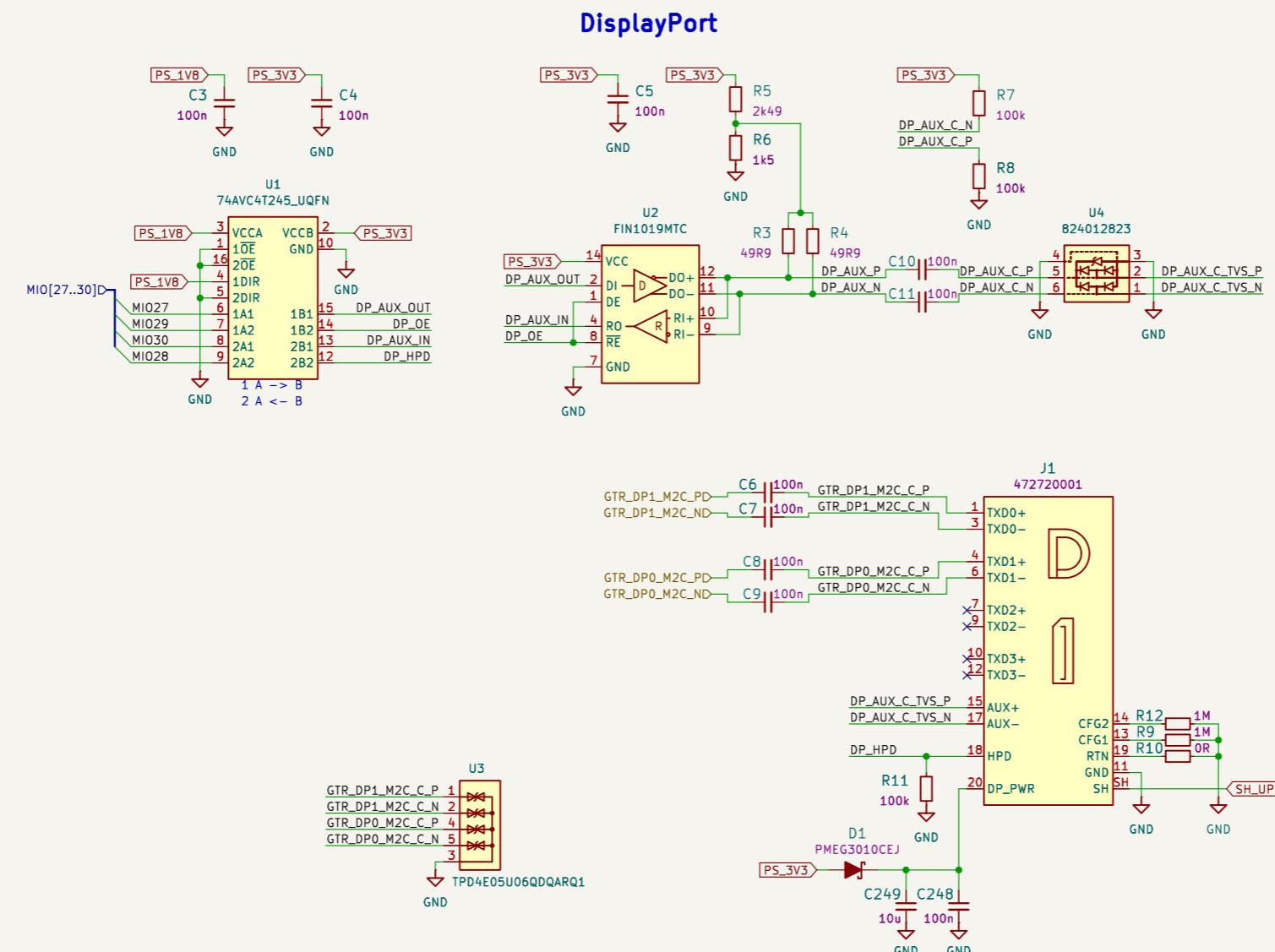
## USB power switches

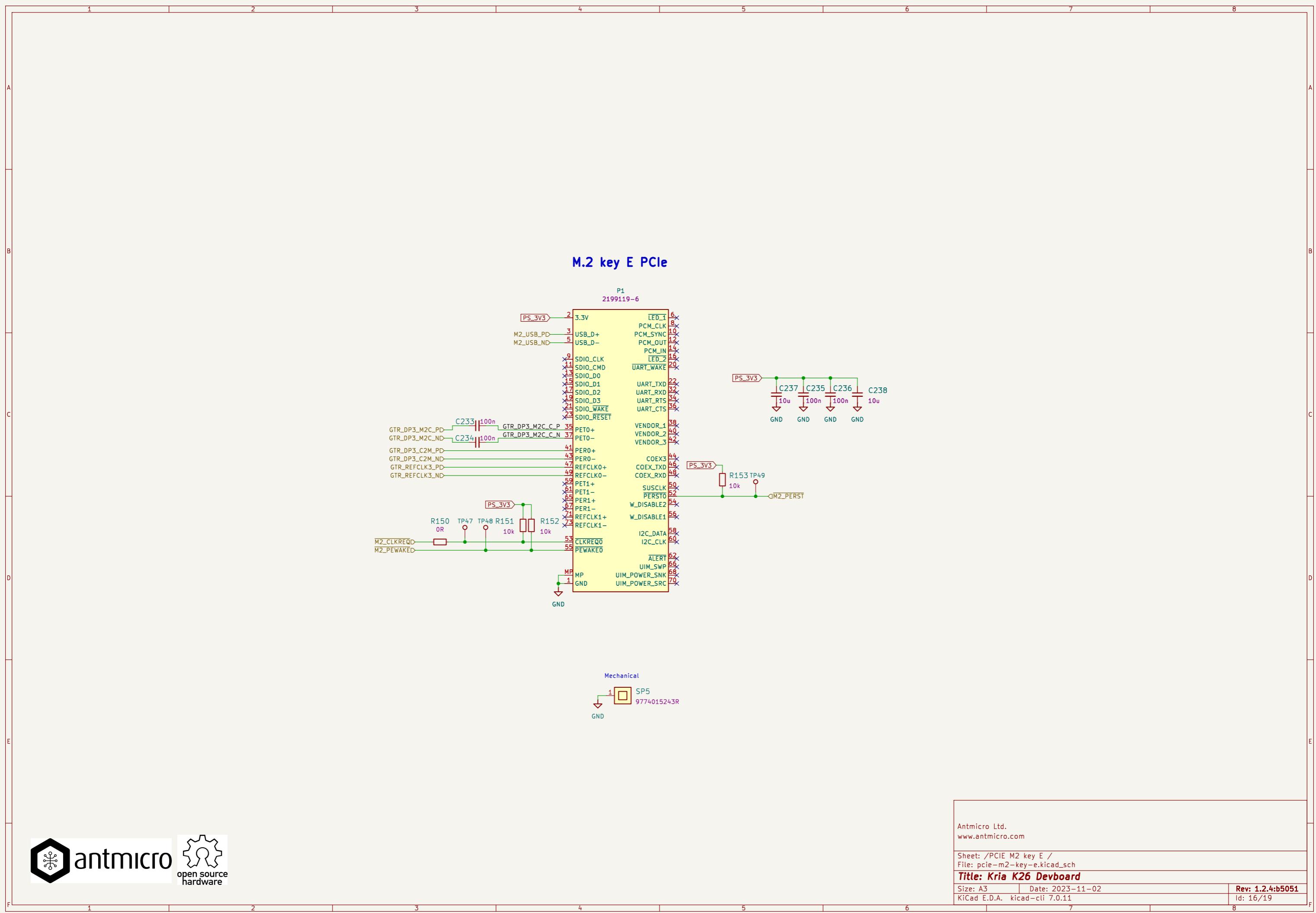


USB 2.0 PHY

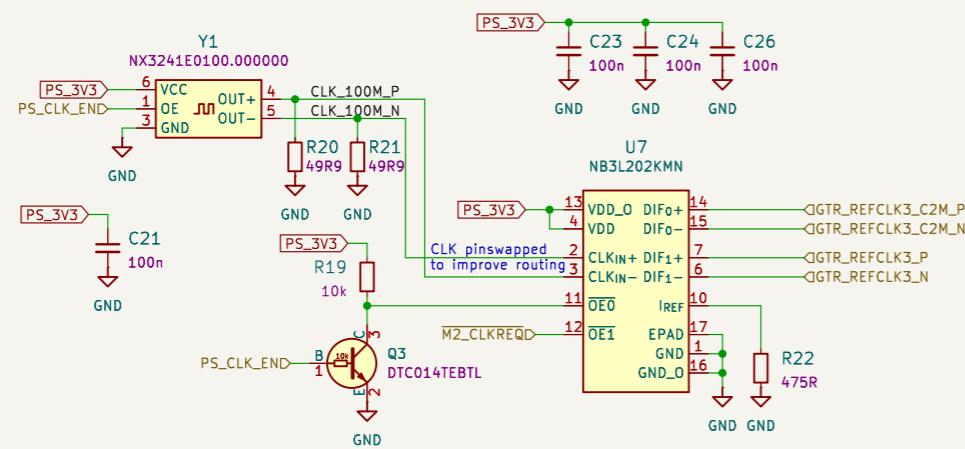
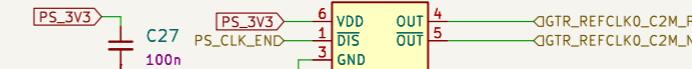
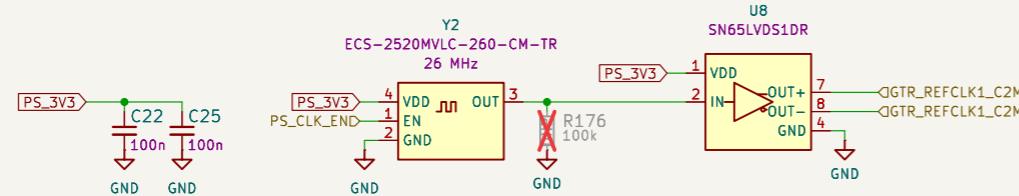
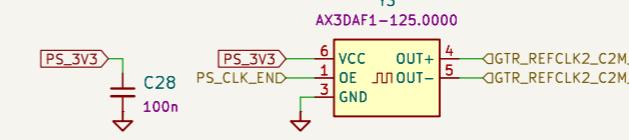








A

**PCIe GTH REFCLK: 2x100MHz HCSL****DisplayPort GTH REFCLK: 27MHz LVDS****USB GTH REFCLK: 26MHz LVDS****ETH GTH REFCLK: 125MHz LVDS**

A

A

B

B

C

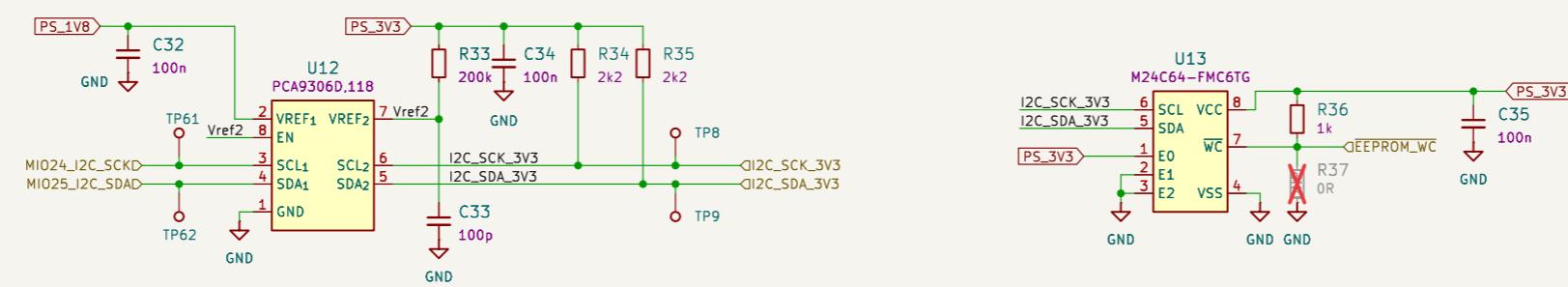
C

D

D

E

E

**I2C**

1 2 3 4 5 6 7 8

A

A

B

B

C

C

D

D

E

E

F

F

## PMOD

