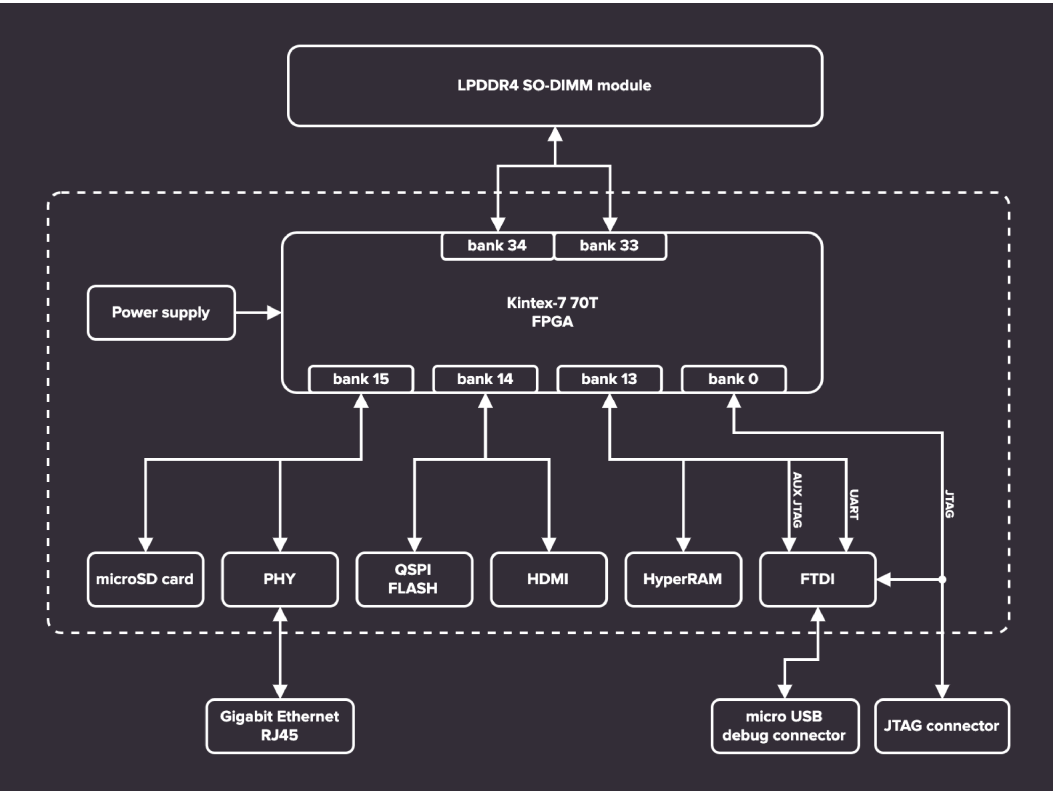
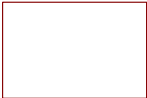


LPDDR4 Test Board



HyperRAM



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FPGA Banks



File: fpga-banks.kicad_sch

Interfaces



File: interfaces.kicad_sch

Config SPI flash



File: config-spi.kicad_sch

FPGA power



File: fpga-power.kicad_sch

Ethernet



File: ethernet.kicad_sch

Supply



File: supply.kicad_sch

SO-DIMM



File: sodimm.kicad_sch

Logo N2 oshw_logo

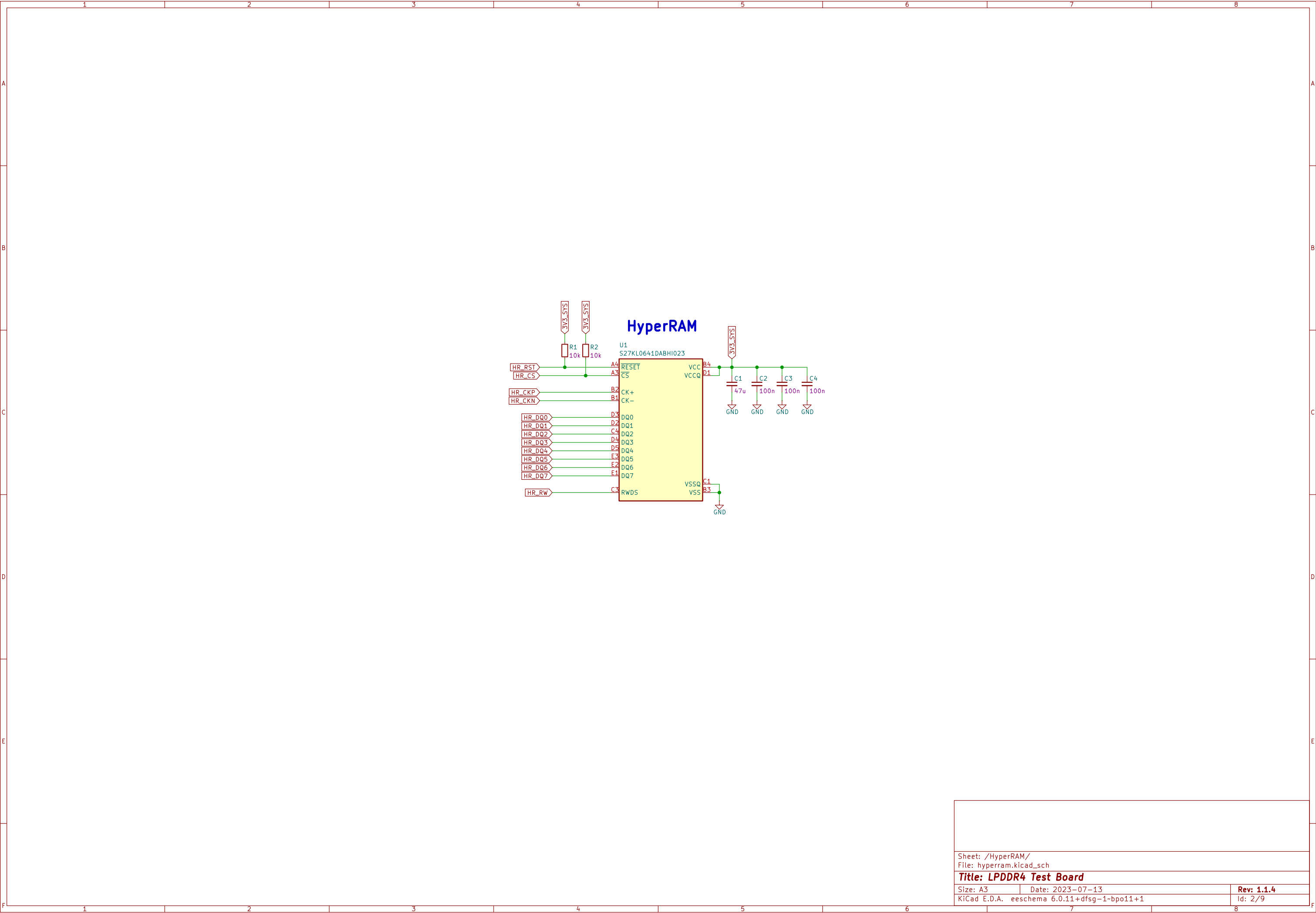
Logo N1 antmicro_logo

LPDDR4 Test Board

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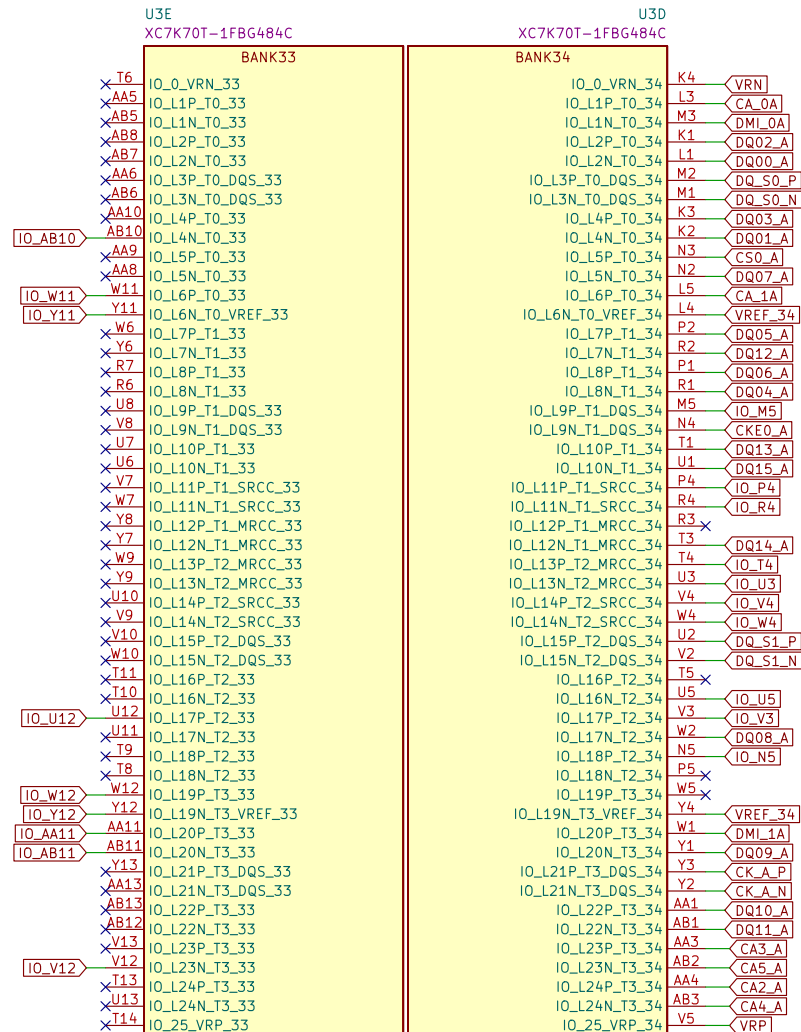
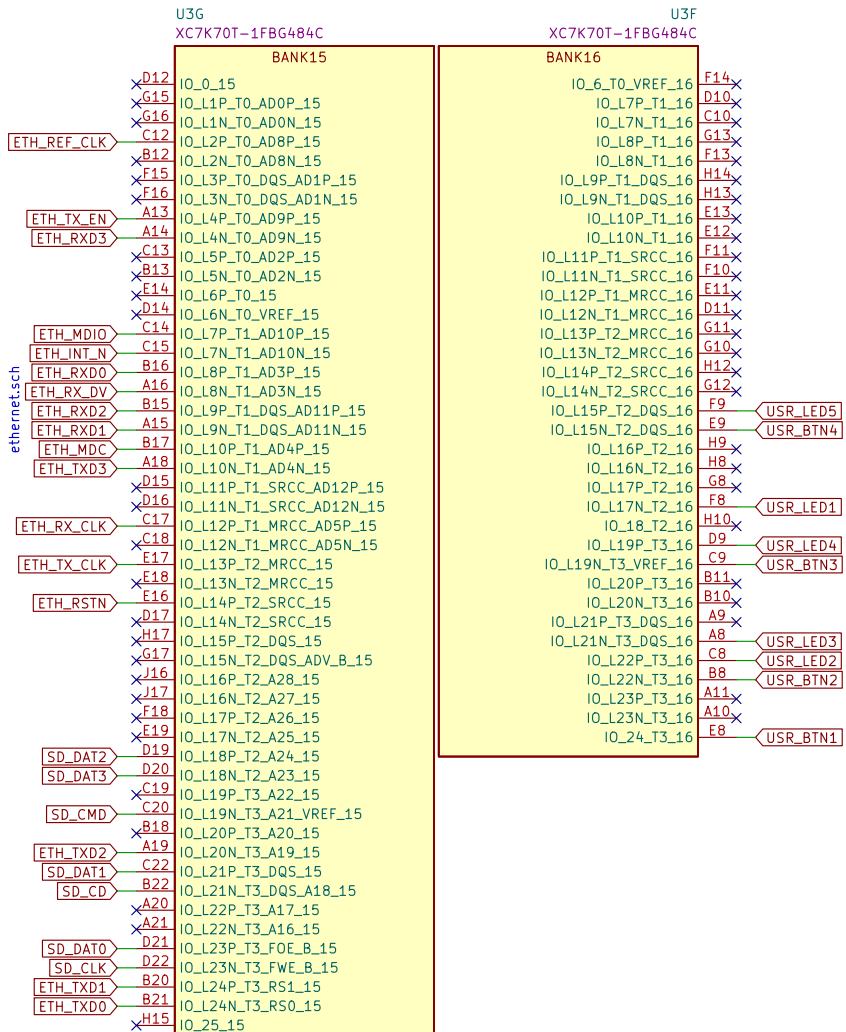
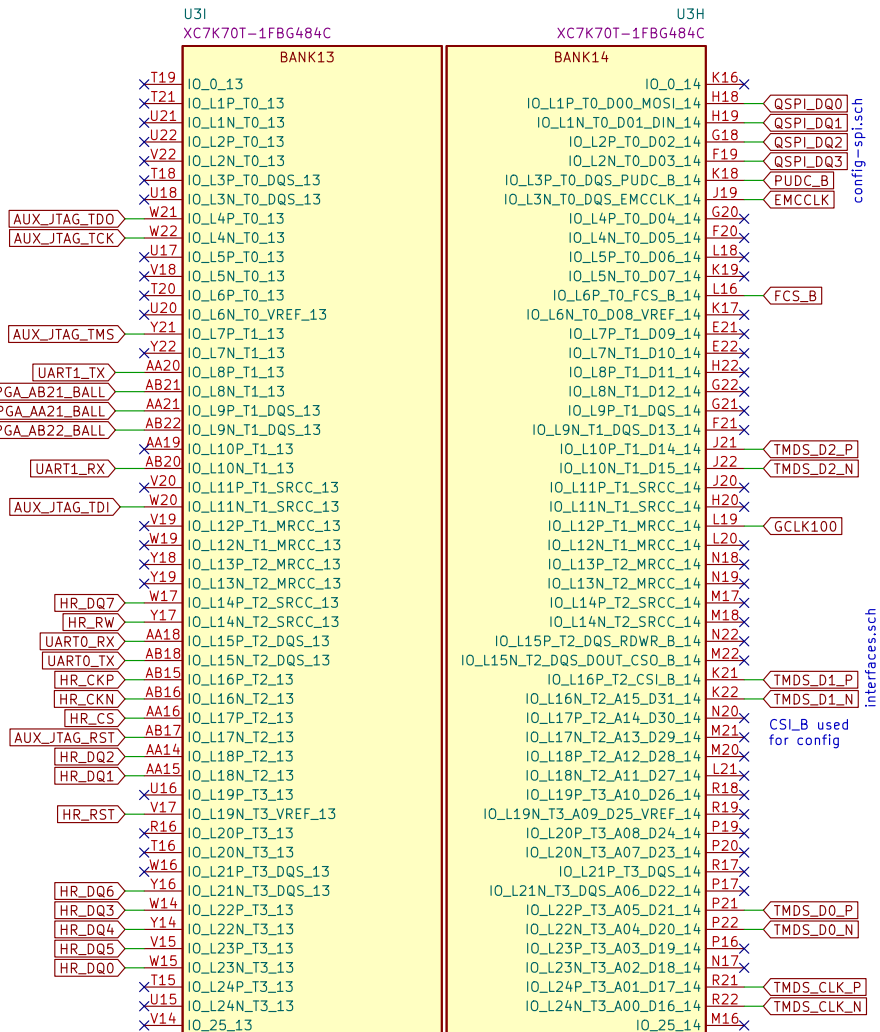
Size: A3	Date: 2023-07-13	Rev: 1.1.4
KiCad E.D.A. eeschema 6.0.11+dfsg-1-bpo11+1		Id: 1/9



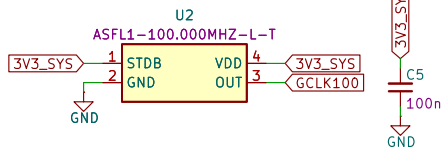
INTERFACES

INTERFACES

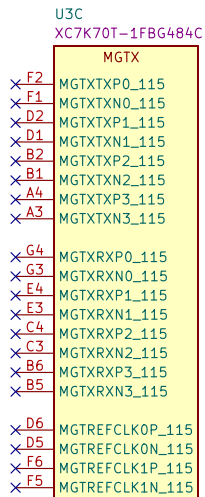
LPDDR4-TESTBED



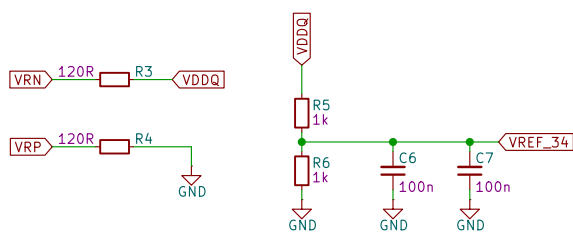
Clock source



UNUSED



LPDDR VREF



Sheet: /FPGA Banks/
File: fpga-banks.kicad_sch

Title: LPDDR4 Test Board

Size: A3 Date: 2023-07-13

Rev: 1.1.4

KiCad E.D.A. eeschema 6.0.11+dfsg-1-bpo11+1

Id: 3/9

The schematic diagram illustrates the LPDDR4 Test Board, a custom PCB designed for testing LPDDR4 memory modules. The board is populated with several key components and interfaces:

- Microcontroller (U4):** FT4232H_VQFN, which manages the USB-to-UART bridge and provides control signals to the memory module.
- USB Interface (J1):** USB-Micro-B_629105150521, connected to the microcontroller via a USB-to-UART bridge.
- HDMI Interface (J2):** 685119134923, used for video output from the test board.
- SD Card Interface (J3):** MicroSD_1140084168, used for data storage and logging.
- User Buttons (USR_BTN1-4):** Four push buttons (USR_BTN1, USR_BTN2, USR_BTN3, USR_BTN4) connected to the microcontroller for user interaction.
- User LEDs (USR_LED1-4):** Four LEDs (USR_LED1, USR_LED2, USR_LED3, USR_LED4) connected to the microcontroller for status indication.
- Debug UART:** A dedicated UART interface for debugging the microcontroller's operation.
- Power and Grounding:** The board includes multiple power planes (3V3_SYS, 1V8_FT, 1V8_VPHY) and ground planes, with various decoupling capacitors (C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21) and voltage regulators (FB1, FB2) to ensure stable power delivery.

The schematic is a detailed representation of the board's internal connections, showing the placement of components, the routing of signals, and the connection of the board to external devices and power sources.

The schematic diagram illustrates the LPDDR4 Test Board, featuring a central microcontroller (U4: FT4232H_VQFN) connected to various interfaces and components. The board is organized into several functional sections:

- Debug UART:** Includes connections for VREGIN, VCCIO, VREGOUT, VPHY, VPLL, VCORE, and various bus signals (ADBUS0-7, BDBUS0-7, CDBUS0-7, DDBUS0-7). It also shows connections for UART0_RX/TX, UART1_RX/TX, and auxiliary JTAG signals.
- HDMI:** Features an HDMI connector (J2) connected to the microcontroller's TMDS signals (TMDS_D0_P, TMDS_D0_N, TMDS_D1_P, TMDS_D1_N, TMDS_D2_P, TMDS_D2_N, TMDS_D3_P, TMDS_D3_N, TMDS_CLK_P, TMDS_CLK_N) and other signals like SCL, SDA, HPD, CEC, and SH.
- SD card:** Includes an SD card connector (J3) connected to the microcontroller's SD signals (SD_DAT0, SD_DAT1, SD_DAT2, SD_DAT3, SD_CMD, SD_CLK, SD_CD) and other signals like DAT0, DAT1, DAT2, DAT3, CMD, CLK, VDD, VSS, and SH.
- User buttons:** Shows four push buttons (USR_BTN1-4) connected to the microcontroller's I/O pins (USR_BTN1-4) through pull-up resistors (R9-R12).
- User LEDs:** Features four LEDs (USR_LED1-4) connected to the microcontroller's I/O pins (USR_LED1-4) through current-limiting resistors (R26-R29).

The schematic also includes power and ground connections, such as 3V3_SYS, GND, and various capacitors (C1-C21) for decoupling and timing. The board is labeled with various components like resistors (R1-R46), capacitors (C1-C21), and integrated circuits (U1-U4).

Sheet: /Interfaces/
File: interfaces.kicad_sch
Title: LPDDR4 Test Board
Size: A3 Date: 2023-07-13 Rev: 1.1.4
KiCad E.D.A. eeschema 6.0.11+dfsg-1-bpo11+1 Id: 4/9

The schematic diagram illustrates the LPDDR4 Test Board, featuring a central microcontroller (U4: FT4232H_VQFN) connected to various interfaces and components. The board is organized into several functional sections:

- Debug UART:** Includes connections for VREGIN, VCCIO, VREGOUT, VPHY, VPLL, VCORE, and various bus signals (ADBUS0-7, BDBUS0-7, CDBUS0-7, DDBUS0-7). It also shows connections for UART0_RX/TX, UART1_RX/TX, and auxiliary JTAG signals.
- HDMI:** Features an HDMI connector (J2) connected to the microcontroller's TMDS signals (TMDS_D0_P, TMDS_D0_N, TMDS_D1_P, TMDS_D1_N, TMDS_D2_P, TMDS_D2_N, TMDS_D3_P, TMDS_D3_N, TMDS_CLK_P, TMDS_CLK_N) and other signals like SCL, SDA, HPD, CEC, and SH.
- SD card:** Includes an SD card connector (J3) connected to the microcontroller's SD signals (SD_DAT0, SD_DAT1, SD_DAT2, SD_DAT3, SD_CMD, SD_CLK, SD_CD) and other signals like DAT0, DAT1, DAT2, DAT3, CMD, CLK, VDD, VSS, and SH.
- User buttons:** Shows four push buttons (USR_BTN1-4) connected to the microcontroller's I/O pins (USR_BTN1-4) through pull-up resistors (R9-R12).
- User LEDs:** Features four LEDs (USR_LED1-4) connected to the microcontroller's I/O pins (USR_LED1-4) through current-limiting resistors (R26-R29).

The schematic also includes power and ground connections, such as 3V3_SYS, GND, and various capacitors (C1-C21) for decoupling and timing. The board is labeled with various components like resistors (R1-R46), capacitors (C1-C21), and integrated circuits (U1-U4).

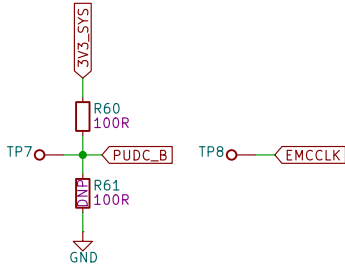
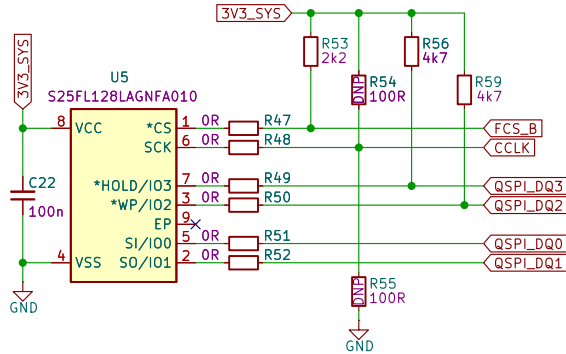
Sheet: /Interfaces/
File: interfaces.kicad_sch
Title: LPDDR4 Test Board
Size: A3 Date: 2023-07-13 Rev: 1.1.4
KiCad E.D.A. eeschema 6.0.11+dfsg-1-bpo11+1 Id: 4/9

[illegible][illegible][illegible]

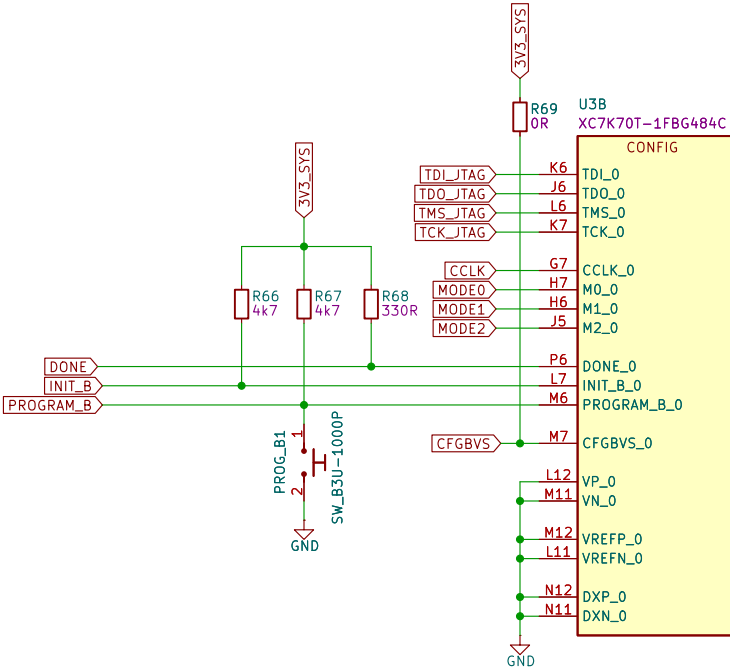
Master SPI Quad (x4) configuration scheme

Follows Figure 2–14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

(Q)SPI flash

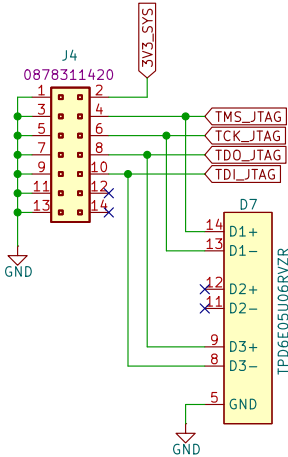


FPGA BANK 0

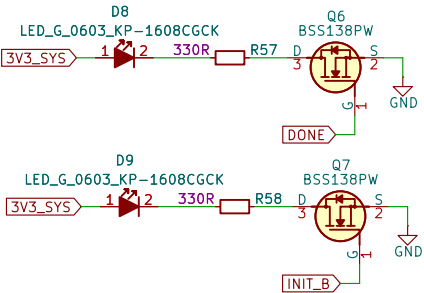


JTAG Connector

Compatible with Xilinx Platform Cable

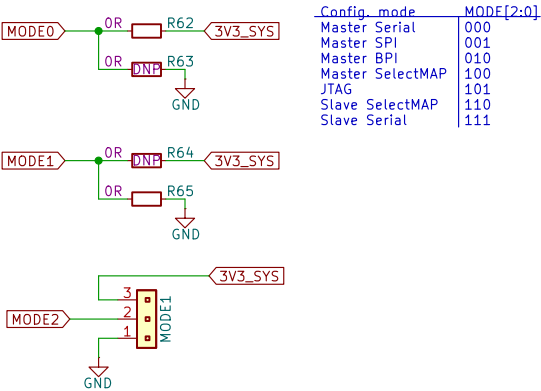


STATUS LEDs



Configuration Modes

For details, see UG470 p. 21



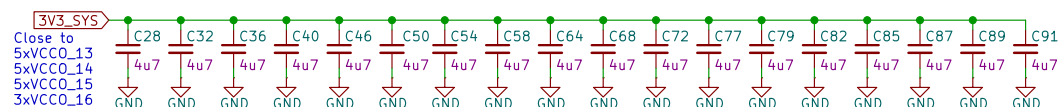
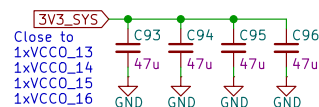
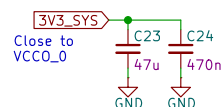
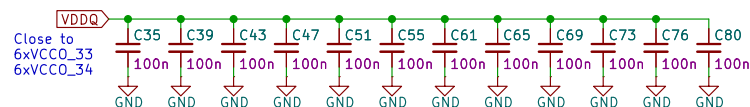
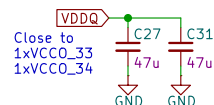
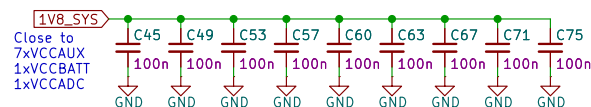
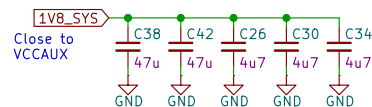
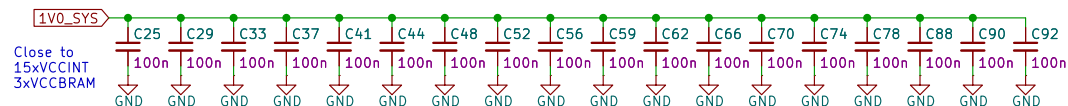
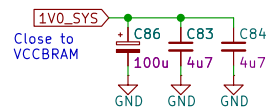
1V0_SYS

Close to VCCINT

C81

330u

GND



U3A
XC7K70T-1FBG484C

POWER

VCC0_0
VCCAUX
VCCINT
VCCBATT_0
VCCBRAM
VCCADC_0

3V3_SYS J7
1V8_SYS K10
1V0_SYS J11
1V8_SYS P7
1V0_SYS L13
1V8_SYS K12

VCCAUX max: 2.0V
VCCINT max: 1.1V
VCCBATT max: 2.0V
VCCBRAM max: 1.1V
VCCADC max: 2.0V

MGTVCC
MGTA VTT
MGTVCCAUX
MGTA VTTTRCAL_115
MGTRREF_115

A6
A2
J4
H1
H2

VCC0 (33-34 banks) max: 2.0V

VCC0 (13-16 banks) max: 3.6V

VCC1 max: 1.1V

VDDQ AB4
VDDQ AA7
C11
3V3_SYS A17
3V3_SYS F22
3V3_SYS AA17

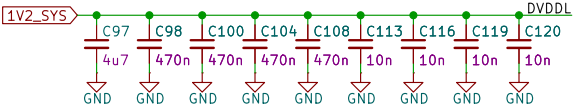
VCC0_34
VCC0_33
VCC0_16
VCC0_15
VCC0_14
VCC0_13

GNDADC_0
GND

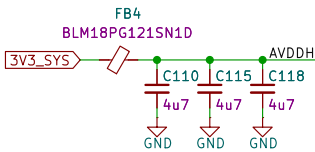
K11
A1

GND

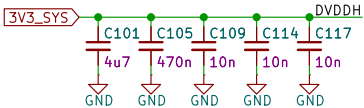
DVDDL decoupling



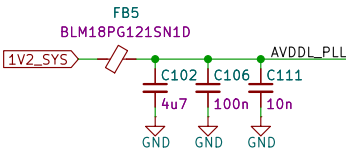
AVDDH decoupling



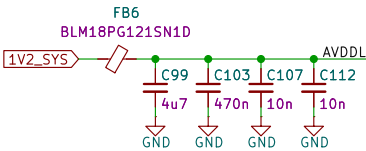
DVDDH decoupling



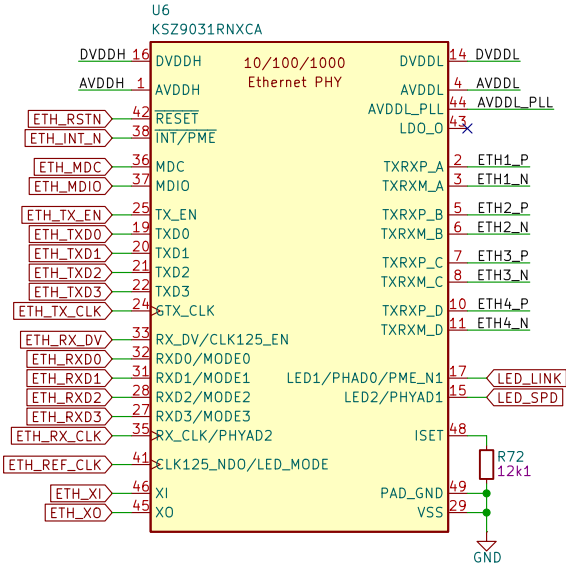
AVDDL_PLL decoupling



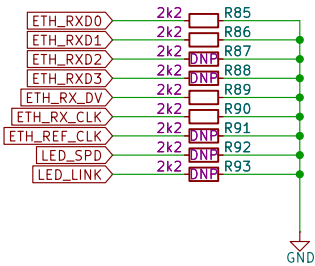
AVDDL decoupling



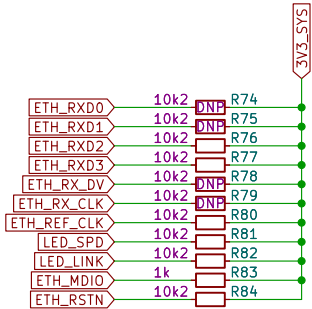
PHY



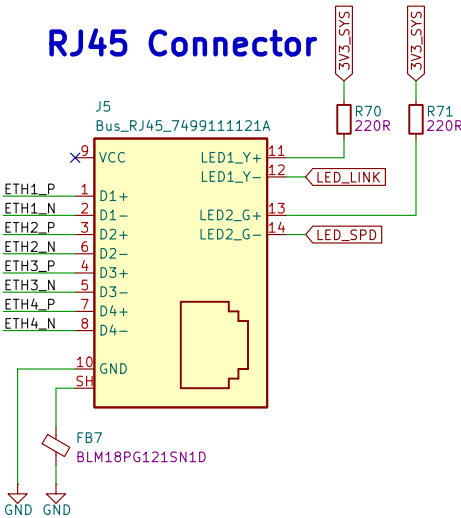
Pull down resistors



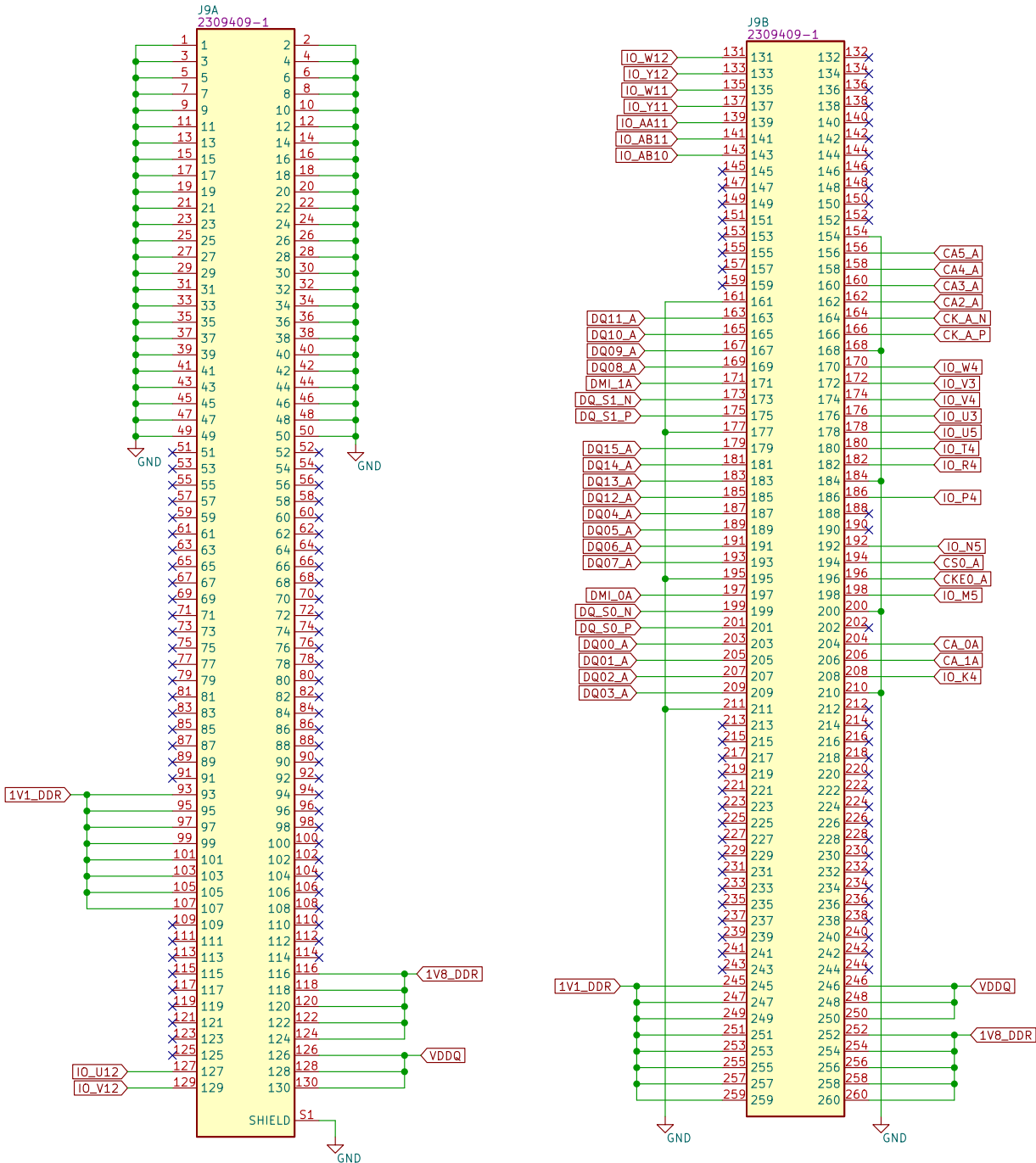
Pull up resistors



RJ45 Connector



DDR4 SODIMM connector



M1
DNP
ddr5--testbed

Mechanical protection

SP1
Spacer_H5.0mm_9774050151