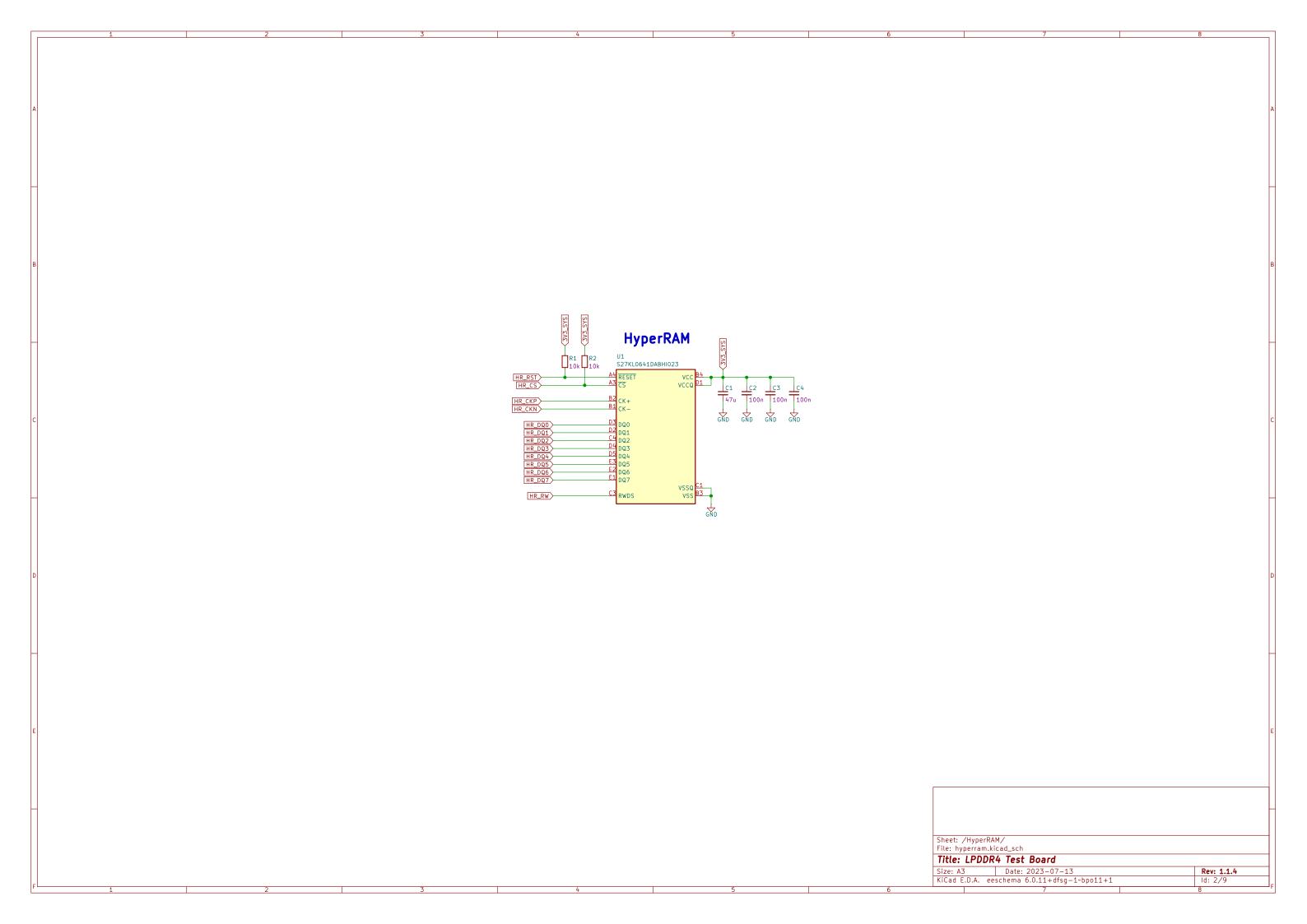
LPDDR4 Test Board LPDDR4 SO-DIMM module bank 34 bank 33 Kintex-7 70T FPGA Power supply bank 15 bank 14 bank 13 bank 0 HDMI Gigabit Ethe RJ45 micro USB debug connector JTAG connector HyperRAM FPGA Banks Interfaces Config SPI flash FPGA power Ethernet Supply File: hyperram.kicad_sch File: fpga-banks.kicad_sch File: interfaces.kicad_sch File: config-spi.kicad_sch File: fpga-power.kicad_sch File: ethernet.kicad_sch File: supply.kicad_sch File: sodimm.kicad_sch Logo N2 oshw_logo LPDDR4 Test Board Logo N1 antmicro_logo Sheet: / File: lpddr4-test-board.kicad_sch Title: LPDDR4 Test Board Size: A3 Date: 2023-07-13
KiCad E.D.A. eeschema 6.0.11+dfsg-1~bpo11+1 **Rev: 1.1.4** Id: 1/9



XC7K70T-1FBG484C XC7K70T-1FBG484C BANK13 O_L1P_T0_13 O_L1N_T0_13 O_L2P_T0_13 0_L2N_T0_13 0_L3P_T0_DQS_13 _L3N_T0_DQS_13 O_L4P_T0_13 IO_L4P_T0_D04_14 G 10_L4P_10_D04_14 10_L4N_T0_D05_14 10_L5P_T0_D06_14 10_L5N_T0_D07_14 10_L6P_T0_FCS_B_14 10_L6N_T0_D08_REF_14 10_L6N_T0_D08_REF_14 10_L6N_T0_D08_REF_14 AUX_JTAG_TCK W22)_L4N_T0_13 O_L5P_T0_13 O_L5N_T0_13 0_L6P_T0_13 0_L6N_T0_VREF_13 AUX_JTAG_TMS> _L7P_T1_13 17N T1 13 IO L7N T1 D10 14 10_L8P_T1_D11_14 10_L8N_T1_D12_14 10_L9P_T1_DQS_14 10_L9P_T1_DQS_14 _L8P_T1_13 AB21 FPGA_AB21_BALL FPGA_AA21_BALL FPGA_AB22_BALL O_L8N_T1_13 O_L9P_T1_DQS_13 AA2: _L9N_T1_DQS_13 IO_L9N_T1_DQS_D13_14 F21 | 10_L10P_T1_D14_14 | 10_L10P_T1_D15_14 | 10_L10P_T1_SRCC_14 | 10_L11P_T1_SRCC_14 0 L10P T1 13 UART1_RX> _L10N_T1_13 O L11P T1 SRCC 13 AUX_JTAG_TDI> W20 _L11N_T1_SRCC_13 0 L12P T1 MRCC 13 O_L12N_T1_MRCC_13 O_L13P_T2_MRCC_13 O_L13N_T2_MRCC_13 HR_DQ7 W17 HR_RW Y17 UARTO_RX AR18 O_L14P_T2_SRCC_13 IO_L14N_T2_SRCC_14 M18 O L14N T2 SRCC 13 _L15P_T2_DQS_13 UARTO TX AB18 UARTO TX AB18 HR_CKP AB15 HR_CKN AB16 HR_CS A416 HR_DQ2 A414 HR_DQ1 A415 HR_DQ1 J416 AB18 O_L15N_T2_DQS_13 _L16P_T2_13 0_L16N_T2_13 0_L17P_T2_13 _L17N_T2_13 _L18P_T2_13 _L18N_T2_13 0_L19P_T3_13 10_L19N_T3_A09_D25_VRFF_14 10_L20P_T3_A08_D24_14 10_L20N_T3_A07_D23_14 HR_RST> _L19N_T3_VREF_13 0_L20P_T3_13 0_L20N_T3_13 10_L21P_T3_A07_D23_14 P20x 10_L21P_T3_D0S_14 R17x 10_L21N_T3_D0S_A06_D22_14 P17x 10_L22P_T3_A05_D23_T4 P17x O_L21P_T3_DQS_13 O_L21N_T3_DQS_13 HR_DQ6 Y16 HR_DQ3 W14 IO_L22P_T3_A05_D20_14 IO_L22P_T3_A05_D20_14 IO_L22N_T3_A03_D19_14 IO_L23N_T3_A02_D18_14 IO_L23N_T3_A02_D18_14 0 L22N T3 13 V15 0 L23N T3 13 0_L24P_T3_13 _L24N_T3_13 25 13

Clock source

ASFL1-100.000MHZ-L-T

VDD 4 3V3_SYS OUT GCLK100

3V3_SYS ___ STDB

2 GND

INTERFACES

INTERFACES

XC7K70T-1FBG484C XC7K70T-1FBG484C O_L1P_T0_AD0P_15 D_L1N_T0_AD0N_15 ETH_REF_CLK D_L2P_T0_AD8P_15 D_L2N_T0_AD8N_15 0 L3P TO DQS AD1P 15 ETH_TX_EN ETH_RXD3 0 14P TO AD9P 15 A14 D_L4N_T0_AD9N_15 O_L5P_T0_AD2P_15 D_L5N_T0_AD2N_15 O_L6P_T0_15 IO_L6N_T0_VREF_15 _L7P_T1_AD10P_15 ETH_INT_N ETH_RXD0 0 I 7N T1 AD10N 15 B16 _L8P_T1_AD3P_15 D L8N T1 AD3N 15 B1: _L9P_T1_DQS_AD11P_15 A15 L9N_T1_DQS_AD11N_15 B1 0 L10P T1 AD4P 15 A18 _L10N_T1_AD4N_15 D L11P T1 SRCC AD12P 15 O_L11N_T1_SRCC_AD12N_15 ETH_RX_CLK D L12P T1 MRCC AD5P 15 D_L12N_T1_MRCC_AD5N_15 ETH_TX_CLK O_L13P_T2_MRCC_15 O_L13N_T2_MRCC_15 ×E16 ETH_RSTN> _L14P_T2_SRCC_15 10_L21P_T3_DQS_16 A9 X ×D1 ×H1 ×G1 114N T2 SRCC 15 IO_L21N_T3_DQS_16 A8 O_L15N_T2_DQS_ADV_B_15 D_L16P_T2_A28_15 0_L16N_T2_A27_15 0_L17P_T2_A26_15 D_L17N_T2_A25_15 D19 D20 D_L18P_T2_A24_15 _L18N_T2_A23_15 SD_DAT3 0 119P T3 A22 15 SD_CMD> _L19N_T3_A21_VREF_15 L20P T3 A20 15 ^A19 _L20N_T3_A19_15 SD_DAT1 C22 _L21P_T3_DQS_15

LPDDR4-TESTBED

U3E	U3D	
XC7K70T-1FBG484C	XC7K70T-1FBG484C	
BANK33	BANK34	
× T6 10_0_VRN_33	IO_0_VRN_34	K4 VRN
VAA5 10 14 D TO 33	IO_L1P_T0_34	L3 CA OA
×AB5 10 L1N TO 33	IO_L1N_T0_34	M3 DMI OA
XAB8 10_L2P_T0_33	I0_L2P_T0_34	K1 DQ02_A
XAB7 10_L2N_T0_33	I0_L2N_T0_34	L1 DQ00_A
AA6 10_L3P_T0_DQS_33	I0_L3P_T0_DQS_34	M2 DQ_S0_P
AA40 10_L3N_10_DQ3_J3	10_L3N_T0_DQS_34	VZ DQ_SU_N
AB10 10 L(N) TO 77	IO_L4P_T0_34	K2 DQUS_A
10_AB10	10_L4N_T0_34 10_L5P_T0_34	NZ DQUI_A
AA8 10_L5N_T0_33	10_L5N_T0_34	N2 DQ07_A
10 W11 N H 10 L6P T0 33	IO_L6P_T0_34	L5 CA_1A
Y11 10 16N TO VDEE 77	IO_L6N_T0_VREF_34	L4 VRFF 34
10_Y11	IO_L7P_T1_34	P2 DQ05_A
× Y6 10_L7N_T1_33	IO_L7N_T1_34	R2 DQ12_A
R7 R7 10_L8P_T1_33 R6 10_L8N_T1_33	IO_L8P_T1_34	DQU6_A
	IO_L8N_T1_34	ME DQU4_A
10_Fab_11_nd2_22	IO_L9P_T1_DQS_34	N/ı
× V0 IO_L9N_T1_DQS_33 × U7	IO_L9N_T1_DQS_34 IO_L10P_T1_34	T1 CKEO_A DQ13_A
× U6 10_L10N_T1_33	IO_L10N_T1_34	U1 DQ15_A
× V7 IO_L11P_T1_SRCC_33	IO_L11P_T1_SRCC_34	P4 [IO P4]
×W7 IO_L11N_T1_SRCC_33	IO_L11N_T1_SRCC_34	R4 IO PA
× Y8 I0_L12P_T1_MRCC_33	IO_L12P_T1_MRCC_34	R3 × (10_K4)
$\times \frac{Y7}{W0}$ IO_L12N_T1_MRCC_33	IO_L12N_T1_MRCC_34	T3 DQ14_A
× W9 10_L13P_T2_MRCC_33	IO_L13P_T2_MRCC_34	T4 10_T4
TITO TO_LISN_IZ_MRCC_33	IO_L13N_T2_MRCC_34	10_03
X910 IO_L14P_T2_SRCC_33 X	IO_L14P_T2_SRCC_34 IO_L14N_T2_SRCC_34	W4 10_V4 10_W4
V10 IO_L15P_T2_DQS_33	IO_L14N_I2_SRCC_34	U2 DQ_S1_P
×W10 IO_L15N_T2_DQS_33	IO_L15N_T2_DQS_34	V2 DO \$1 N
VI11 10 1460 TO 77	IO_L16P_T2_34	
×T10 10_L16N_T2_33	IO_L16N_T2_34	U5 (10 U5)
10_U12 U12 10_L17P_T2_33	IO_L17P_T2_34	V3 10_V3 W2 P0000 A
VU11 VI11 VI19 VI19 VI19 VI19 VI19 VI19 VI	IO_L17N_T2_34	NE DQU8_A
	IO_L18P_T2_34	P5 × (10_N5)
10_K12	IO_L18N_T2_34 IO_L19P_T3_34	W5 ×
10_V12 Y12 10_L19N_T3_VREF_33	IO_L19P_I3_34	Y4 VREF_34
10_AA11 AA11 10_L20P_T3_33	10_L20P_T3_34	W1 DMI_1A
AB11 10 1 20N TZ ZZ	IO_L20N_T3_34	V1 DQ09 A
×Y13 10 L21P T3 DQS 33	IO_L21P_T3_DQS_34	Y3 CK A P
AA13 IO_L21N_T3_DQS_33	IO_L21N_T3_DQS_34	Y2 CK_A_N
AB13 10_L22P_T3_33	I0_L22P_T3_34	AA1 DQ10_A
XB12 IO_L22N_T3_33	IO_L22N_T3_34	AB1 DQ11_A
V12 10_L23P_I3_33	IO_L23P_T3_34	AB2 CAS_A
10_V12	10_L23N_T3_34 10_L24P_T3_34	AA4 CA2_A
U13 10_L24P_13_33	10_L24P_13_34 10_L24N_T3_34	
×T14 10_25_VRP_33	IO_25_VRP_34	
	.52557111 25 1	

UNUSED

L21N_T3_DQS_A18_15

D L22N T3 A16 15

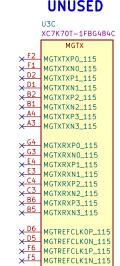
SD_CLK D22
TH_TXD1 B20

B21

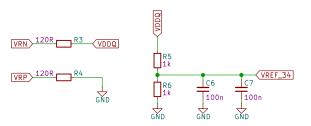
O_L23N_T3_FWE_B_15 O_L24P_T3_RS1_15

0_L24N_T3_RS0_15

25 15

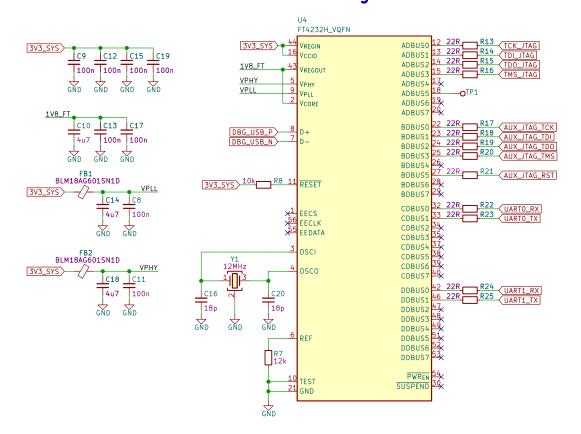


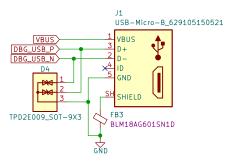
LPDDR VREF



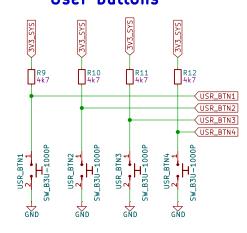
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Size: A3 Date: 2023-07-13	Rev: 1.1.4
KiCad E.D.A. eeschema 6.0.11+dfsg-1~bpo11+1	ld: 3/9

Debug UART

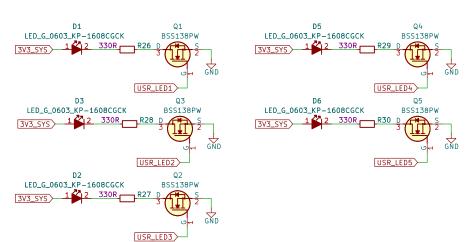




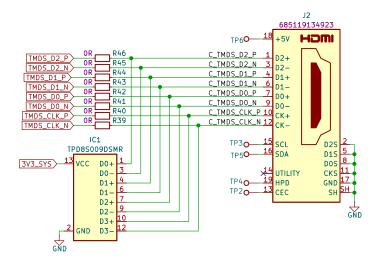
User buttons



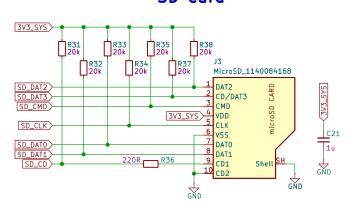
User LEDs



HDMI



SD card



Sheet: /Interfaces/
File: interfaces.kicad_sch

Title: LPDDR4 Test Board

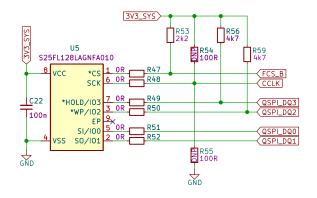
Size: A3 Date: 2023-07-13 Rev: 1.1.4

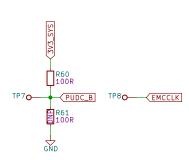
KiCad E.D.A. eeschema 6.0.11+dfsg-1-bpo11+1 Id: 4/9

Master SPI Quad (x4) configuration scheme

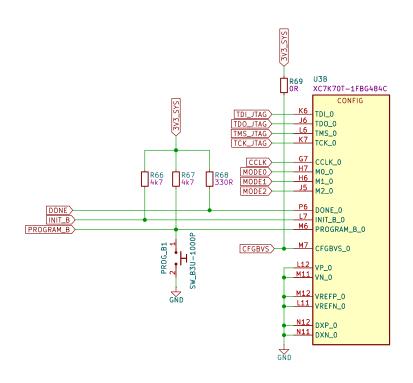
Follows Figure 2–14 7 Series FPGAs Configuration User Guide UG470 (v1.13.1)

(Q)SPI flash

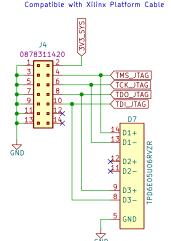




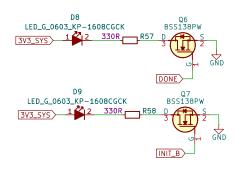
FPGA BANK 0



JTAG Connector Compatible with Xilinx Platform Cable

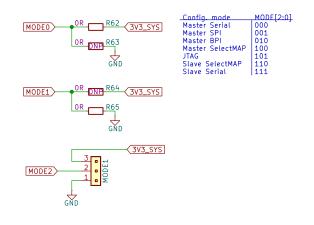


STATUS LEDs



Configuration Modes

For details, see UG470 p. 21

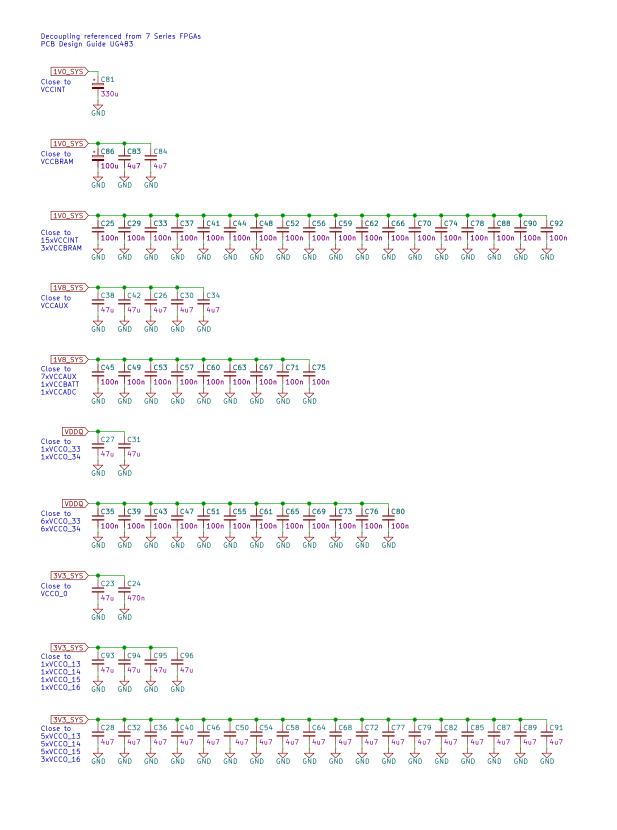


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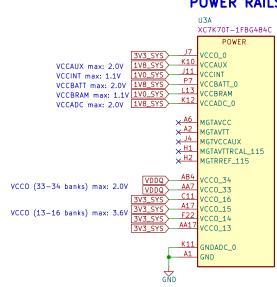
Title: LPDDR4 Test Board

 Size: A3
 Date: 2023-07-13
 Rev: 1.1.4

 KiCad E.D.A. eeschema 6.0.11+dfsg-1-bpo11+1
 Id: 5/9

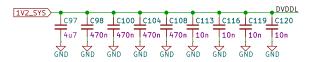


POWER RAILS

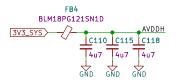


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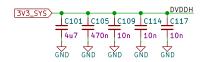
DVDDL decoupling



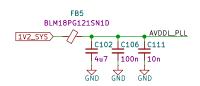
AVDDH decoupling



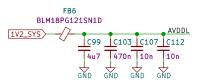
DVDDH decoupling



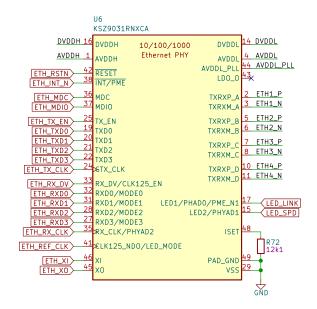
AVDDL_PLL decoupling



AVDDL decoupling



PHY

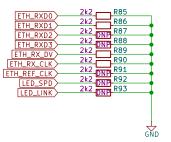


1M8____R73

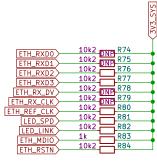
C122 22p GND

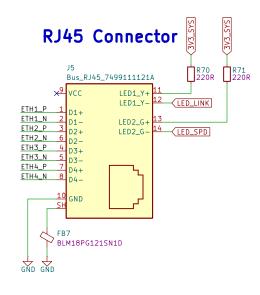
Y2 25MHz 1113 C1211N

Pull down resistors

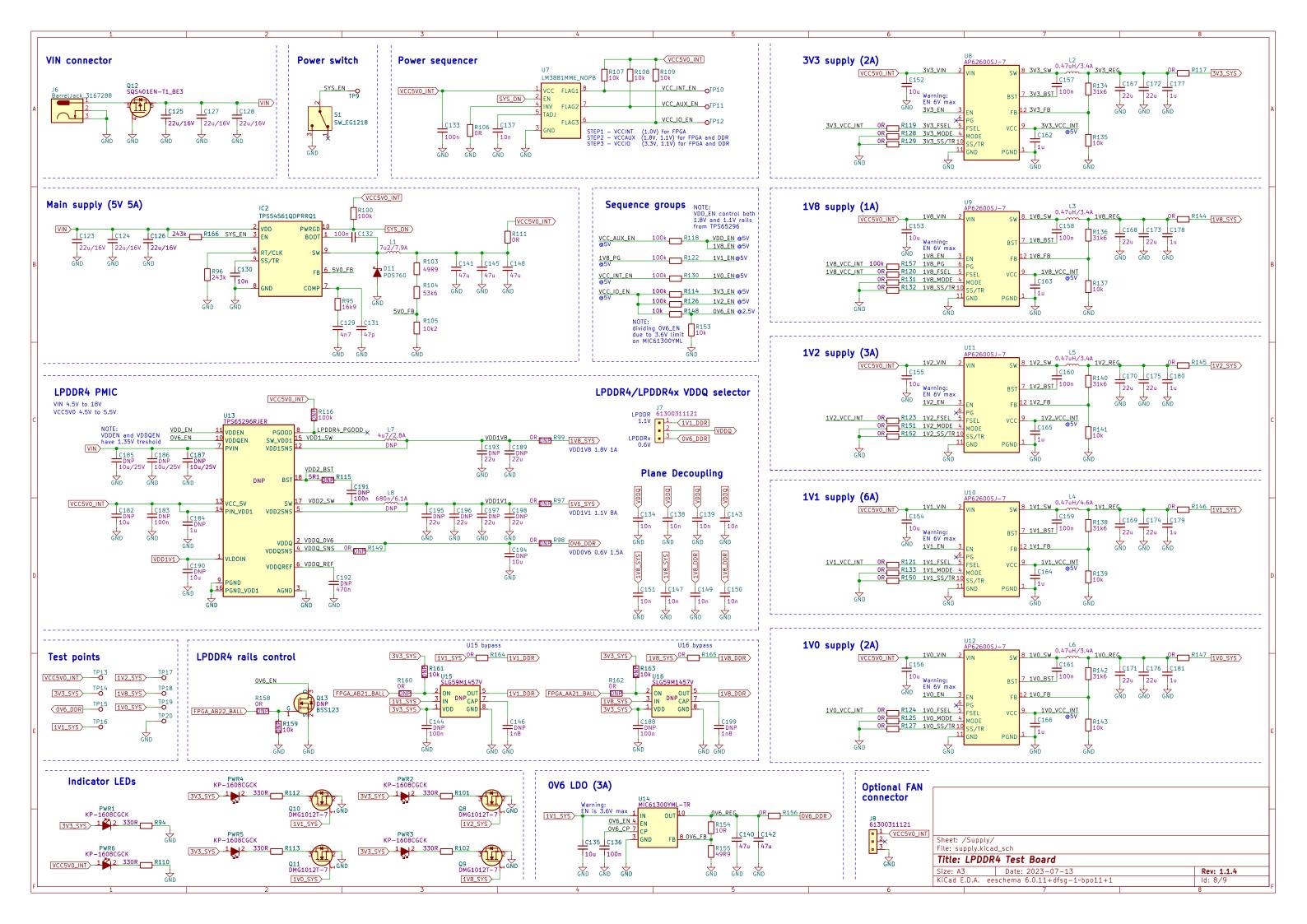


Pull up resistors





neet: /Ethern	et /	
le: ethernet.k		
itle: LPDD	R4 Test Board	
ze: A3	Date: 2023-07-13	Rev: 1.1.4
Cad E.D.A. e	eschema 6.0.11+dfsg-1~bpo11+1	ld: 7/9
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DDR4 SODIMM connector 10_P4 199 199
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255 255 1V1_DDR> 1V8_DDR 1V1_DDR> VDDQ 250 252 254 256 258 260 1V8_DDR VDDQ DNP ddr5—testbed SHIELD S1 Mechanical protection SP1 Spacer_H5.0mm_9774050151 ×¹ Sheet: /SO-DIMM/ File: sodimm.kicad_sch Title: LPDDR4 Test Board Size: A3 Date: 2023-07-13
KiCad E.D.A. eeschema 6.0.11+dfsg-1~bpo11+1