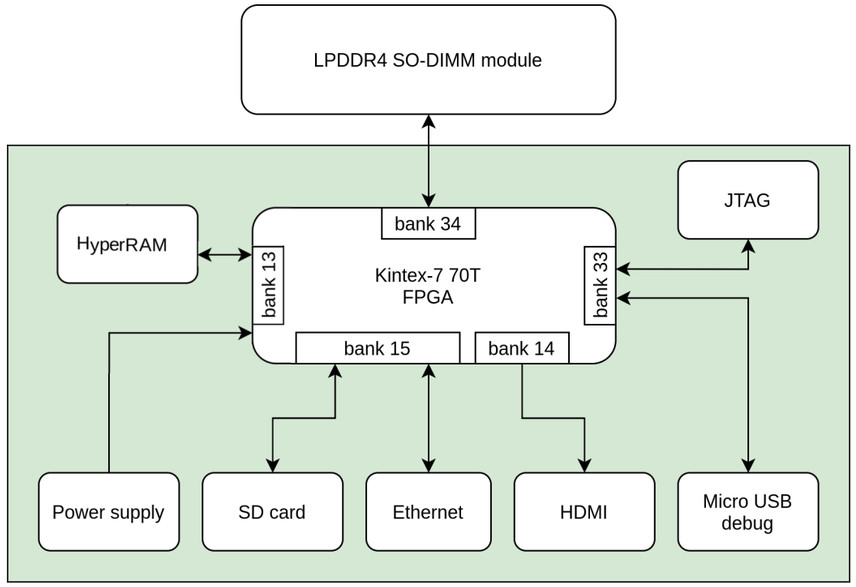
LPDDR4 Test Board



Sheet: HyperRAM
File: hyperram.sch

Sheet: FPGA Banks
File: fpga-banks.sch

Sheet: Interfaces
File: interfaces.sch

Sheet: Config SPI flash
File: config-spi.sch

Sheet: FPGA power
File: fpga-power.sch

Sheet: Ethernet
File: ethernet.sch

Sheet: Supply
File: supply.sch

Sheet: SO-DIMM
File: sodimm.sch

Logo N1
oshw_logo

Logo N2
antmicro_logo

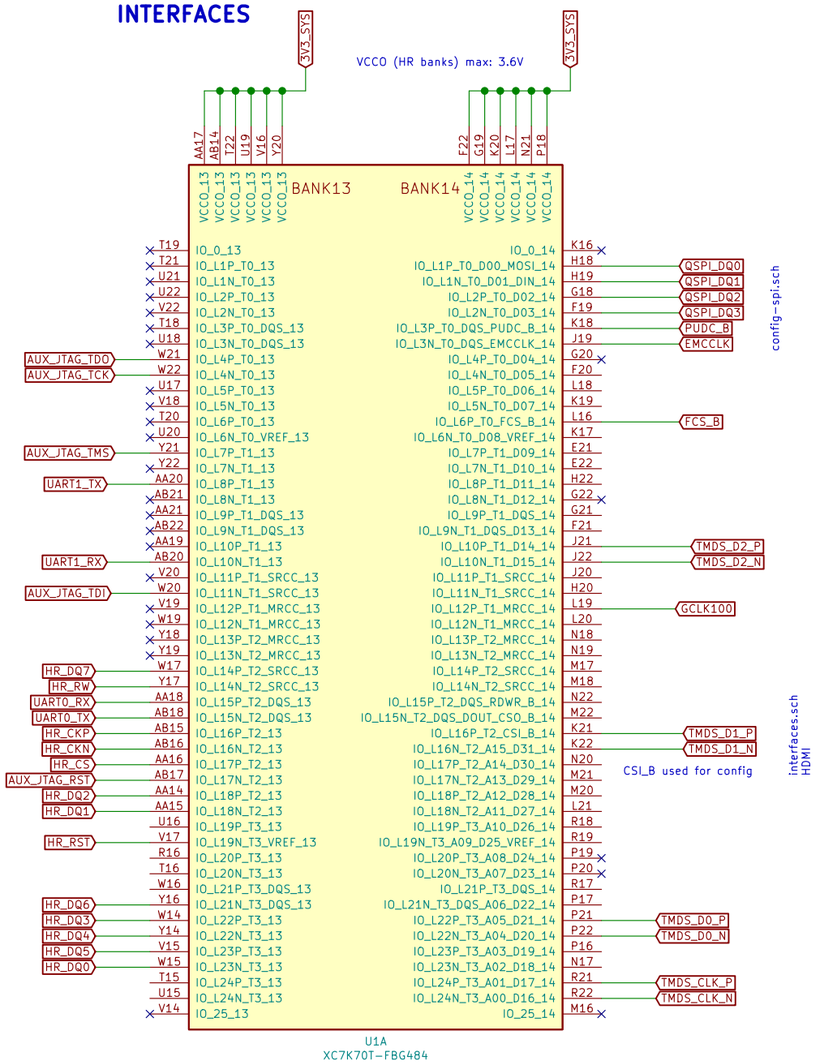
LPDDR4 Test Board

Sheet: /
File: lpddr4-test-board.sch

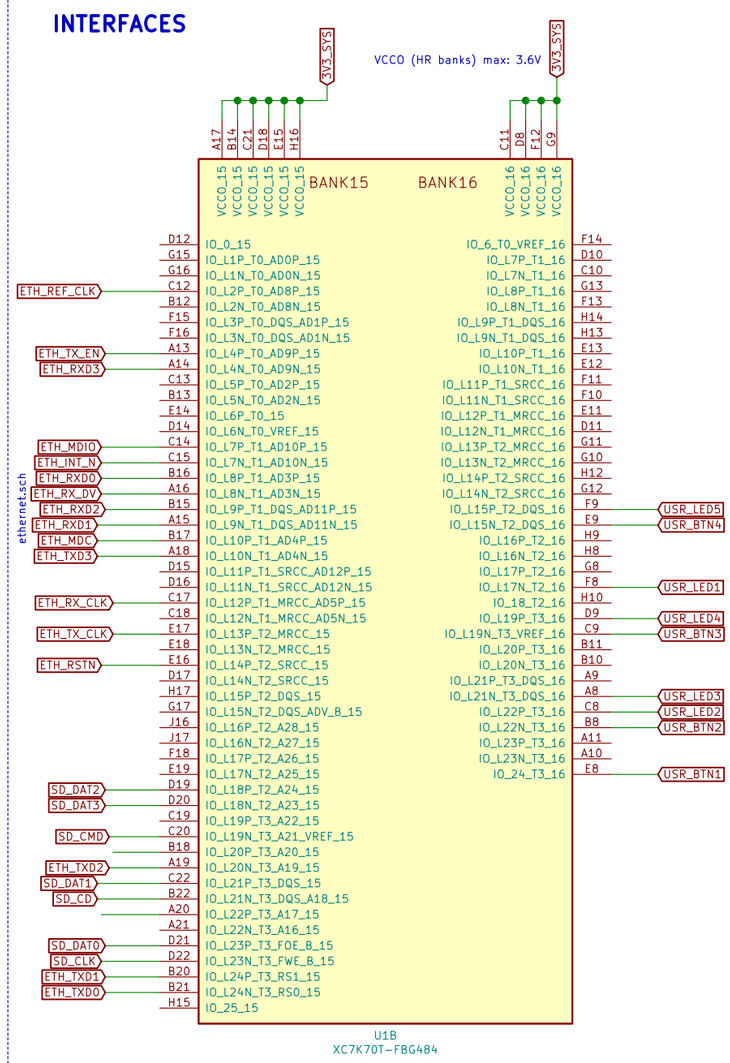
Title: LPDDR4 Test Board

Size: A3	Date:	**Rev: 1.0.4**
KiCad E.D.A. eeschema 5.1.5+dfsg1-2bpo10+1		Id: 1/9

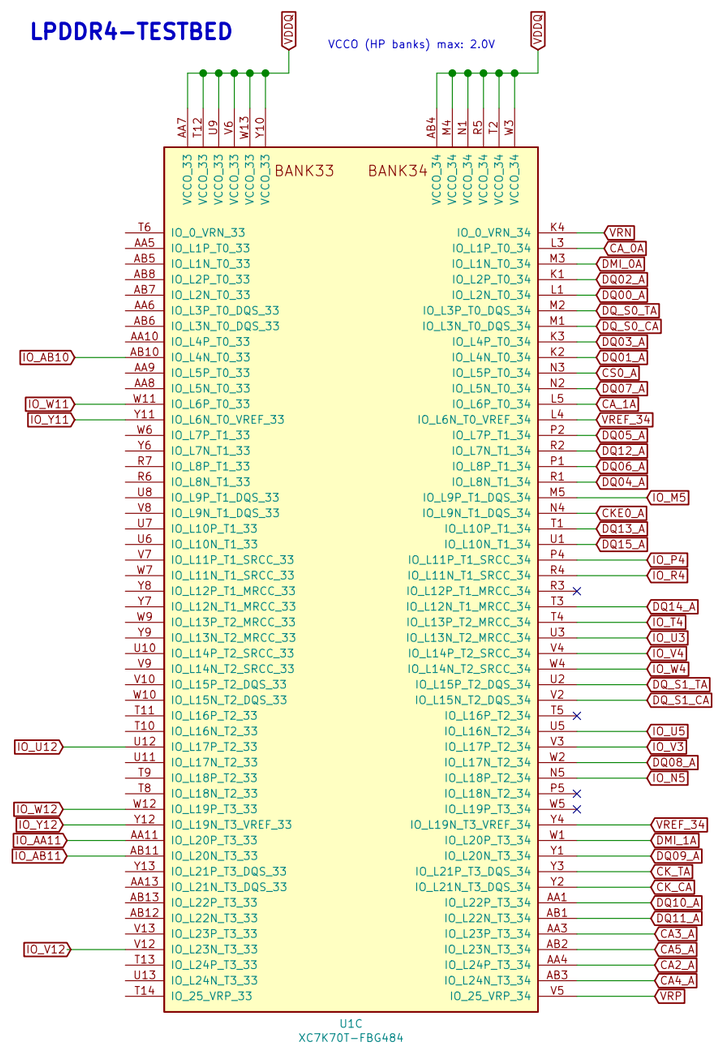
INTERFACES



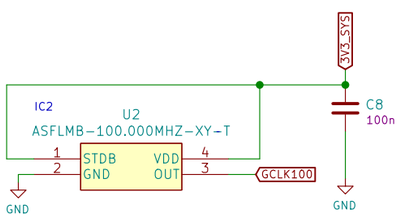
INTERFACES



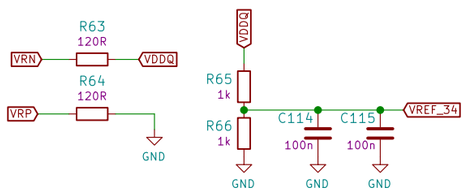
LPDDR4-TESTBED



Clock source



LPDDR VREF

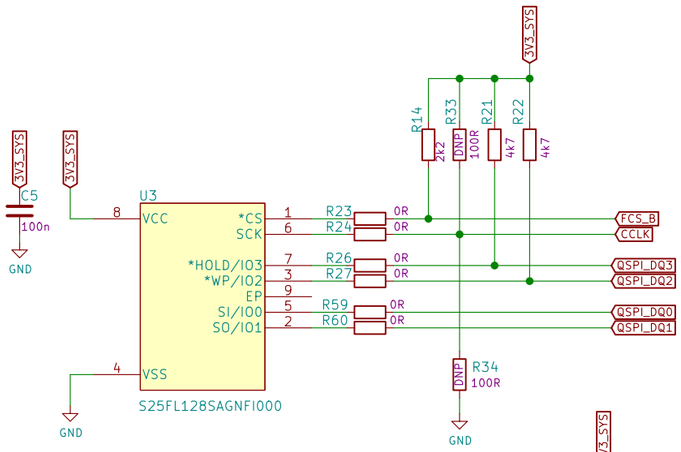


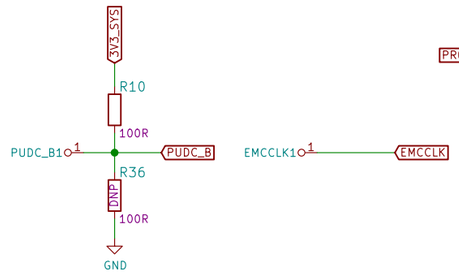
Sheet: /FPGA Banks/		
File: fpga-banks.sch		
Title: LPDDR4 Test Board		
Size: A3	Date:	**Rev: 1.0.4**
KiCad E.D.A. eeschema 5.1.5+dfsg1-2bpo10+1		Id: 2/9

Master SPI Quad (x4) configuration scheme

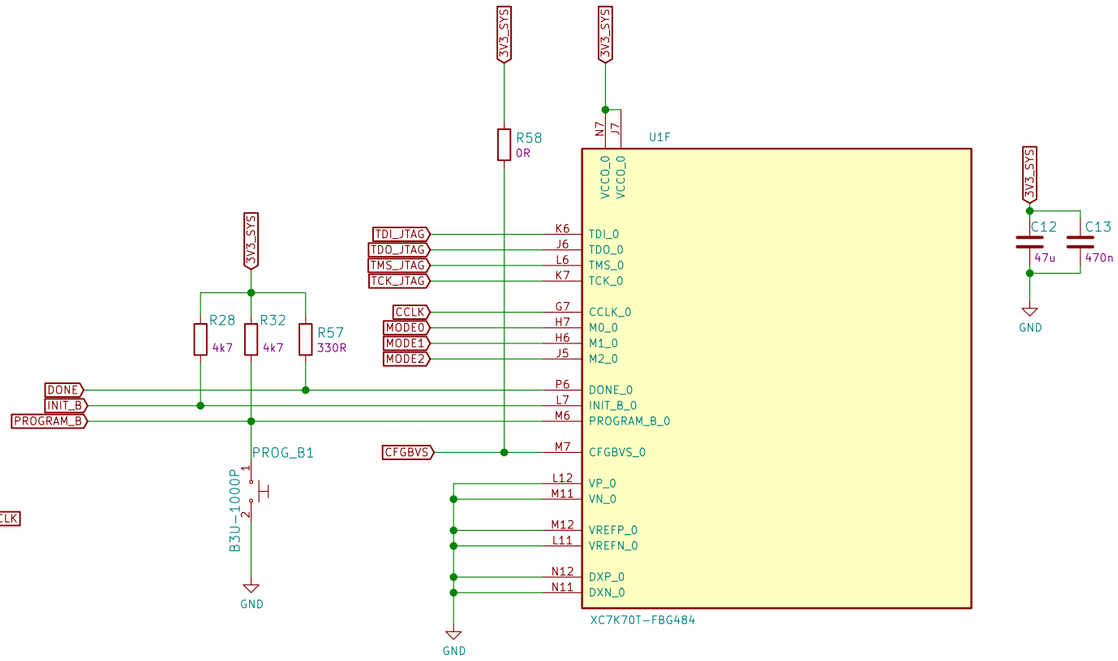
Follows Figure 2–14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

(Q)SPI flash



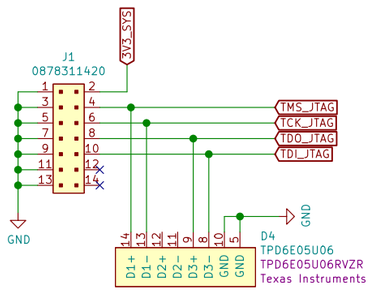


FPGA BANK 0

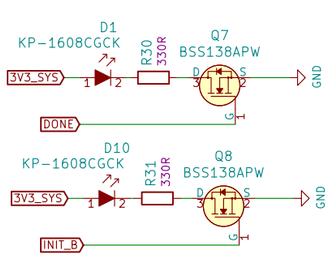


JTAG Connector

Compatible with Xilinx Platform Cable

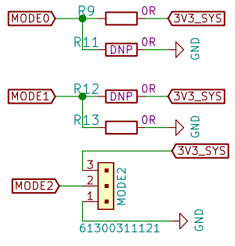


STATUS LEDs



Configuration Modes

For details, see UG470 p. 21



Config. mode	MODE[2:0]
Master Serial	000
Master SPI	001
Master BPI	010
Master SelectMAP	100
JTAG	101
Slave SelectMAP	110
Slave Serial	111

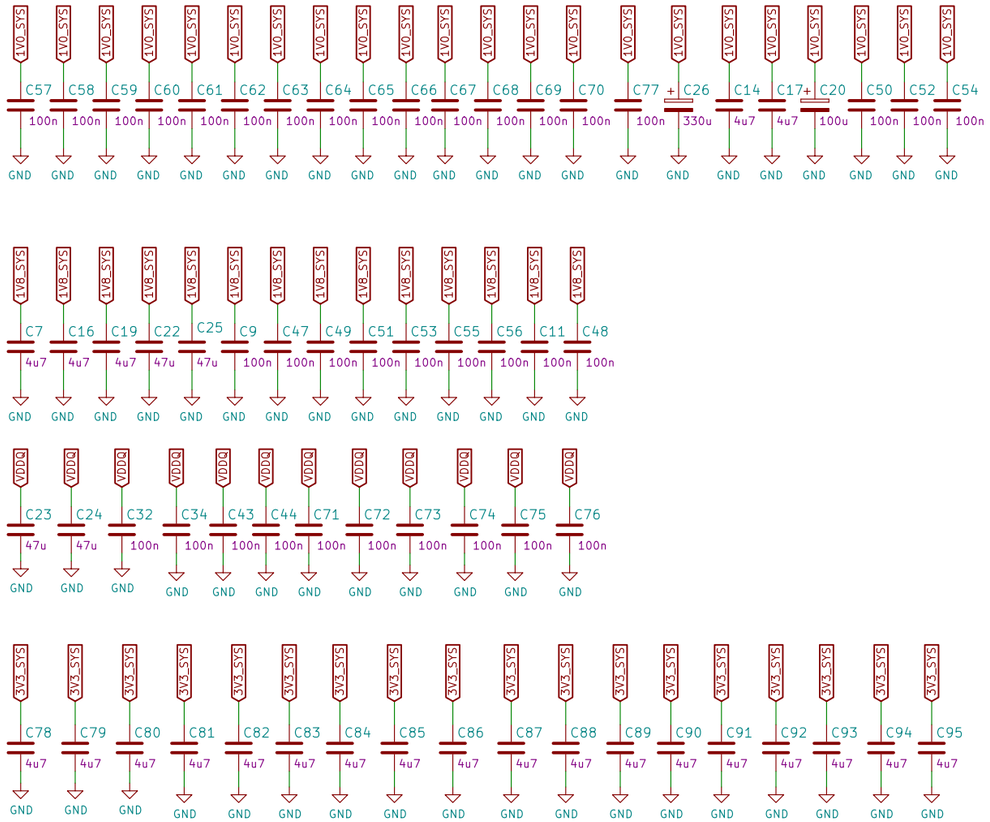
Sheet: /Config SPI flash/
File: config-spi.sch

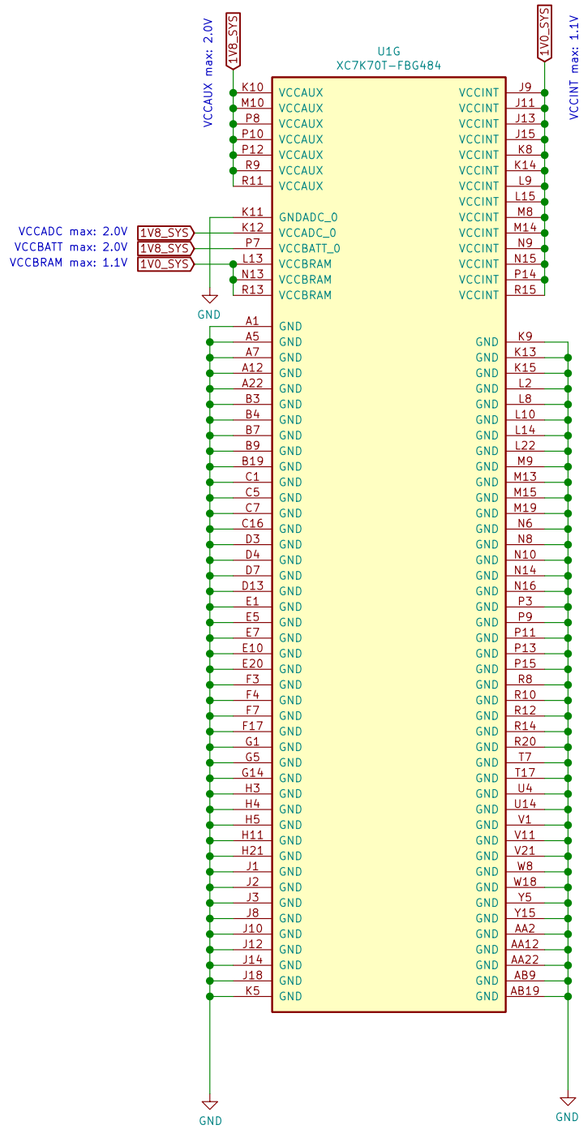
Title: LPDDR4 Test Board

Size: A3	Date:	Rev: 1.0.4
KiCad E.D.A. eeschema 5.1.5+dfsg1-2bpo10+1		Id: 3/9

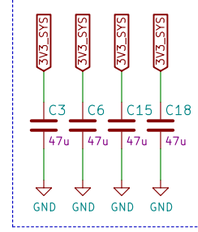
POWER RAILS

Decoupling referenced from 7 Series FPGAs
PCB Design Guide UG483

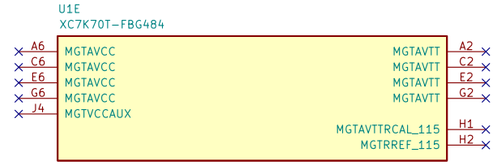


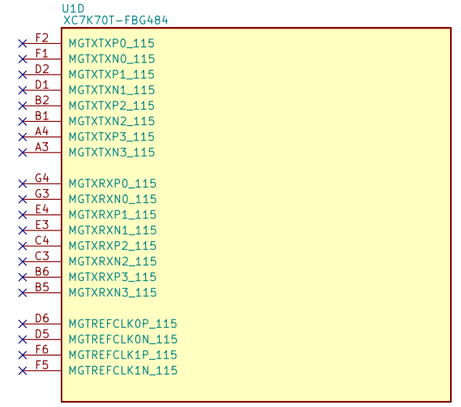


Place close to FPGA banks power supply



UNUSED



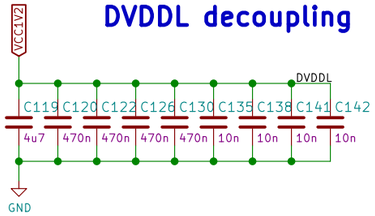


Sheet: /FPGA power/
File: fpga-power.sch

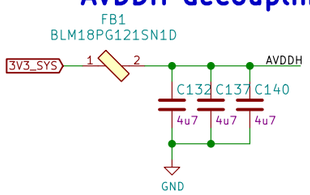
Title: LPDDR4 Test Board

Size: A3	Date:	**Rev: 1.0.4**
KiCad E.D.A. eeschema 5.1.5+dfsg1-2bpo10+1		Id: 4/9

DVDL decoupling

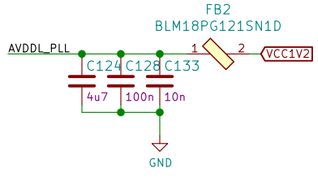


AVDDH decoupling

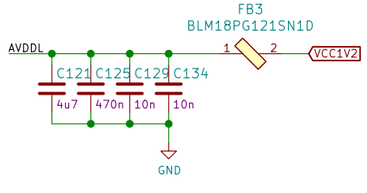


DVDDH decoupling

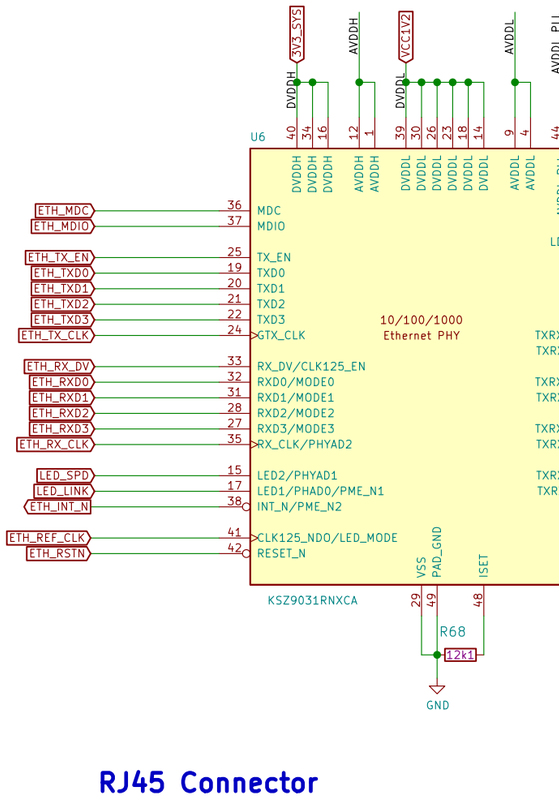
AVDDL_PLL decoupling



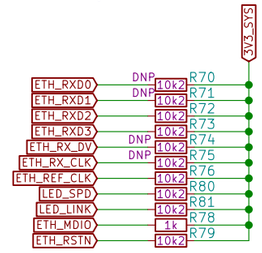
AVDDL decoupling



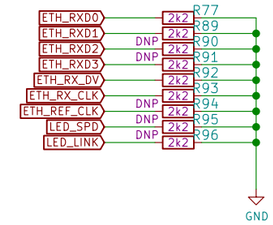
PHY



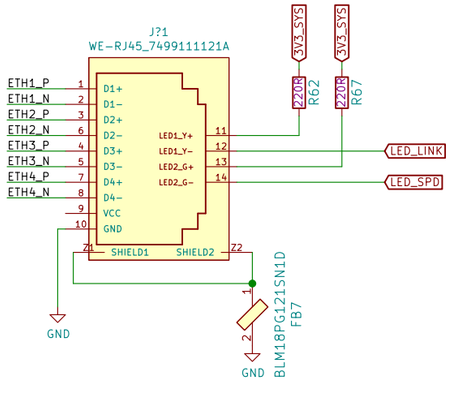
Pull up resistors



Pull down resistors



RJ45 Connector



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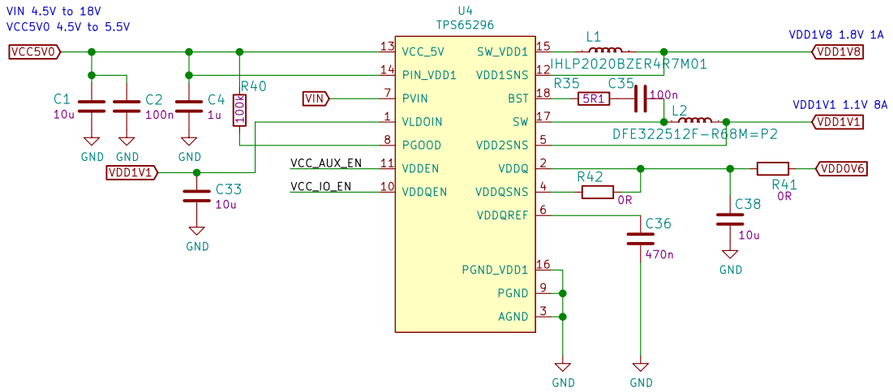
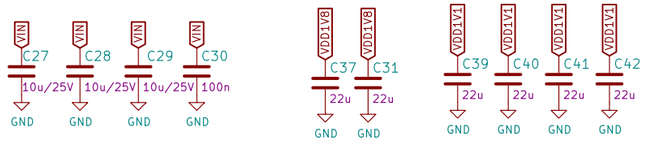
Title: LPDDR4 Test Board		
Size: A3	Date:	**Rev: 1.0.4**
KiCad E.D.A. eeschema 5.1.5+dfsg1-2bpo10+1		Id: 5/9

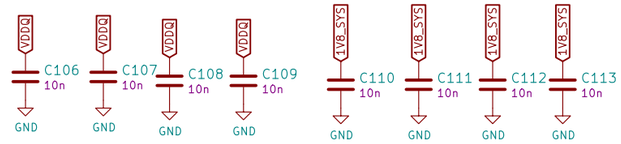
LPDDR4 PMIC



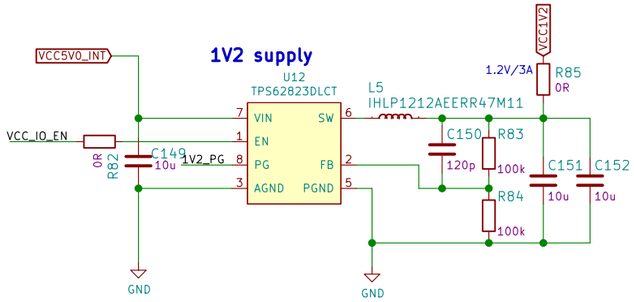
Filtering



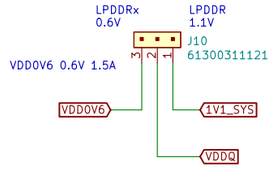
Plane Decoupling



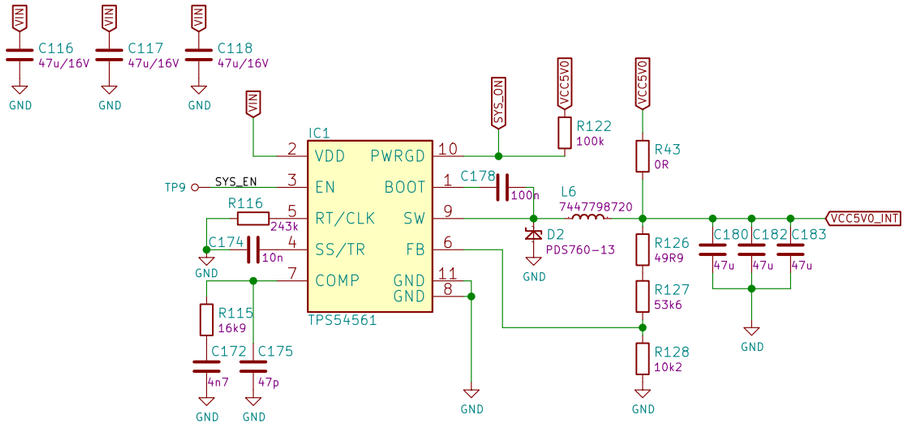
1V2 supply



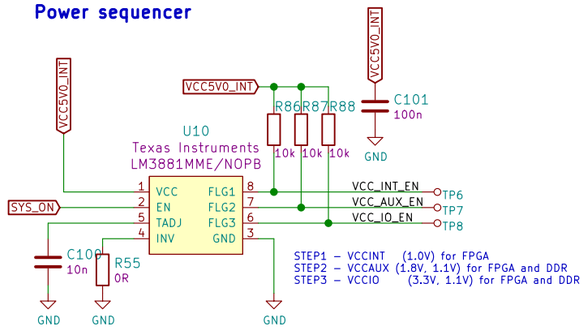
LPDDR4/LPDDR4x VDDQ selector



Main supply (5V 5A)

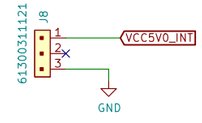


Power sequencer

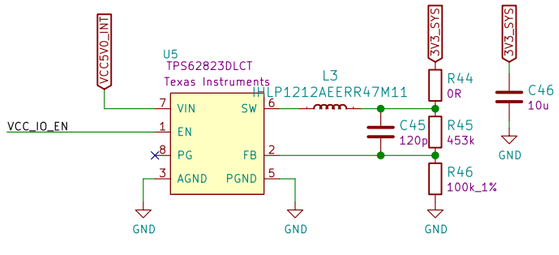


Shunt resistors

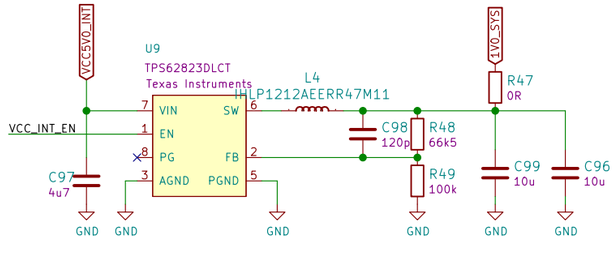
Optional FAN connector



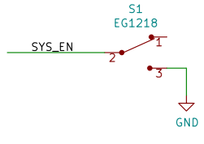
3V3 supply (2A)



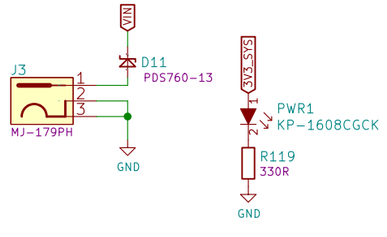
VCCINT (1.0V 2A)



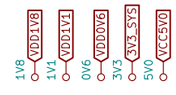
Power switch



Input power connector



Probes



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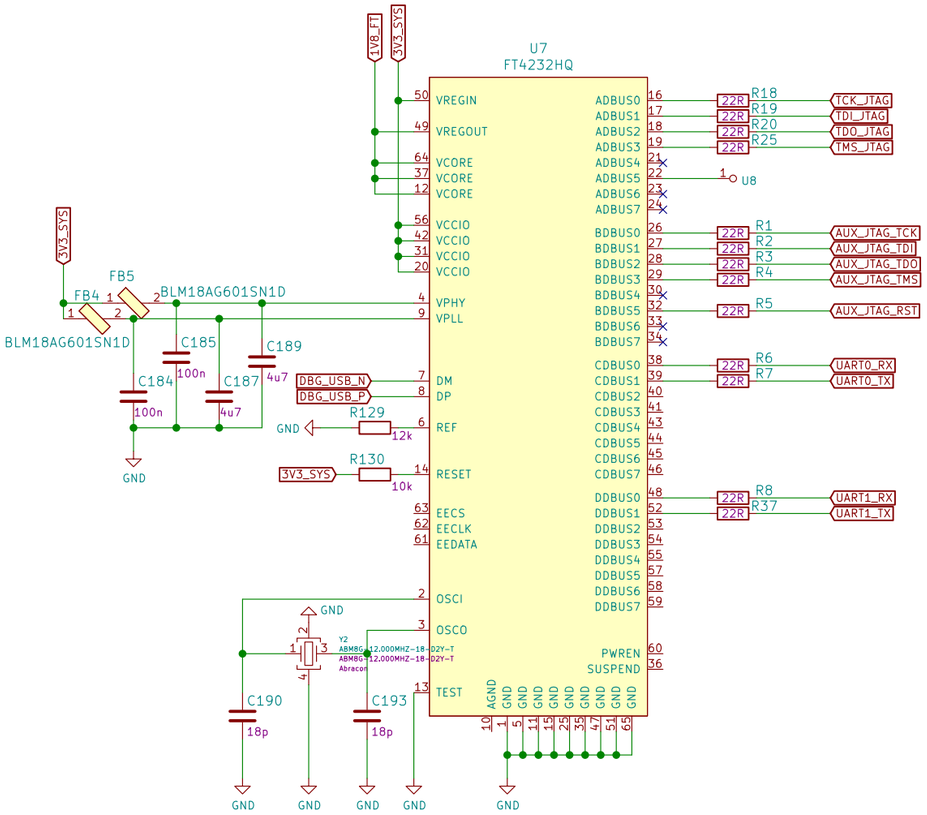
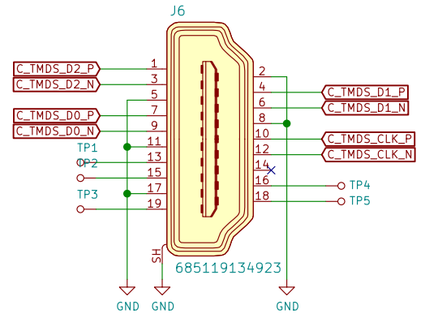
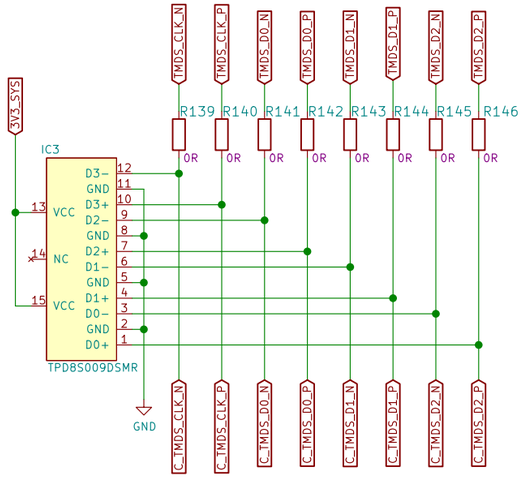
Title: LPDDR4 Test Board	
Size: A3	Date:
KiCad E.D.A. eeschema 5.1.5+dfsg1-2bpo10+1	Id: 6/9
	Rev: 1.0.4

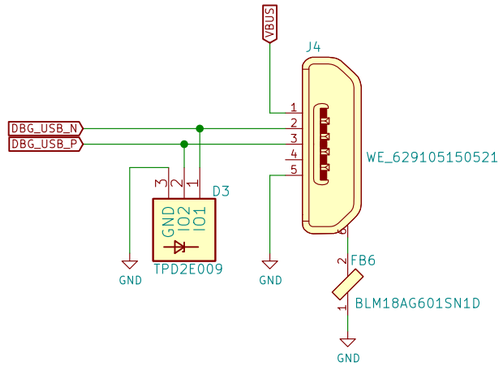
Debug UART



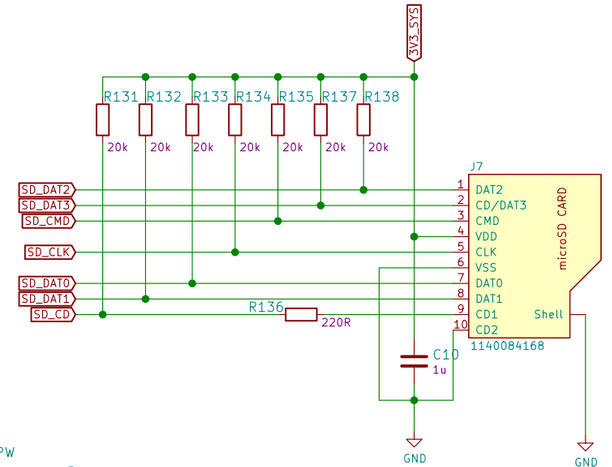
HDMI



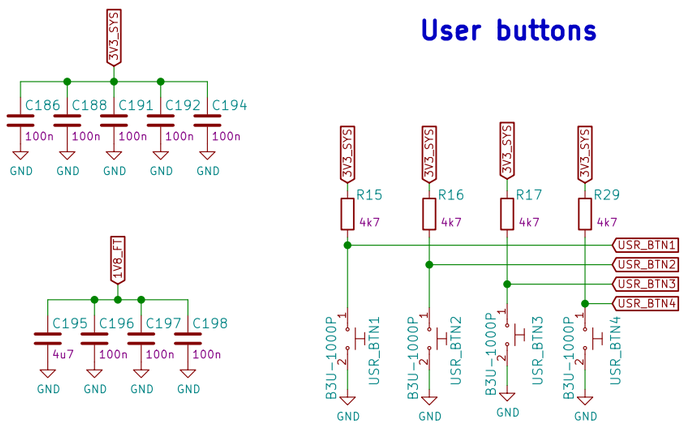




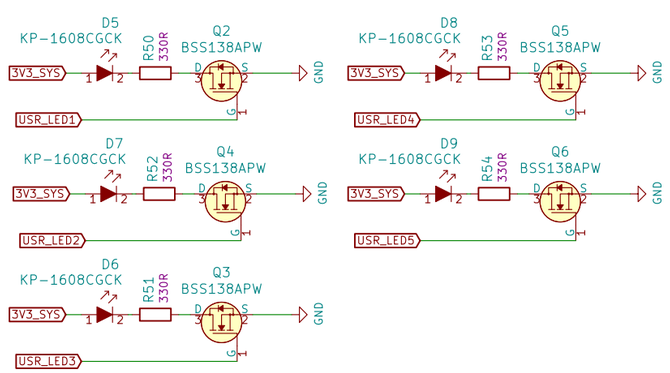
SD card



User buttons



User LEDs



Sheet: /Interfaces/	
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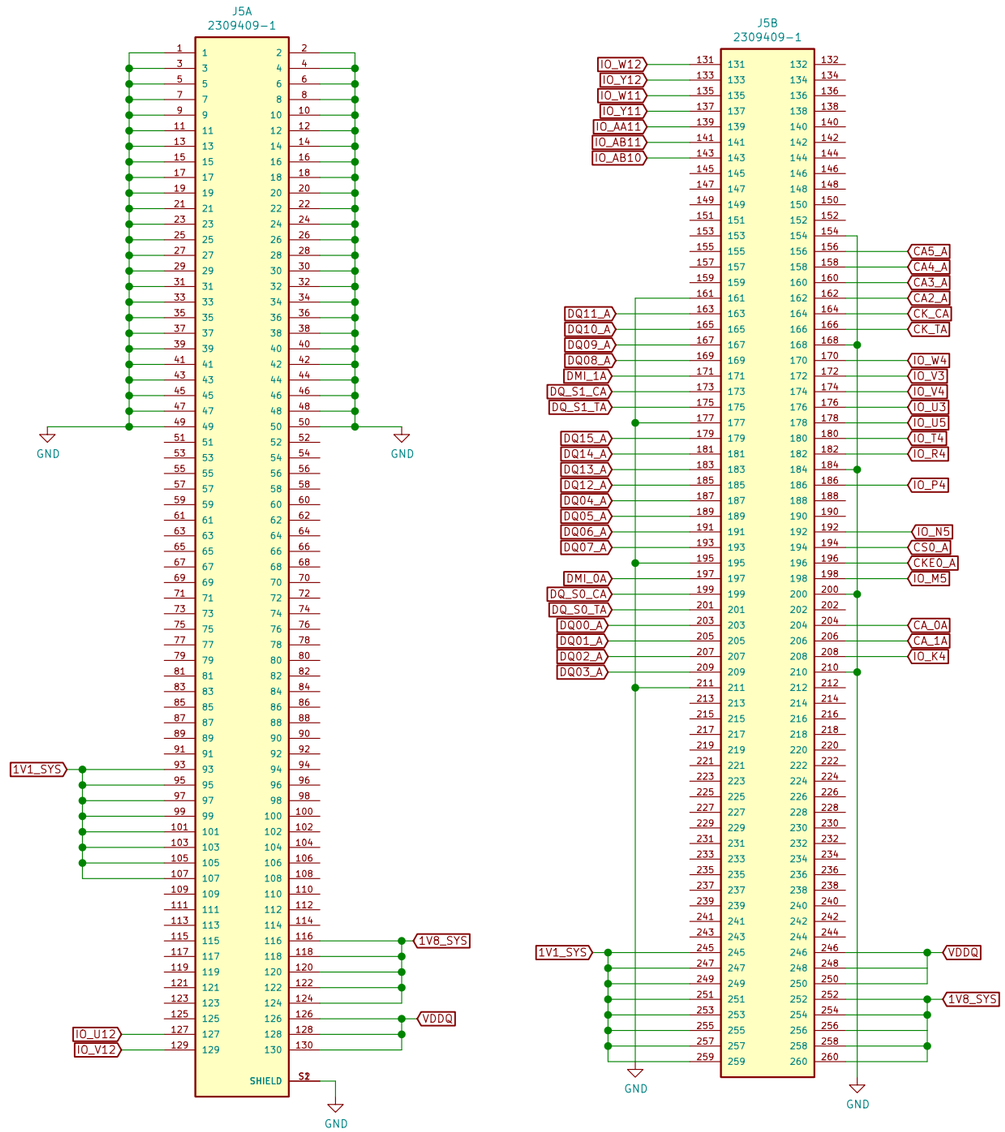
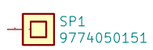
Title: LPDDR4 Test Board	
Size: A3	Date:
KiCad E.D.A. eeschema 5.1.5+dfsg1-2bpo10+1	Id: 7/9

Rev: 1.0.4

DDR4 SODIMM connector



Mechanical protection



Sheet: /SO-DIMM/	
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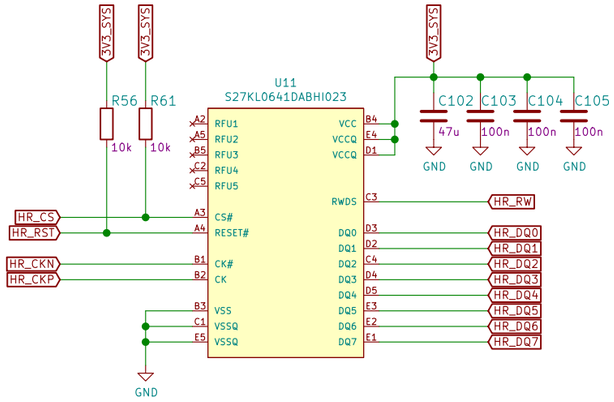
Title: LPDDR4 Test Board	
Size: A3	Date:
KiCad E.D.A. eeschema 5.1.5+dfsg1-2bpo10+1	Id: 8/9

Rev: 1.0.4

HyperRAM



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Size: A3	Date:	**Rev: 1.0.4**
KiCad E.D.A. eeschema 5.1.5+dfsg1-2bpo10+1		Id: 9/9