

LPDDR4 Test Board

A

B

C

D

E

F

A

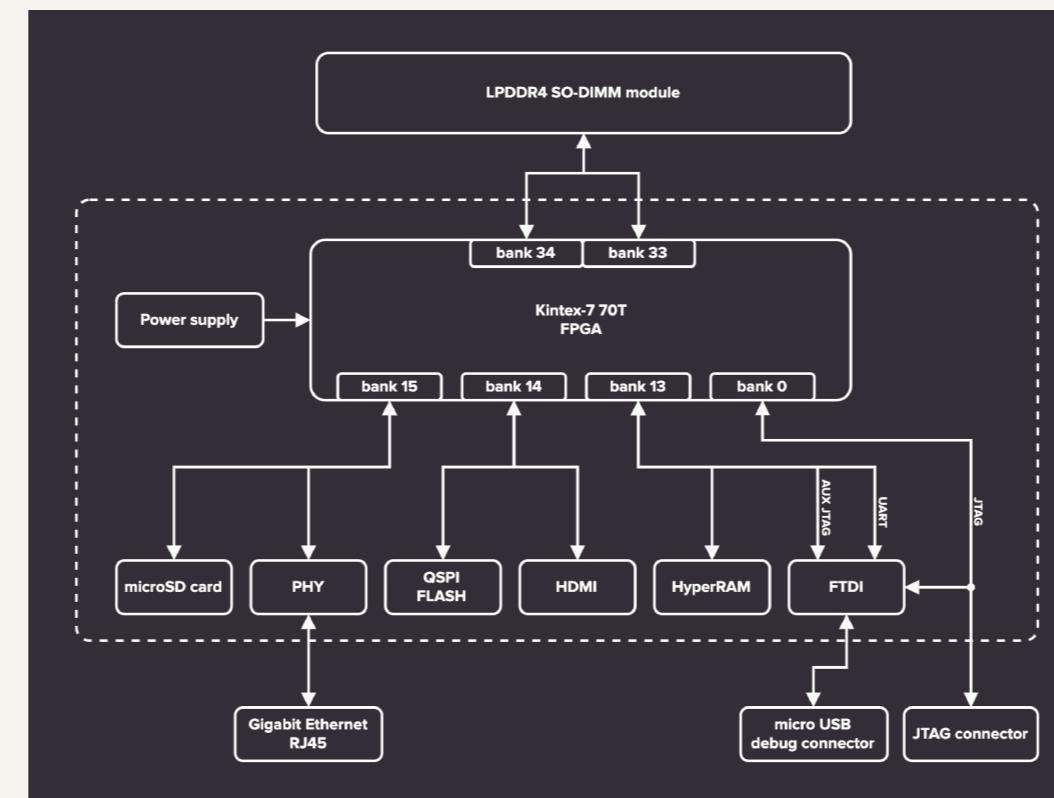
B

C

D

E

F



HyperRAM

File: hyperram.kicad_sch

FPGA Banks

File: fpga-banks.kicad_sch

Interfaces

File: interfaces.kicad_sch

Config SPI flash

File: config-spi.kicad_sch

FPGA power

File: fpga-power.kicad_sch

Ethernet

File: ethernet.kicad_sch

Supply

File: supply.kicad_sch

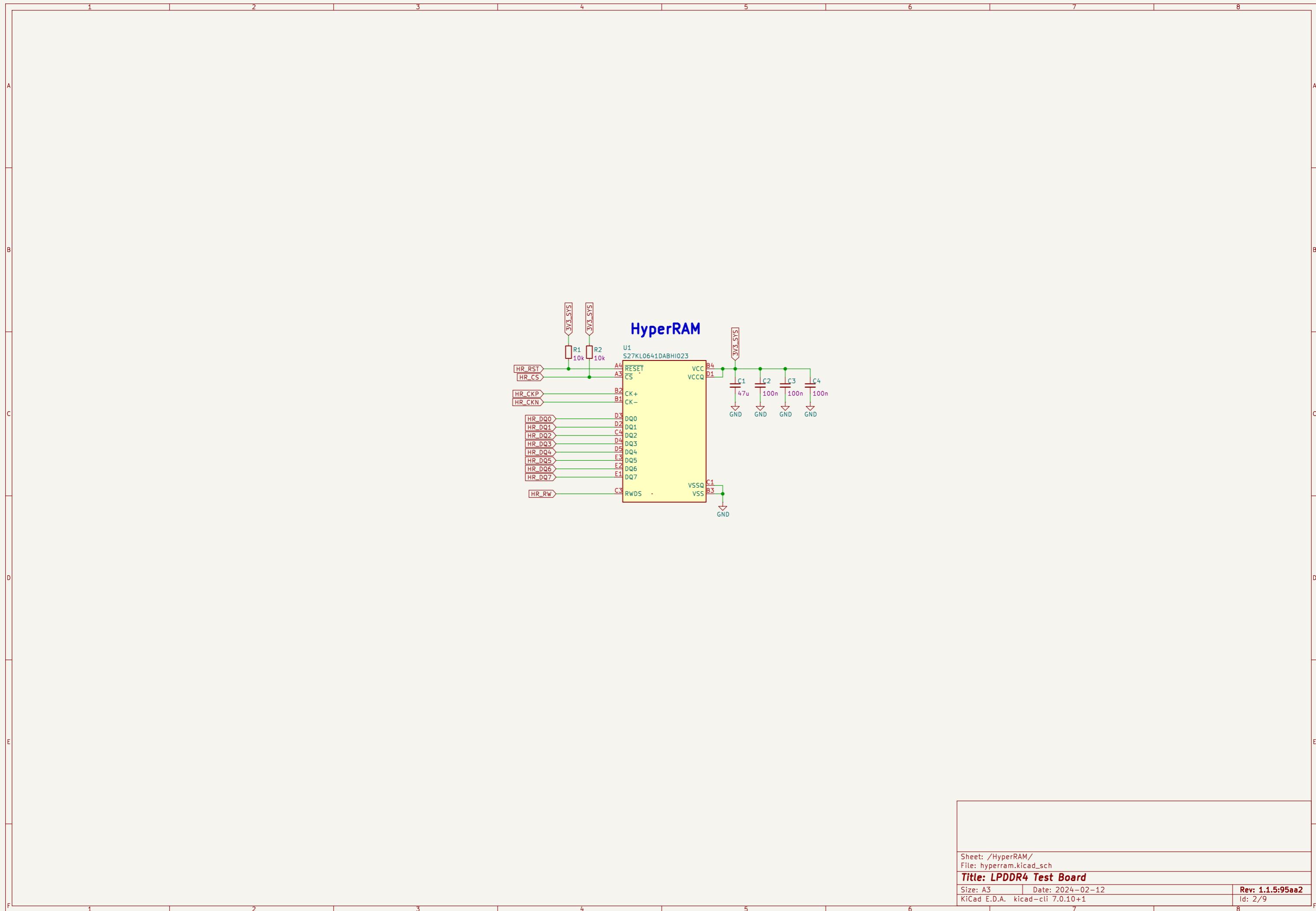
SO-DIMM

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Logo N2
oshw_logoLogo N1
antmicro_logo

LPDDR4 Test Board

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KiCad E.D.A. kicad-cli 7.0.10+1Rev: 1.1.5:95aa2
Id: 1/9

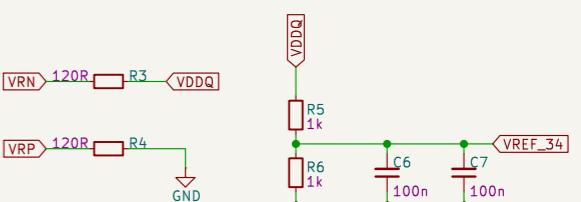
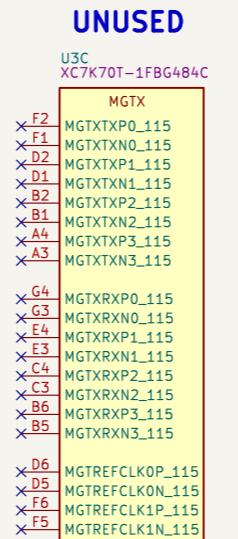
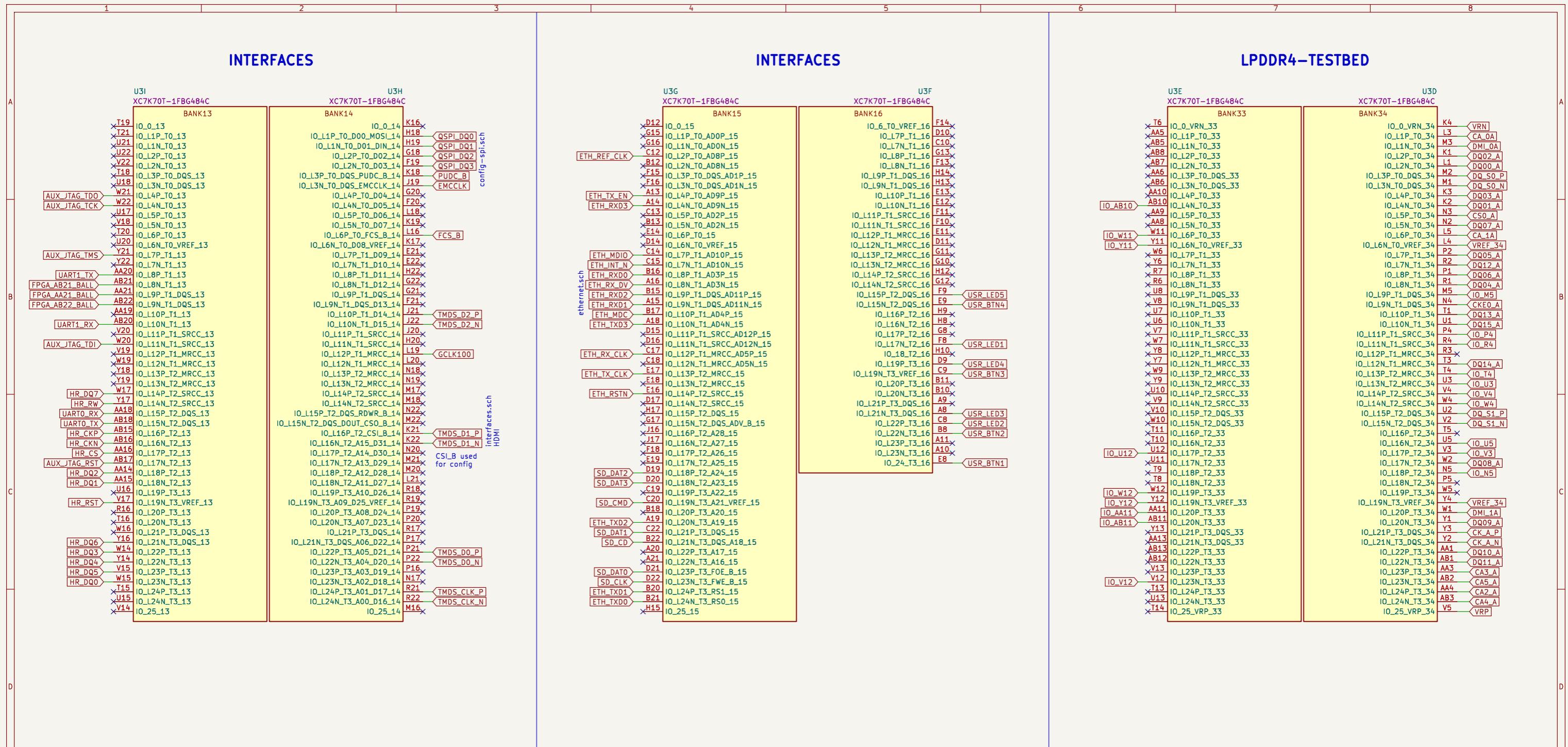


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Title: LPDDR4 Test Board

Size: A3 | Date: 2024-02-12
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Rev: 1.1.5:95aa2 | Id: 2/9



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Title: LPDDR4 Test Board

Date: 2024-02-12
kicad E.D.A. kicad-cli 7.0.10+1

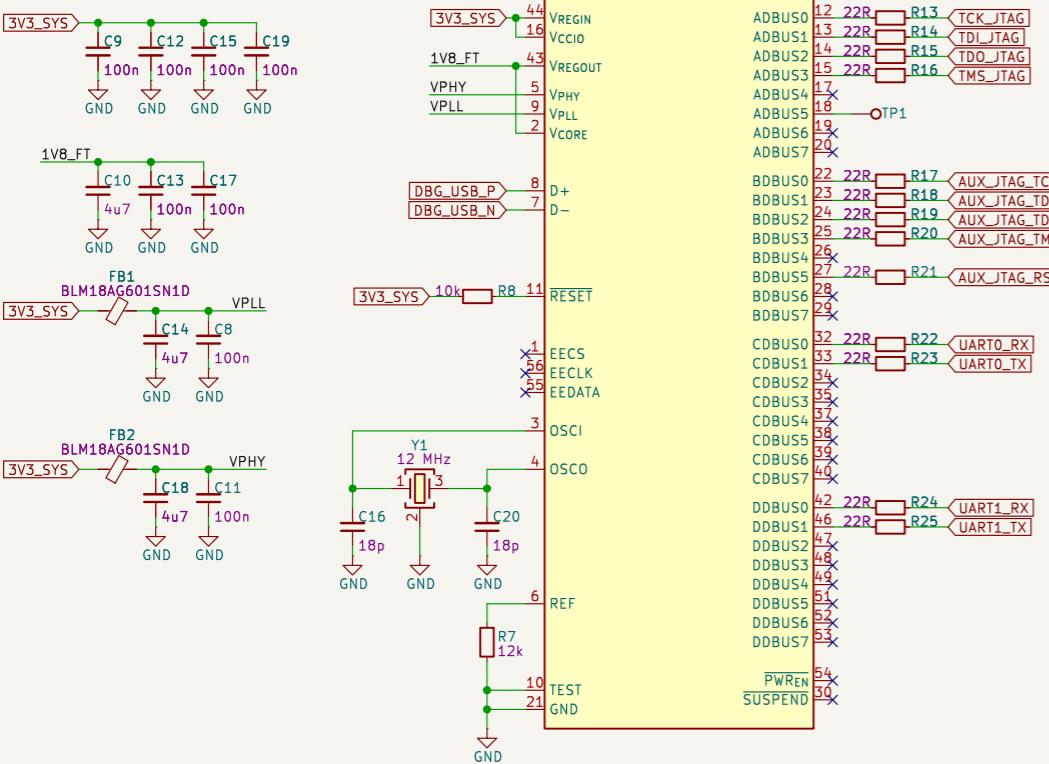
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Digitized by srujanika@gmail.com

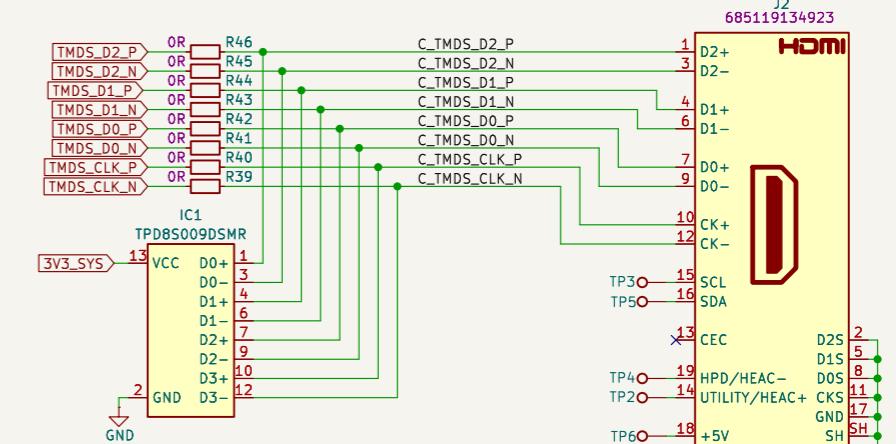
3 F

1 2 3 4 5 6 7 8

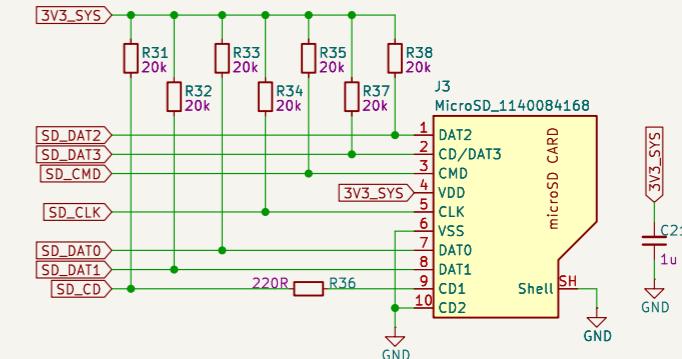
Debug UART



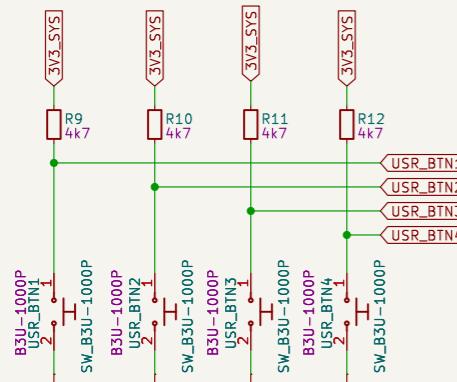
HDMI



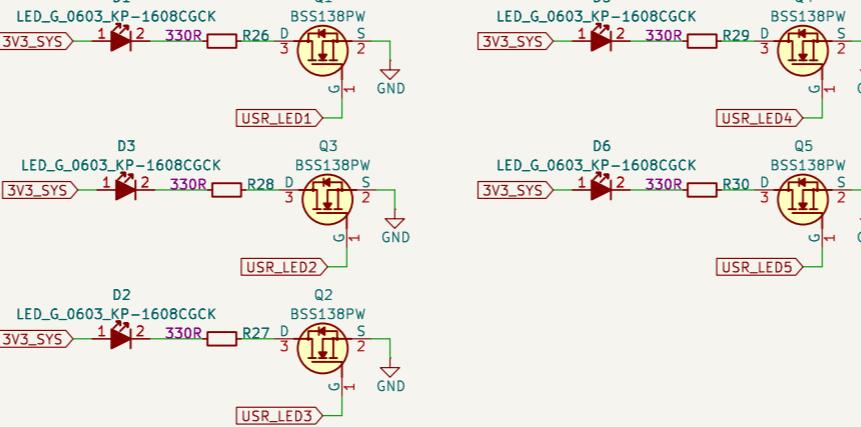
SD card



User buttons



User LEDs



Sheet: /Interfaces/
File: interfaces.kicad_sch

Title: LPDDR4 Test Board

Size: A3 Date: 2024-02-12
KiCad E.D.A. kicad-cl 7.0.10+1

Rev: 1.1.5:95aa2
Id: 4/9

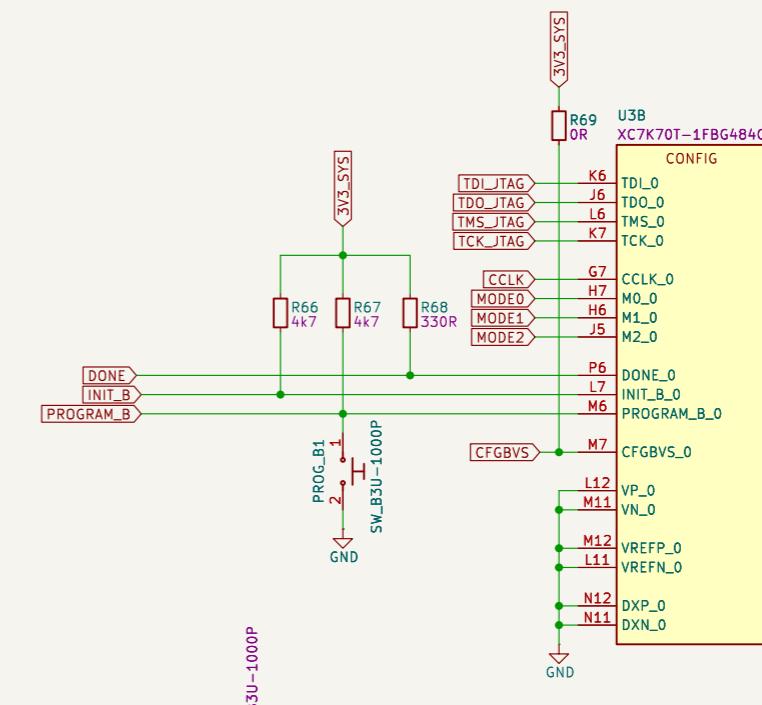
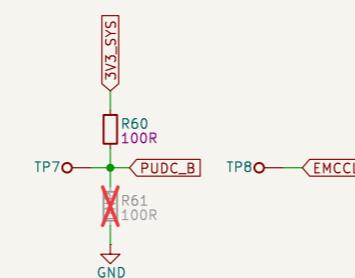
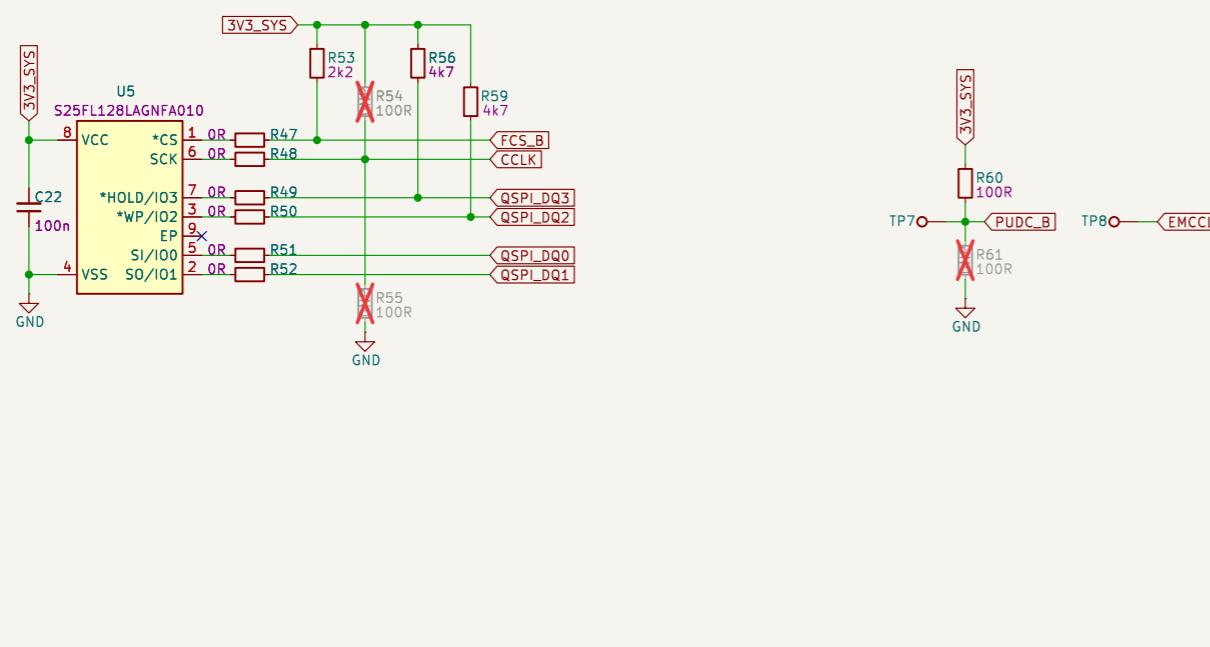
1 2 3 4 5 6 7 8

Master SPI Quad (x4) configuration scheme

Follows Figure 2-14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

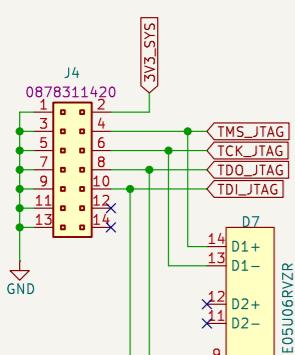
FPGA BANK 0

(Q)SPI flash

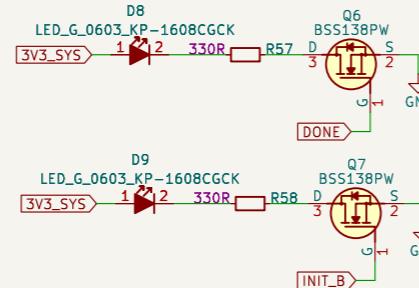


JTAG Connector

Compatible with Xilinx Platform Cable

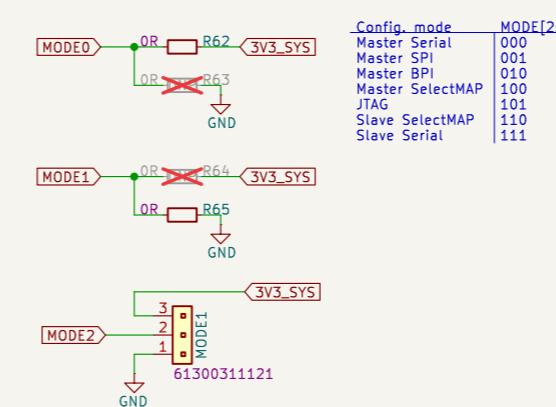


STATUS LEDs



Configuration Modes

For details, see UG470 p. 21



Config_mode	MODE[2:0]
Master Serial	000
Master SPI	001
Master BPI	010
Master SelectMAP	100
JTAG	101
Slave SelectMAP	110
Slave Serial	111

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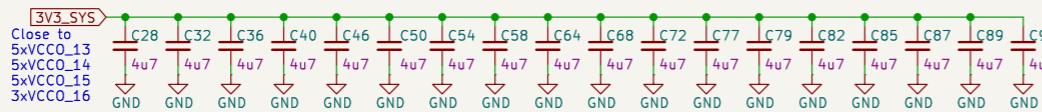
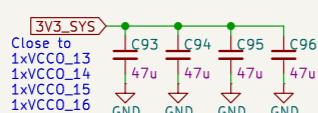
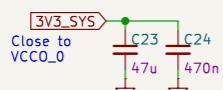
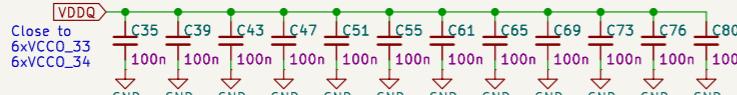
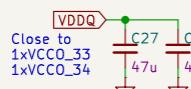
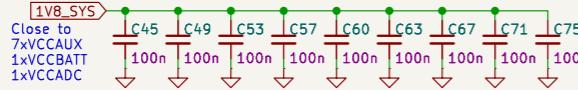
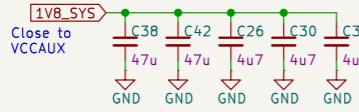
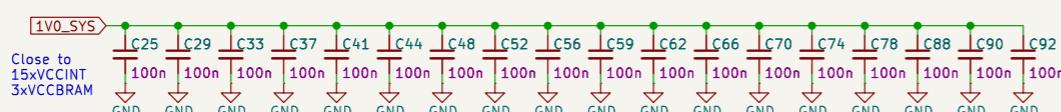
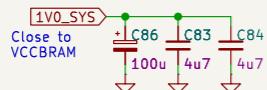
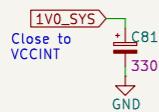
Title: LPDDR4 Test Board

Size: A3 Date: 2024-02-12
KiCad E.D.A. kicad-cl 7.0.10+1

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A

Decoupling referenced from 7 Series FPGAs
PCB Design Guide UG483

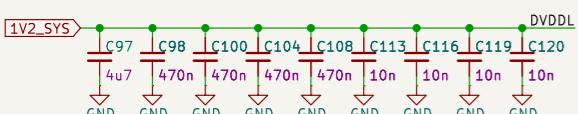
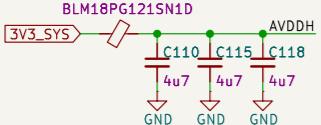
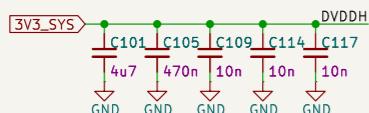
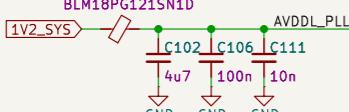
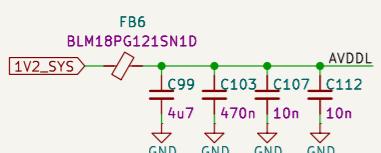
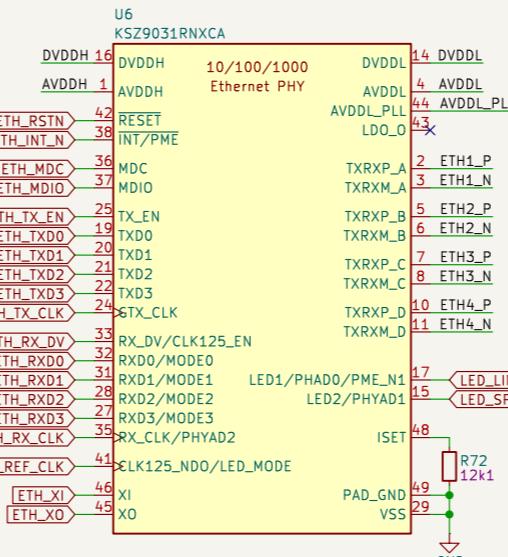
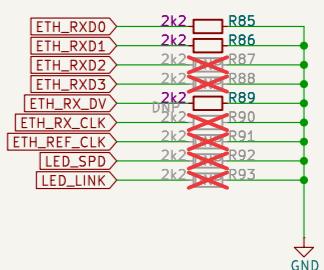
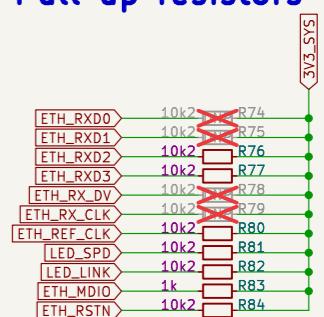
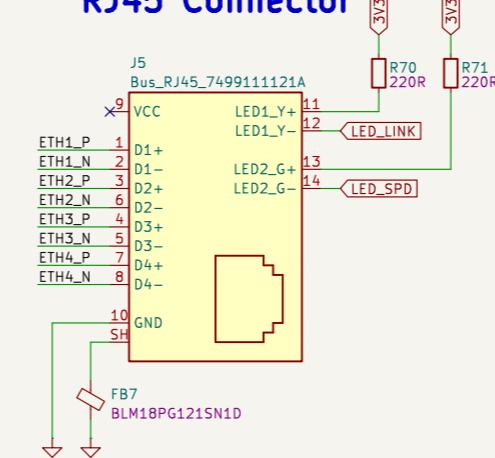


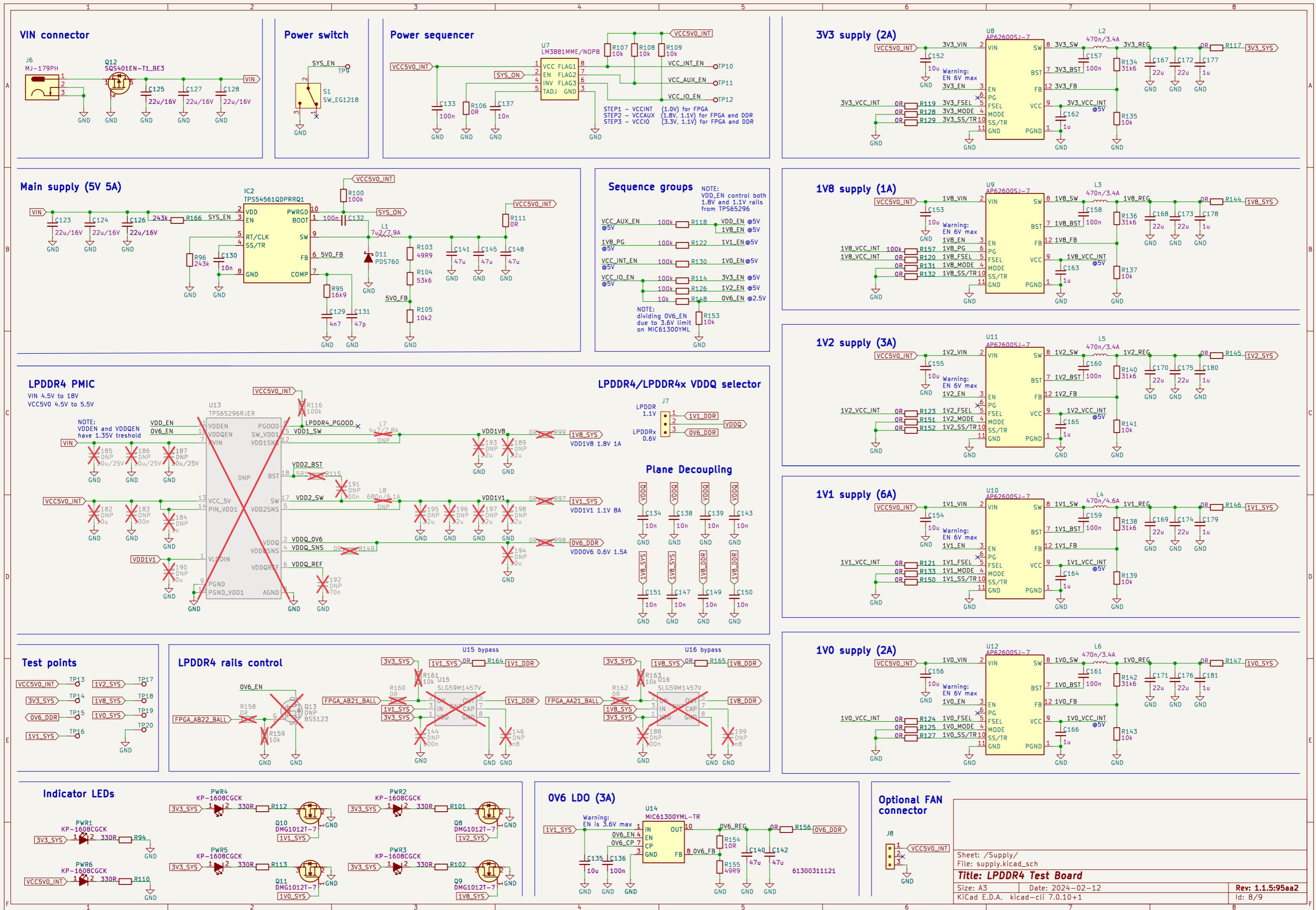
POWER RAILS

U3A XC7K70T-1FBG484C	
POWER	J7
VCCAUX max: 2.0V	K10
VCCINT max: 1.1V	J11
VCCBATT max: 2.0V	P7
VCCBRAM max: 1.1V	L13
VCCADC max: 2.0V	K12
VCCADDC max: 2.0V	1V8_SYS

X ⁶ A	MGTAVCC
X ²⁴ A	MGTAVTT
X ¹⁴ H	MGTVCaux
X ¹² H1	MGTAVTRCAL_115
X ¹² H2	MGRREF_115
VCCO (33-34 banks) max: 2.0V	A84
VCCO (13-16 banks) max: 3.6V	A7
VCCO_34	VCCO_34
VCCO_33	A17
VCCO_16	C11
VCCO_15	A17
VCCO_14	F22
VCCO_13	VCCO_15
VCCO_12	A17
K11	GNDADC_0
A1	GND

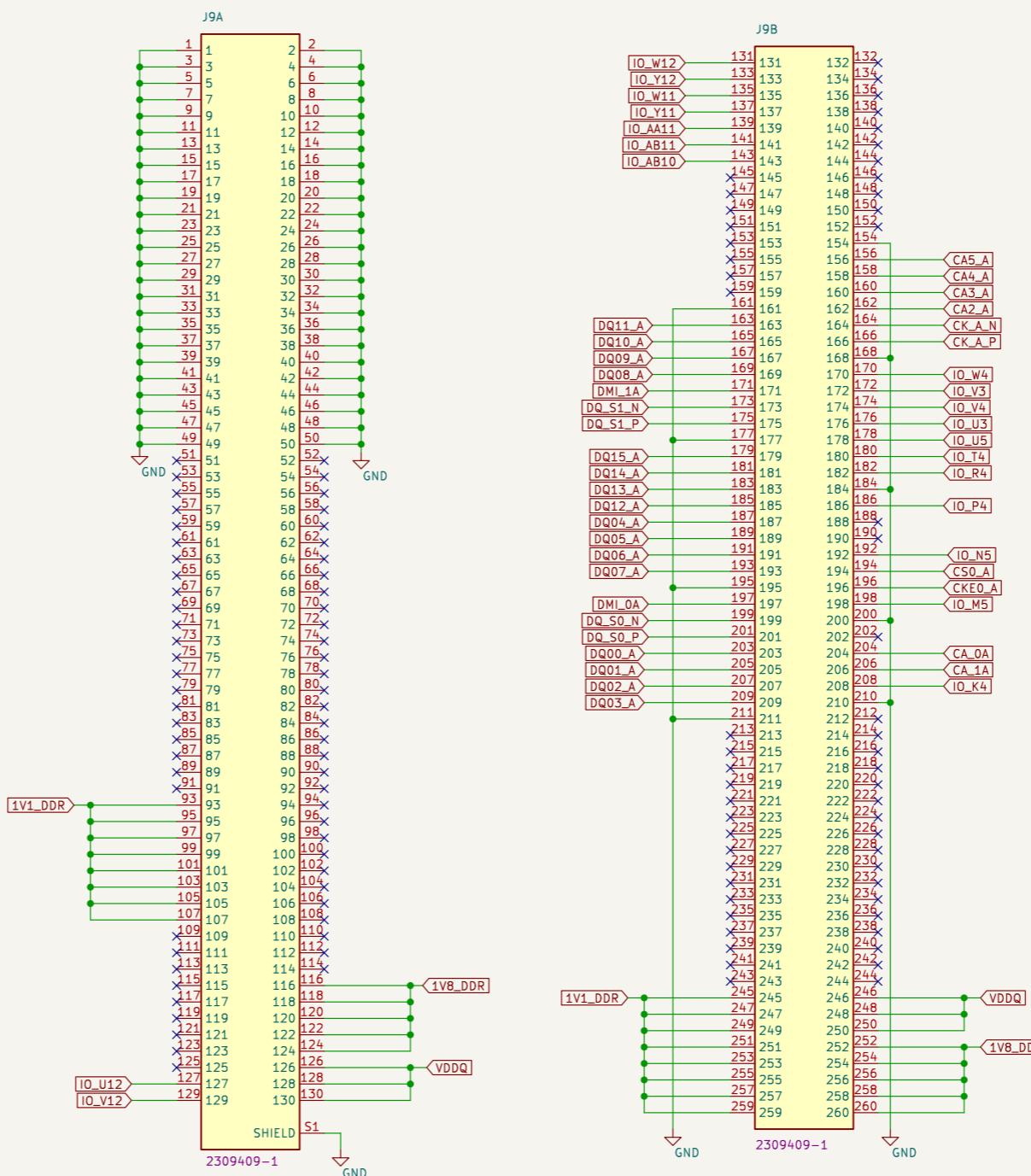
A

DVDDL decoupling**AVDDH decoupling****DVDDH decoupling****AVDDL_PLL decoupling****AVDDL decoupling****PHY****Pull down resistors****Pull up resistors****RJ45 Connector**



DDR4 SODIMM connector

A

**Mechanical protection**

SP1
Spacer_H5.0mm_9774050151
x1

F

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