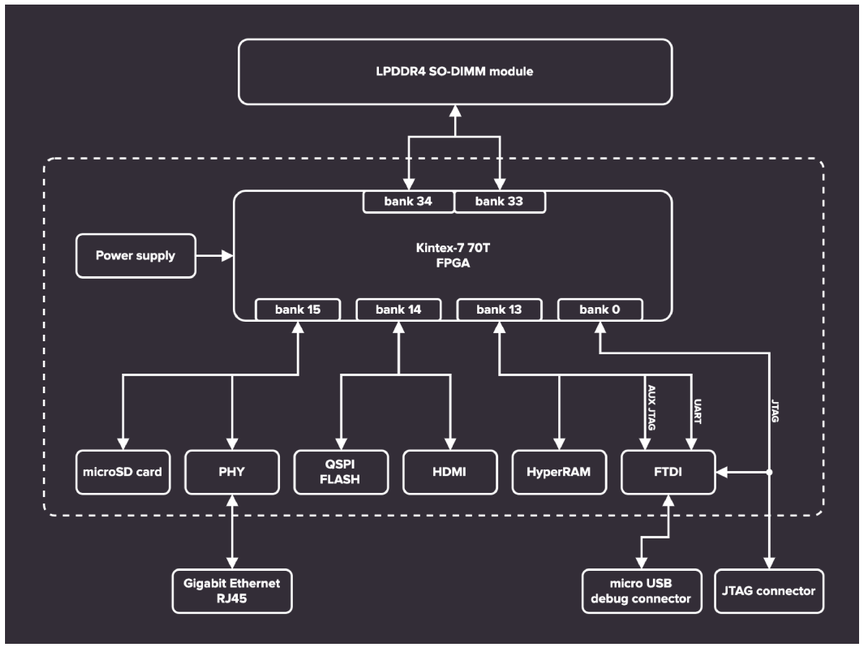
LPDDR4 Test Board



HyperRAM — File: hyperram.kicad_sch

FPGA Banks — File: fpga-banks.kicad_sch

Interfaces — File: interfaces.kicad_sch

Config SPI flash — File: config-spi.kicad_sch

FPGA power — File: fpga-power.kicad_sch

Ethernet — File: ethernet.kicad_sch

Supply — File: supply.kicad_sch

SO-DIMM — File: sodimm.kicad_sch

Logo N2
oshw_logo

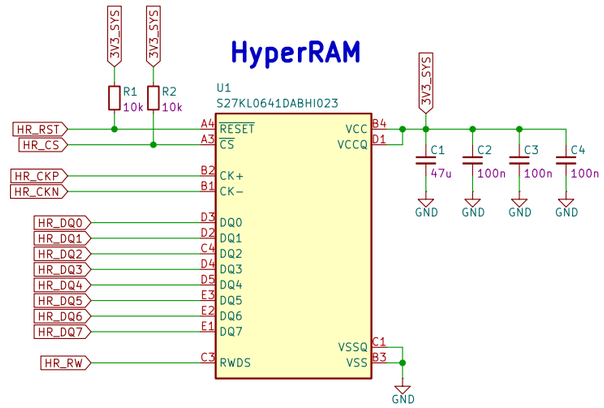
Logo N1
antmicro_logo

LPDDR4 Test Board

Sheet: /
File: lpddr4-test-board.kicad_sch

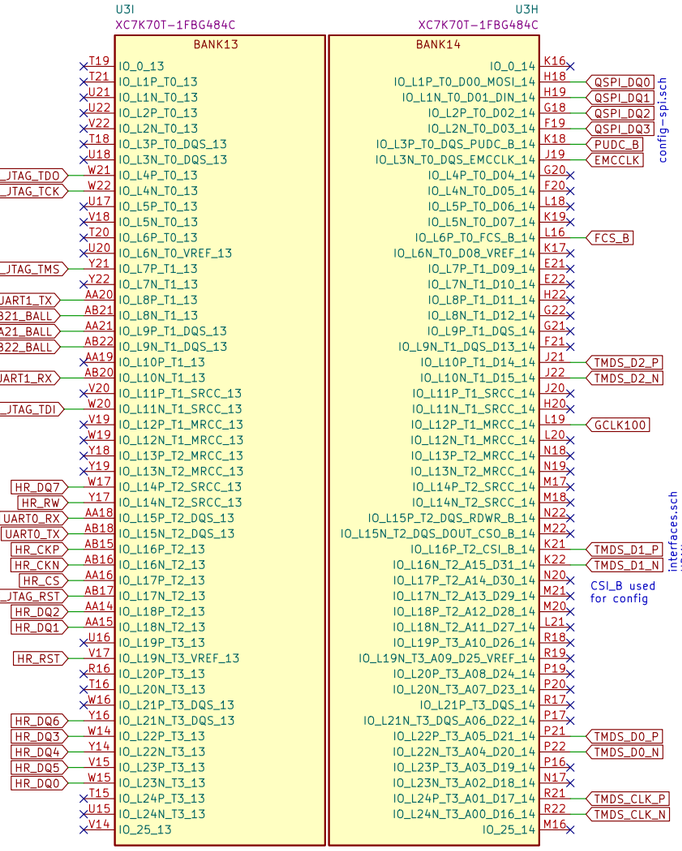
Title: LPDDR4 Test Board

Size: A3	Date: 2023-07-13	**Rev: 1.1.4**
KiCad E.D.A. eeschema 6.0.11+dfsg-1-bpo11+1		Id: 1/9

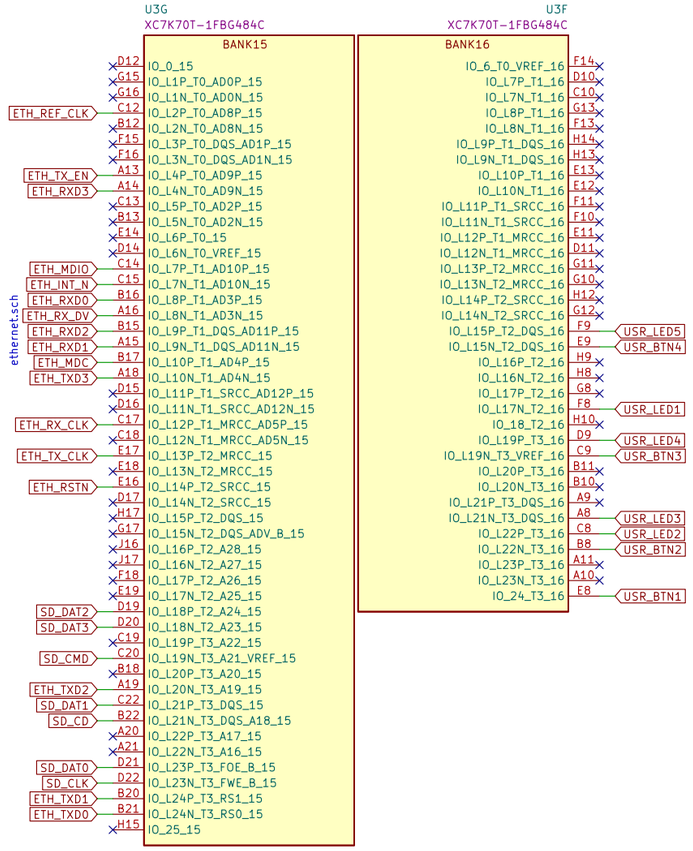


Sheet: /HyperRAM/		
File: hyperram.kicad_sch		
Title: LPDDR4 Test Board		
Size: A3	Date: 2023-07-13	**Rev: 1.1.4**
KiCad E.D.A. eeschema 6.0.11+dfsg-1-bpo11+1		Id: 2/9

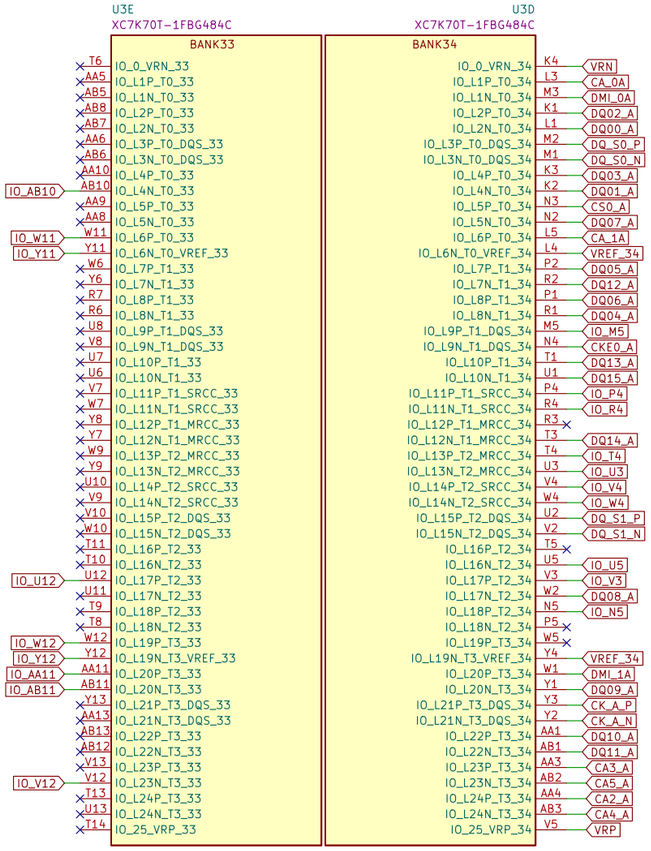
INTERFACES



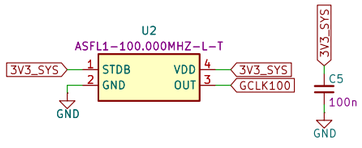
INTERFACES



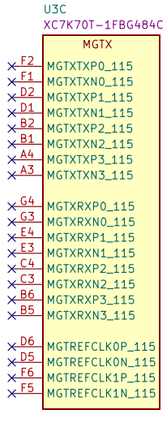
LPDDR4-TESTBED



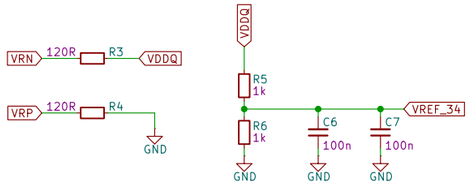
Clock source



UNUSED



LPDDR VREF

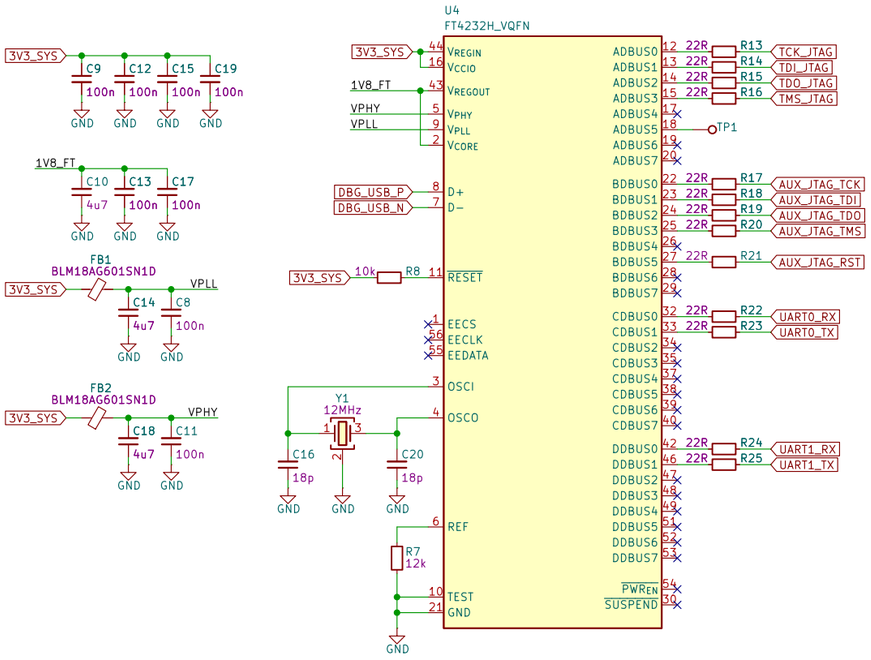


Sheet: /FPGA Banks/
File: fpga-banks.kicad_sch

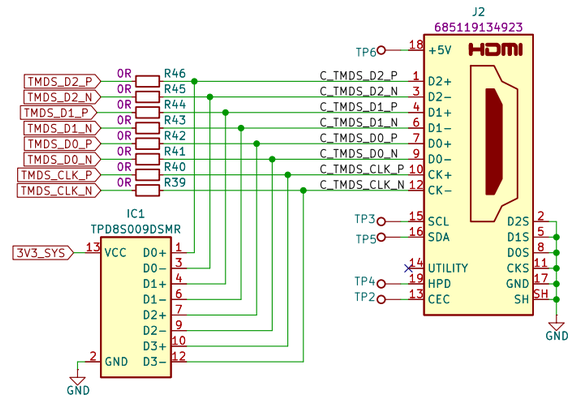
Title: LPDDR4 Test Board

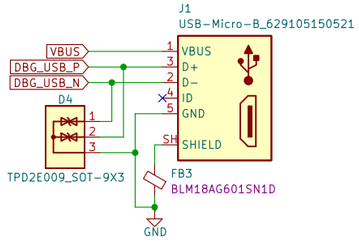
Size: A3	Date: 2023-07-13	**Rev: 1.1.4**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1-bpo11+1	Id: 3/9

Debug UART

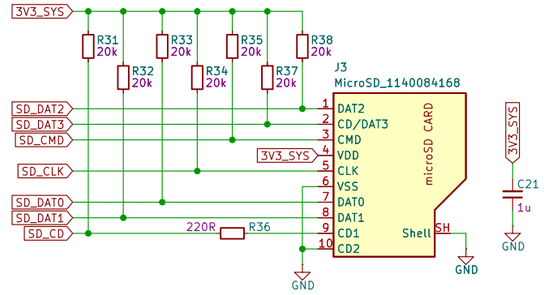


HDMI

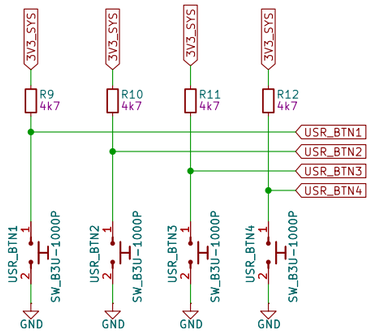




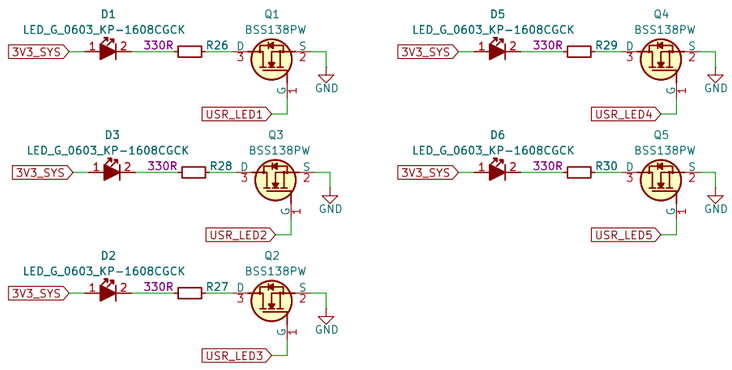
SD card



User buttons



User LEDs

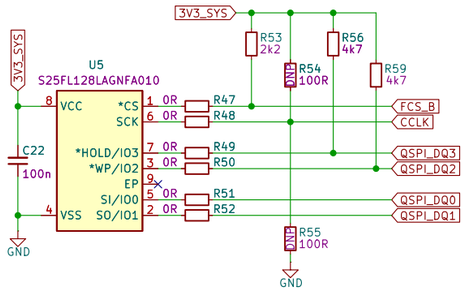


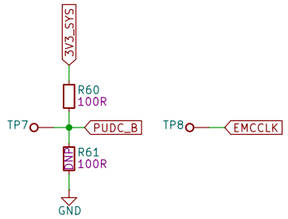
Sheet: /Interfaces/		
File: interfaces.kicad_sch		
Title: LPDDR4 Test Board		
Size: A3	Date: 2023-07-13	**Rev: 1.1.4**
KiCad E.D.A. eeschema 6.0.11+dfsg-1-bpo11+1		Id: 4/9

Master SPI Quad (x4) configuration scheme

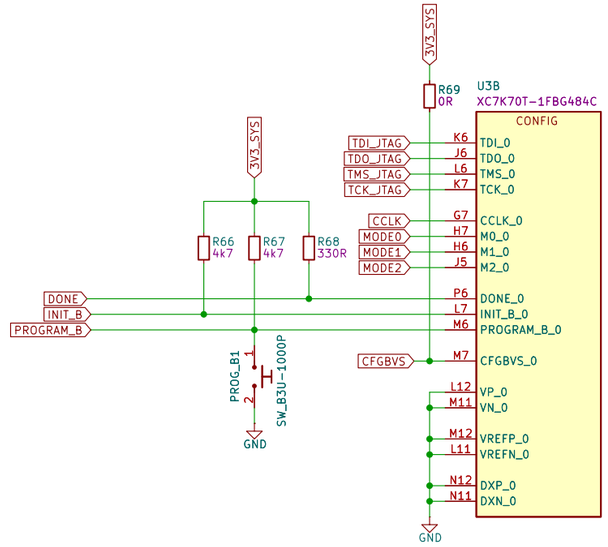
Follows Figure 2–14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

(Q)SPI flash



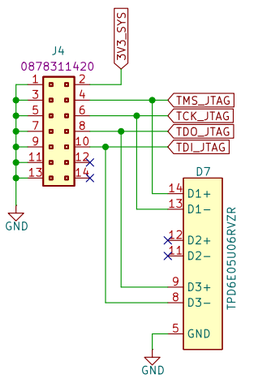


FPGA BANK 0

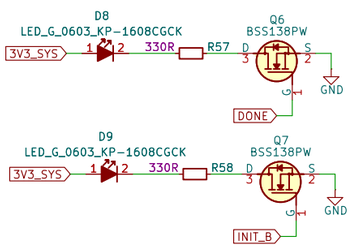


JTAG Connector

Compatible with Xilinx Platform Cable

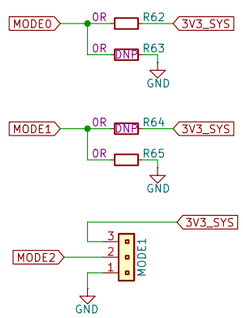


STATUS LEDs



Configuration Modes

For details, see UG470 p. 21



Config. mode	MODE[2:0]
Master Serial	000
Master SPI	001
Master BPI	010
Master SelectMAP	100
JTAG	101
Slave SelectMAP	110
Slave Serial	111

Sheet: /Config SPI flash/
File: config-spi.kicad_sch

Title: LPDDR4 Test Board

Size: A3	Date: 2023-07-13	**Rev: 1.1.4**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1-bpo11+1	Id: 5/9

Decoupling referenced from 7 Series FPGAs
PCB Design Guide UG483

1V0_SYS
Close to
VCCINT
C81
330u
GND

1V0_SYS
Close to
VCCBRAM
C86 C83 C84
100u 4u7 4u7
GND GND GND

1V0_SYS
Close to
15xVCCINT
3xVCCBRAM
C25 C29 C33 C37 C41 C44 C48 C52 C56 C59 C62 C66 C70 C74 C78 C88 C90 C92
100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n
GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND

1V8_SYS
Close to
VCCAUX
C38 C42 C26 C30 C34
47u 47u 4u7 4u7 4u7
GND GND GND GND GND

1V8_SYS
Close to
7xVCCAUX
1xVCCBATT
1xVCCADC
C45 C49 C53 C57 C60 C63 C67 C71 C75
100n 100n 100n 100n 100n 100n 100n 100n 100n
GND GND GND GND GND GND GND GND GND

VDDQ
Close to
1xVCCO_33
1xVCCO_34
C27 C31
47u 47u
GND GND

VDDQ
Close to
6xVCCO_33
6xVCCO_34
C35 C39 C43 C47 C51 C55 C61 C65 C69 C73 C76 C80
100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n
GND GND GND GND GND GND GND GND GND GND GND GND

3V3_SYS
Close to
VCCO_0
C23 C24
47u 470n
GND GND

3V3_SYS
Close to
1xVCCO_13
1xVCCO_14
1xVCCO_15
1xVCCO_16
C93 C94 C95 C96
47u 47u 47u 47u
GND GND GND GND

3V3_SYS
Close to
5xVCCO_13
5xVCCO_14
5xVCCO_15
3xVCCO_16
C28 C32 C36 C40 C46 C50 C54 C58 C64 C68 C72 C77 C79 C82 C85 C87 C89 C91
4u7 4u7 4u7 4u7 4u7 4u7 4u7 4u7 4u7 4u7 4u7 4u7 4u7 4u7 4u7 4u7 4u7 4u7
GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND

POWER RAILS

U3A
XC7K70T-1FBG484C

VCCAUX max: 2.0V
VCCINT max: 1.1V
VCCBATT max: 2.0V
VCCBRAM max: 1.1V
VCCADC max: 2.0V

3V3_SYS J7 VCCO_0
1V8_SYS K10 VCCAUX
1V0_SYS J11 VCCINT
1V8_SYS P7 VCCBATT_0
1V0_SYS L13 VCCBRAM
1V8_SYS K12 VCCADC_0

A6 MGTAVCC
A2 MGTAVTT
J4 MGTVCCAUX
H1 MGTAVTTRCAL_115
H2 MGTRREF_115

VCCO (33-34 banks) max: 2.0V
VCCO (13-16 banks) max: 3.6V

VDDQ AB4 VCCO_34
VDDQ AA7 VCCO_33
3V3_SYS C11 VCCO_16
3V3_SYS A17 VCCO_15
3V3_SYS F22 VCCO_14
3V3_SYS AA17 VCCO_13

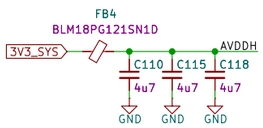
K11 GNDADC_0
A1 GND
GND

POWER

Sheet: /FPGA power/	
File: fpga-power.kicad_sch	
Title: LPDDR4 Test Board	
Size: A3	Date: 2023-07-13
KiCad E.D.A.	eeschema 6.0.11+dfsg-1-bpo11+1
Rev: 1.1.4	
Id: 6/9	

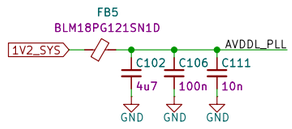
DVDL decoupling

AVDDH decoupling

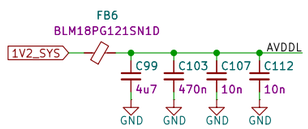


DVDDH decoupling

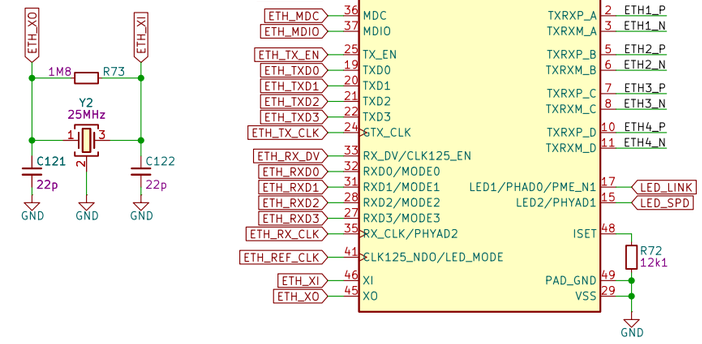
AVDDL_PLL decoupling



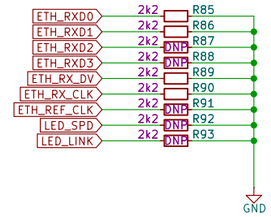
AVDDL decoupling



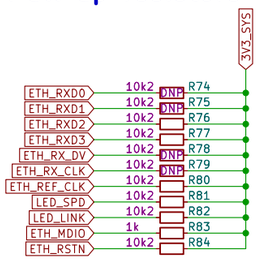
PHY



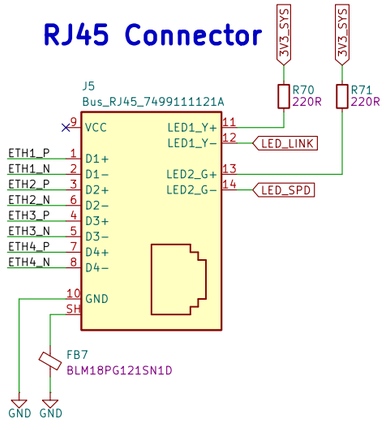
Pull down resistors



Pull up resistors



RJ45 Connector

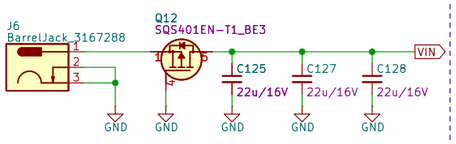


Sheet: /Ethernet/
File: ethernet.kicad_sch

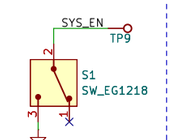
Title: LPDDR4 Test Board

Size: A3	Date: 2023-07-13	**Rev: 1.1.4**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1-bpo11+1	Id: 7/9

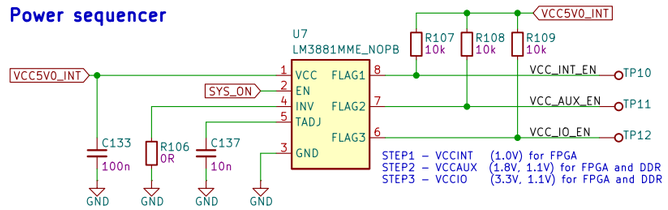
VIN connector



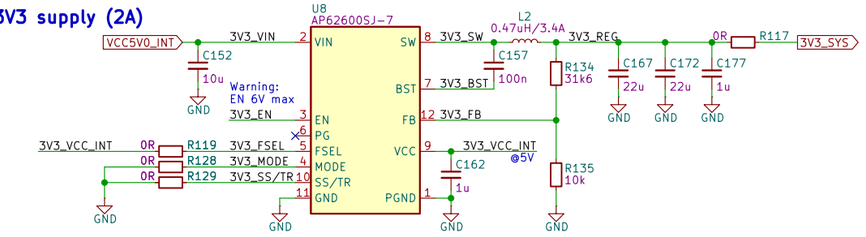
Power switch



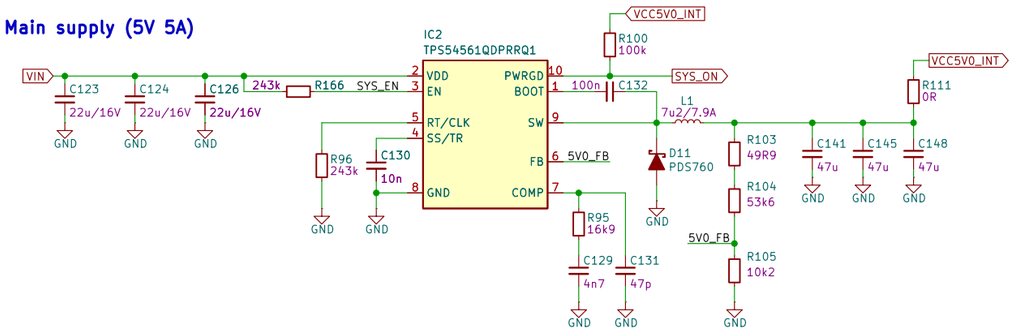
Power sequencer



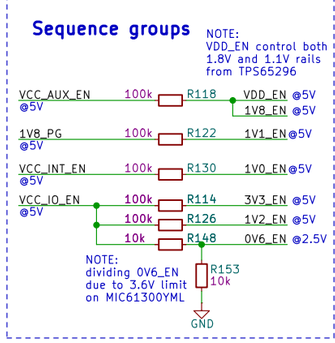
3V3 supply (2A)



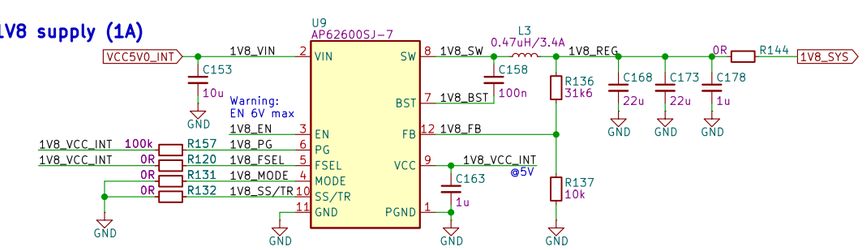
Main supply (5V 5A)



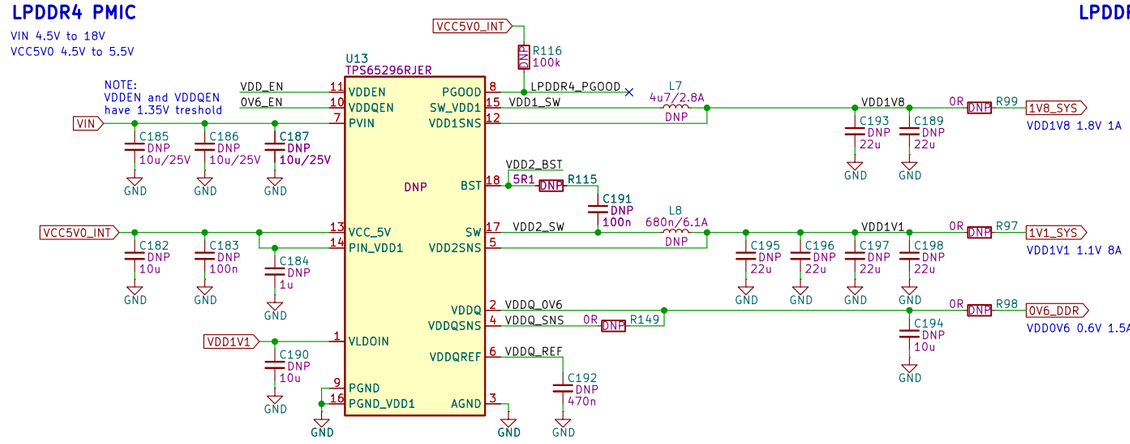
Sequence groups



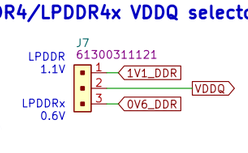
1V8 supply (1A)



LPDDR4 PMIC

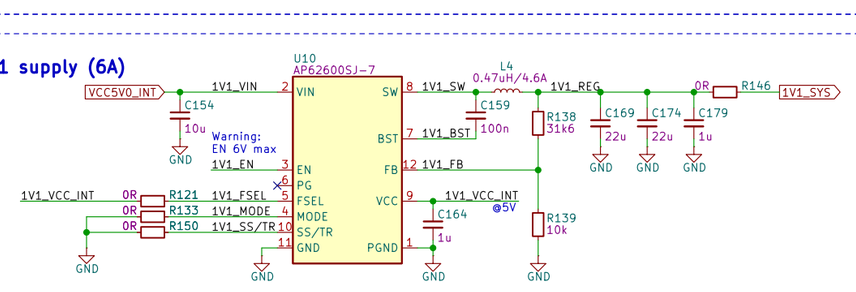


LPDDR4/LPDDR4x VDDQ selector

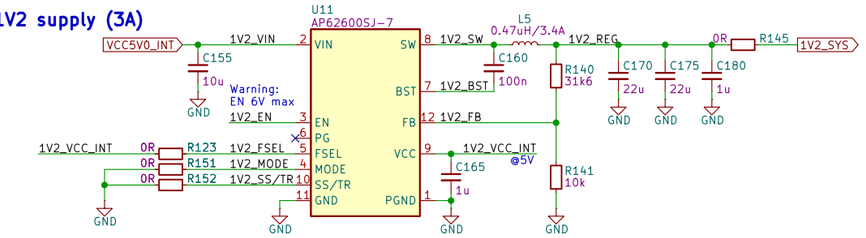


Plane Decoupling

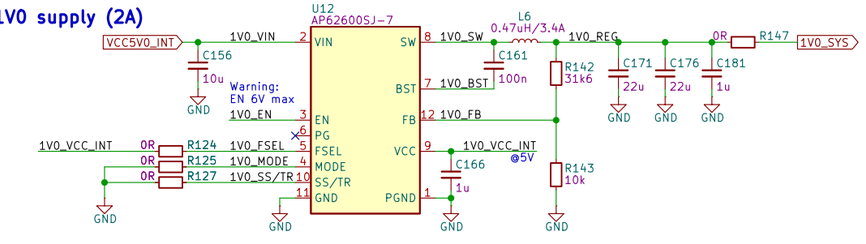
1V1 supply (6A)



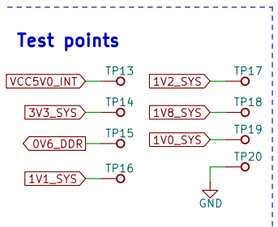
1V2 supply (3A)



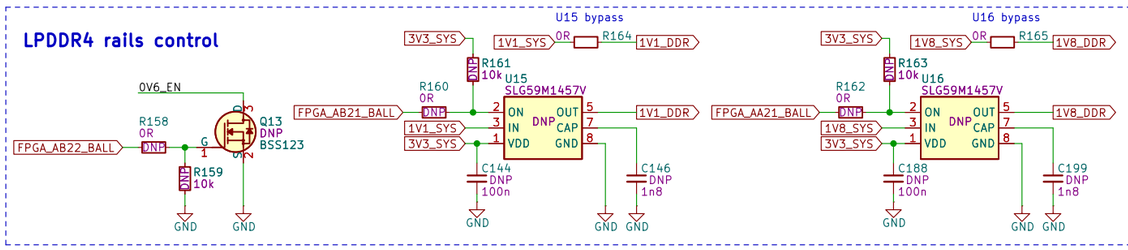
1V0 supply (2A)



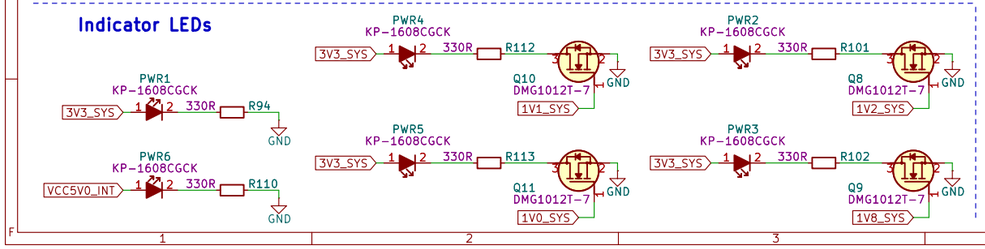
Test points



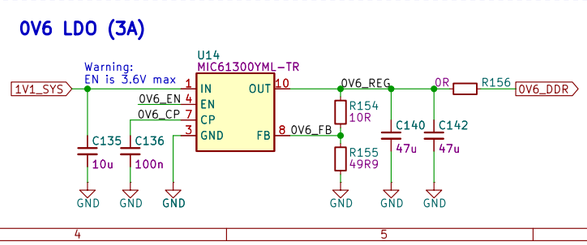
LPDDR4 rails control



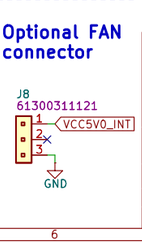
Indicator LEDs



0V6 LDO (3A)



Optional FAN connector

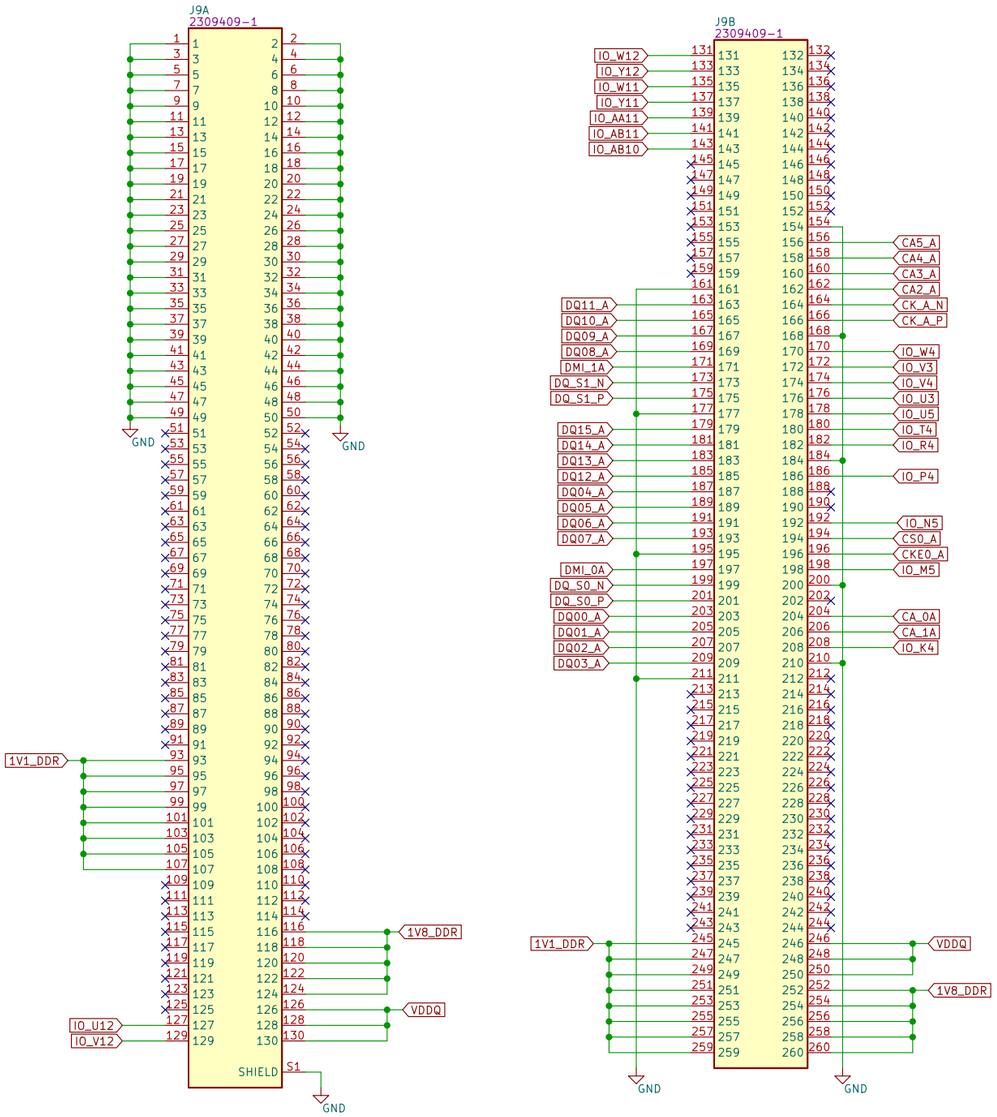


Sheet: /Supply/
File: supply.kicad_sch

Title: LPDDR4 Test Board

Size: A3	Date: 2023-07-13	**Rev: 1.1.4**
KiCad E.D.A.	eeschema 6.0.11+dfsg-1-bpo11+1	Id: 8/9

DDR4 SODIMM connector



M1

DNP
ddr5-testbed

Mechanical protection

SP1
Spacer_H5.0mm_9774050151

Sheet: /SO-DIMM/		
File: sodimm.kicad_sch		
Title: LPDDR4 Test Board		
Size: A3	Date: 2023-07-13	**Rev: 1.1.4**
KiCad E.D.A. eeschema 6.0.11+dfsg-1-bpo11+1		Id: 9/9