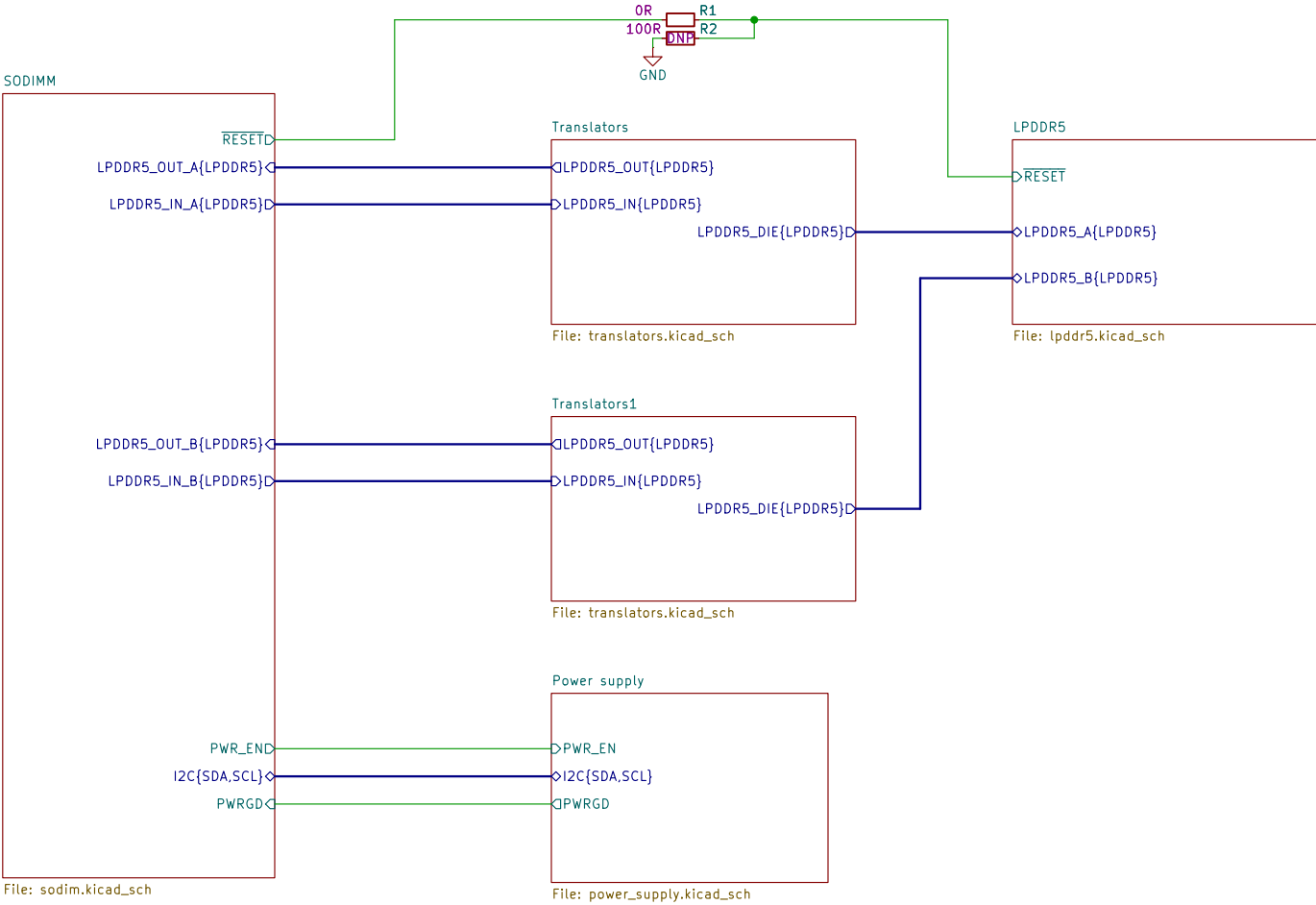
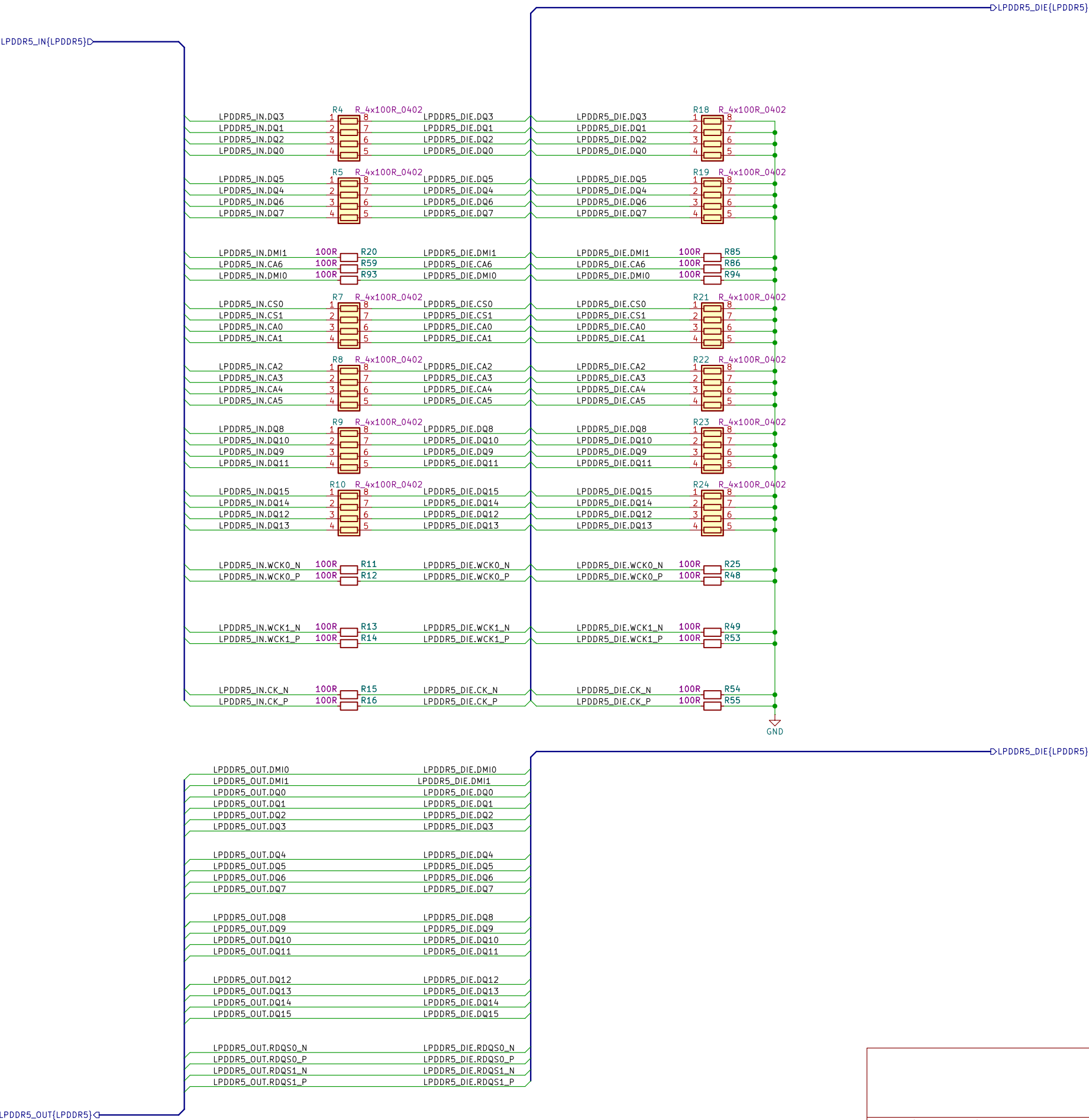


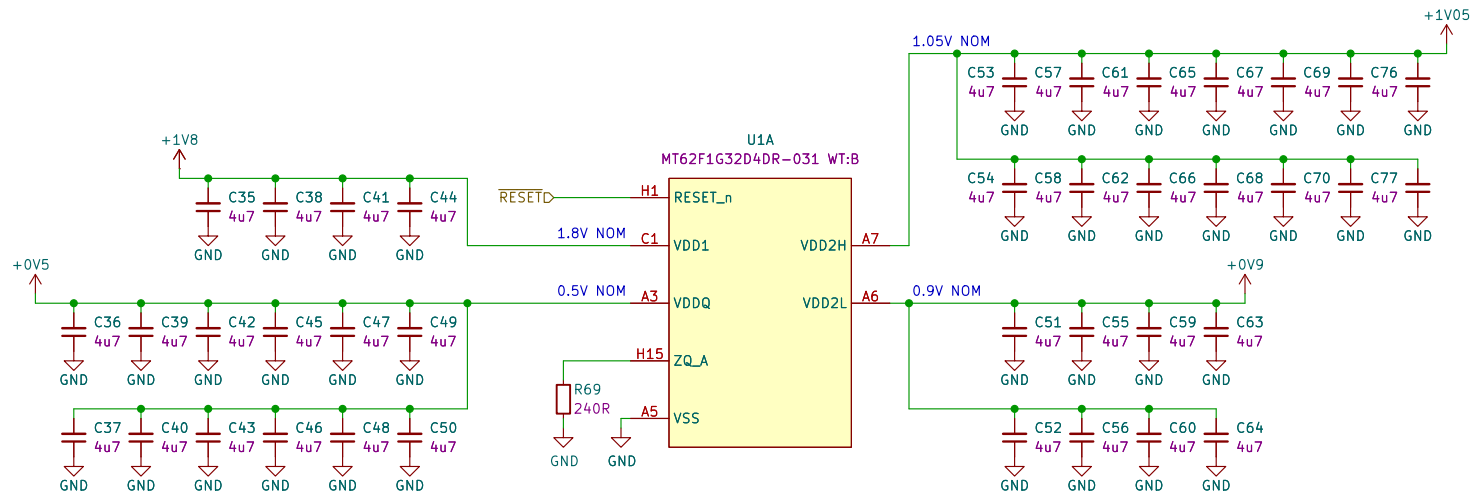
LPDDR5 Testbed



Voltage translators

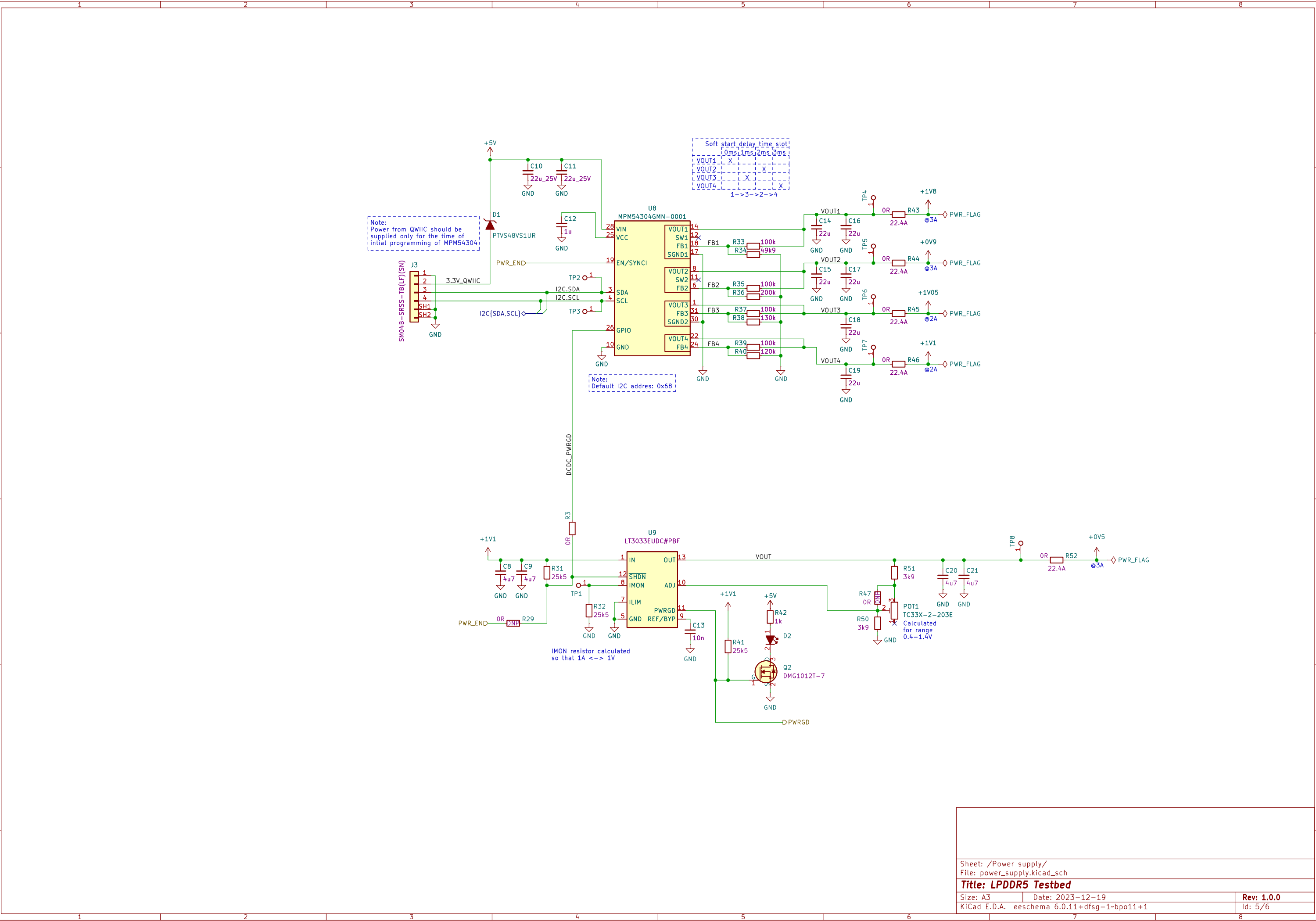


LPDDR5



LPDDR5_A{LPDDR5}									
U1B MT62F1G32D4DR-031 WT:B									
LPDDR5_A.CS0	H7	CS0_A	RDQS0_t_A	B3	LPDDR5_A.RDQS0_P				
LPDDR5_A.CS1	G6	CS1_A	RDQS0_c_A	C4	LPDDR5_A.RDQS0_N				
LPDDR5_A.DMI0	A4	DMI0_A	RDQS1_t_A	B13	LPDDR5_A.RDQS1_P				
LPDDR5_A.DMI1	A12	DMI1_A	RDQS1_c_A	C12	LPDDR5_A.RDQS1_N				
LPDDR5_A.WCK0_P	E4	WCK0_t_A	DQ0_A	D1	LPDDR5_A.DQ0				
LPDDR5_A.WCK0_N	D5	WCK0_c_A	DQ1_A	C2	LPDDR5_A.DQ1				
LPDDR5_A.WCK1_P	E12	WCK1_t_A	DQ2_A	F2	LPDDR5_A.DQ2				
LPDDR5_A.WCK1_N	D11	WCK1_c_A	DQ3_A	D3	LPDDR5_A.DQ3				
			DQ4_A	B5	LPDDR5_A.DQ4				
			DQ5_A	C6	LPDDR5_A.DQ5				
LPDDR5_A.CK_P	H9	CK_t_A	DQ6_A	E6	LPDDR5_A.DQ6				
LPDDR5_A.CK_N	J9	CK_c_A	DQ7_A	F5	LPDDR5_A.DQ7				
			DQ8_A	D15	LPDDR5_A.DQ8				
LPDDR5_A.CA0	G4	CA0_A	DQ9_A	C14	LPDDR5_A.DQ9				
LPDDR5_A.CA1	H5	CA1_A	DQ10_A	E14	LPDDR5_A.DQ10				
LPDDR5_A.CA2	G8	CA2_A	DQ11_A	D13	LPDDR5_A.DQ11				
LPDDR5_A.CA3	H11	CA3_A	DQ12_A	B11	LPDDR5_A.DQ12				
LPDDR5_A.CA4	G10	CA4_A	DQ13_A	C10	LPDDR5_A.DQ13				
LPDDR5_A.CA5	H13	CA5_A	DQ14_A	E10	LPDDR5_A.DQ14				
LPDDR5_A.CA6	G12	CA6_A	DQ15_A	F11	LPDDR5_A.DQ15				

LPDDR5_B{LPDDR5}									
U1C MT62F1G32D4DR-031 WT:B									
LPDDR5_B.CS0	P9	CS0_B	RDQS0_t_B	Y13	LPDDR5_B.RDQS0_P				
LPDDR5_B.CS1	R10	CS1_B	RDQS0_c_B	W12	LPDDR5_B.RDQS0_N				
LPDDR5_B.DMI0	AA12	DMI0_B	RDQS1_t_B	Y3	LPDDR5_B.RDQS1_P				
LPDDR5_B.DMI1	AA4	DMI1_B	RDQS1_c_B	W4	LPDDR5_B.RDQS1_N				
LPDDR5_B.WCK0_P	U12	WCK0_t_B	DQ0_B	V15	LPDDR5_B.DQ0				
LPDDR5_B.WCK0_N	V11	WCK0_c_B	DQ1_B	W14	LPDDR5_B.DQ1				
LPDDR5_B.WCK1_P	U4	WCK1_t_B	DQ2_B	U14	LPDDR5_B.DQ2				
LPDDR5_B.WCK1_N	V5	WCK1_c_B	DQ3_B	V13	LPDDR5_B.DQ3				
			DQ4_B	Y11	LPDDR5_B.DQ4				
			DQ5_B	W10	LPDDR5_B.DQ5				
LPDDR5_B.CK_P	P7	CK_t_B	DQ6_B	U10	LPDDR5_B.DQ6				
LPDDR5_B.CK_N	N7	CK_c_B	DQ7_B	T11	LPDDR5_B.DQ7				
			DQ8_B	V1	LPDDR5_B.DQ8				
LPDDR5_B.CA0	R12	CA0_B	DQ9_B	W2	LPDDR5_B.DQ9				
LPDDR5_B.CA1	P11	CA1_B	DQ10_B	U2	LPDDR5_B.DQ10				
LPDDR5_B.CA2	R8	CA2_B	DQ11_B	V3	LPDDR5_B.DQ11				
LPDDR5_B.CA3	P5	CA3_B	DQ12_B	Y5	LPDDR5_B.DQ12				
LPDDR5_B.CA4	R6	CA4_B	DQ13_B	W6	LPDDR5_B.DQ13				
LPDDR5_B.CA5	P3	CA5_B	DQ14_B	U6	LPDDR5_B.DQ14				
LPDDR5_B.CA6	R4	CA6_B	DQ15_B	T5	LPDDR5_B.DQ15				



This diagram illustrates the electrical connections for the LPDDR5 Testbed, showing the interface between the LPDDR5 memory controller (LPDDR5_IN{LPDDR5}) and the LPDDR5 memory die (LPDDR5_DIE{LPDDR5}).

LPDDR5_IN{LPDDR5} Connections:

- LPDDR5_IN.DQ3, LPDDR5_IN.DQ1, LPDDR5_IN.DQ2, LPDDR5_IN.DQ0
- LPDDR5_IN.DQ5, LPDDR5_IN.DQ4, LPDDR5_IN.DQ6, LPDDR5_IN.DQ7
- LPDDR5_IN.DMI1, LPDDR5_IN.CA6, LPDDR5_IN.DMI0
- LPDDR5_IN.CS0, LPDDR5_IN.CS1, LPDDR5_IN.CA0, LPDDR5_IN.CA1
- LPDDR5_IN.CA2, LPDDR5_IN.CA3, LPDDR5_IN.CA4, LPDDR5_IN.CA5
- LPDDR5_IN.DQ8, LPDDR5_IN.DQ10, LPDDR5_IN.DQ9, LPDDR5_IN.DQ11
- LPDDR5_IN.DQ15, LPDDR5_IN.DQ14, LPDDR5_IN.DQ12, LPDDR5_IN.DQ13
- LPDDR5_IN.WCK0_N, LPDDR5_IN.WCK0_P
- LPDDR5_IN.WCK1_N, LPDDR5_IN.WCK1_P
- LPDDR5_IN.CK_N, LPDDR5_IN.CK_P

LPDDR5_DIE{LPDDR5} Connections:

- LPDDR5_DIE.DQ3, LPDDR5_DIE.DQ1, LPDDR5_DIE.DQ2, LPDDR5_DIE.DQ0
- LPDDR5_DIE.DQ5, LPDDR5_DIE.DQ4, LPDDR5_DIE.DQ6, LPDDR5_DIE.DQ7
- LPDDR5_DIE.DMI1, LPDDR5_DIE.CA6, LPDDR5_DIE.DMI0
- LPDDR5_DIE.CS0, LPDDR5_DIE.CS1, LPDDR5_DIE.CA0, LPDDR5_DIE.CA1
- LPDDR5_DIE.CA2, LPDDR5_DIE.CA3, LPDDR5_DIE.CA4, LPDDR5_DIE.CA5
- LPDDR5_DIE.DQ8, LPDDR5_DIE.DQ10, LPDDR5_DIE.DQ9, LPDDR5_DIE.DQ11
- LPDDR5_DIE.DQ15, LPDDR5_DIE.DQ14, LPDDR5_DIE.DQ12, LPDDR5_DIE.DQ13
- LPDDR5_DIE.WCK0_N, LPDDR5_DIE.WCK0_P
- LPDDR5_DIE.WCK1_N, LPDDR5_DIE.WCK1_P
- LPDDR5_DIE.CK_N, LPDDR5_DIE.CK_P

LPDDR5_OUT{LPDDR5} Connections:

- LPDDR5_OUT.DMI0, LPDDR5_OUT.DMI1, LPDDR5_OUT.DQ0, LPDDR5_OUT.DQ1, LPDDR5_OUT.DQ2, LPDDR5_OUT.DQ3
- LPDDR5_OUT.DQ4, LPDDR5_OUT.DQ5, LPDDR5_OUT.DQ6, LPDDR5_OUT.DQ7
- LPDDR5_OUT.DQ8, LPDDR5_OUT.DQ9, LPDDR5_OUT.DQ10, LPDDR5_OUT.DQ11
- LPDDR5_OUT.DQ12, LPDDR5_OUT.DQ13, LPDDR5_OUT.DQ14, LPDDR5_OUT.DQ15
- LPDDR5_OUT.RDQS0_N, LPDDR5_OUT.RDQS0_P, LPDDR5_OUT.RDQS1_N, LPDDR5_OUT.RDQS1_P

Resistor Values and Connections:

- R57, R58, R60, R61, R62, R63, R64, R65, R66, R67, R68, R70: 100R
- R72, R73, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84: 100R
- R88, R89, R95, R96, R91, R92, R93, R94: 100R

Legend:

- LPDDR5_IN{LPDDR5}
- LPDDR5_DIE{LPDDR5}
- LPDDR5_OUT{LPDDR5}

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- Title: LPDDR5 Testbed
- Size: A3
- Date: 2023-12-19
- Rev: 1.0.0
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Sheet: /Translators1/		
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Title: LPDDR5 Testbed		
Size: A3	Date: 2023-12-19	Rev: 1.0.0
KiCad E.D.A. eeschema 6.0.11+dfsg-1-bpo11+1		Id: 6/6