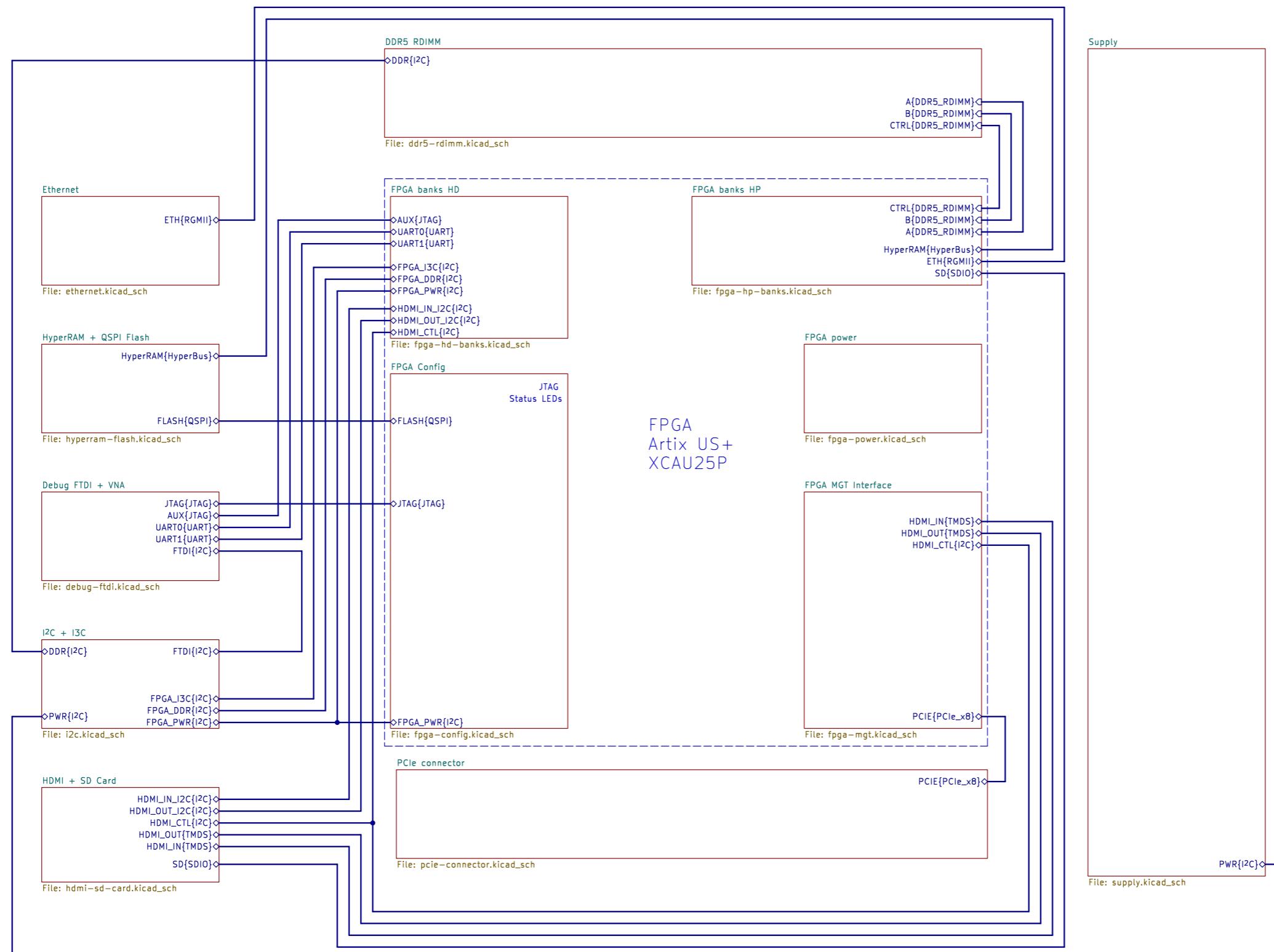
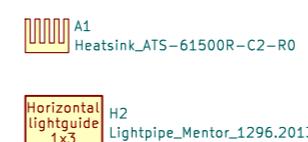


# RDIMM DDR5 Tester



## Mechanical



Antmicro  
www.antmicro.com

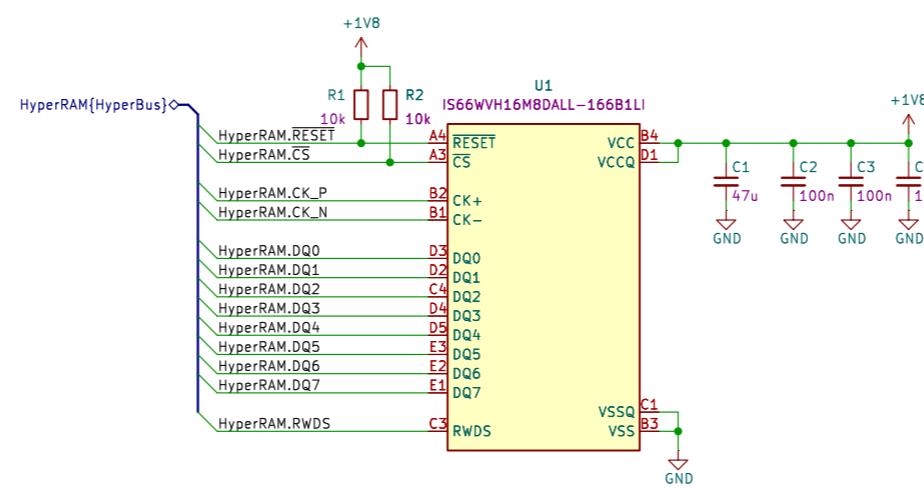
Sheet: /  
File: data-center-rdimm-ddr5-tester.kicad\_sch

**Title: RDIMM DDR5 Tester**

Size: A3 Date: 2024-11-07  
KiCad E.D.A. kicad 7.0.10+1

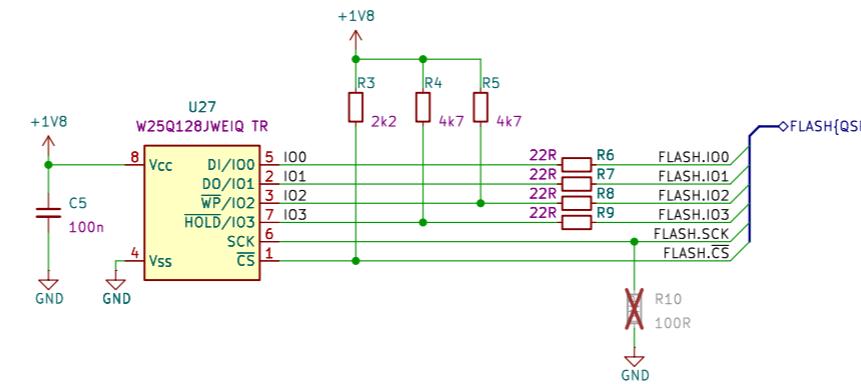
Rev: 2.0.0  
Id: 1/17

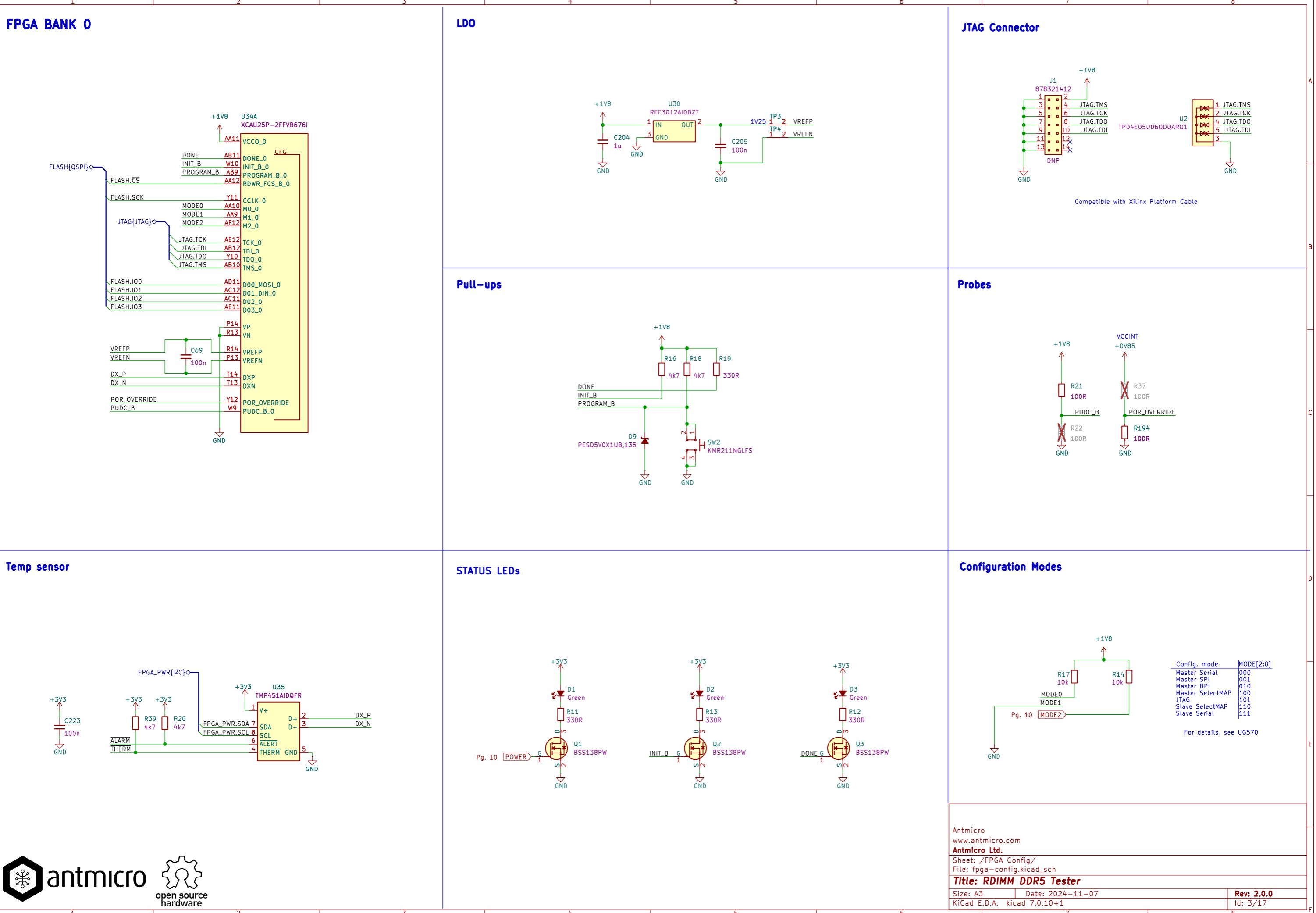
## HyperRAM



## (Q)SPI flash

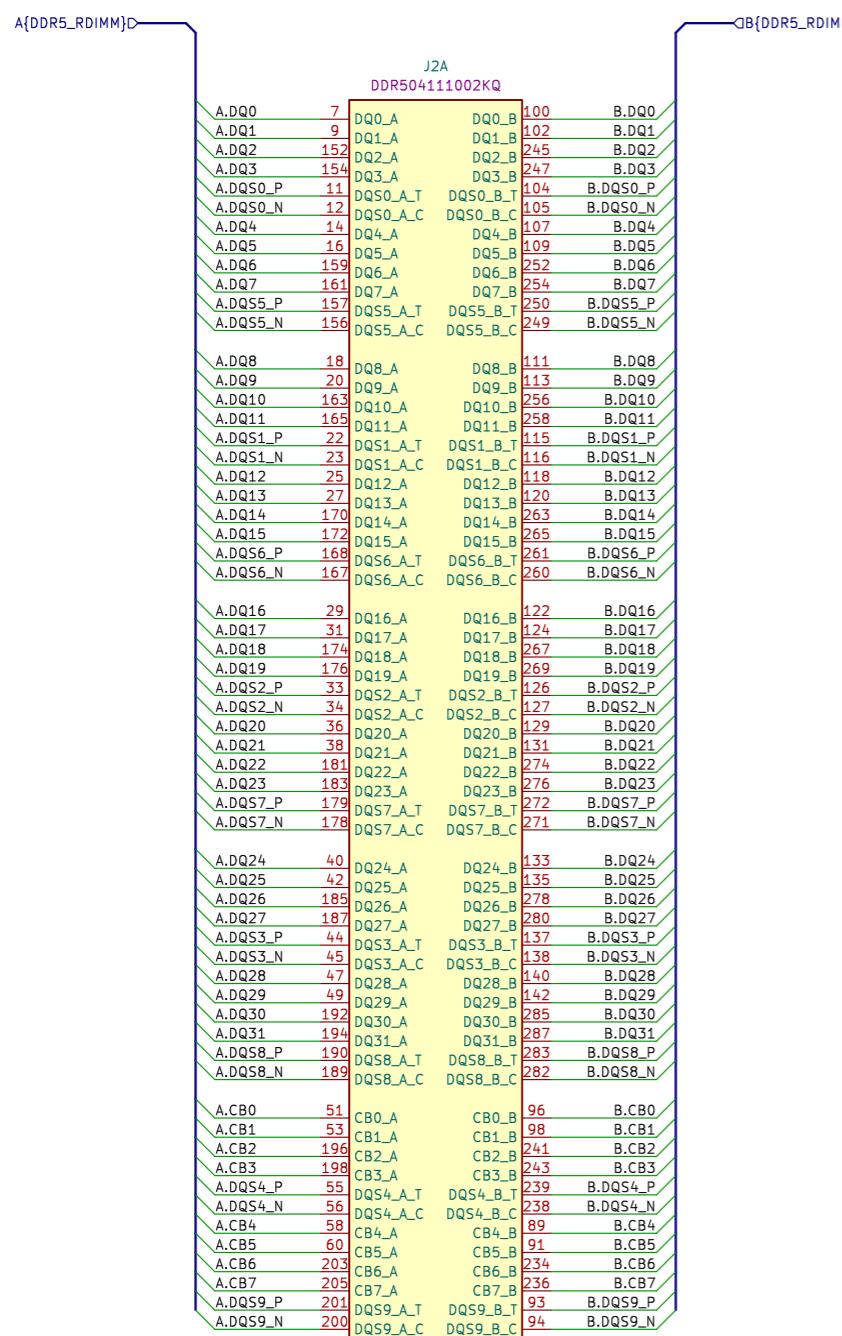
Master SPI Quad (x4) configuration scheme  
Follows FPGAs Configuration User Guide UG570





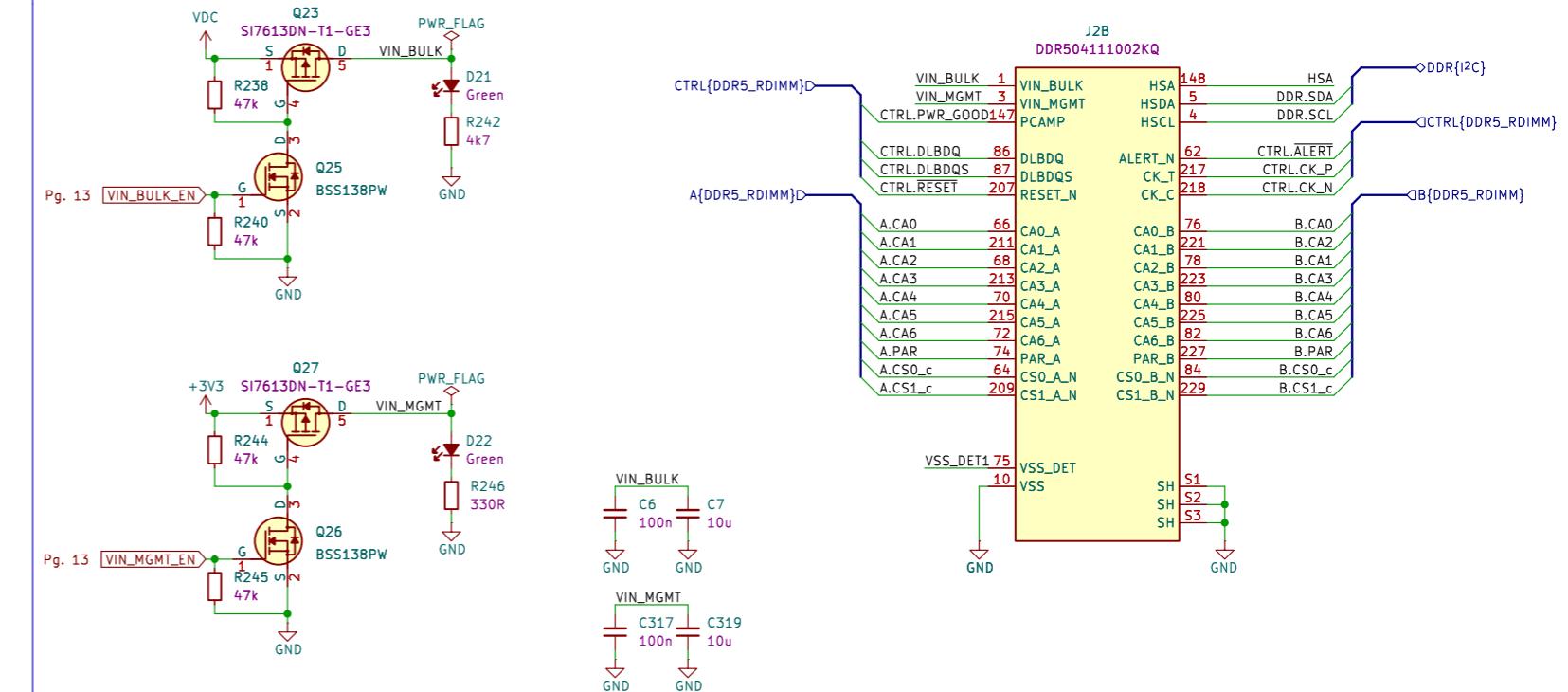
# DDR5 RDIMM connector

Subchannel A

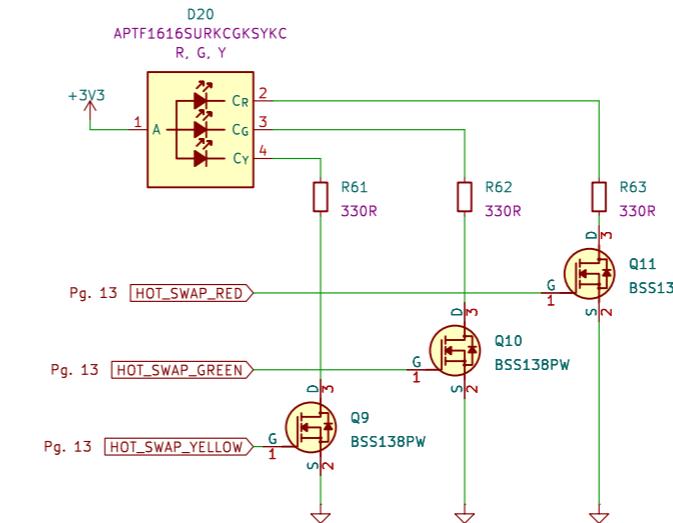


Subchannel B

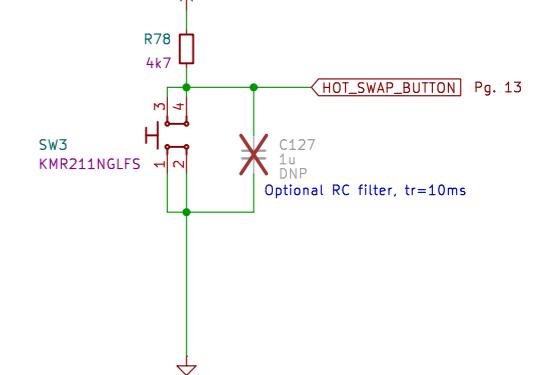
## Power, address command and control



## HOT SWAP status LED



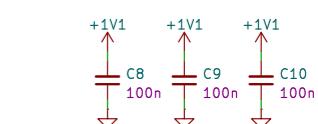
## HOT SWAP eject button



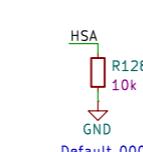
## RDIMM detect



## Plane decoupling



## Serial adress select



1

2

3

4

5

6

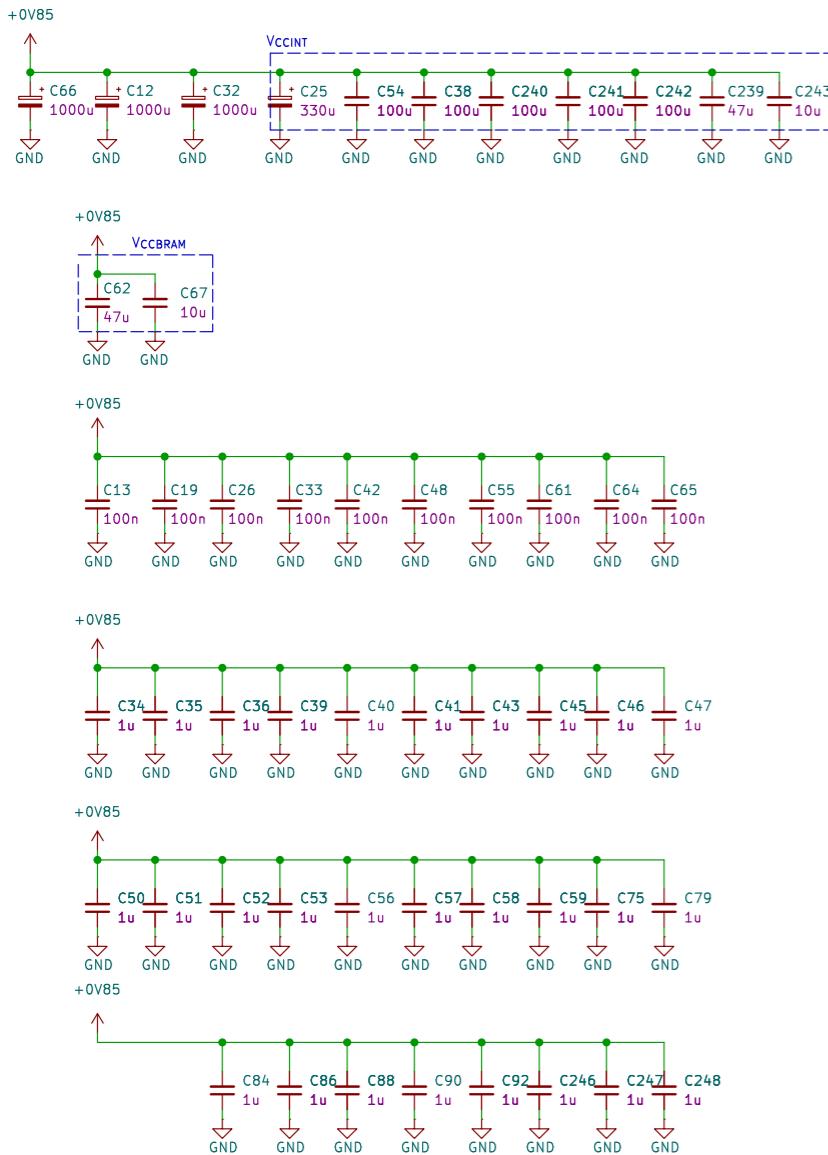
7

8

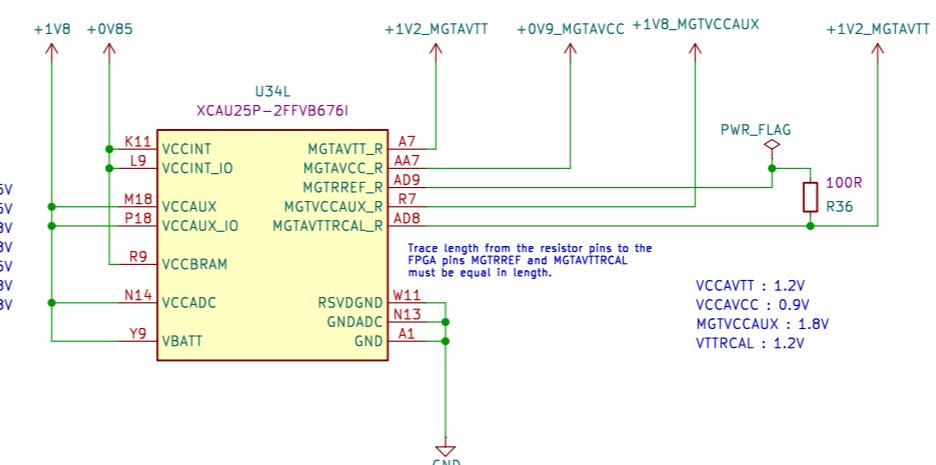
## FPGA Power rails

Bank marked by dashed line  
referenced from US+ Series FPGAs  
PCB Design Guide UG583  
(AUP25P+ XCKU5P FFVB Package worst case)  
MGT decoupling marked by dashed line  
referenced from US+ Series FPGAs  
PCB Design Guide UG576  
(AUP25P+ XCKU5P FFVB Package worst case)

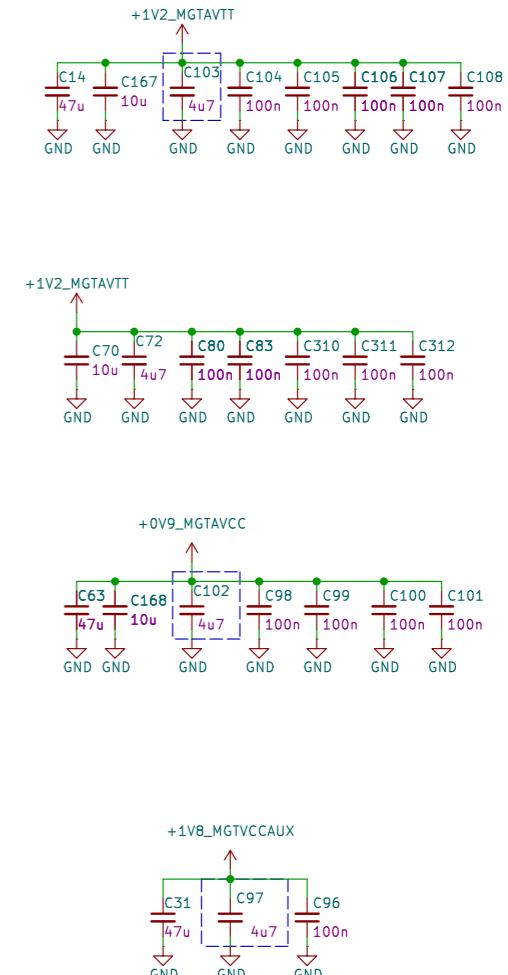
### VCCINT decoupling



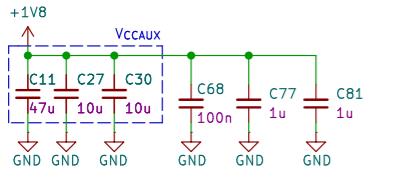
## FPGA



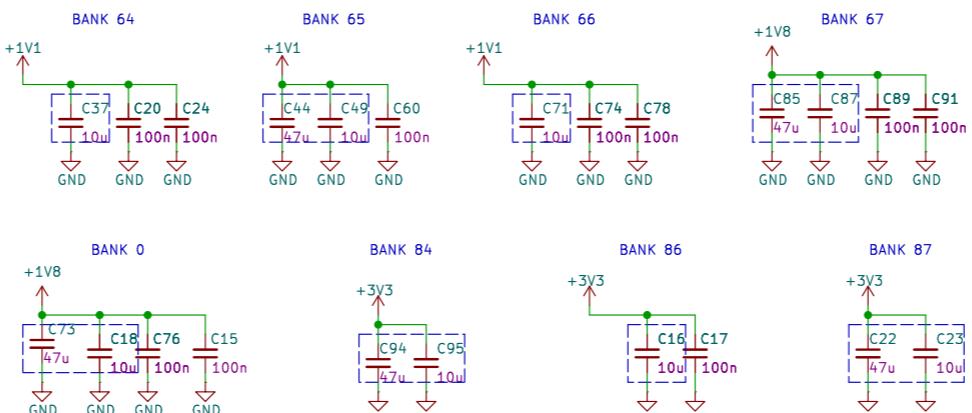
### MGT decoupling



### VCCINT decoupling

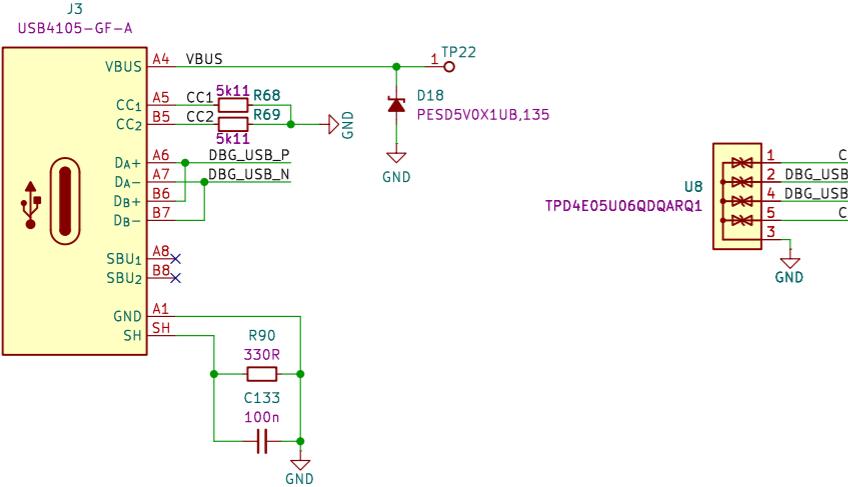


### Bank decoupling

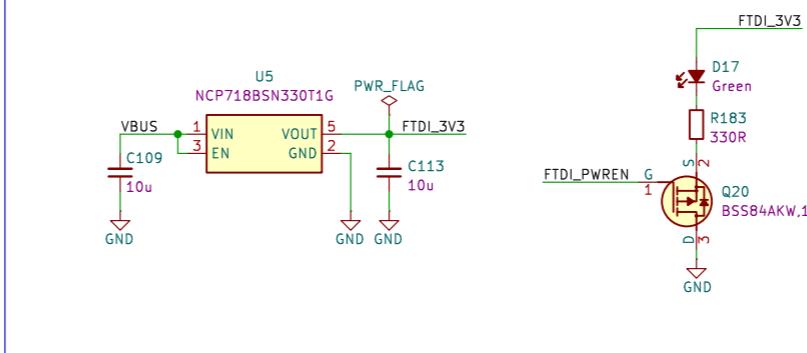


## Debug FTDI

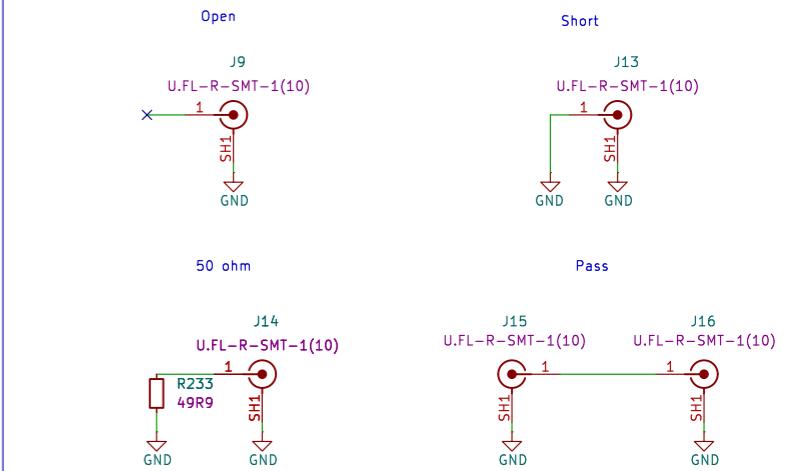
USB-C



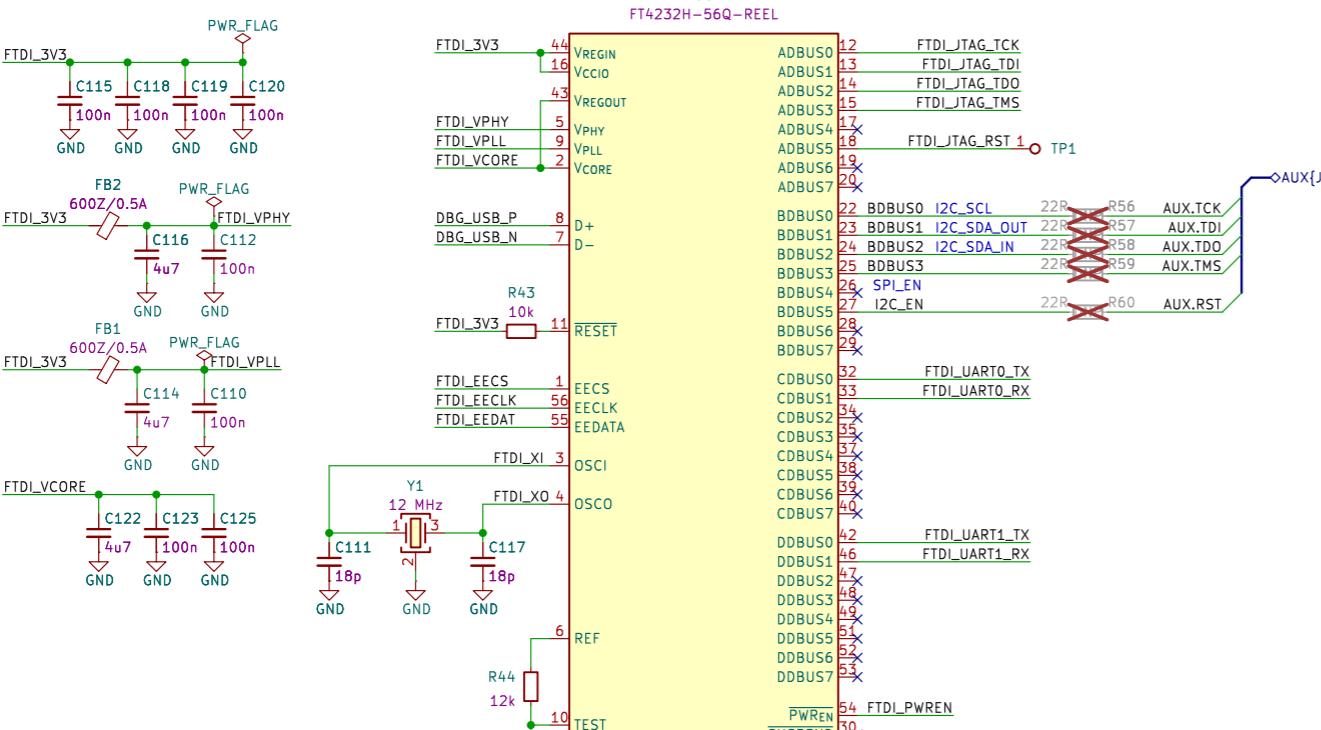
## LDO



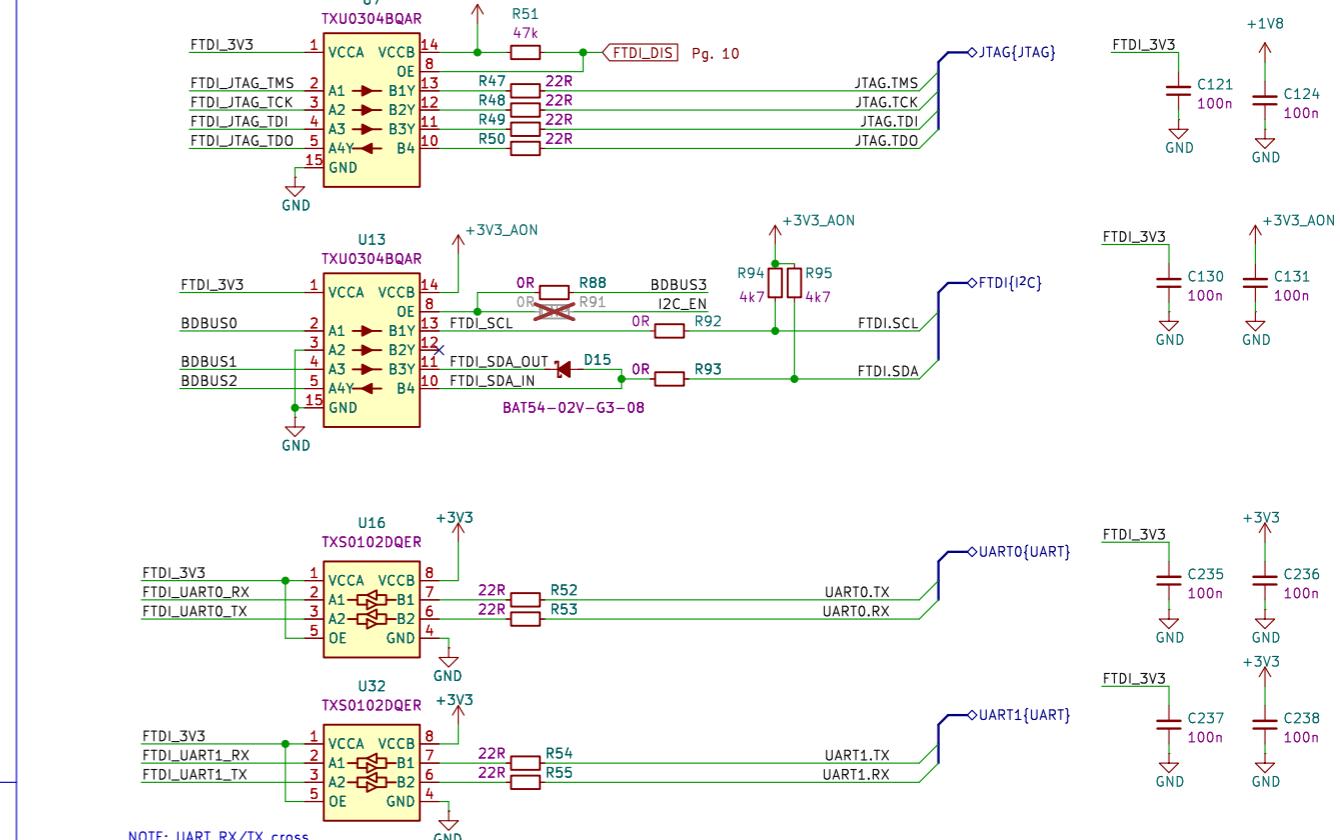
## VNA calibration



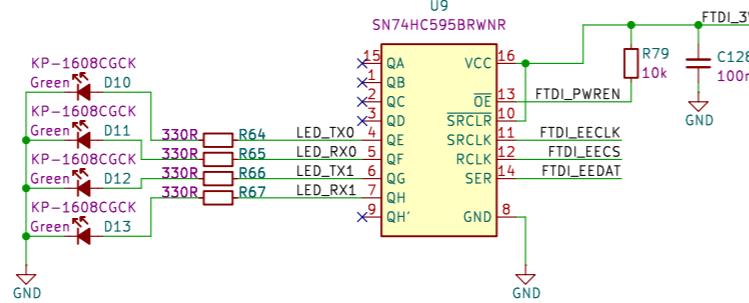
## FTDI



## Logic level translators

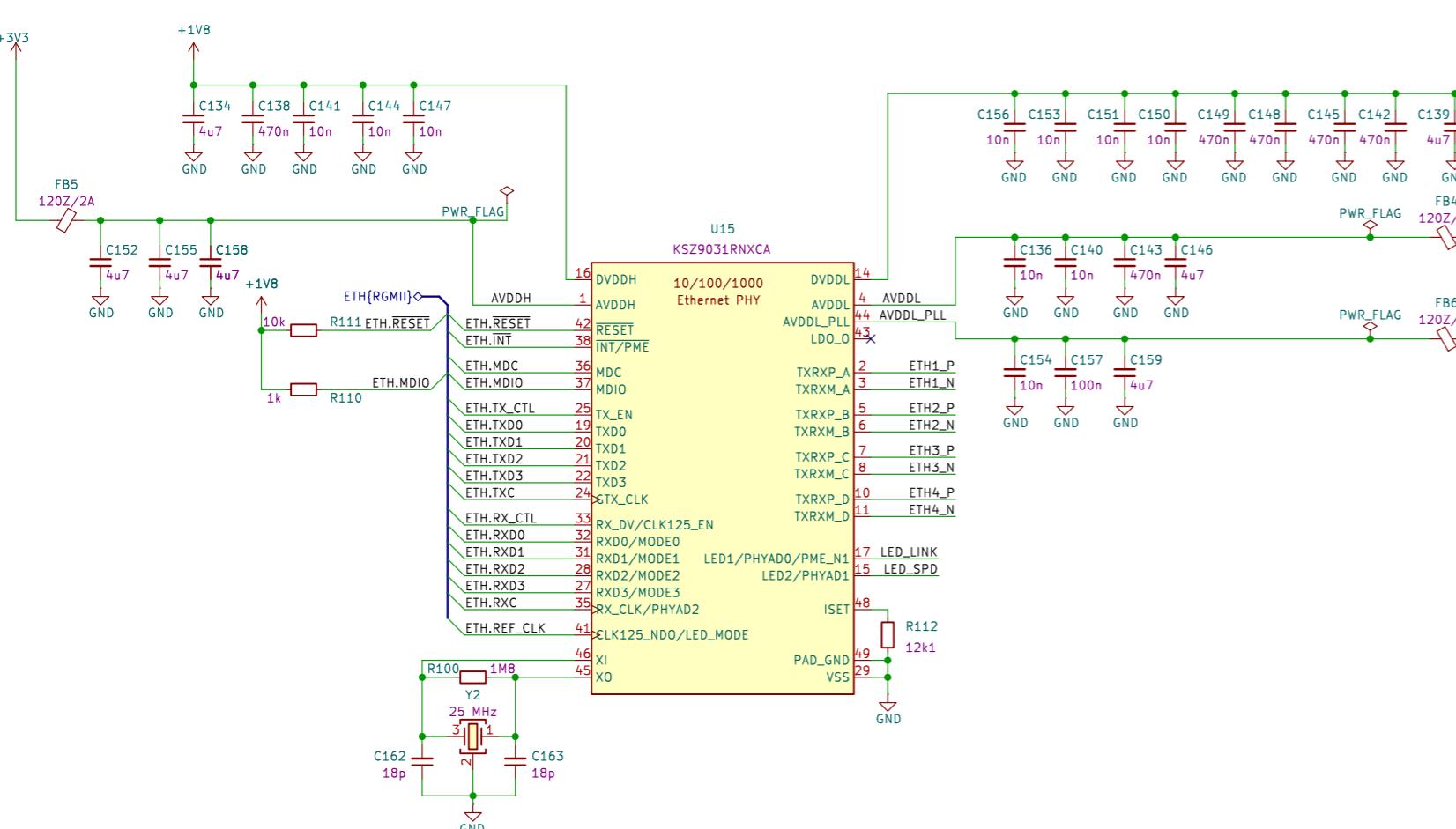


## Shift register

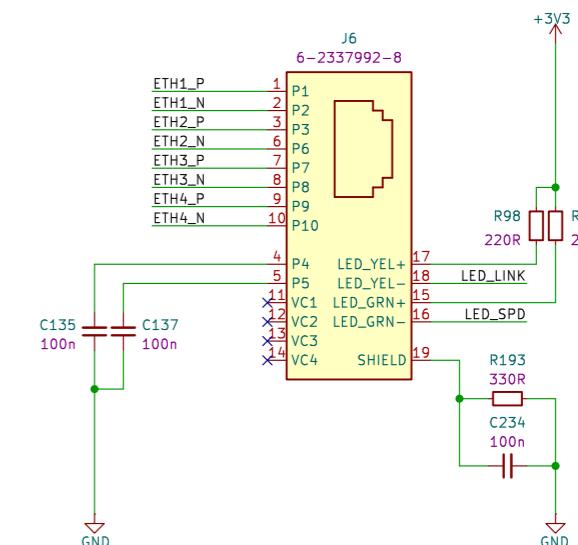


# Gigabit Ethernet

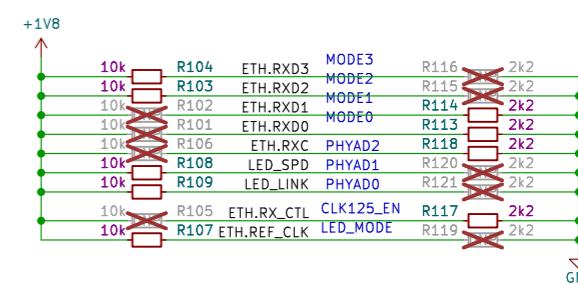
## Ethernet PHY



## RJ45 connector

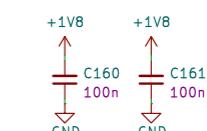


## Bootstrap configuration



MODE[3:0] : 1100 (RMII mode – Advertise 1000BASE-T full-duplex only)  
PHYAD[4:0]: 00011  
CLK125\_EN: 0, disabled  
LED\_MODE: 1, Single LED mode

## Reference plane decoupling



Antmicro  
[www.antmicro.com](http://www.antmicro.com)

Sheet: /Ethernet/  
File: ethernet.kicad.sch

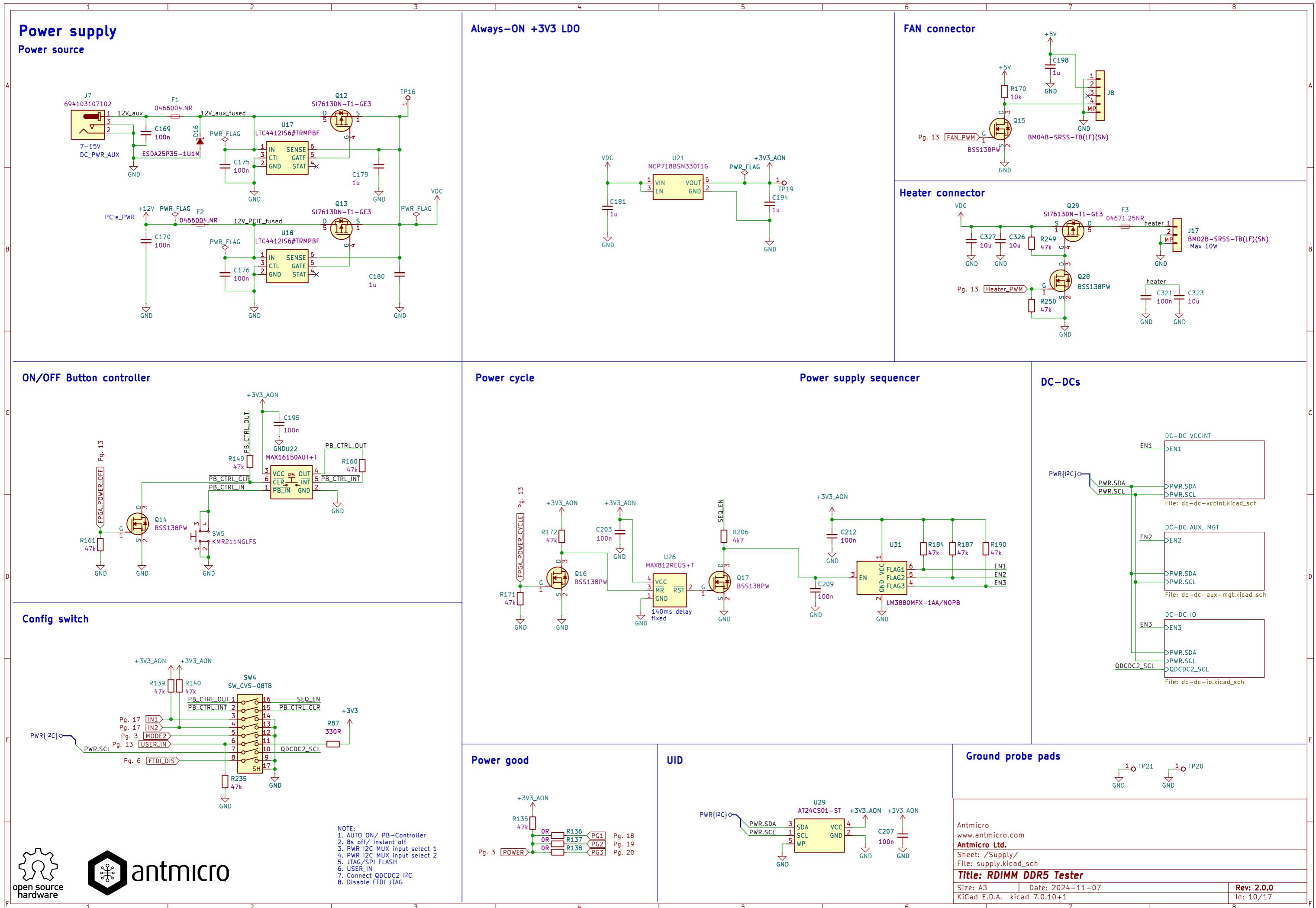
Title: RDIMM DDR5 Tester

Size: A3 Date: 2024-11-07  
KiCad E.D.A. kicad 7.0.10+1

7

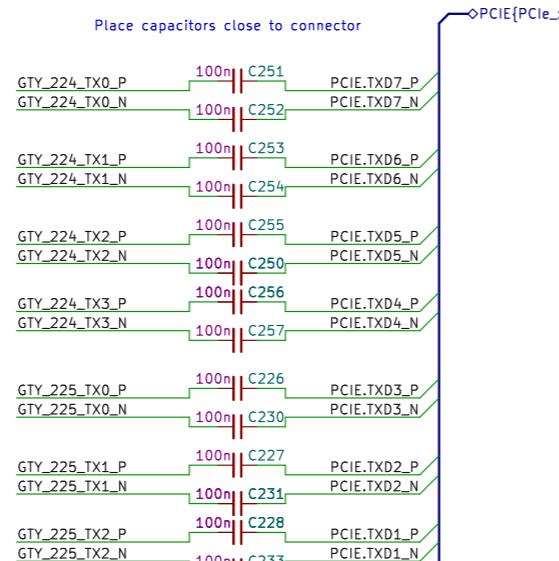
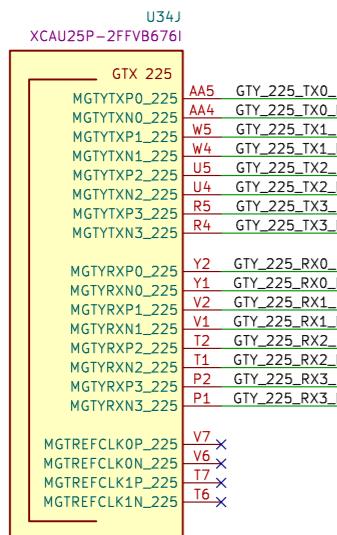
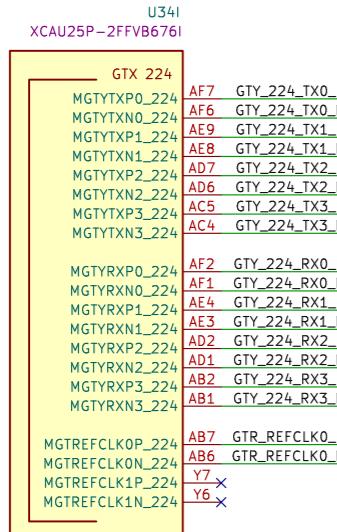
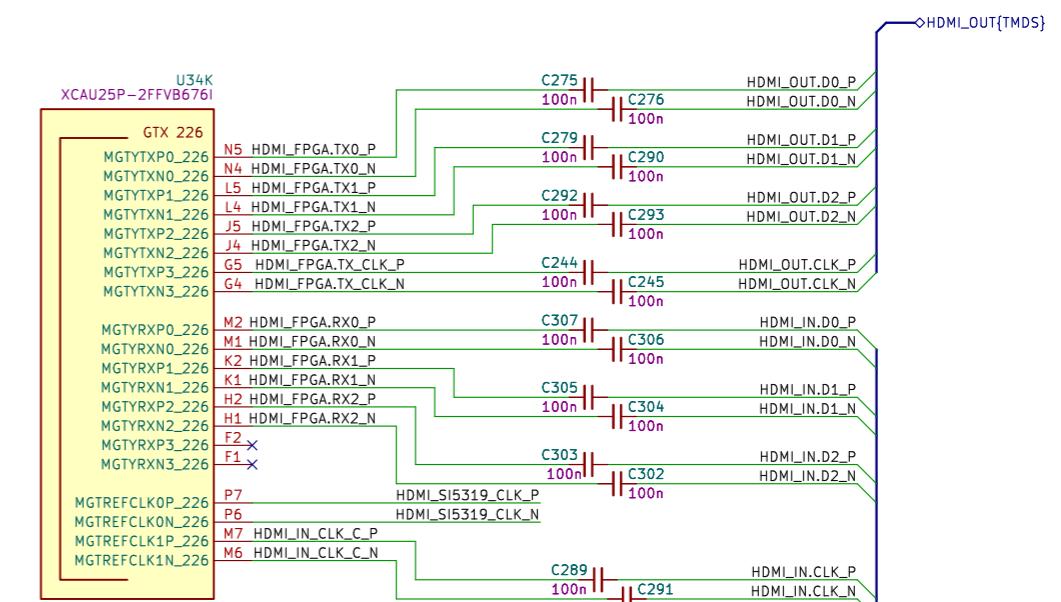
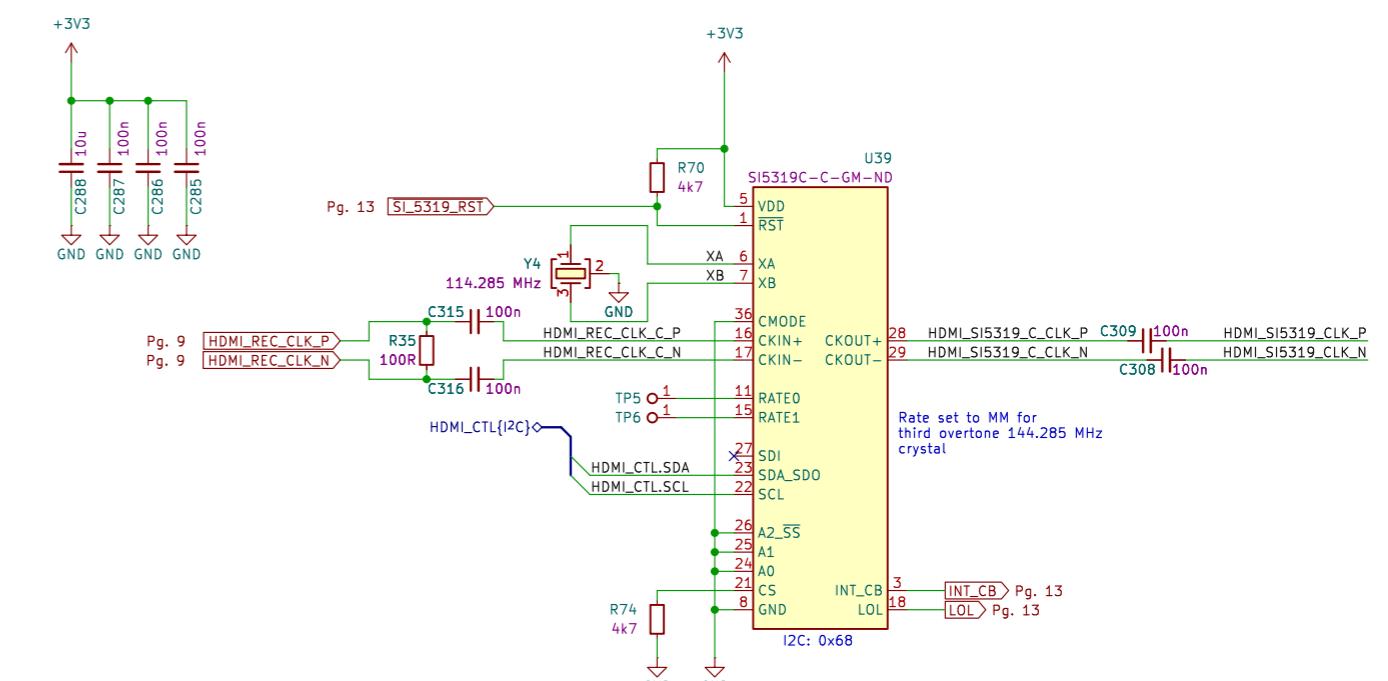






**MGT Interface**

PCIe 3.0 x8

**HDMI****Clock multiplier**

Antmicro  
www.antmicro.com

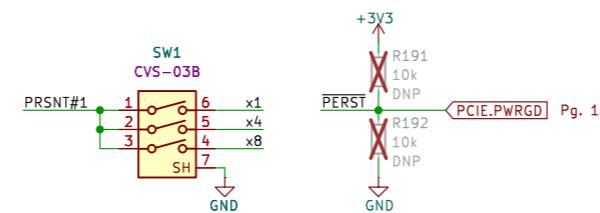
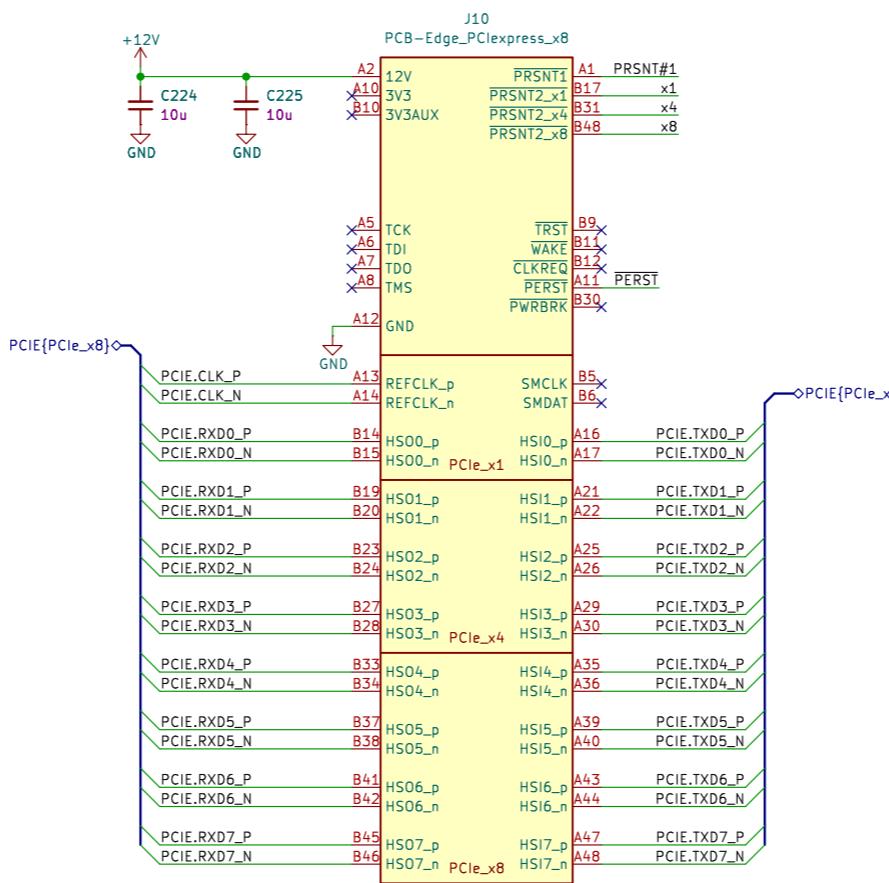
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File: fpga-mgt.kicad\_sch

**Title: RDIMM DDR5 Tester**

Size: A3 Date: 2024-11-07  
KiCad E.D.A. kicad 7.0.10+1

Rev: 2.0.0  
Id: 11/17

# PCIe



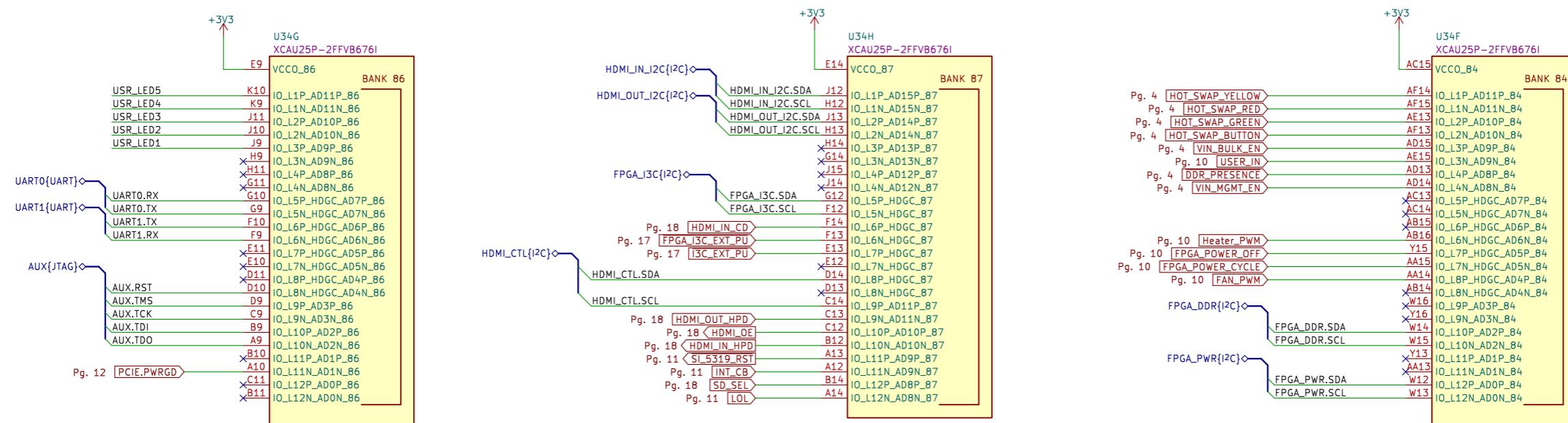
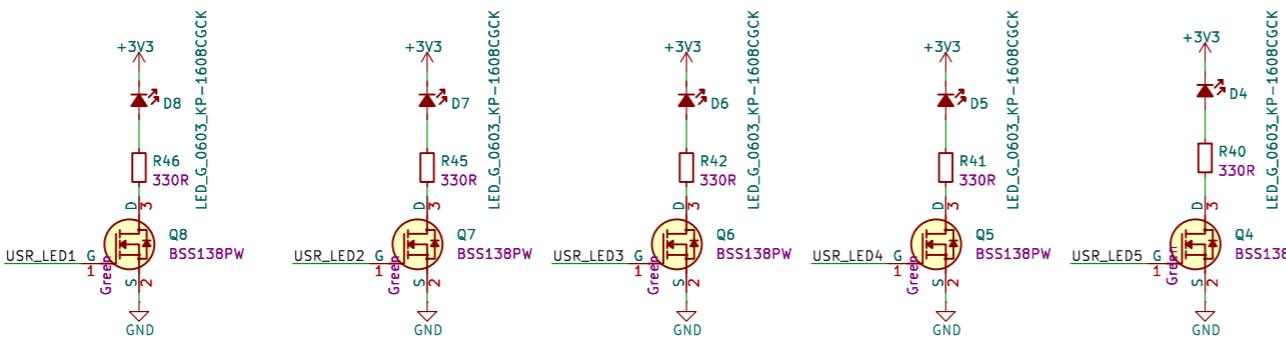
Antmicro  
www.antmicro.com

Sheet: /PCIe connector/  
File: pcie-connector.kicad\_sch

**Title: RDIMM DDR5 Tester**

Size: A3 | Date: 2024-11-07  
KiCad E.D.A. kicad 7.0.10+1

Rev: 2.0.0 | Id: 12/17

**BANKS HD****User LEDs**

Antmicro  
www.antmicro.com

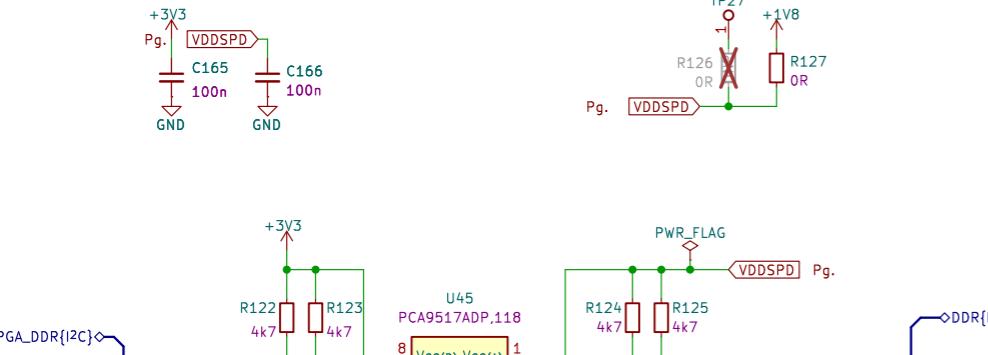
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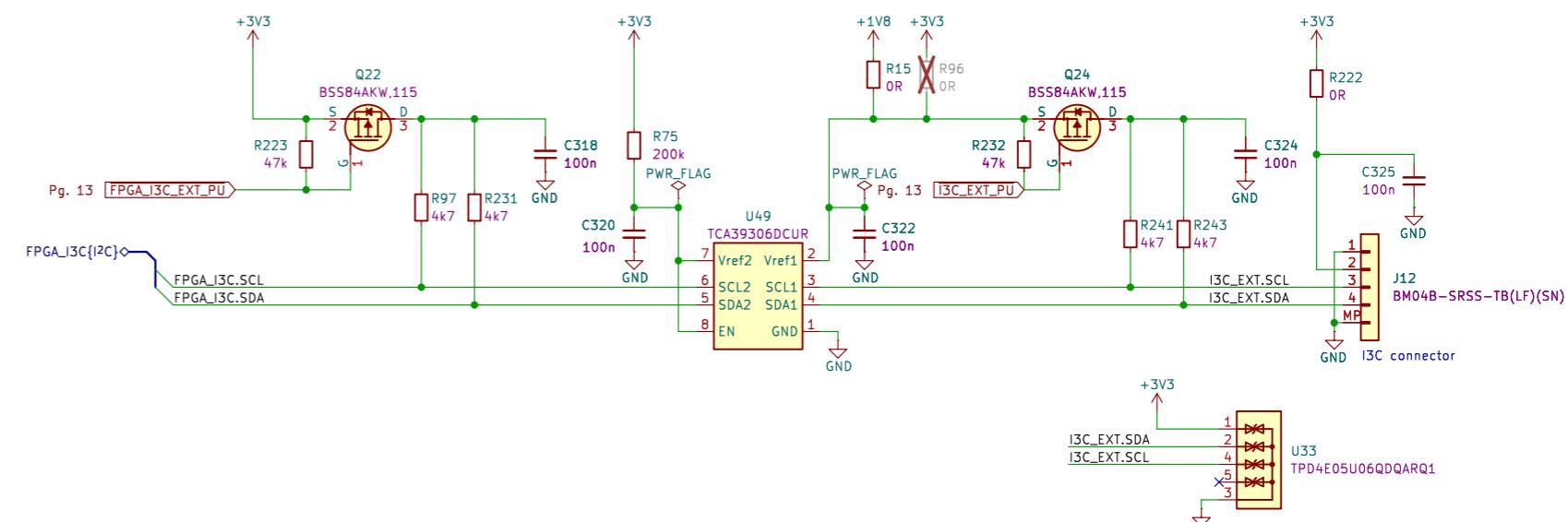
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KiCad E.D.A. kicad 7.0.10+1

Rev: 2.0.0  
Id: 13/17

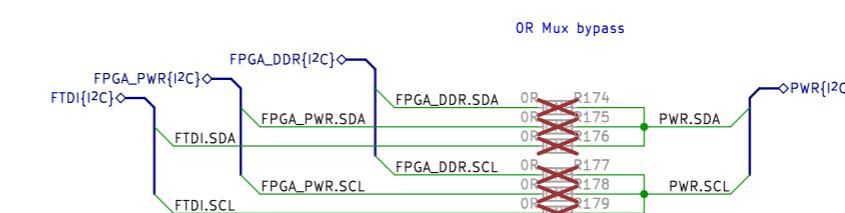
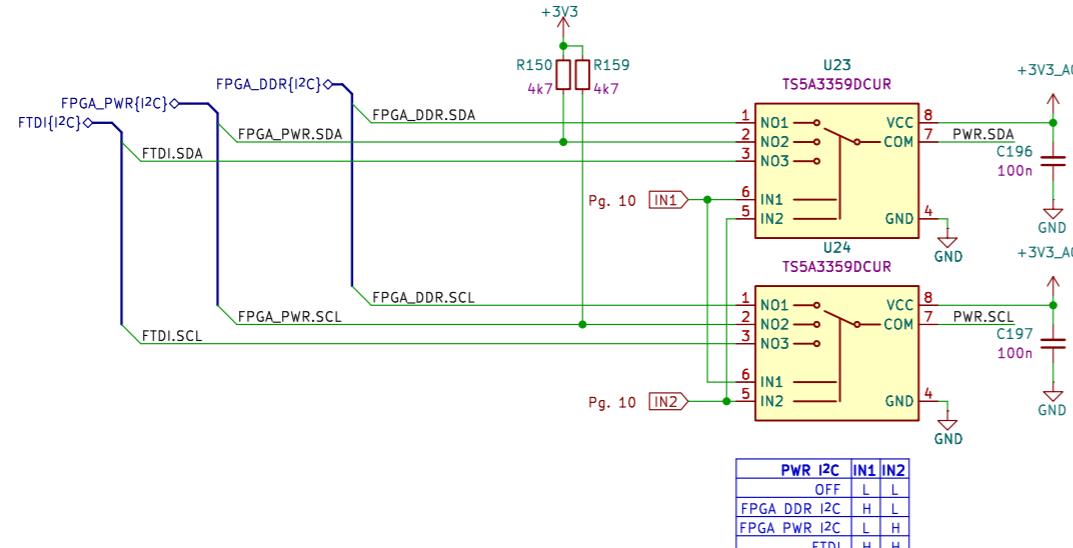
I2C



I3C



PWR I2C MUX



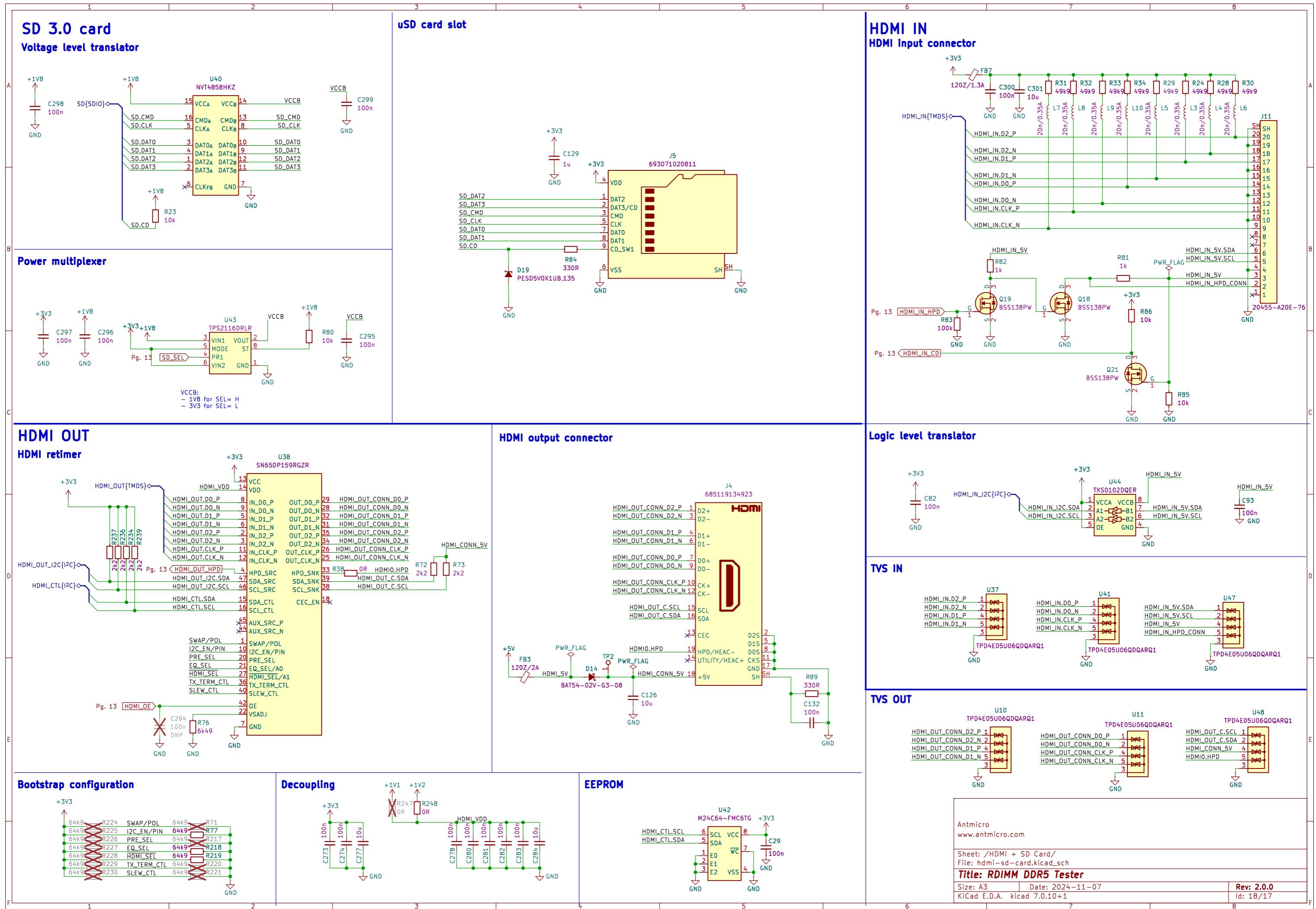
Antmicro  
www.antmicro.com

Sheet: /I2C + I3C/  
File: i2c.kicad\_sch

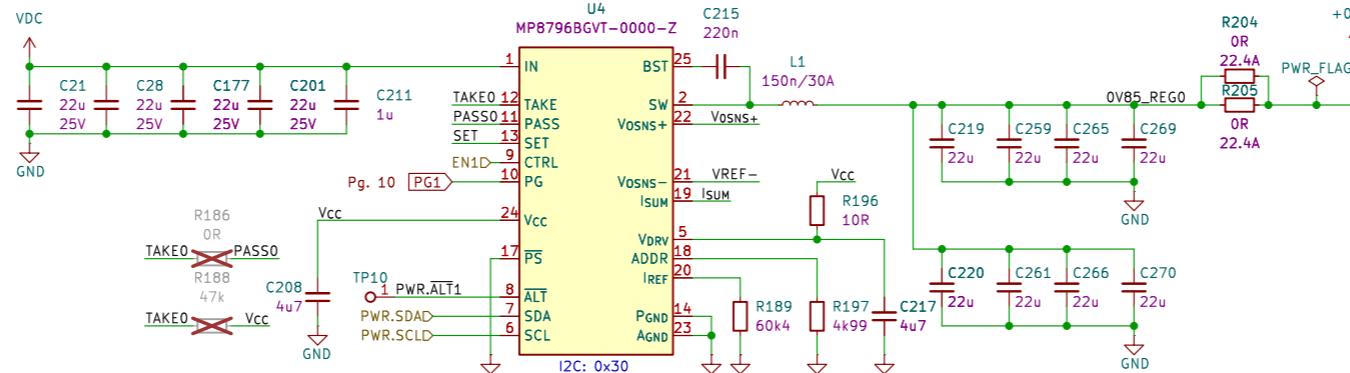
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Size: A3 | Date: 2024-11-07  
KiCad E.D.A. kicad 7.0.10+1

Rev: 2.0.0  
Id: 17/17



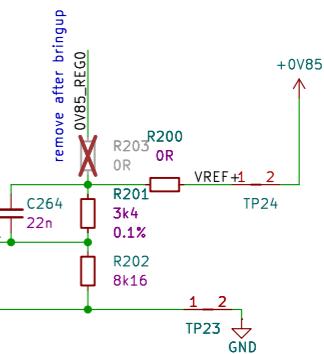
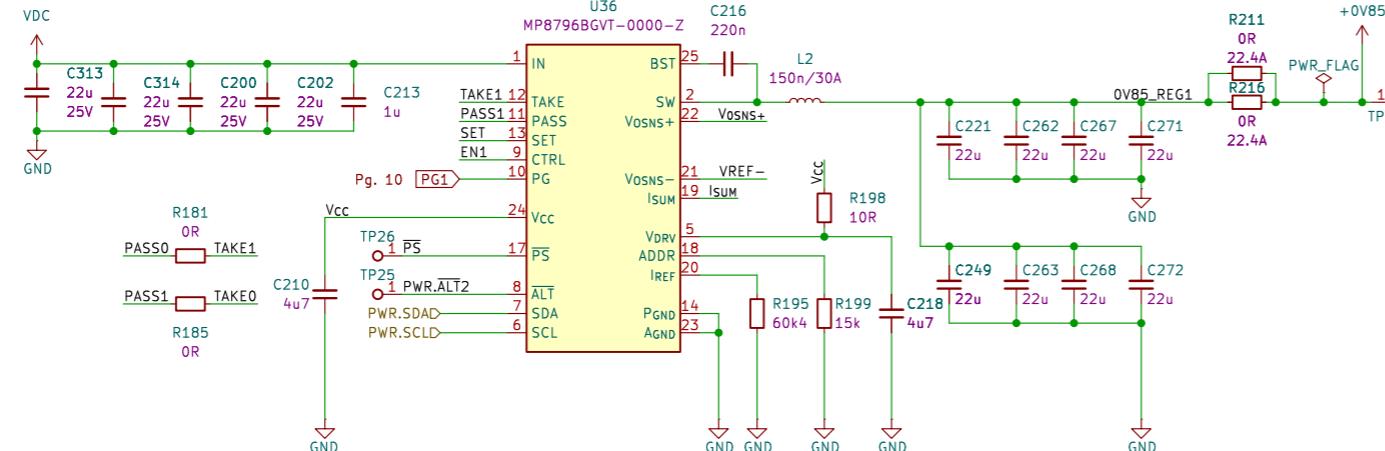
# DC-DC INT



MP8796BGVT-0000-Z selected due to its wide availability on the market  
Replace with MPQ8655GVT when it becomes available on the market

Pin compatible PN: MPQ8645P, MPQ8655GVT

Second phase is for VCCINT > 20A applications  
Do Not Populate if not required  
(place R186 and R188 instead)



Antmicro  
www.antmicro.com

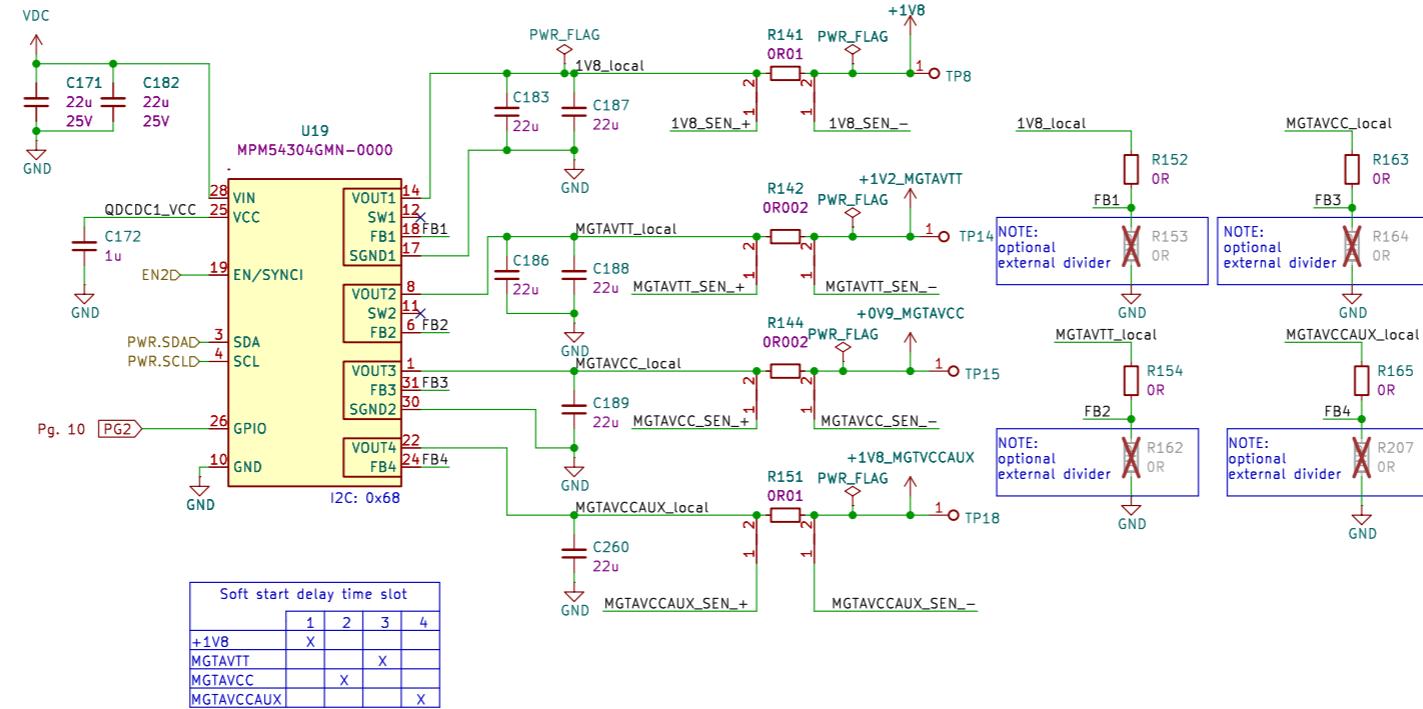
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Title: RDIMM DDR5 Tester

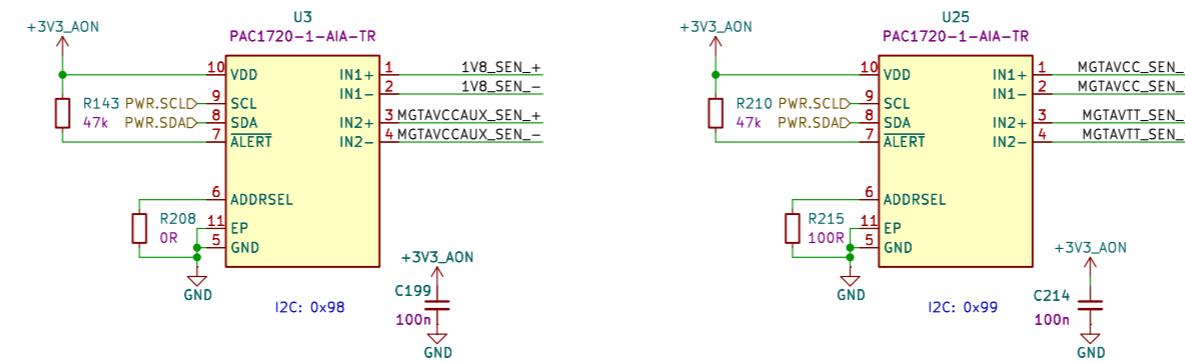
Size: A3 Date: 2024-11-07  
KiCad E.D.A. kicad 7.0.10+1

Rev: 2.0.0  
Id: 18/17

# DC-DC AUX, MGT



## Current sense monitors



Antmicro  
www.antmicro.com

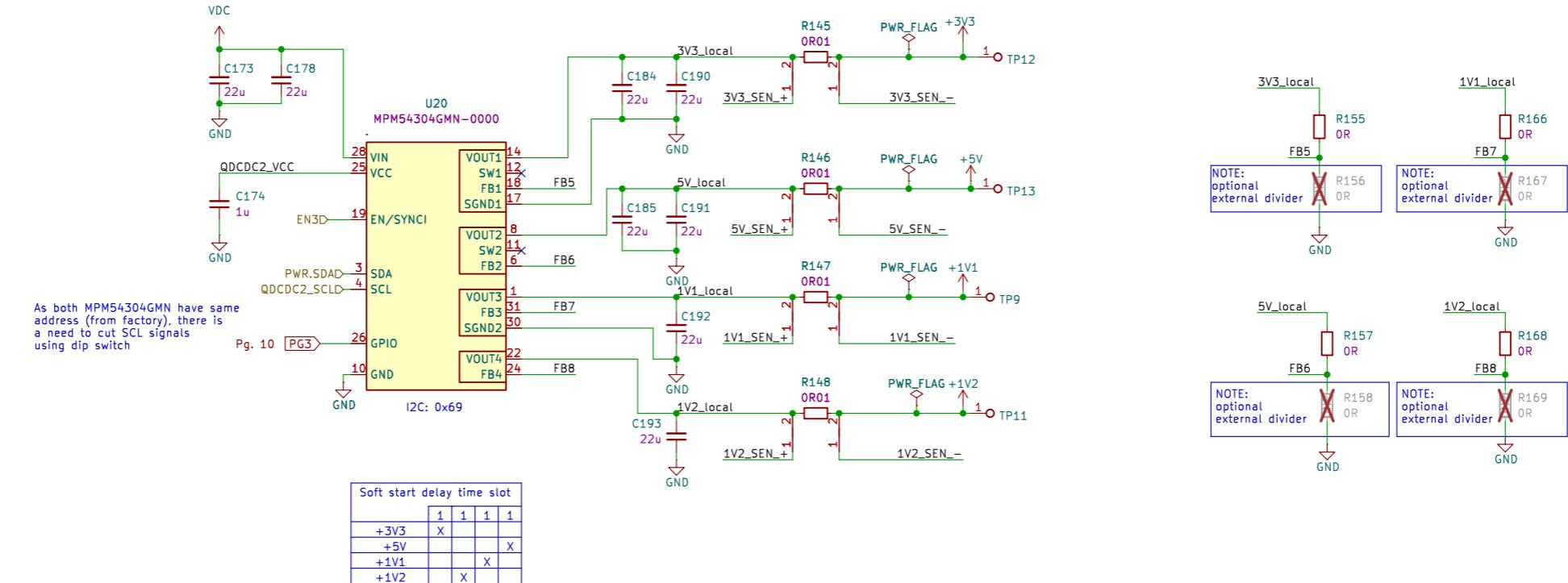
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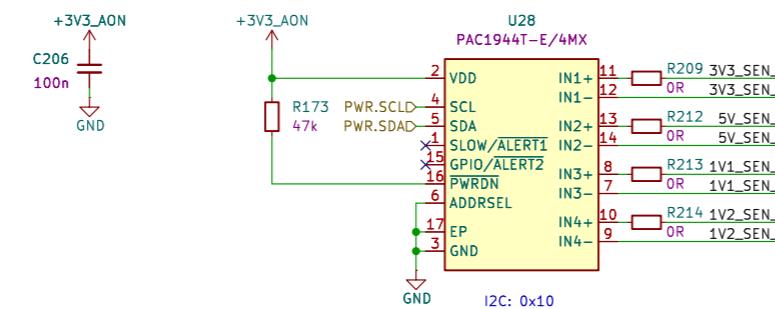
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KiCad E.D.A. kicad 7.0.10+1

Rev: 2.0.0 | Id: 19/17

## DC-DC IO



## Current sense monitor



Antmicro  
www.antmicro.com

Sheet: /Supply/DC-DC IO/  
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**Title: RDIMM DDR5 Tester**

Size: A3 | Date: 2024-11-07  
KiCad E.D.A. kicad 7.0.10+1

Rev: 2.0.0 | Id: 20/17