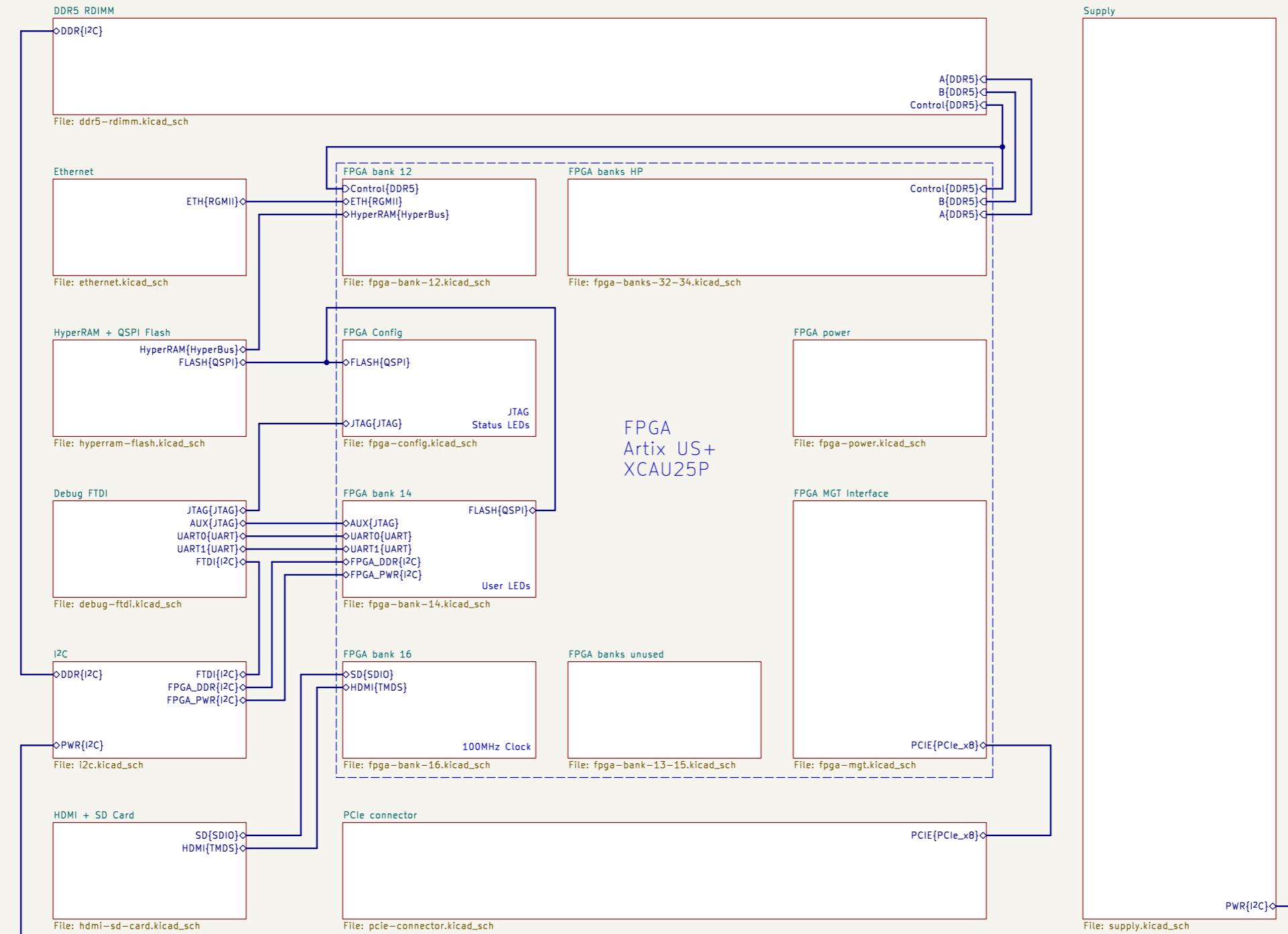
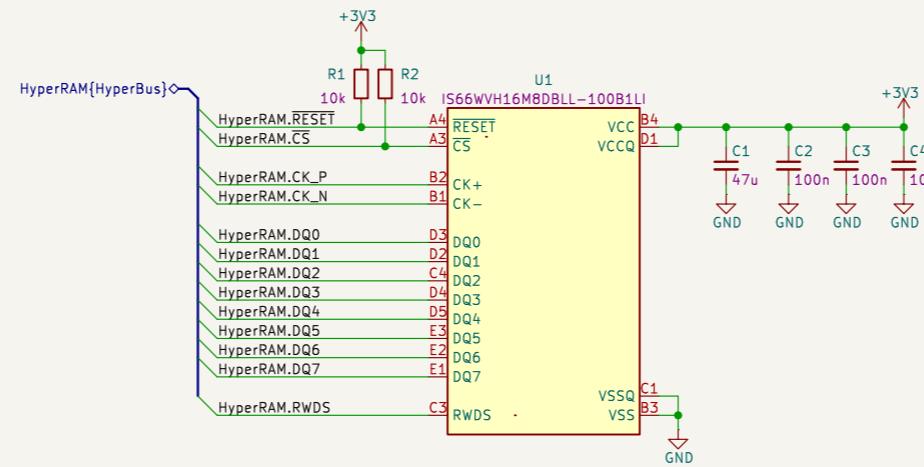


# RDIMM DDR5 Tester Ultrascale Plus

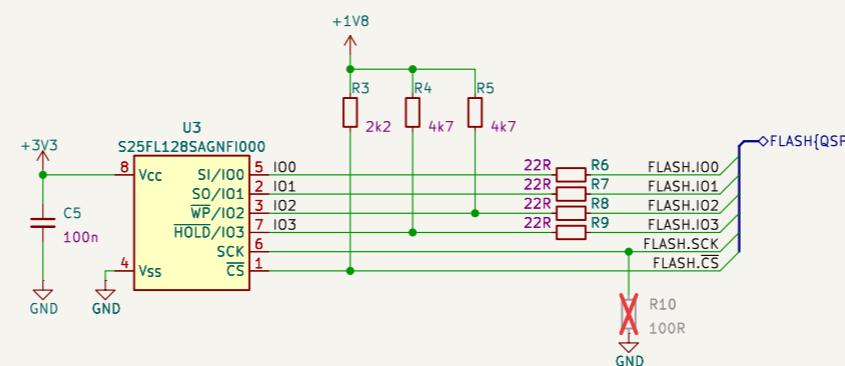


# HyperRAM

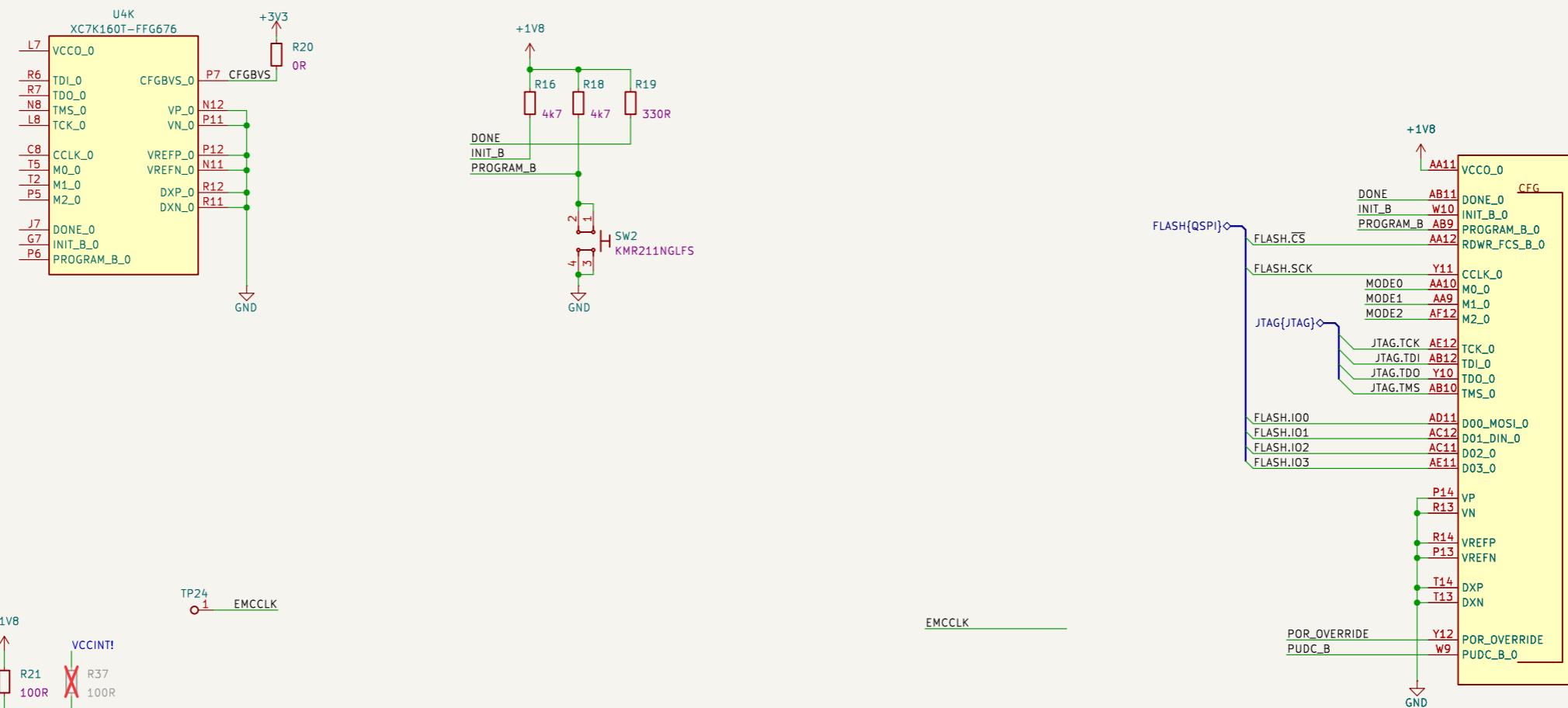


## (Q)SPI flash

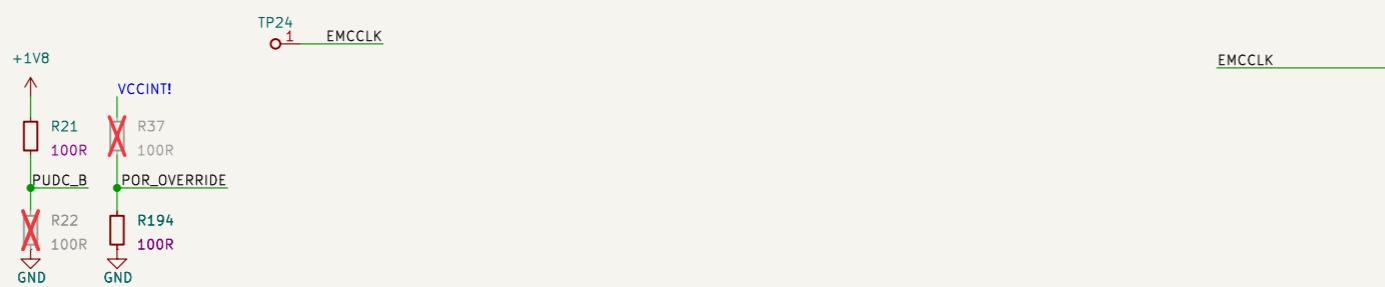
Master SPI Quad (x4) configuration scheme  
Follows Figure 2-14 7 Series FPGAs Configuration User Guide  
UG470 (v1.13.1)



# FPGA BANK 0

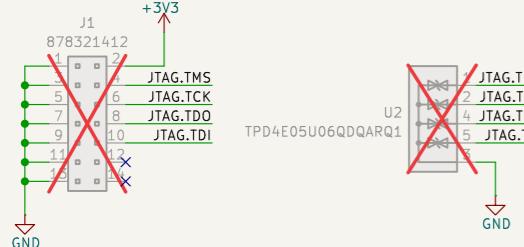


## Probes

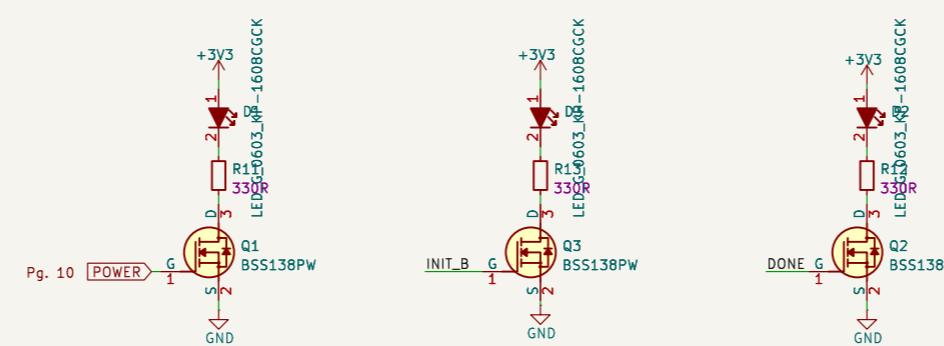


## JTAG Connector

Compatible with Xilinx Platform Cable

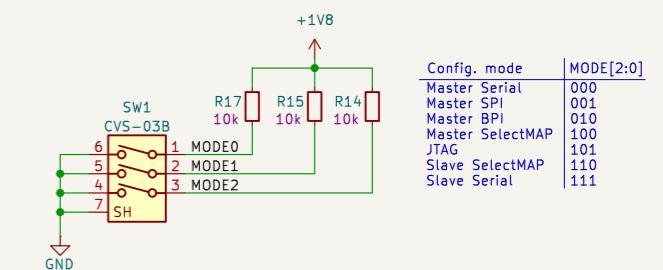


## STATUS LEDs

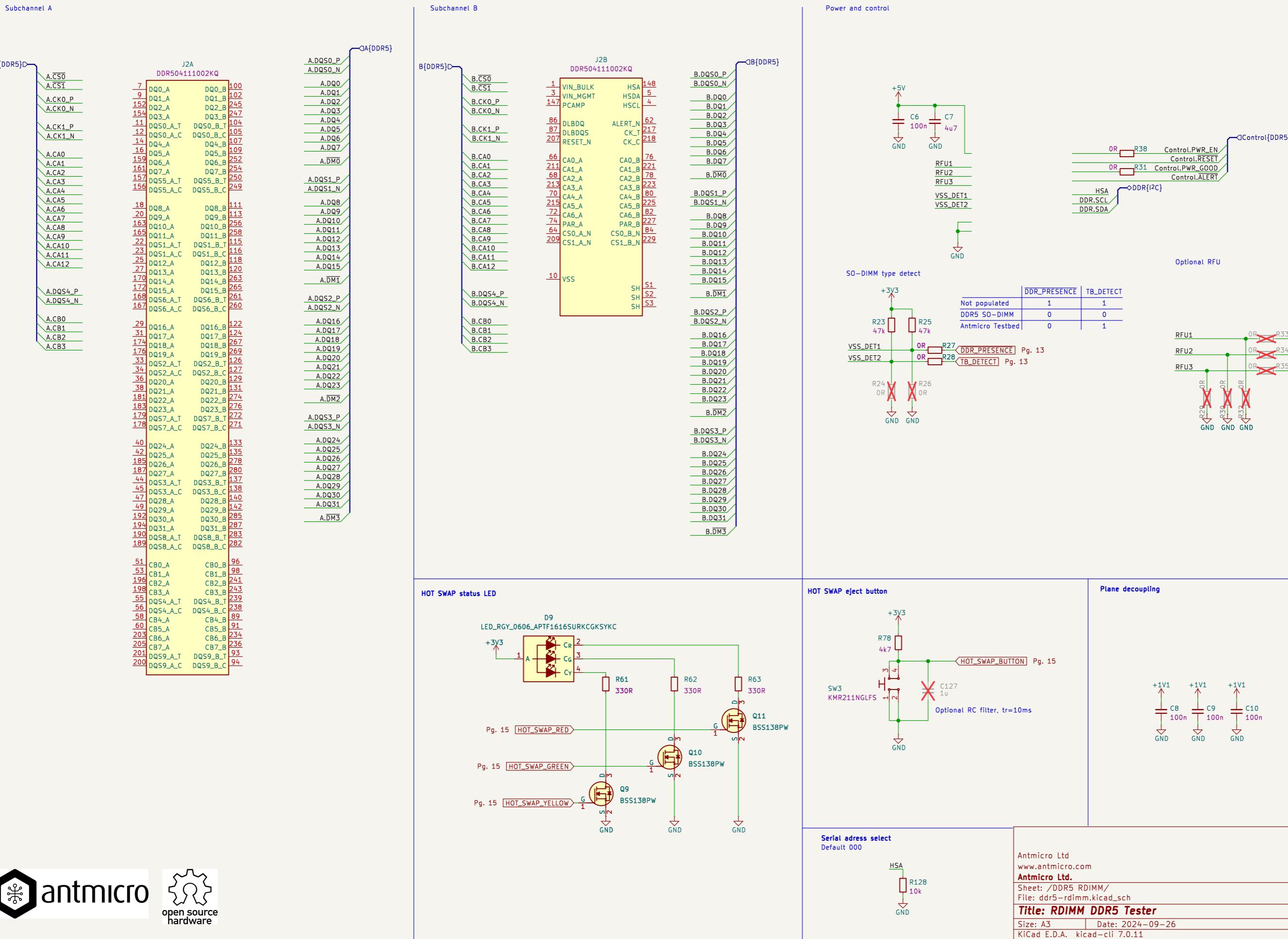


## Configuration Modes

For details, see UG570

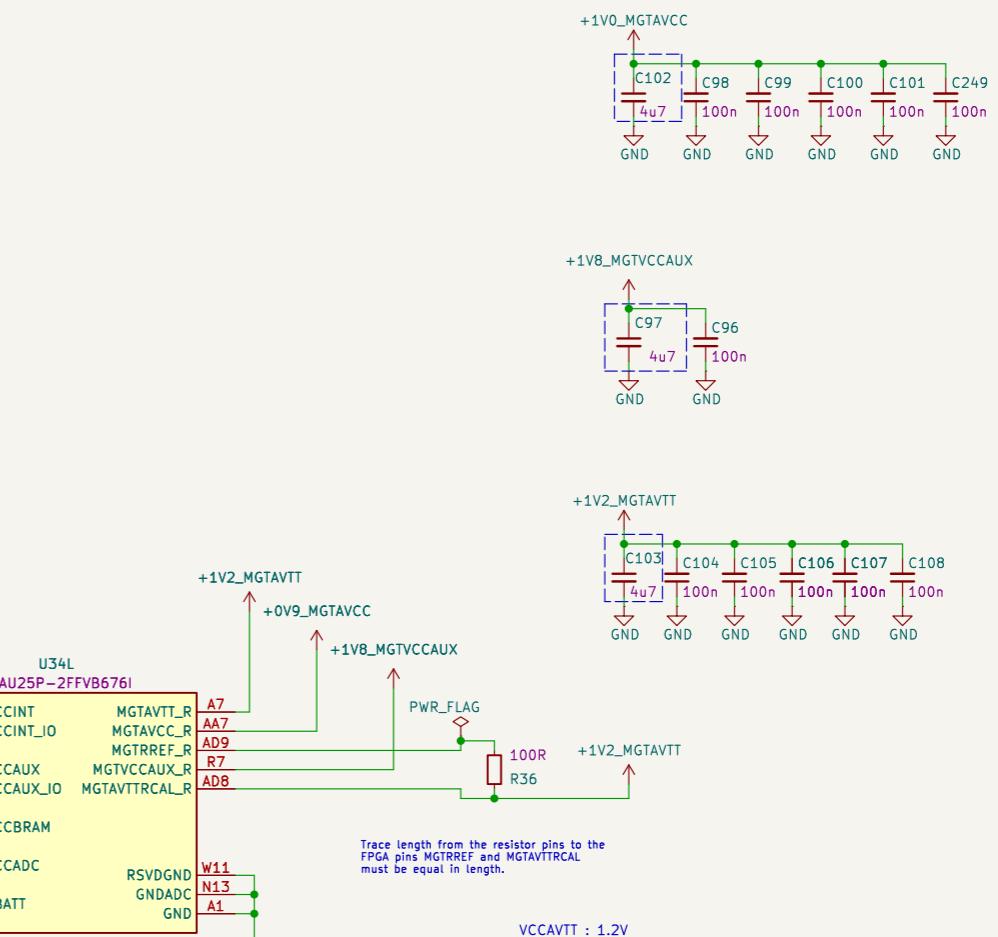
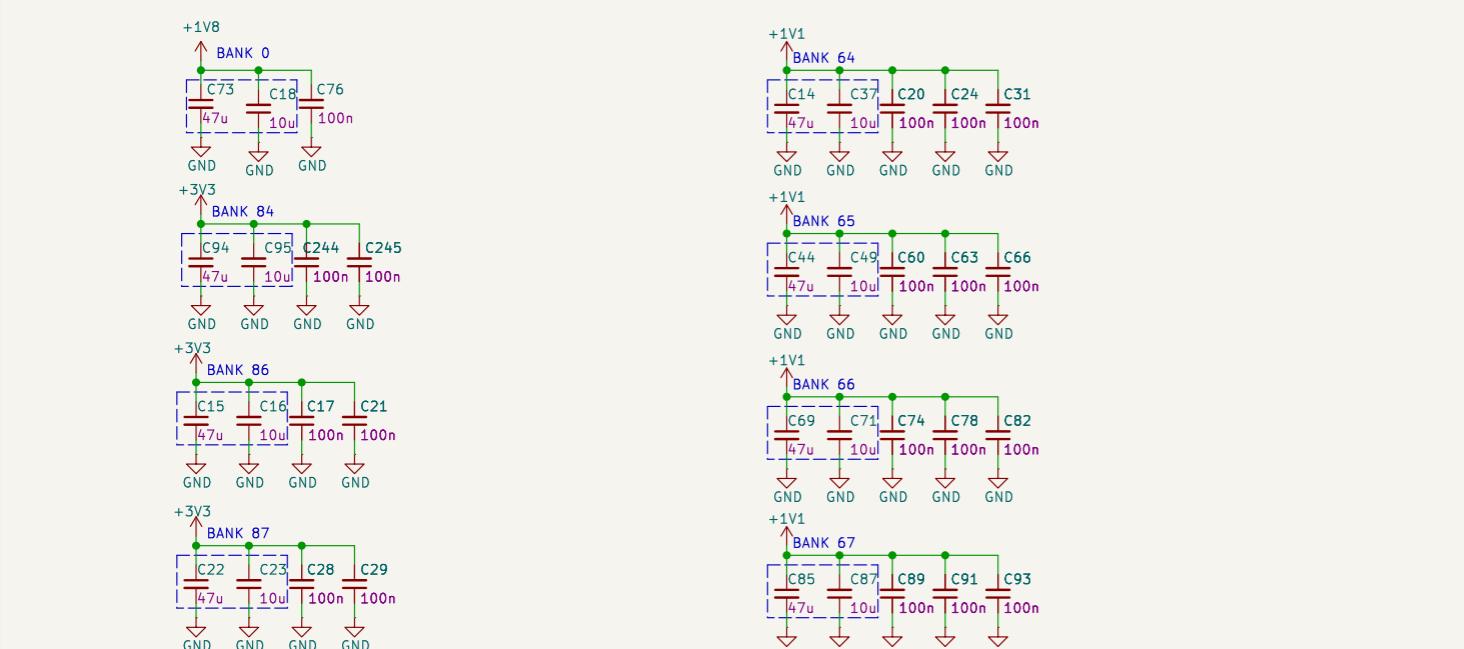
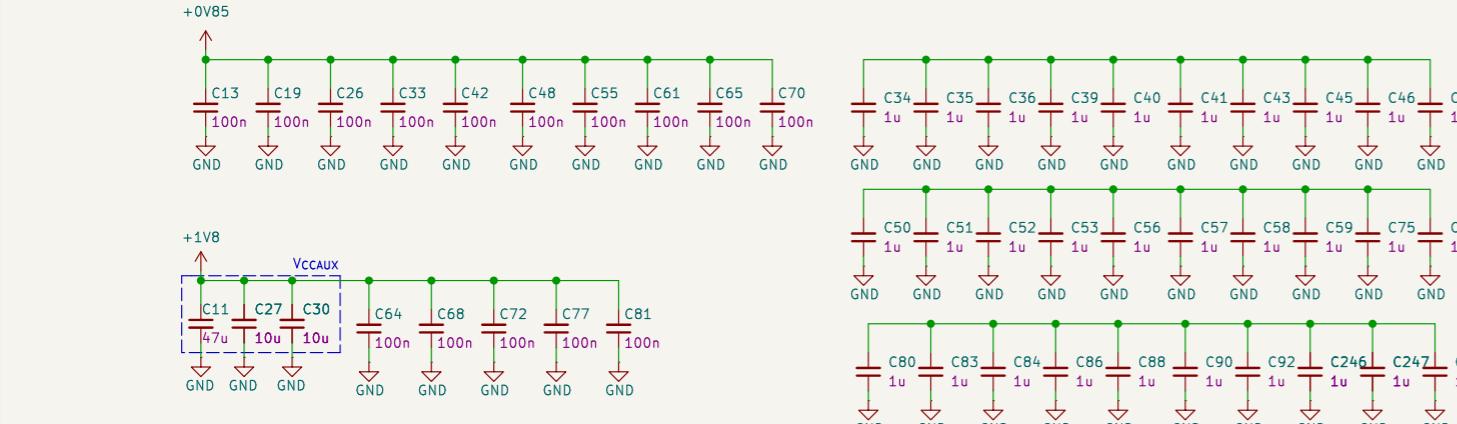
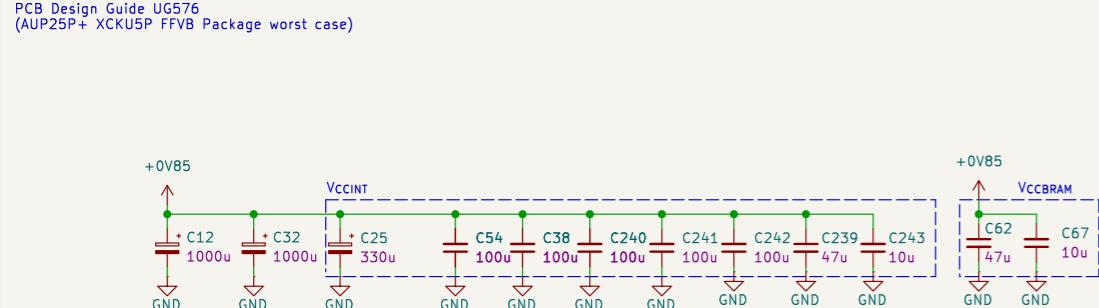


# DDR5 RDIMM connector



**FPGA Power rails**

Bank marked by dashed line  
referenced from US+ Series FPGAs  
PCB Design Guide UG583  
(AUP25P+ XCKU5P FFVB Package worst case)  
MGT decoupling marked by dashed line  
referenced from US+ Series FPGAs  
PCB Design Guide UG576  
(AUP25P+ XCKU5P FFVB Package worst case)



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Sheet: /FPGA power/  
File: fpga-power.kicad\_sch

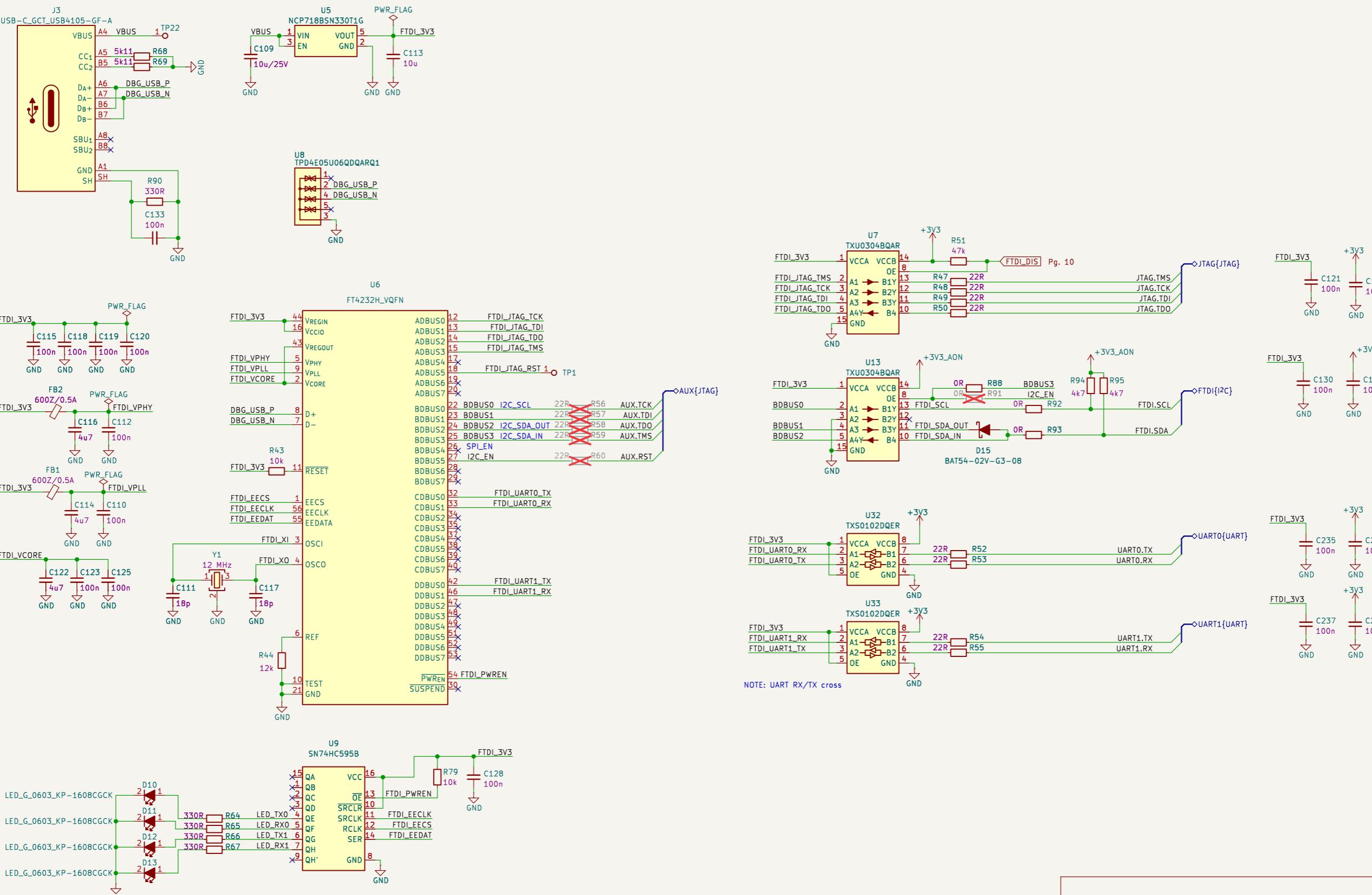
Title: RDIMM DDR5 Tester

Size: A3 Date: 2024-09-26  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 2.0.0:1aec8  
Id: 5/17



# Debug FTDI



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Sheet: /Debug\_FTDI/  
File: debug-ftdi.kicad\_sch

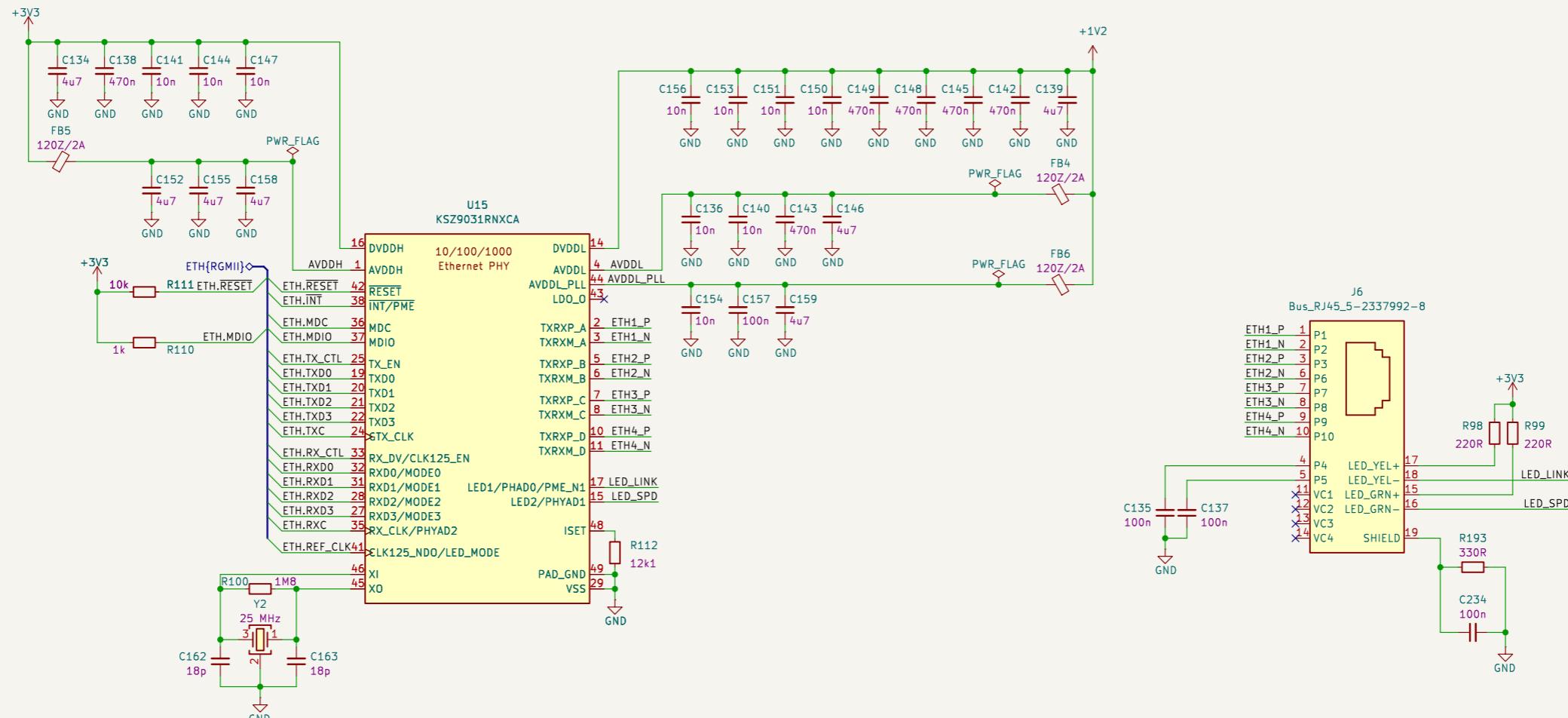
Title: RDIMM DDR5 Tester

Size: A3 Date: 2024-09-26  
KiCad E.D.A. kicad-cli 7.0.11

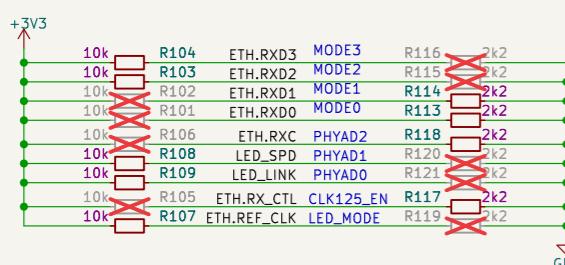
Rev: 2.0.0:1aec8  
Id: 6/17



# Gigabit Ethernet

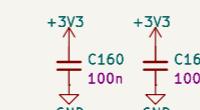


## Bootstrap configuration



MODE[3:0] : 1100 (RGMII mode – Advertise 1000BASE-T full-duplex only)  
PHYAD[4:0] : 00011  
CLK125\_EN: 0, disabled  
LED\_MODE: 1, Single-LED mode

## Reference plane decoupling



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Sheet: /Ethernet/  
File: ethernet.kicad\_sch

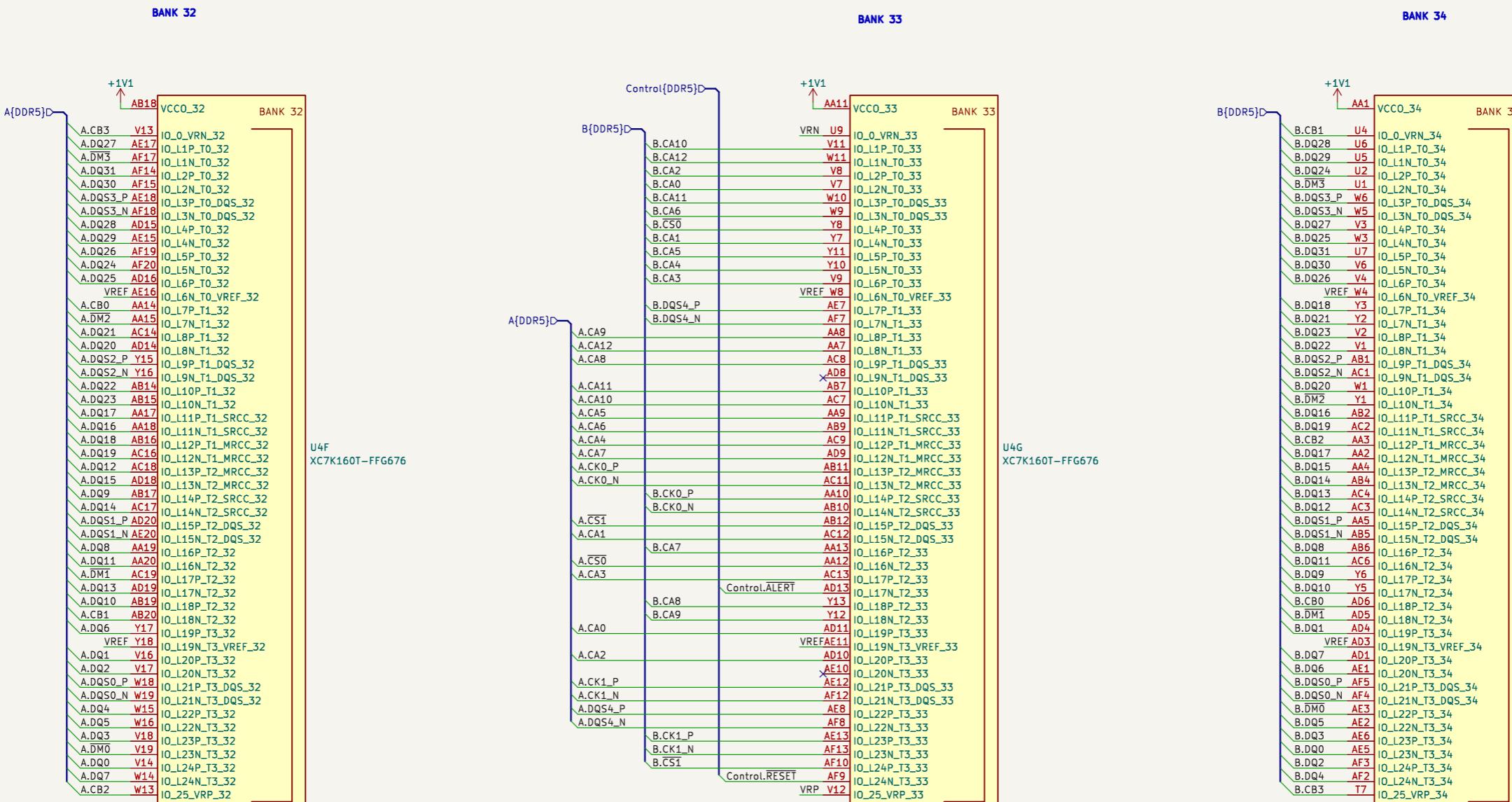
## Title: RDIMM DDR5 Tester

Size: A3 Date: 2024-09-26  
KiCad E.D.A. kicad-cl 7.0.11

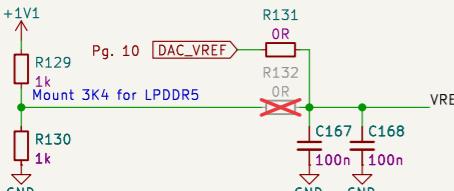
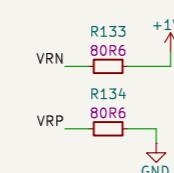
Rev: 2.0.0:1aec8  
Id: 8/17

**HP Banks**

VCCO (HP banks) max: 2.0V



Pinout D.1.1

**VREF****Reference termination**

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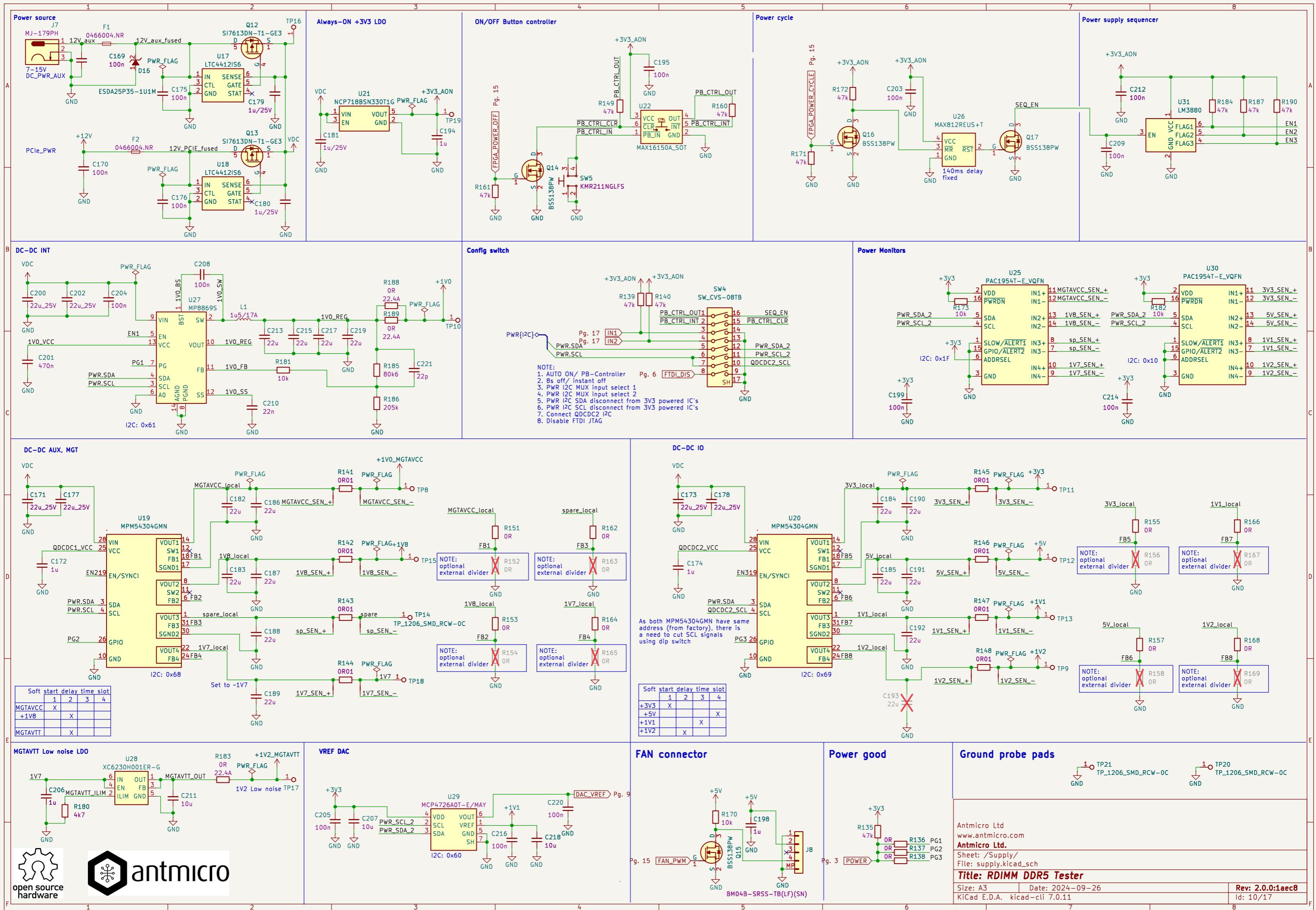
Antmicro Ltd.

Sheet: /FPGA banks HP/  
File: fpga-banks-32-34.kicad\_sch

Title: RDIMM DDR5 Tester

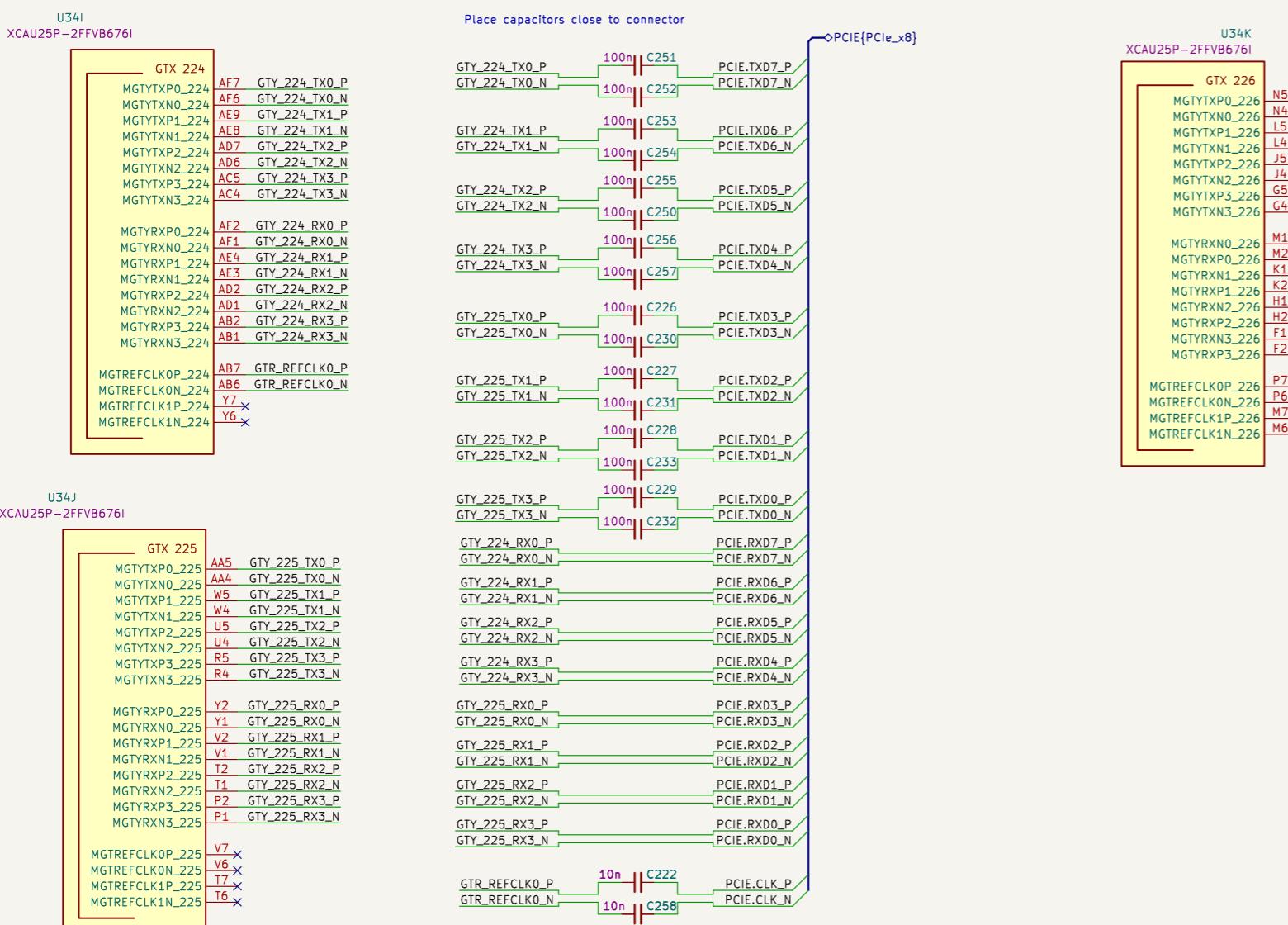
Size: A3 Date: 2024-09-26  
KiCad E.D.A. kicad-cl 7.0.11

Rev: 2.0.0:1aec8  
Id: 9/17



**MGT Interface**

A



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Sheet: /FPGA MGT Interface/  
File: fpga-mgt.kicad\_sch

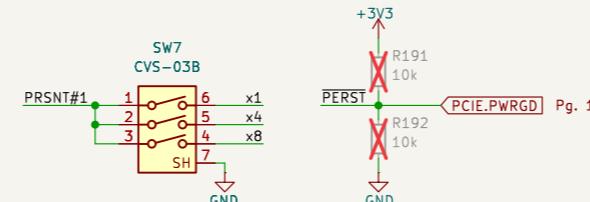
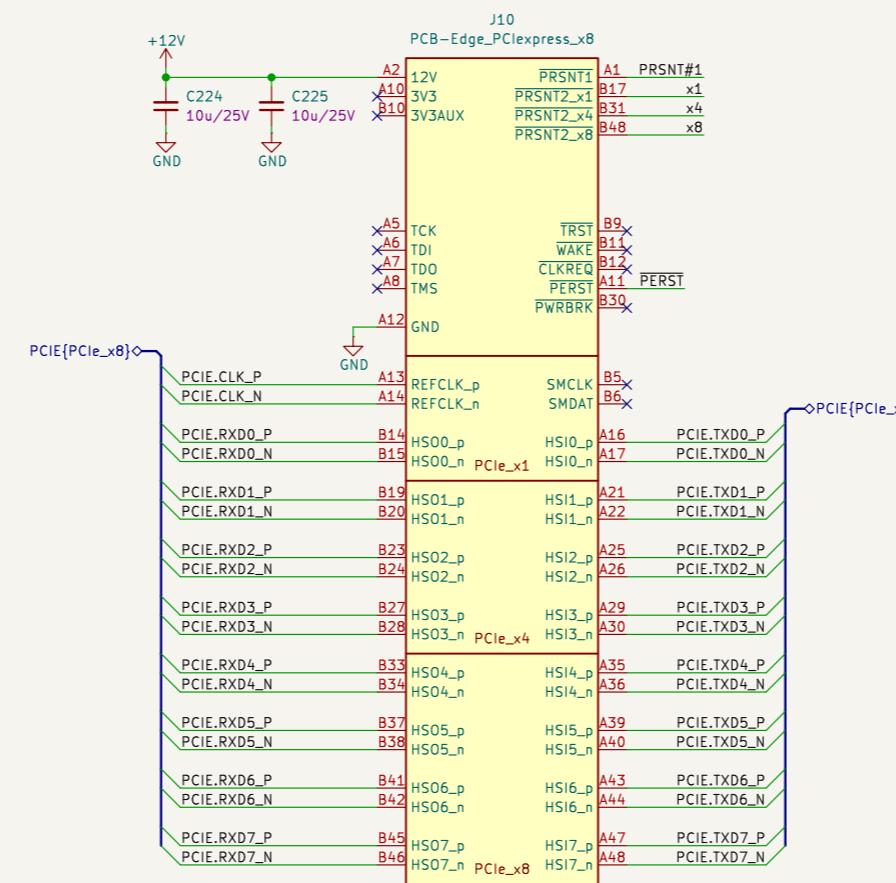
**Title: RDIMM DDR5 Tester**

Size: A3 | Date: 2024-09-26  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 2.0.0:1aec8  
Id: 11/17

F

## PCIe



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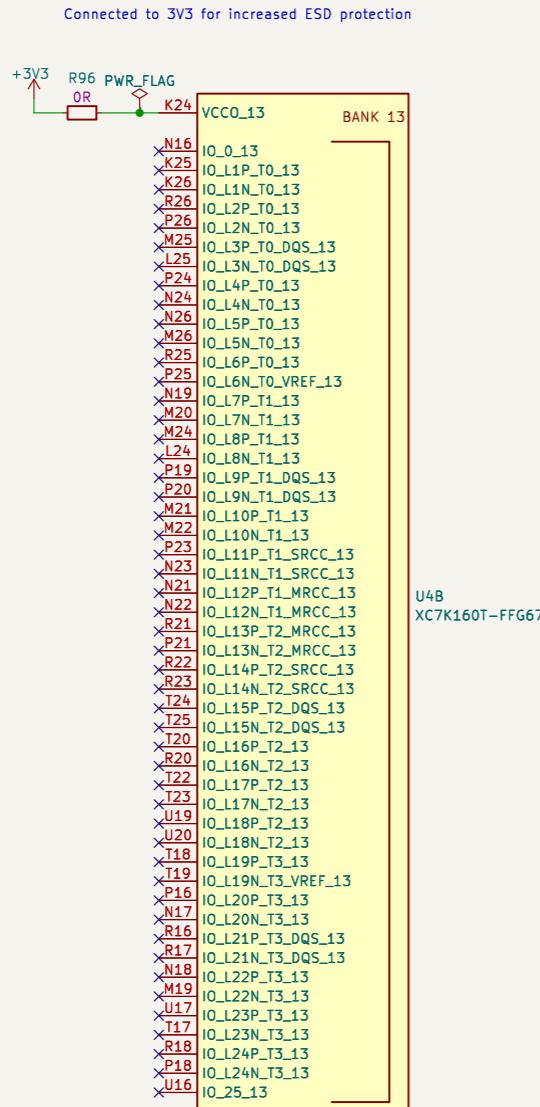
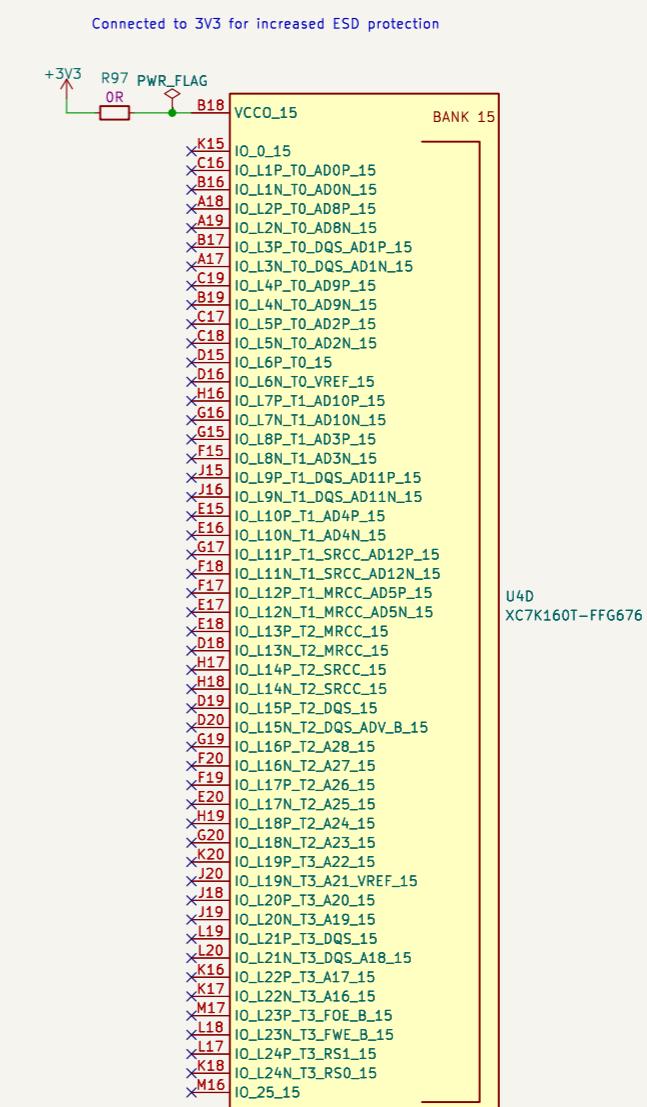
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File: pcie-connector.kicad\_sch

**Title: RDIMM DDR5 Tester**

Size: A3 | Date: 2024-09-26  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 2.0.0:1aec8  
Id: 12/17



**BANK 13****BANK 15**

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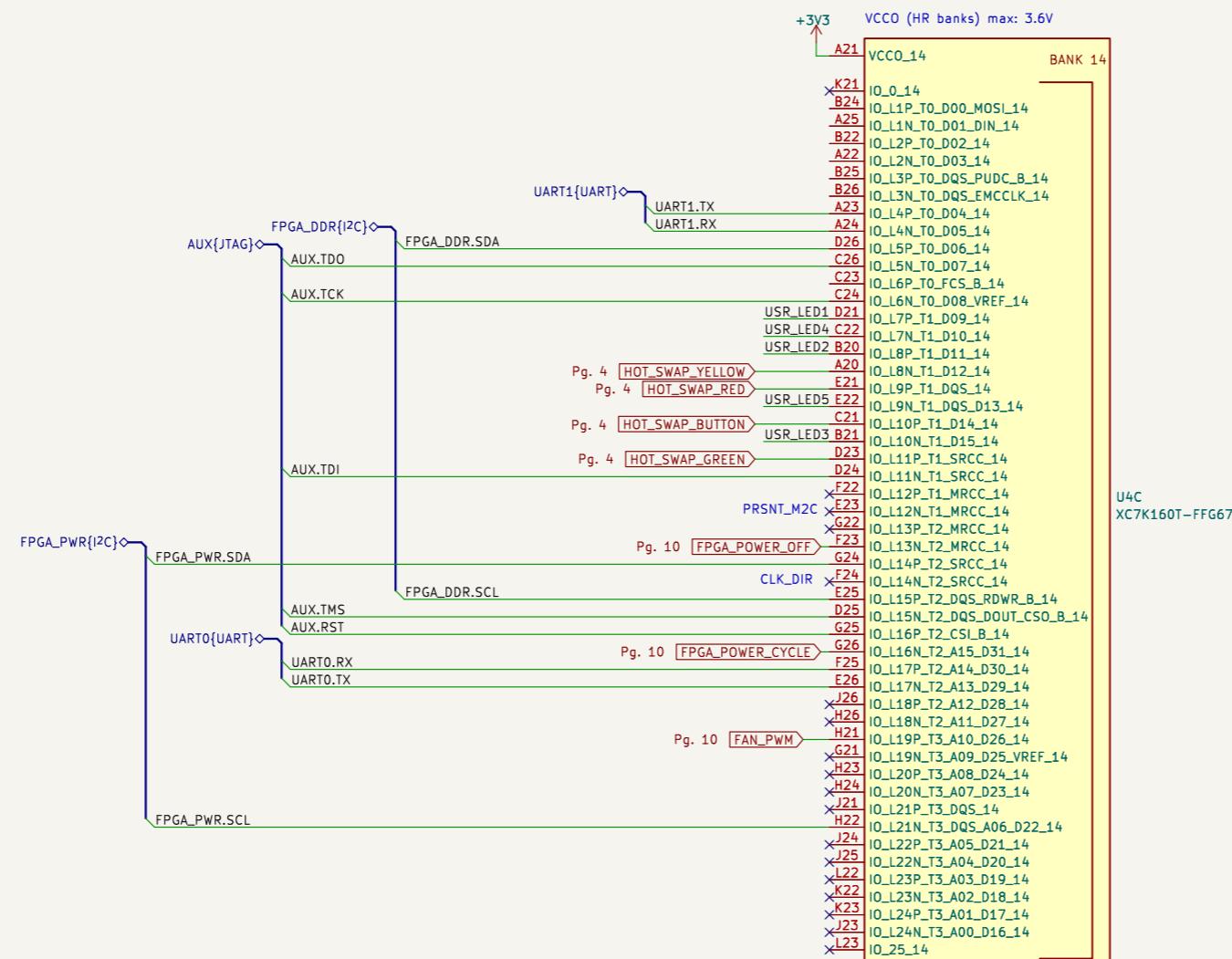
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File: fpga-bank-13-15.kicad\_sch

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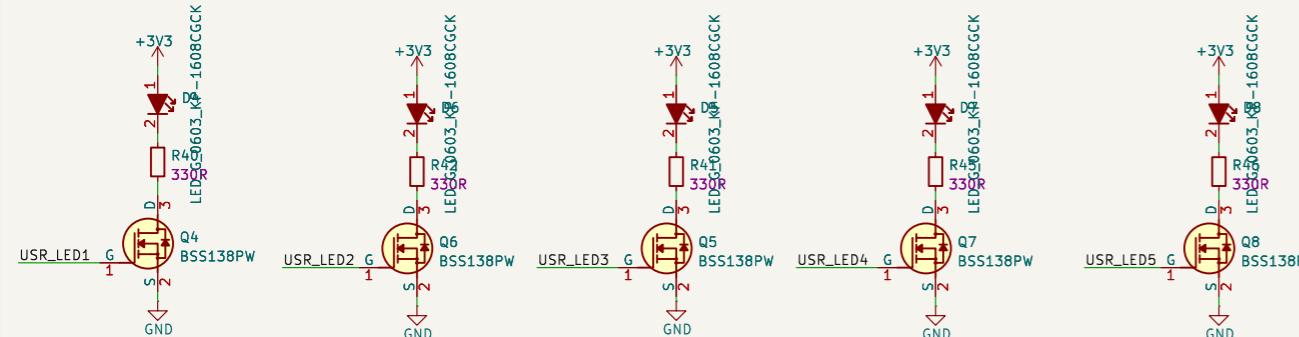
Size: A3 Date: 2024-09-26  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 2.0.0:1aec8  
Id: 14/17

# BANK 14



## User LEDs



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Sheet: /FPGA bank 14/  
File: fpga-bank-14.kicad\_sch

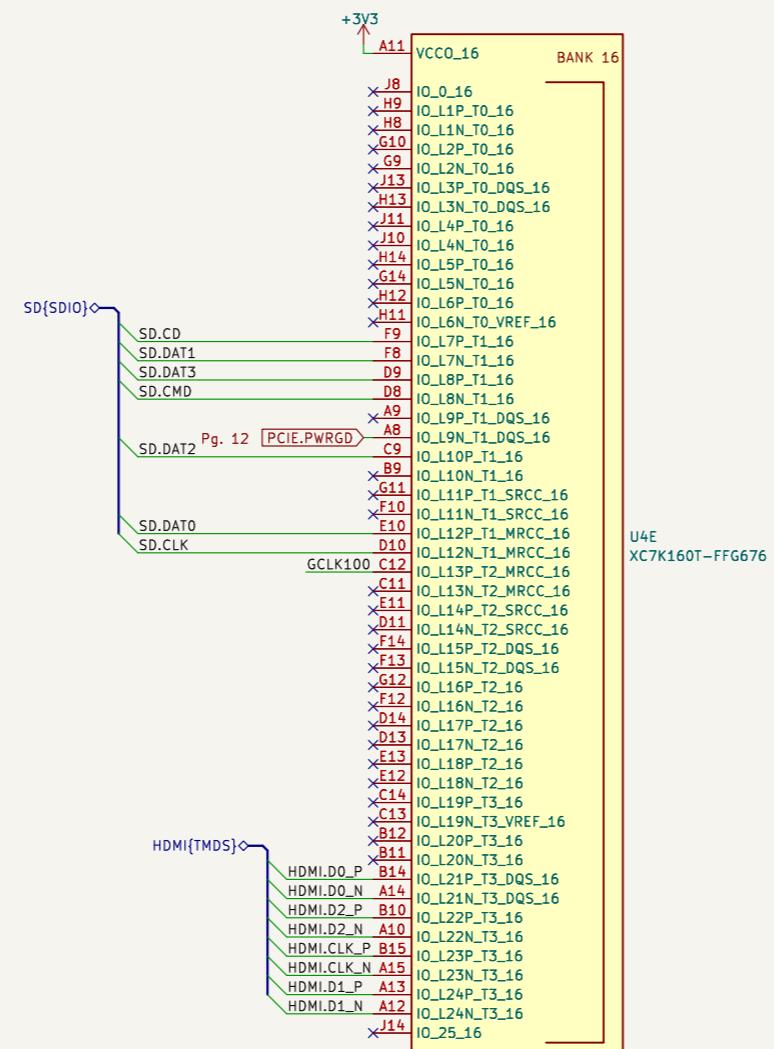
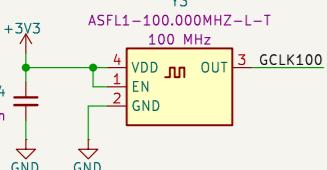
**Title: RDIMM DDR5 Tester**

Size: A3 | Date: 2024-09-26  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 2.0.0:1aec8  
Id: 15/17

**BANK 16**

VCCO (HR banks) max: 3.6V

**Clock source**

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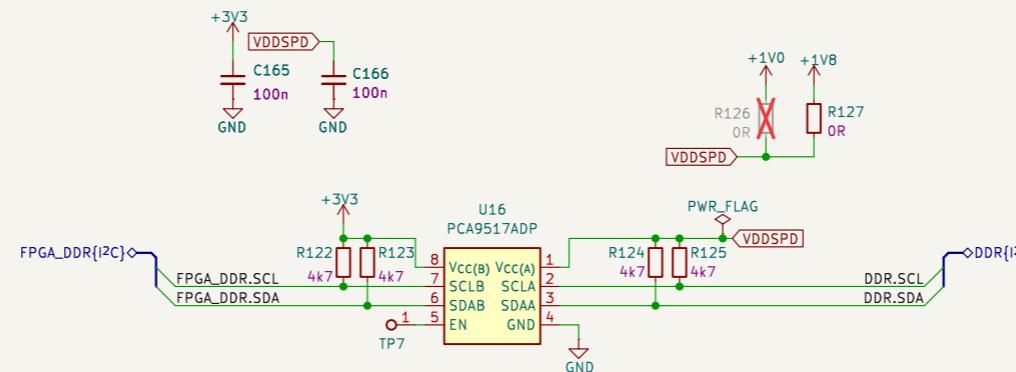
Sheet: /FPGA bank 16/  
File: fpga-bank-16.kicad\_sch

**Title: RDIMM DDR5 Tester**

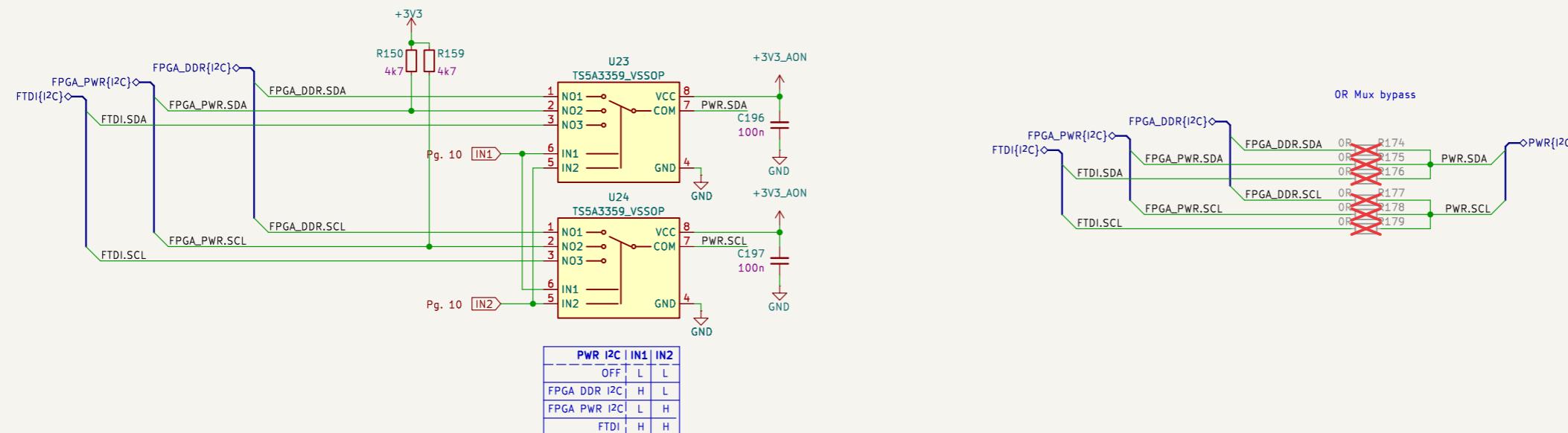
Size: A3 Date: 2024-09-26  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 2.0.0:1aec8  
Id: 16/17

## I2C logic translator



## PWR I2C MUX



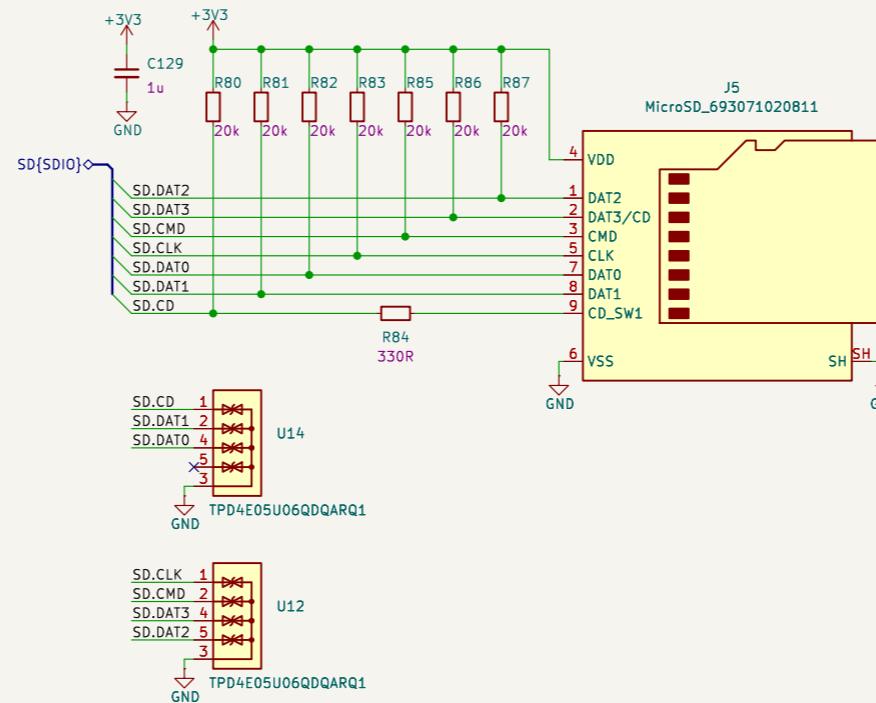
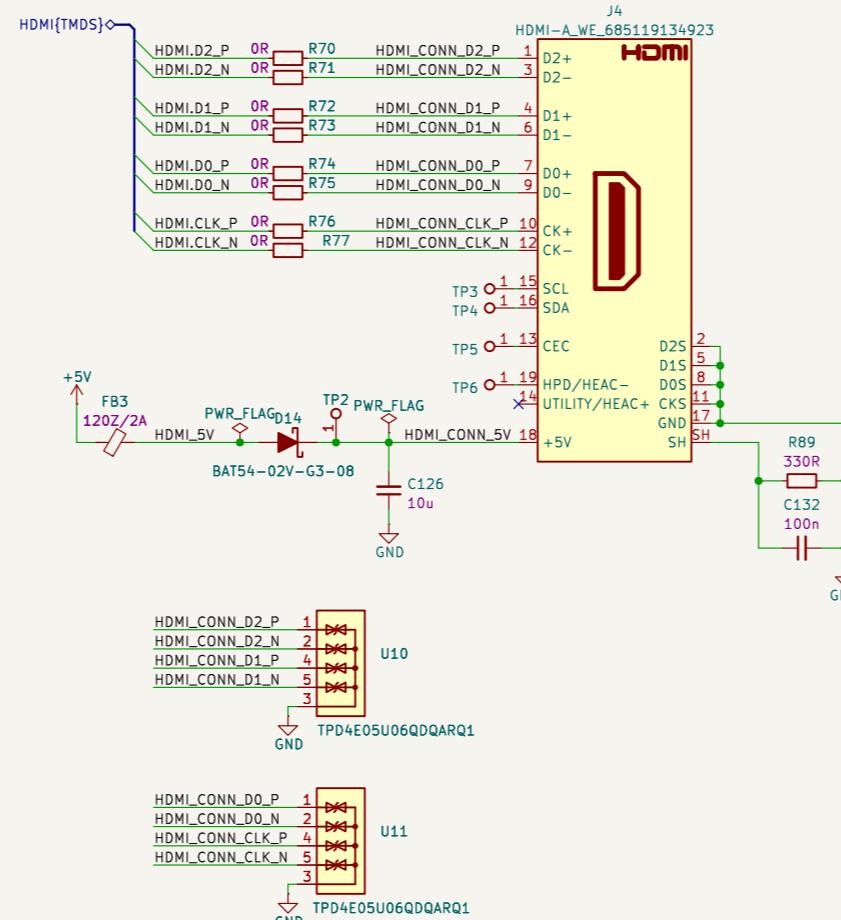
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Sheet: /I2C/  
File: i2c.kicad\_sch

**Title: RDIMM DDR5 Tester**

Size: A3 | Date: 2024-09-26  
KiCad E.D.A. kicad-cl 7.0.11

Rev: 2.0.0:1aec8  
Id: 17/17

**SD card****HDMI**

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Sheet: /HDMI + SD Card/  
File: hdmi-sd-card.kicad\_sch

**Title: RDIMM DDR5 Tester**

Size: A3 | Date: 2024-09-26  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 2.0.0:1aec8  
Id: 17/17