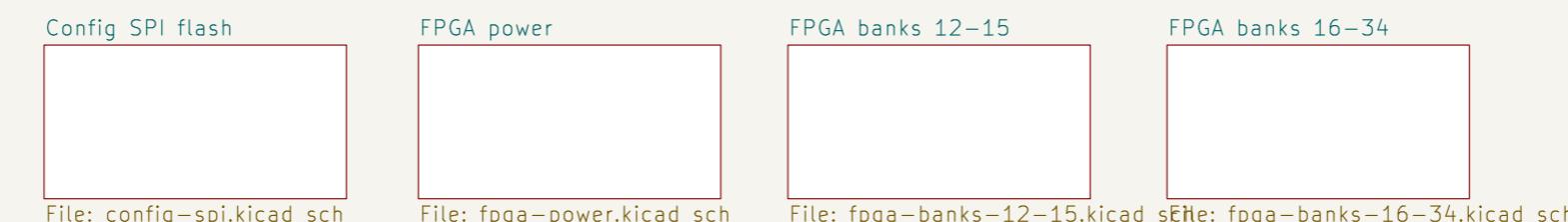
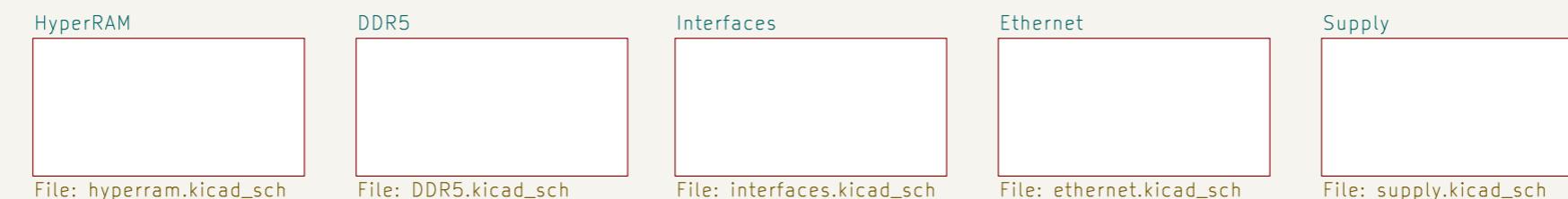


Data Center RDIMM DDR5 Tester

Logo N2
oshw_logoLogo N1
antmicro_logo

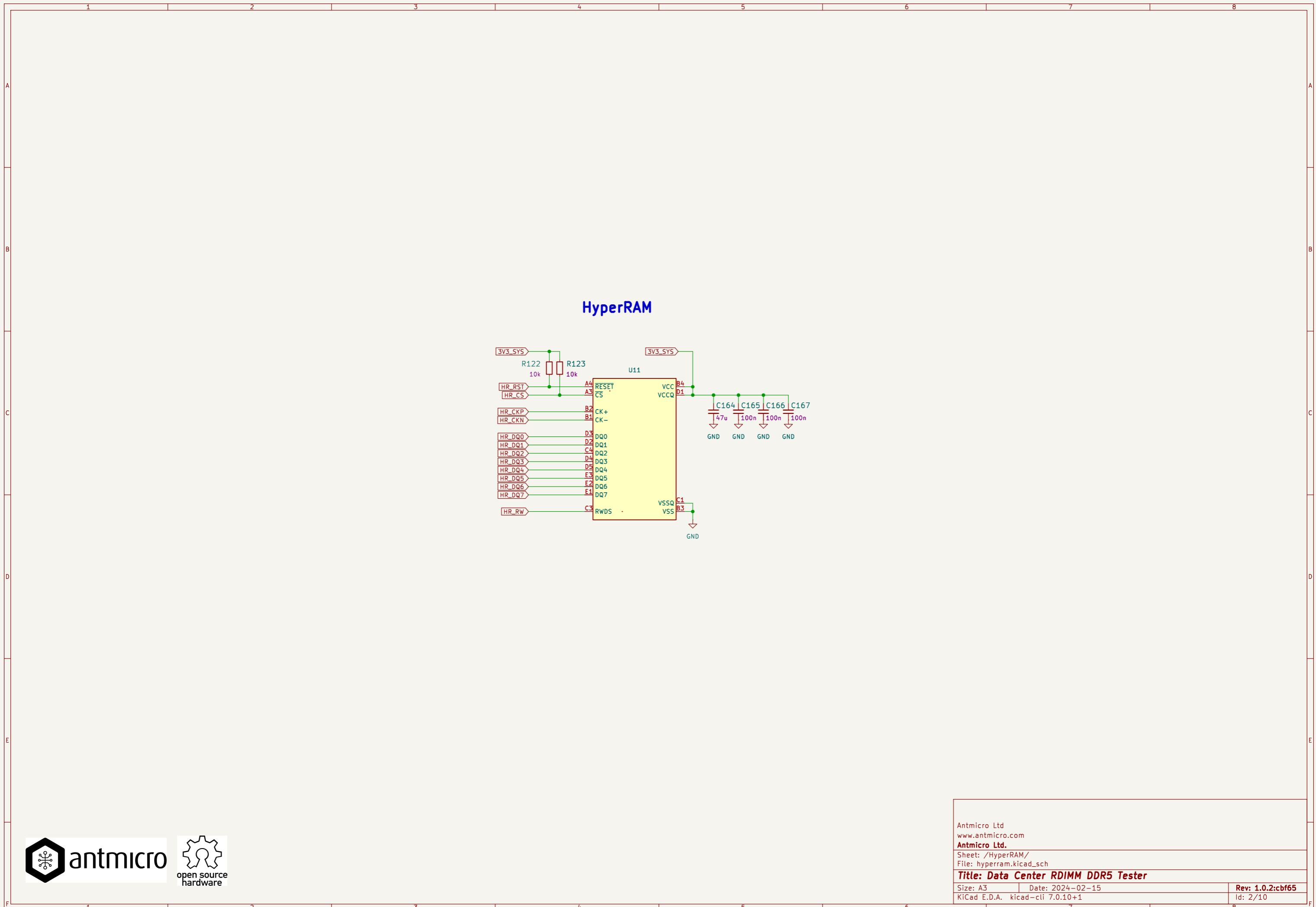
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Size: A3 | Date: 2024-02-15
KiCad E.D.A. kicad-cli 7.0.10+1

Rev: 1.0.2:cbf65
Id: 1/10

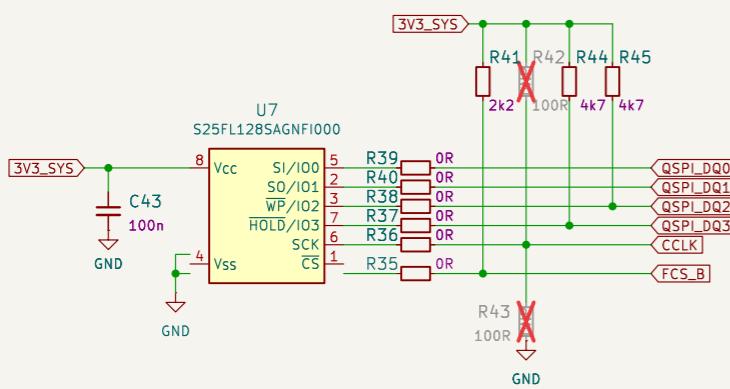


1 2 3 4 5 6 7 8

Master SPI Quad (x4) configuration scheme

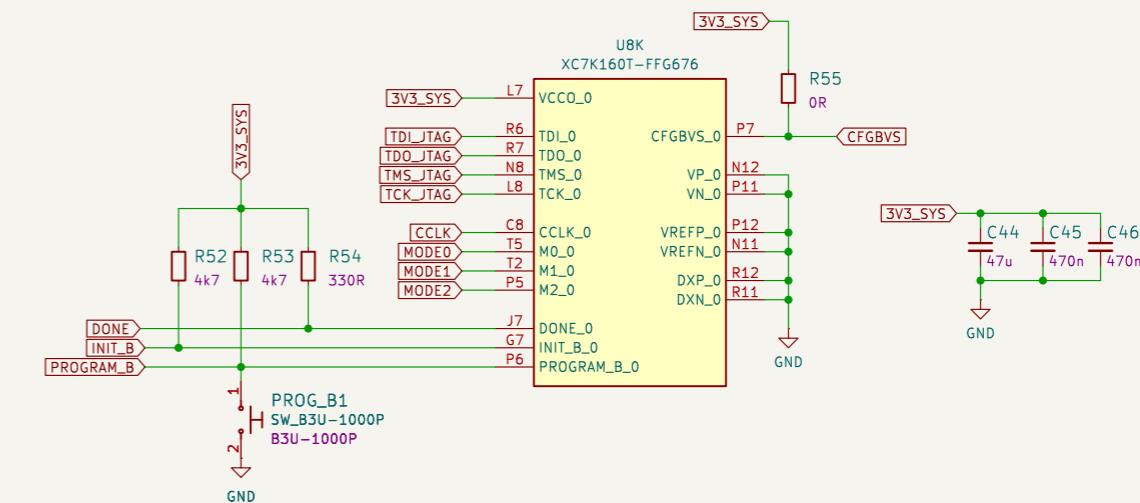
Follows Figure 2-14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)

(Q)SPI flash



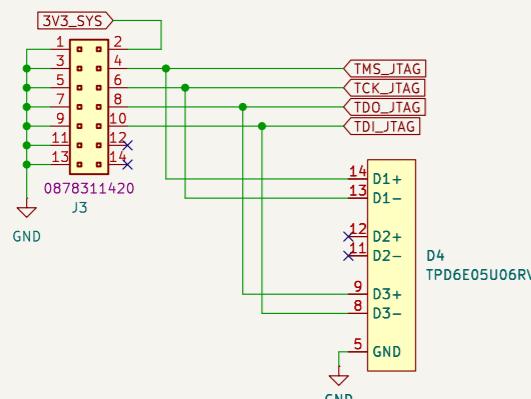
FPGA BANK 0

TODO: verify after FPGA swap

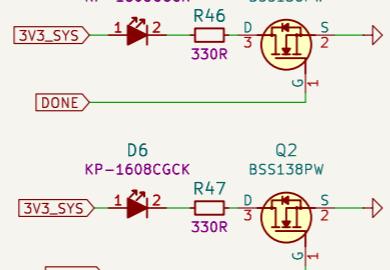


JTAG Connector

Compatible with Xilinx Platform Cable

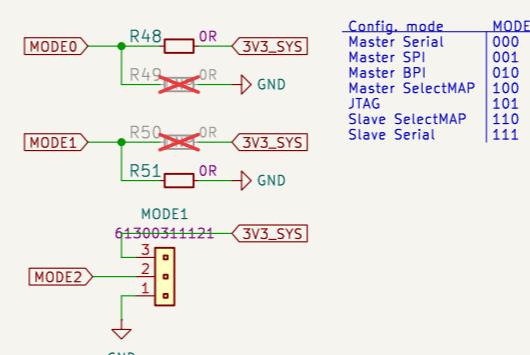


STATUS LEDs

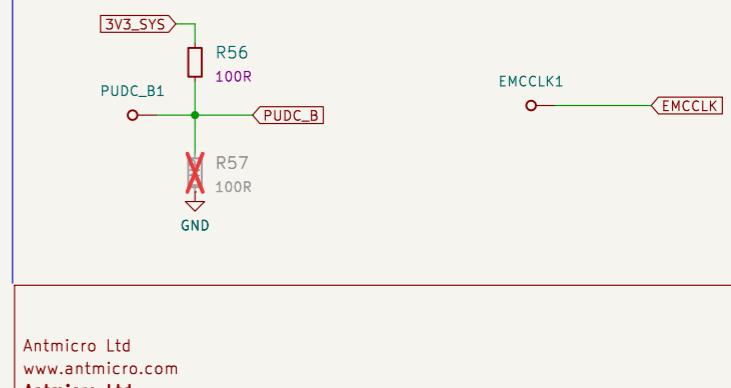


Configuration Modes

For details, see UG470 p. 21



Probes



A

A

B

B

C

C

D

D

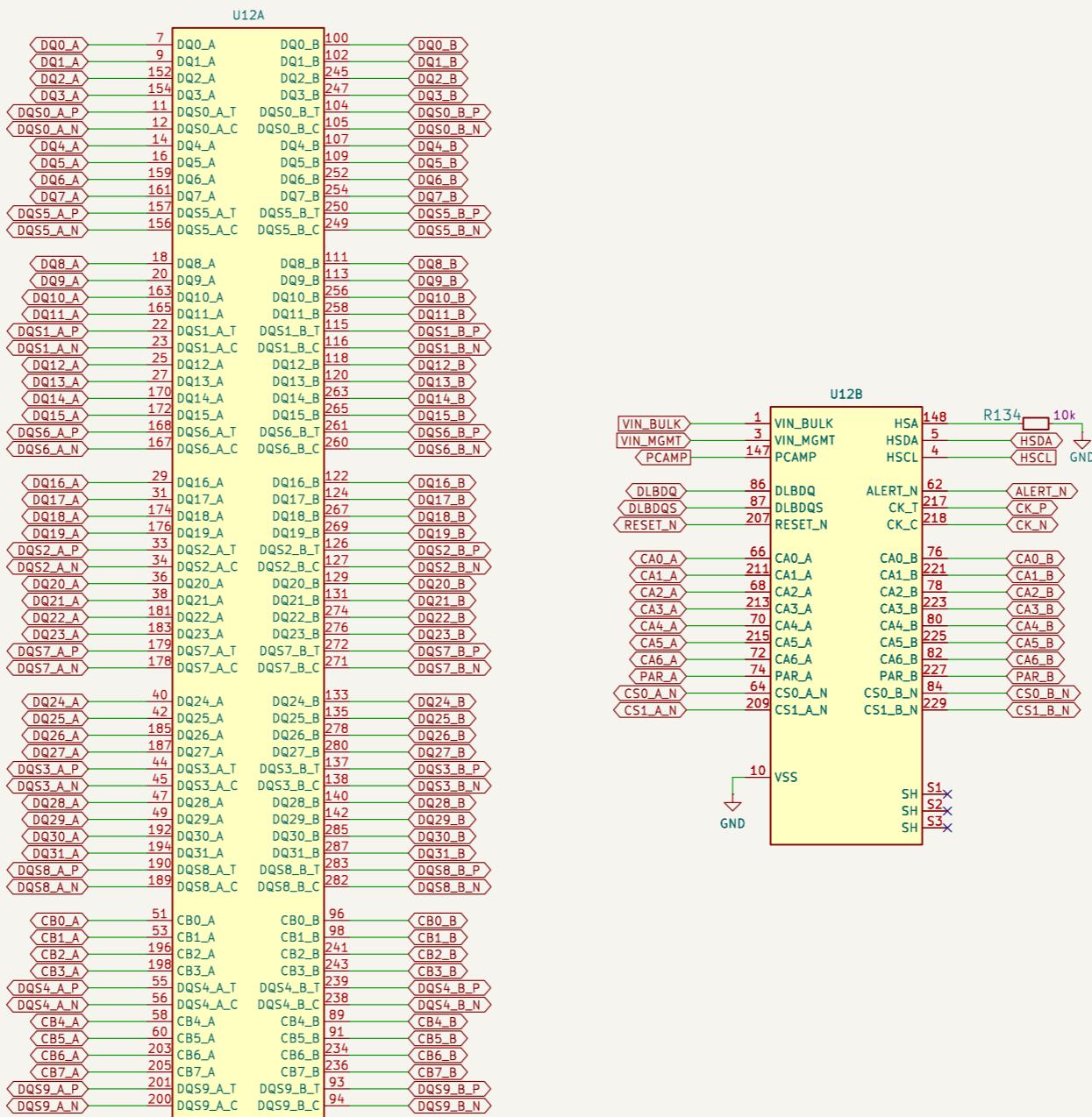
E

E

F

F

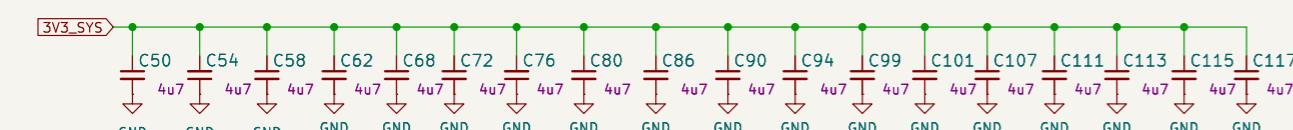
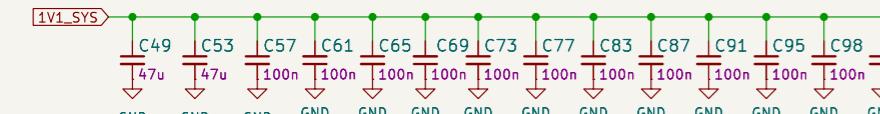
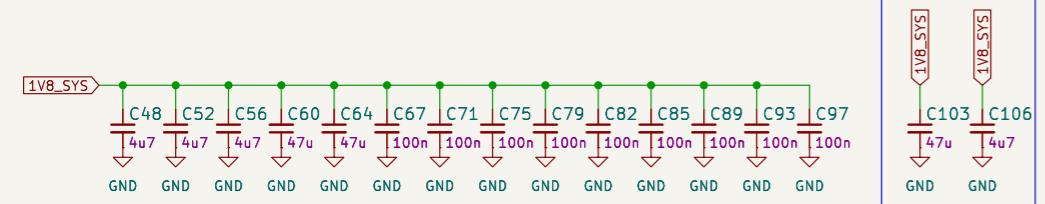
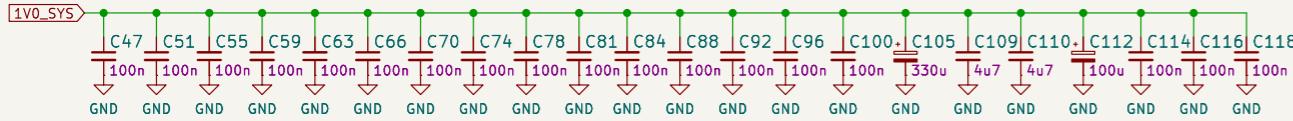
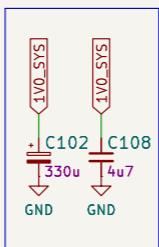
DDR5 RDIMM connector



1 2 3 4 5 6 7 8

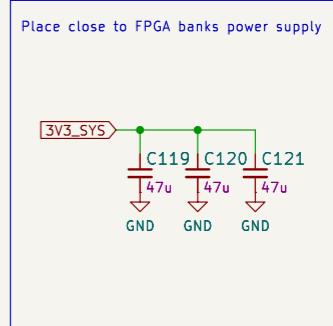
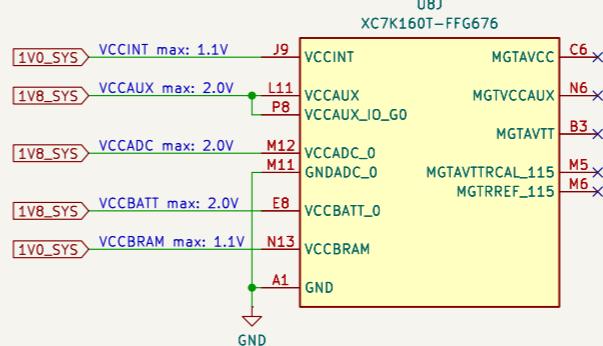
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Added capacitors corresponding to PCB Design Guide UG483

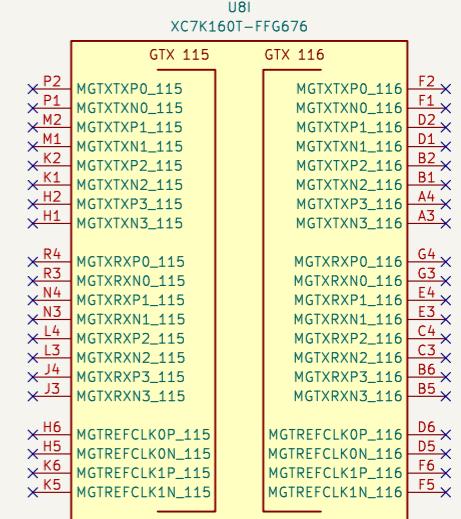


POWER RAILS

Decoupling referenced from 7 Series FPGAs
PCB Design Guide UG483
TODO: verify!



UNUSED



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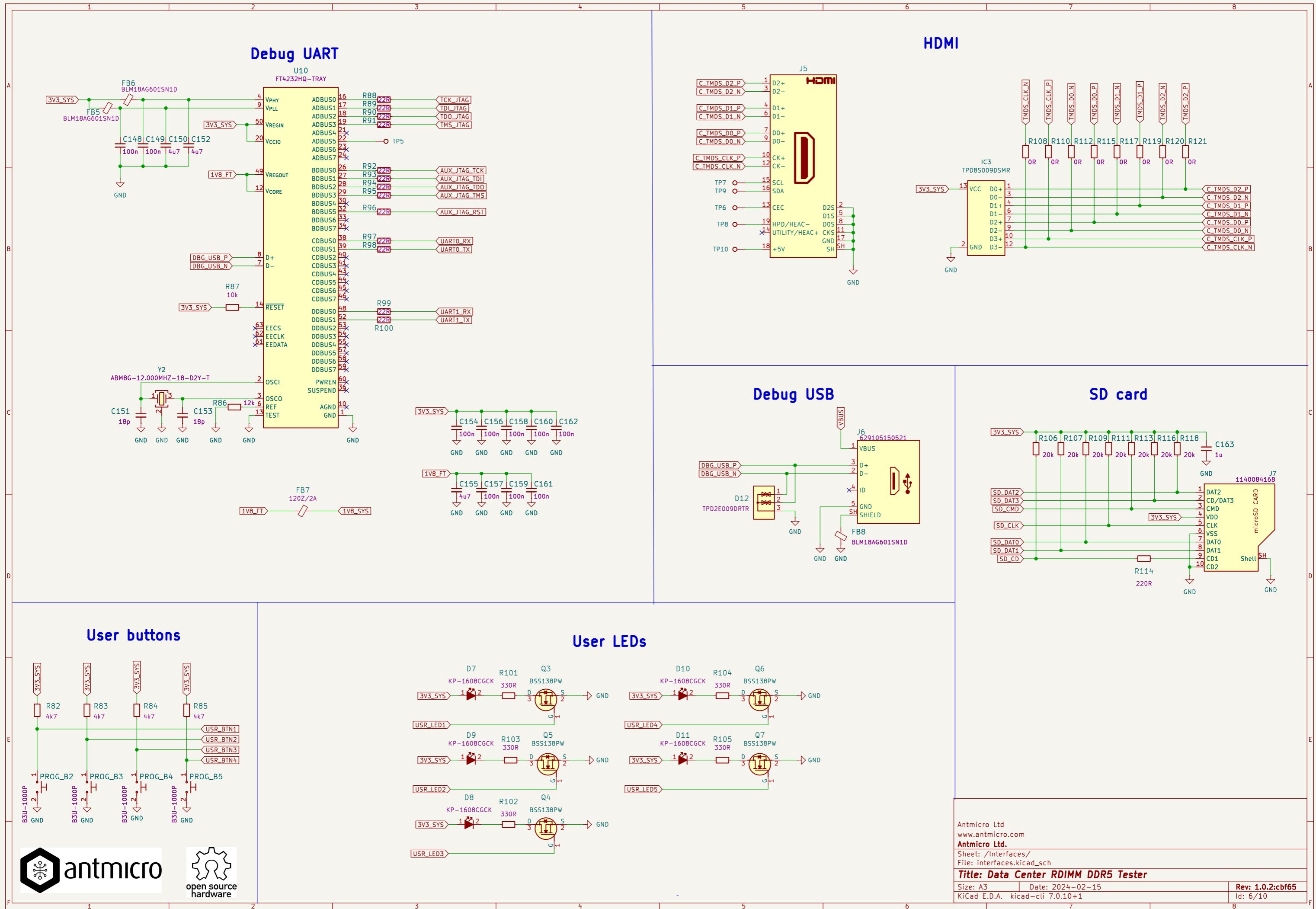
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Size: A3 | Date: 2024-02-15
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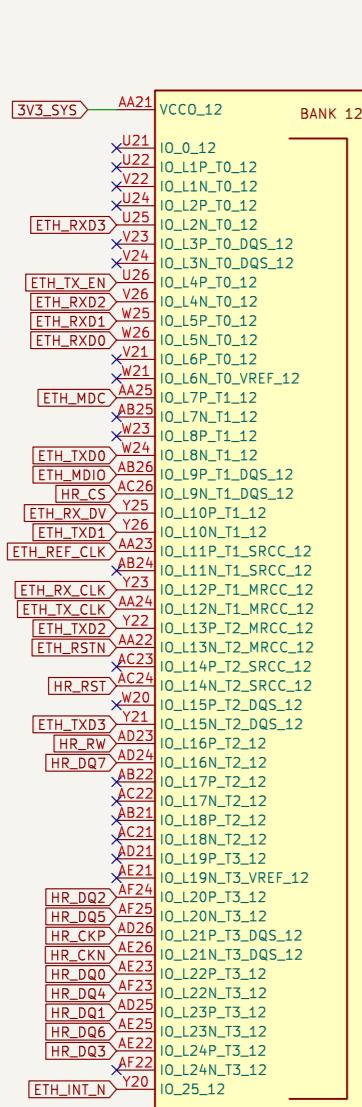
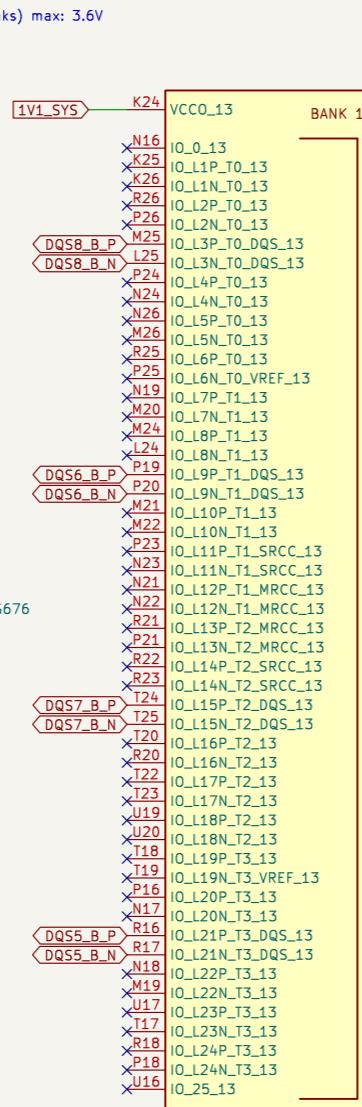
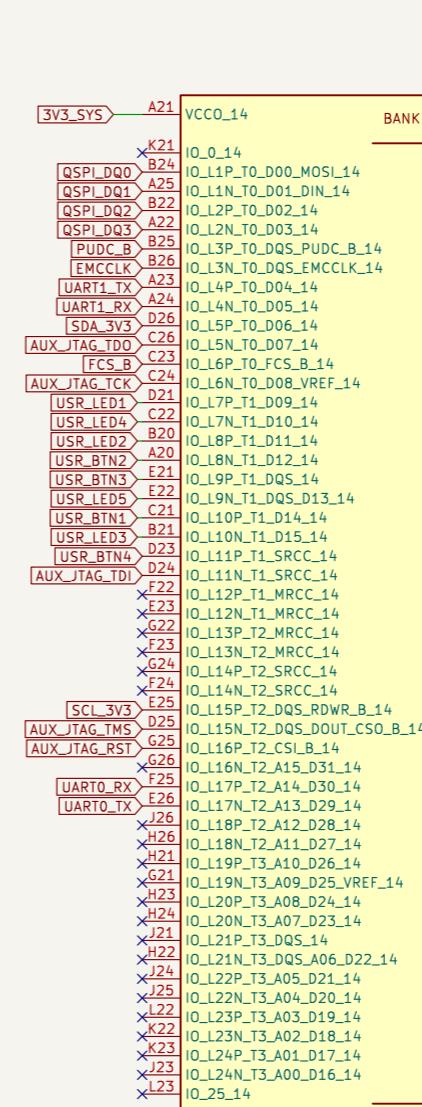
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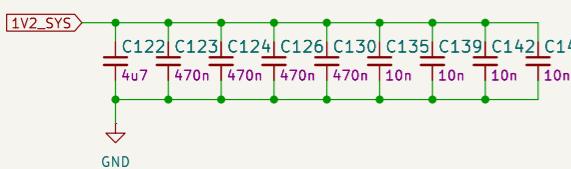
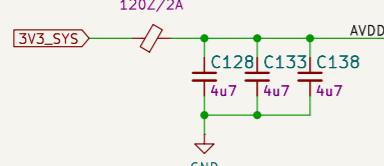
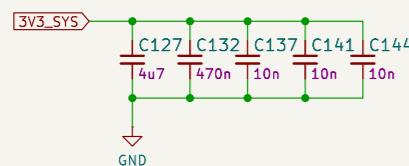
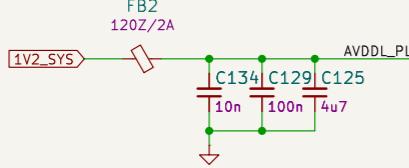
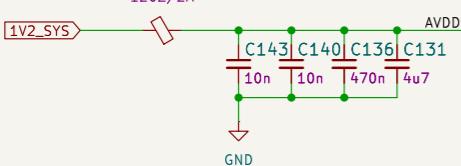
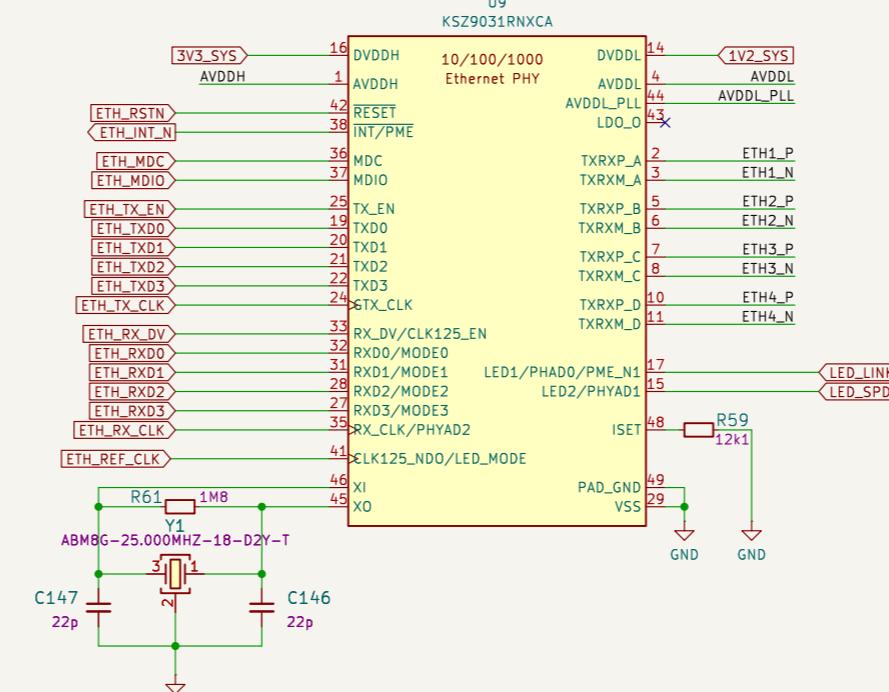
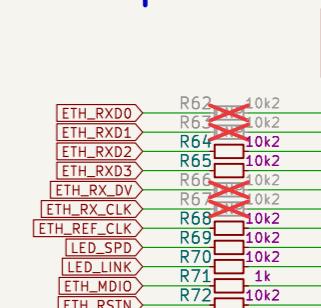
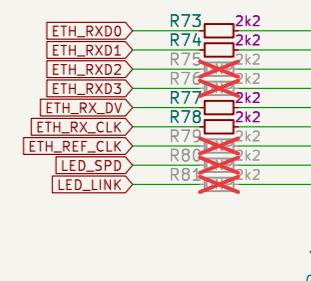


A

A

BANK 12**BANK 13****BANK 14**

1 2 3 4 5 6 7 8

DVDDL decoupling**AVDDH decoupling****DVDDH decoupling****AVDDL_PLL decoupling****AVDDL decoupling****PHY****Pull up resistors****Pull down resistors****RJ45 Connector**