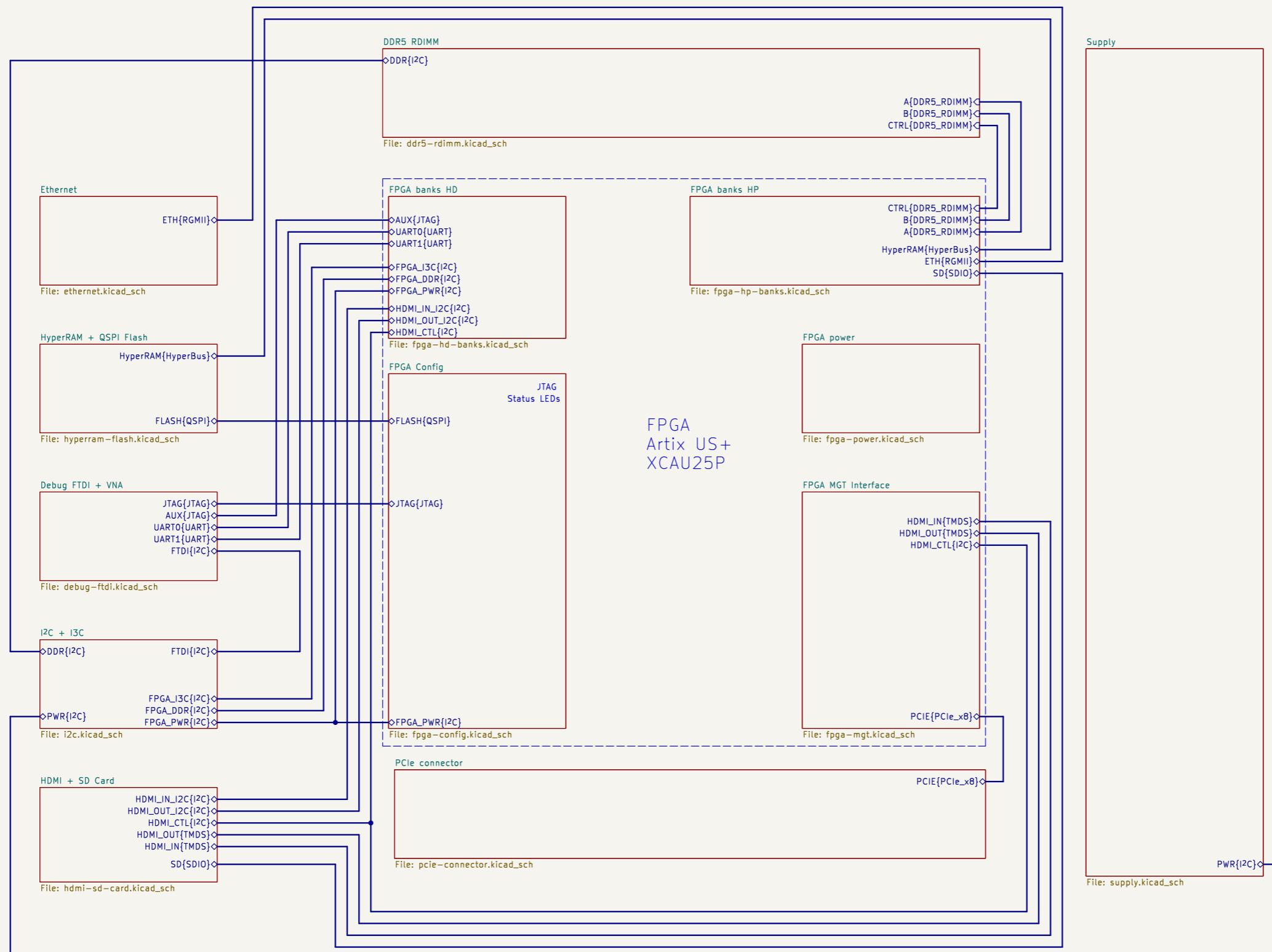
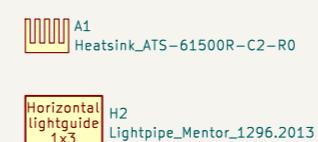


# RDIMM DDR5 Tester



## Mechanical



Antmicro  
www.antmicro.com

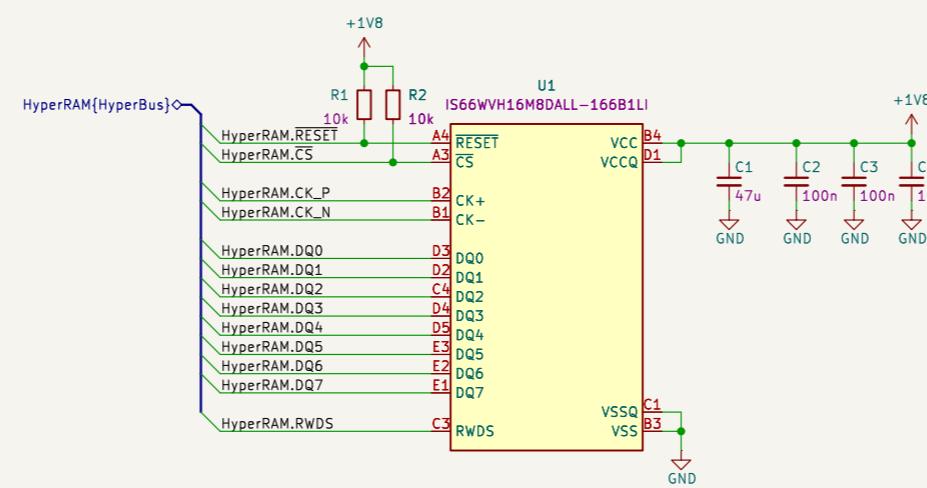
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File: data-center-rdimm-ddr5-tester.kicad\_sch

**Title: RDIMM DDR5 Tester**

Size: A3 Date: 2024-12-20  
KiCad E.D.A. 8.0.5

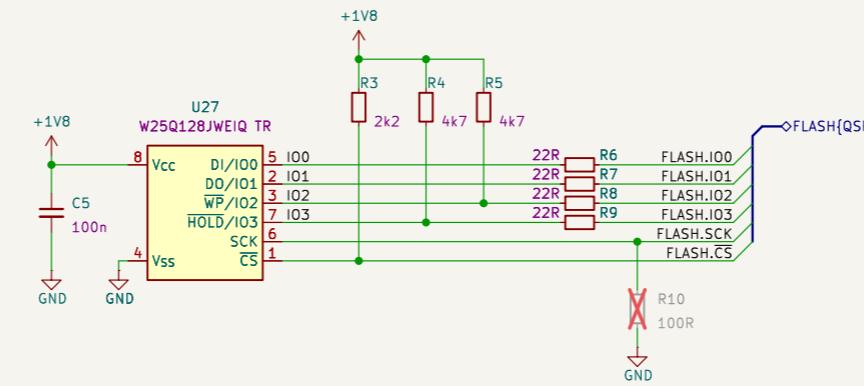
Rev: 2.1.0:1f2bc  
Id: 1/17

# HyperRAM

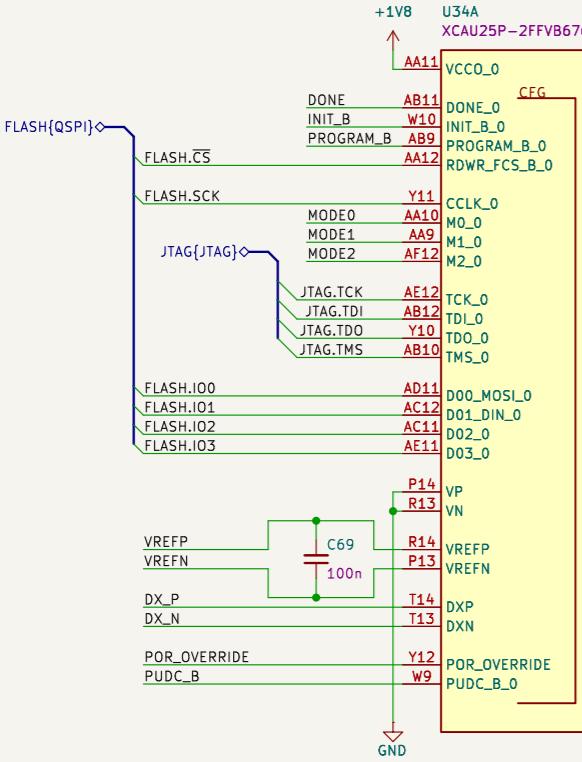


# (Q)SPI flash

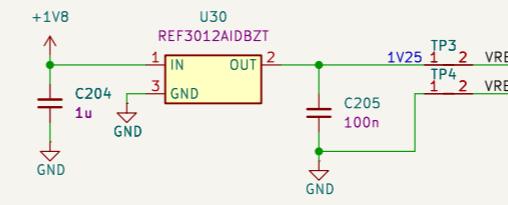
Master SPI Quad (x4) configuration scheme  
Follows FPGAs Configuration User Guide UG570



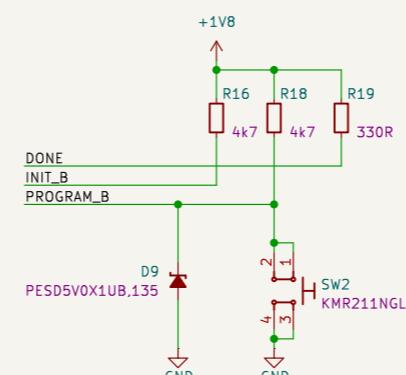
## FPGA BANK 0



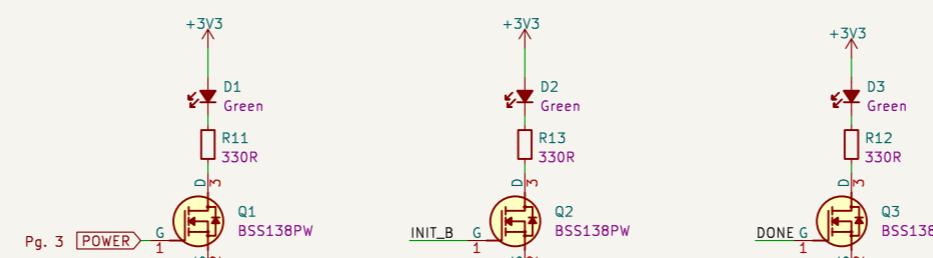
## LDO



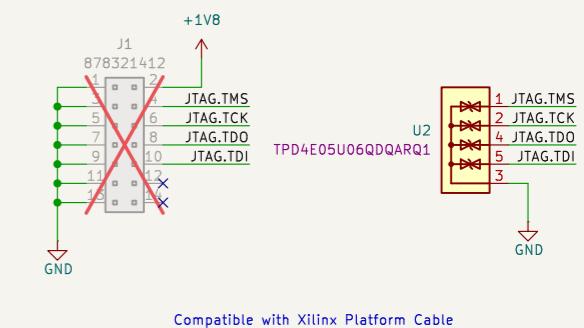
## Pull-ups



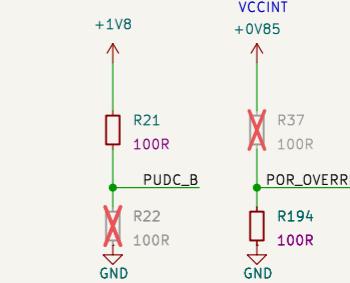
## STATUS LEDs



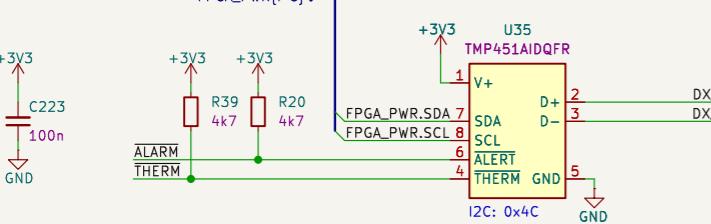
## JTAG Connector



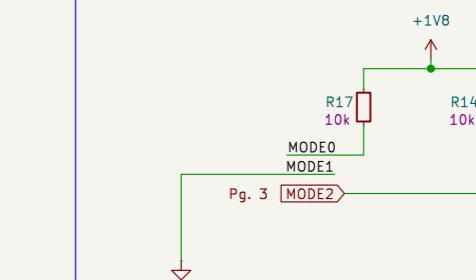
## Probes



## Temp sensor



## Configuration Modes

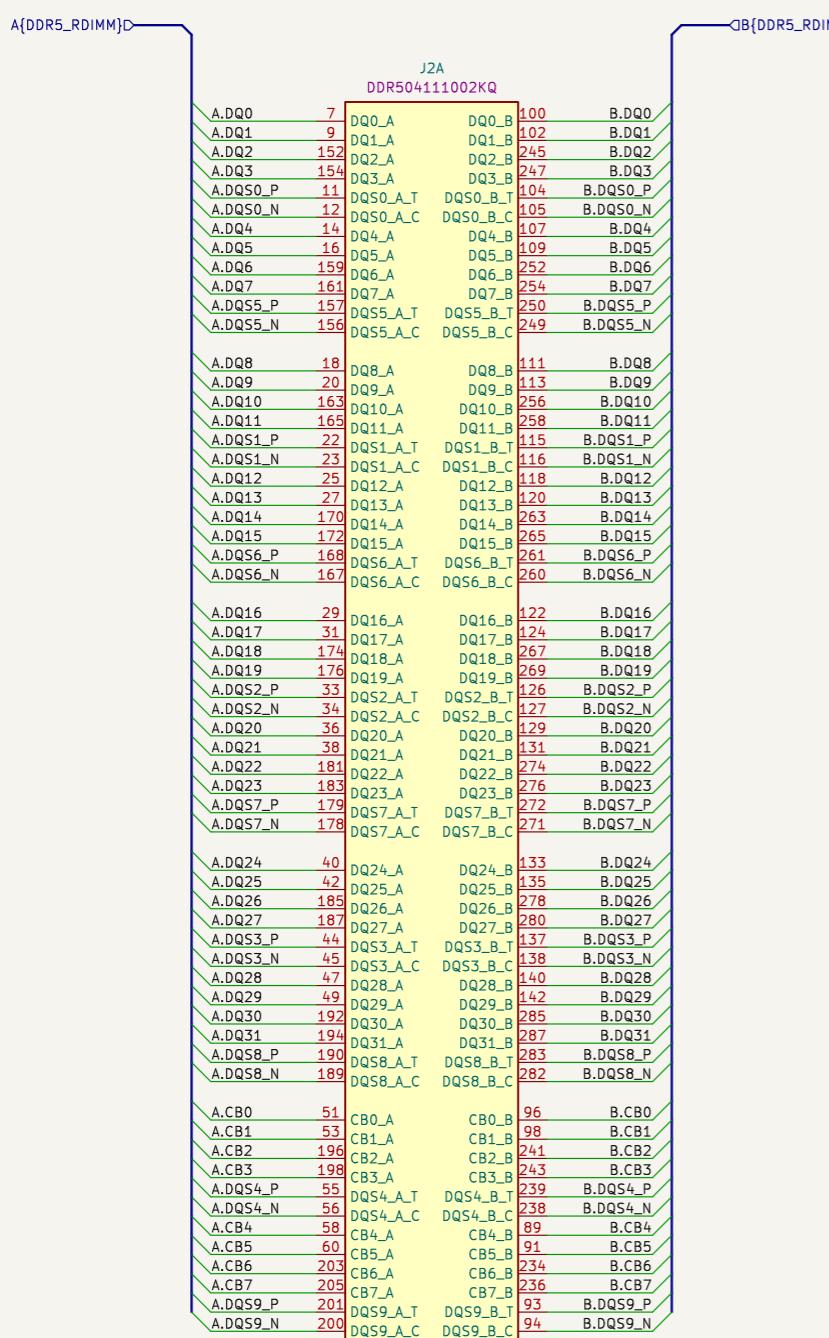


Config. mode	MODE[2:0]
Master Serial	000
Master SPI	001
Master BPI	010
Master SelectMAP	100
JTAG	101
Slave SelectMAP	110
Slave Serial	111

For details, see UG570

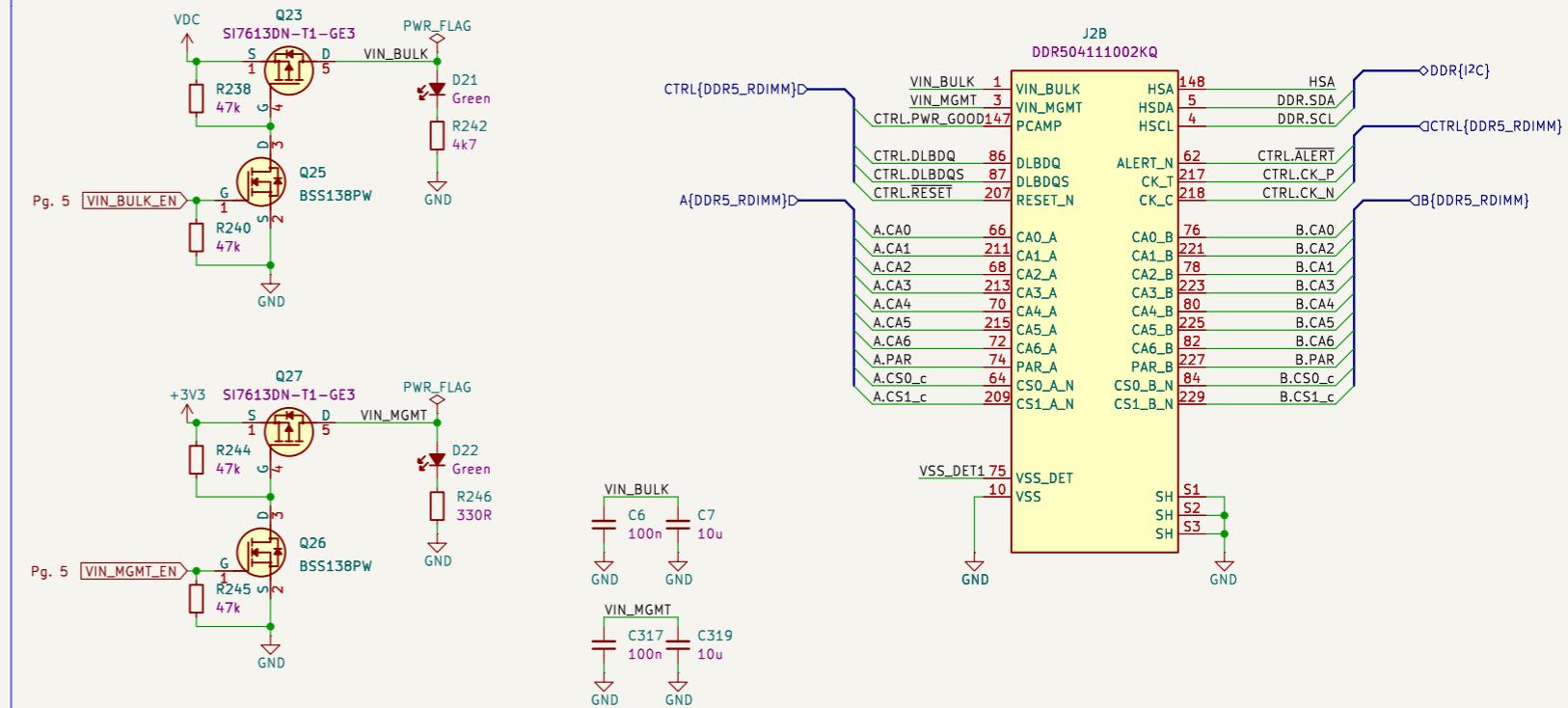
# DDR5 RDIMM connector

Subchannel A

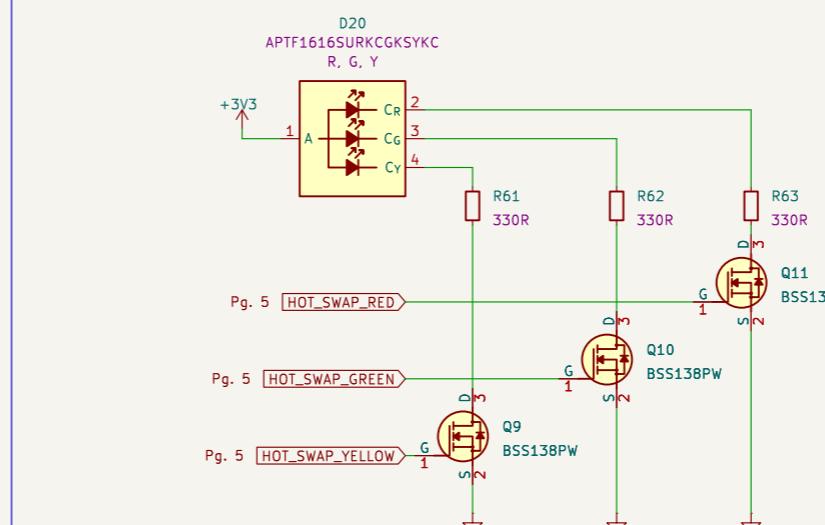


Subchannel B

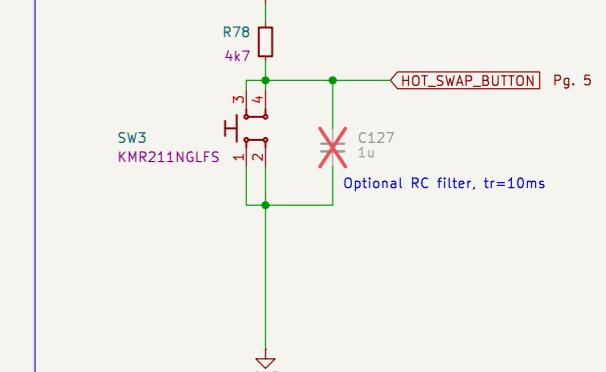
## Power, address command and control



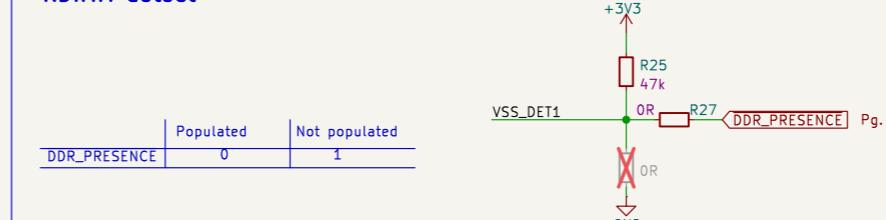
## HOT SWAP status LED



## HOT SWAP eject button



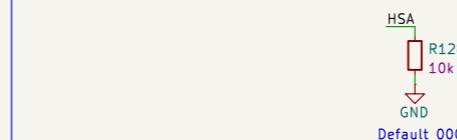
## RDIMM detect



## Plane decoupling



## Serial adress select



Antmicro

[www.antmicro.com](http://www.antmicro.com)

Antmicro Ltd.

Sheet: /DDR5 RDIMM/

File: ddr5-rdimm.kicad\_sch

Title: RDIMM DDR5 Tester

Size: A3 Date: 2024-12-20

KiCad E.D.A. 8.0.5

Rev: 2.1.0:1f2bc

Id: 4/17

1

2

3

4

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6

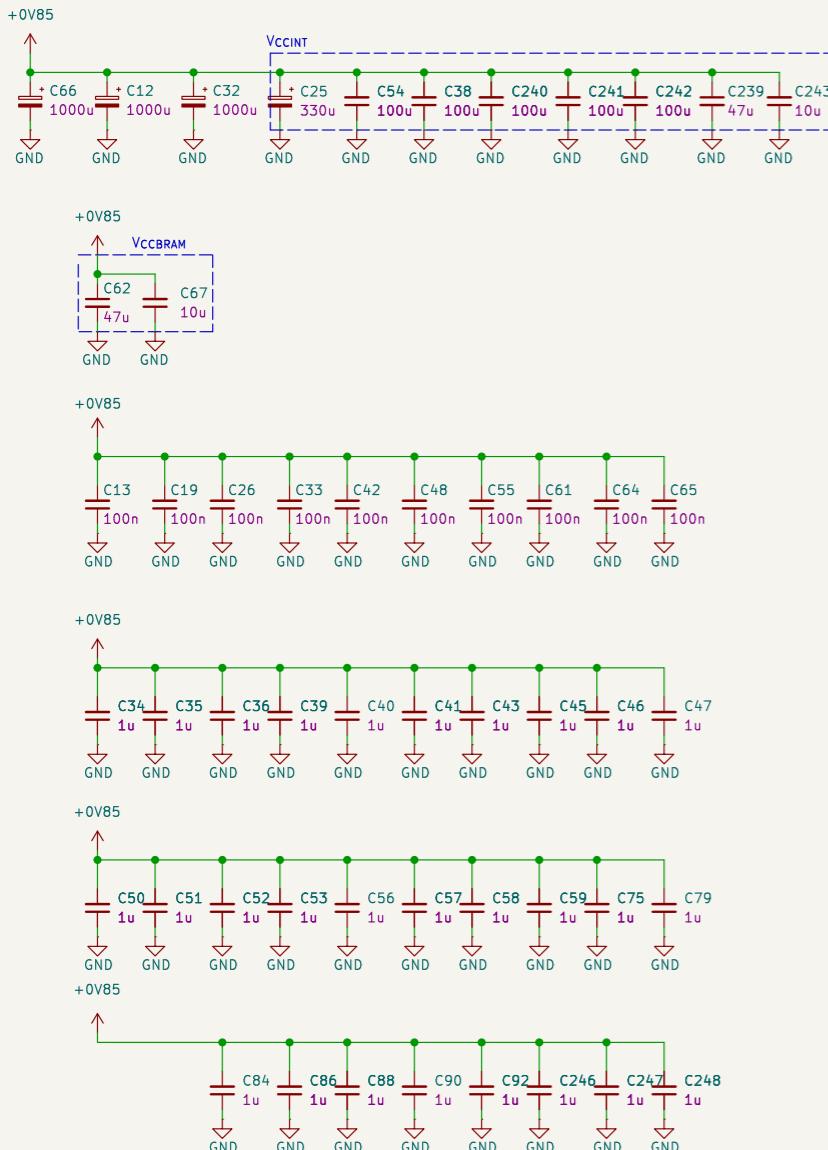
7

8

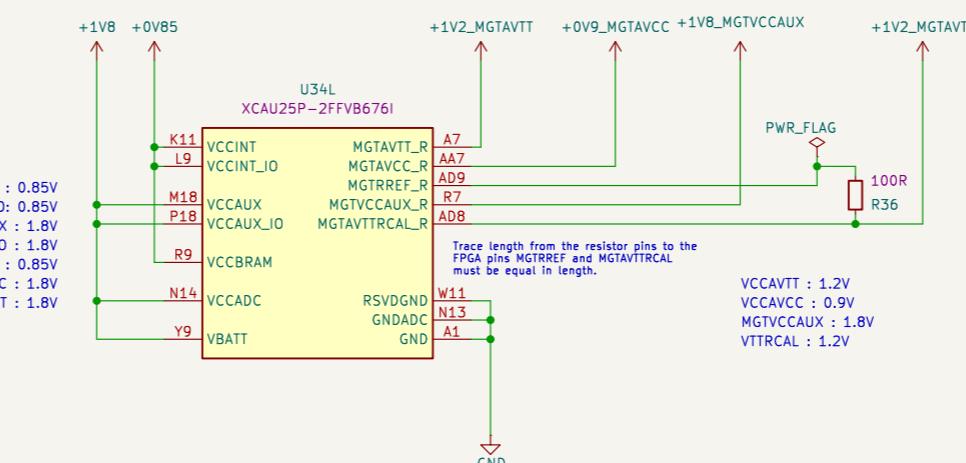
## FPGA Power rails

Bank marked by dashed line  
referenced from US+ Series FPGAs  
PCB Design Guide UG583  
(AUP25P+ XCKU5P FFVB Package worst case)  
MGT decoupling marked by dashed line  
referenced from US+ Series FPGAs  
PCB Design Guide UG576  
(AUP25P+ XCKU5P FFVB Package worst case)

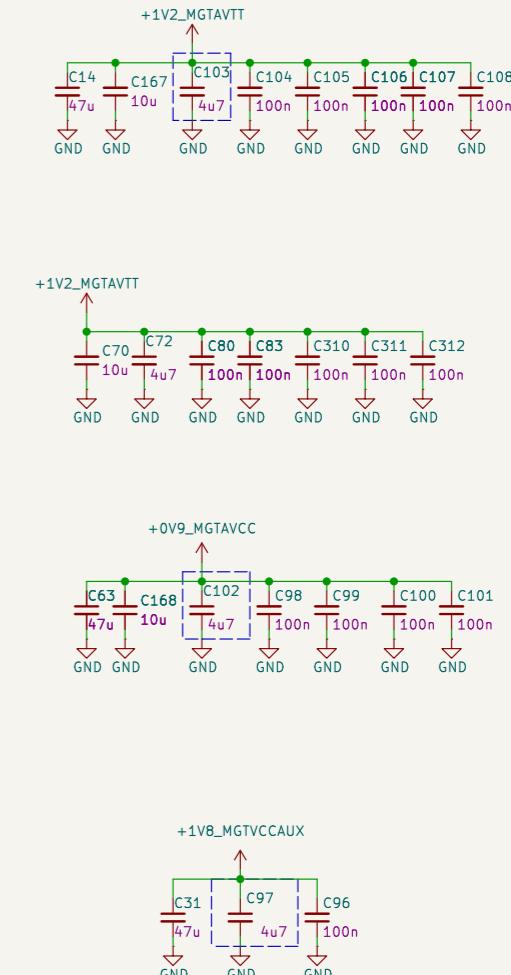
### VCCINT decoupling



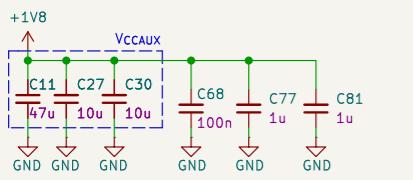
## FPGA



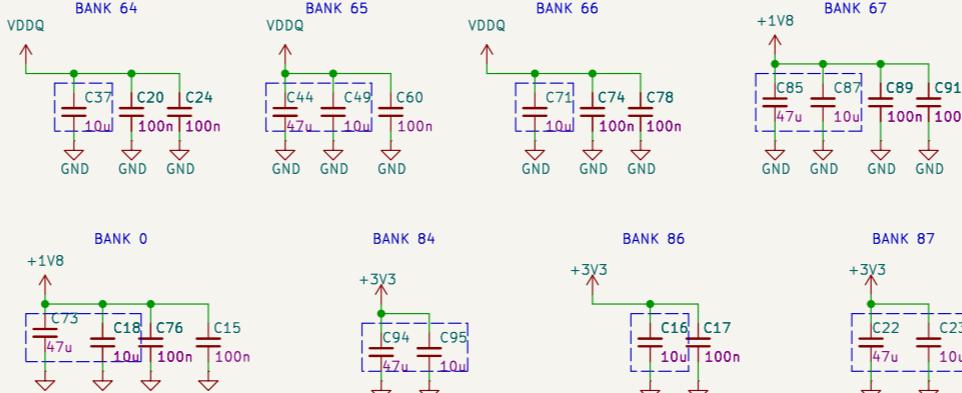
### MGT decoupling



### VCCINT decoupling

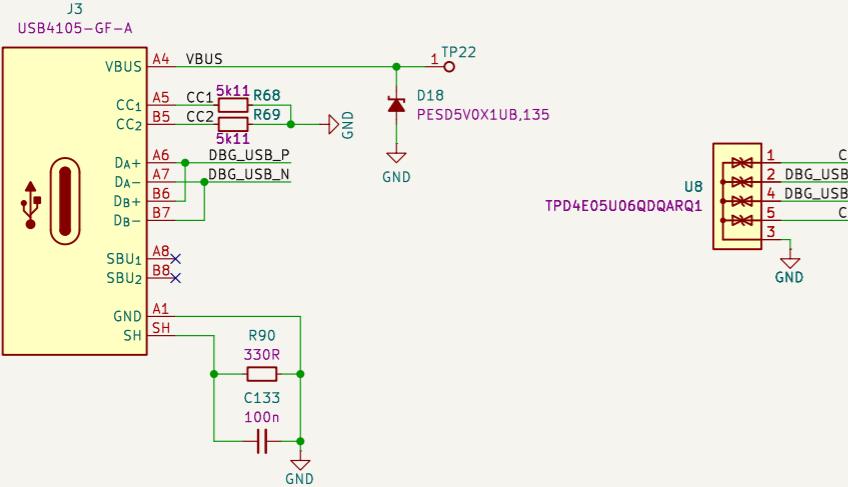


### Bank decoupling

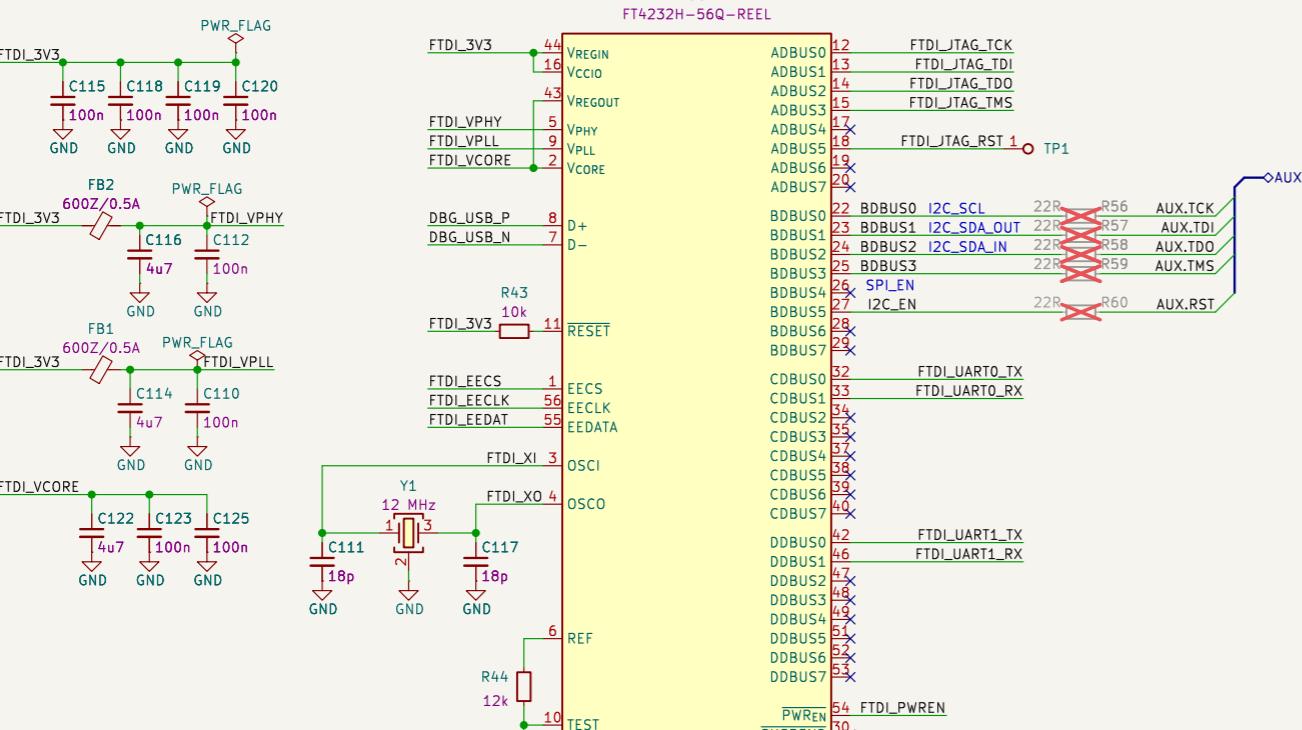


## Debug FTDI

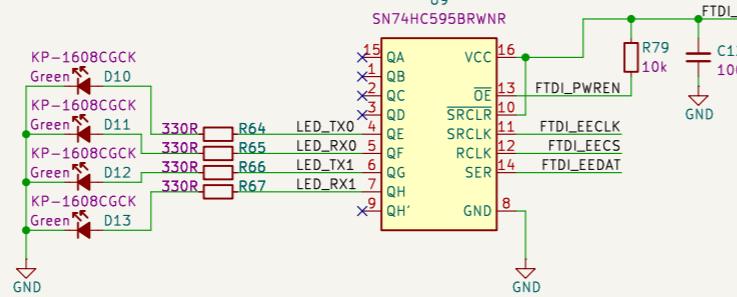
USB-C



## FTDI

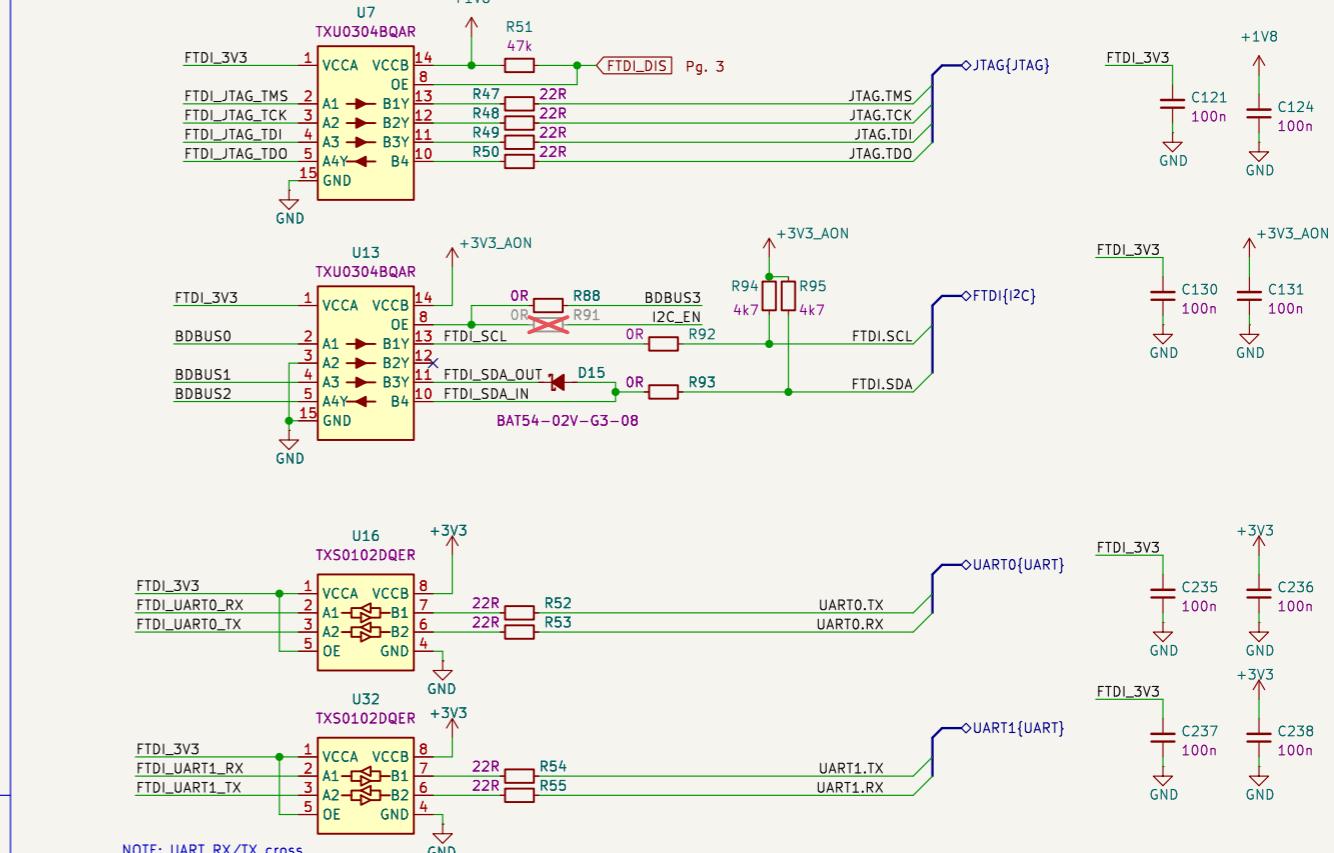


## Shift register

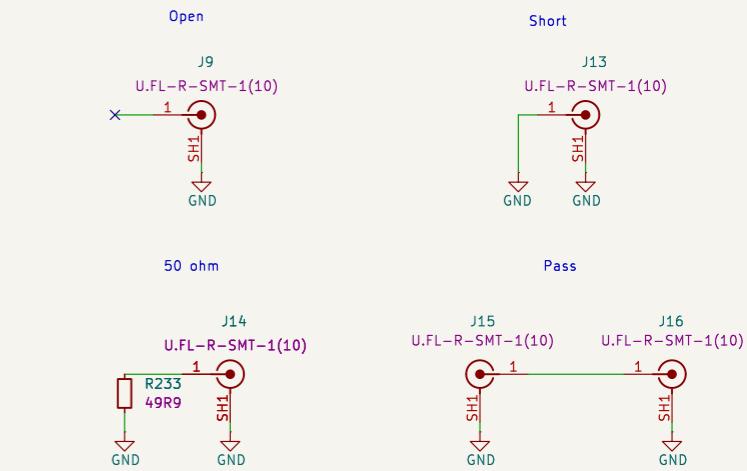


## FTDI

## Logic level translators

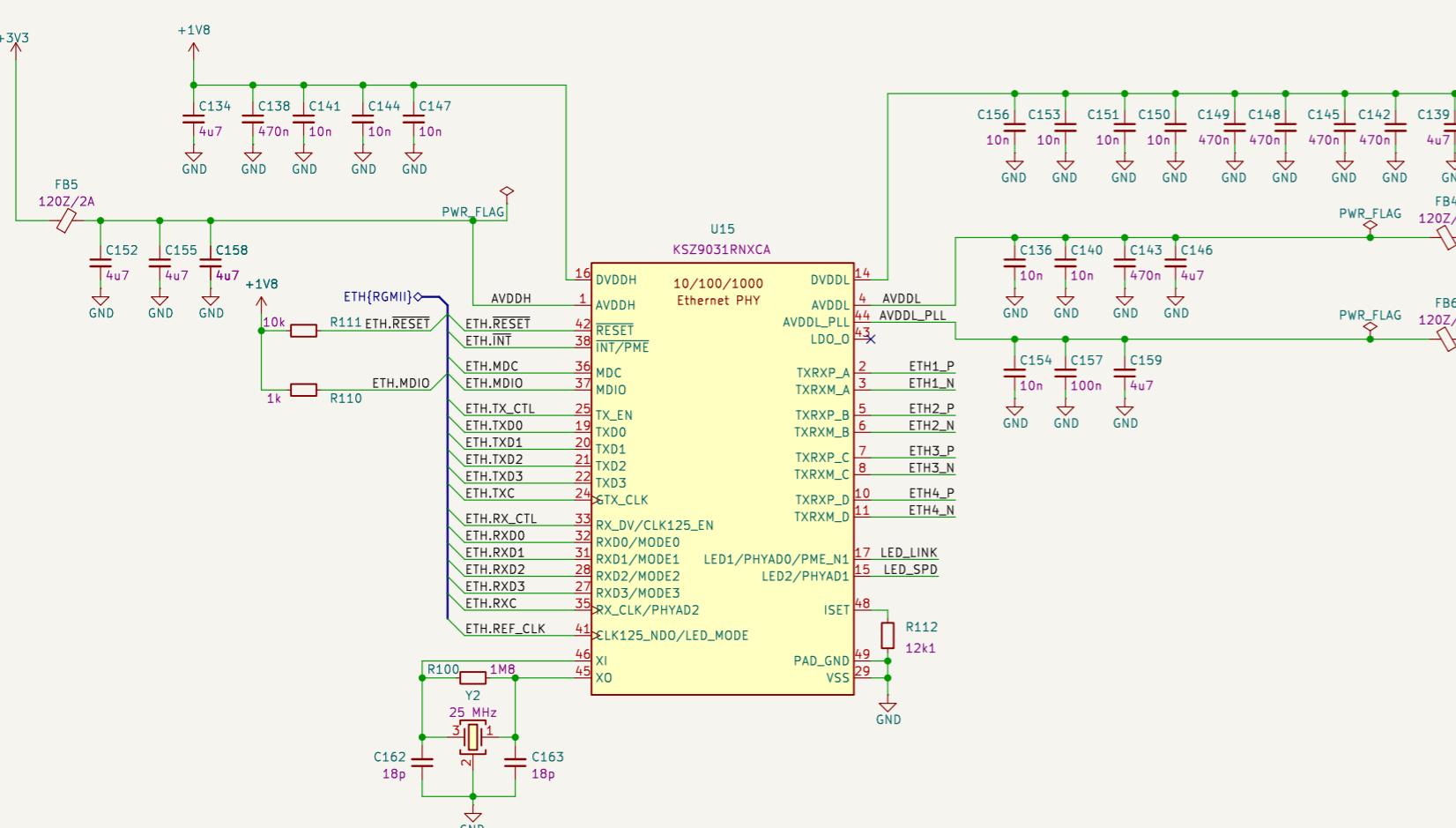


## VNA calibration

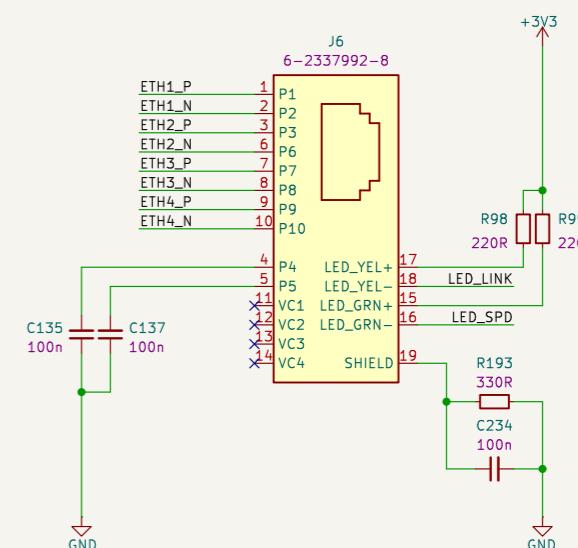


# Gigabit Ethernet

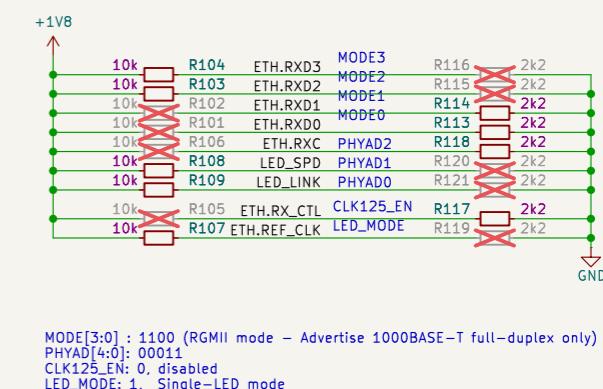
Ethernet PHY



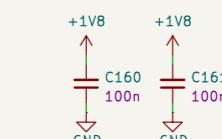
# RJ45 connector



# Bootstrap configuration

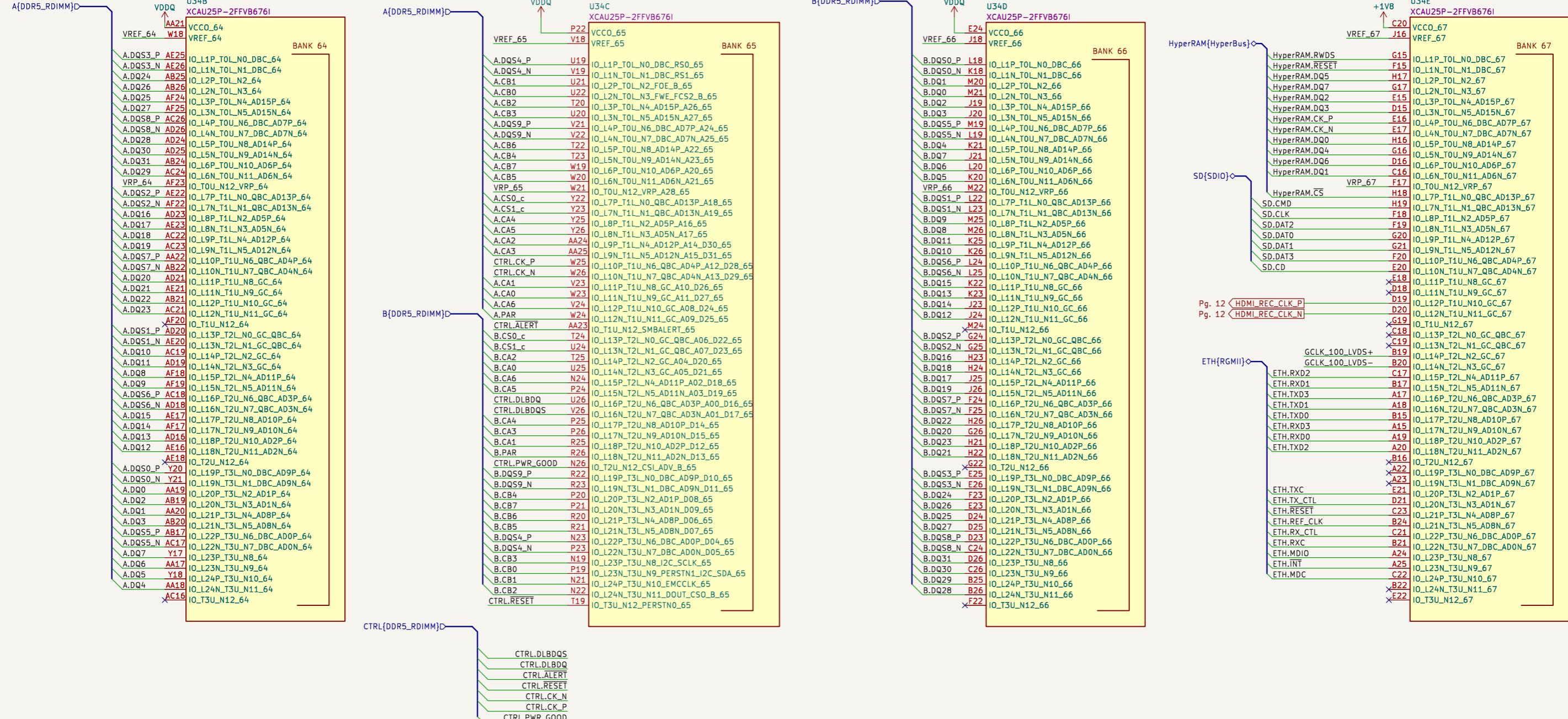


# Reference plane decoupling

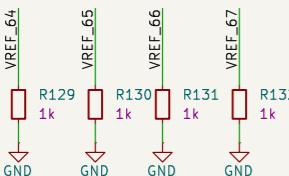


# HP Banks

VCCO (HP banks) max: 1.9V

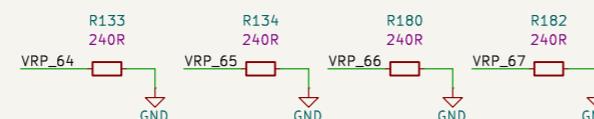


VREF

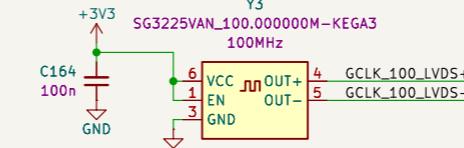


The logo consists of a stylized gear icon above the text "open source hardware".

## Reference termination



## Clock source



Antmicro  
[www.antmicro.com](http://www.antmicro.com)

Sheet: /FPGA banks HP/  
File: fpga-hp-banks.kicad\_sch

## Title: RDIMM DDR5 Tester

Size: A3 Date: 2024-12-20

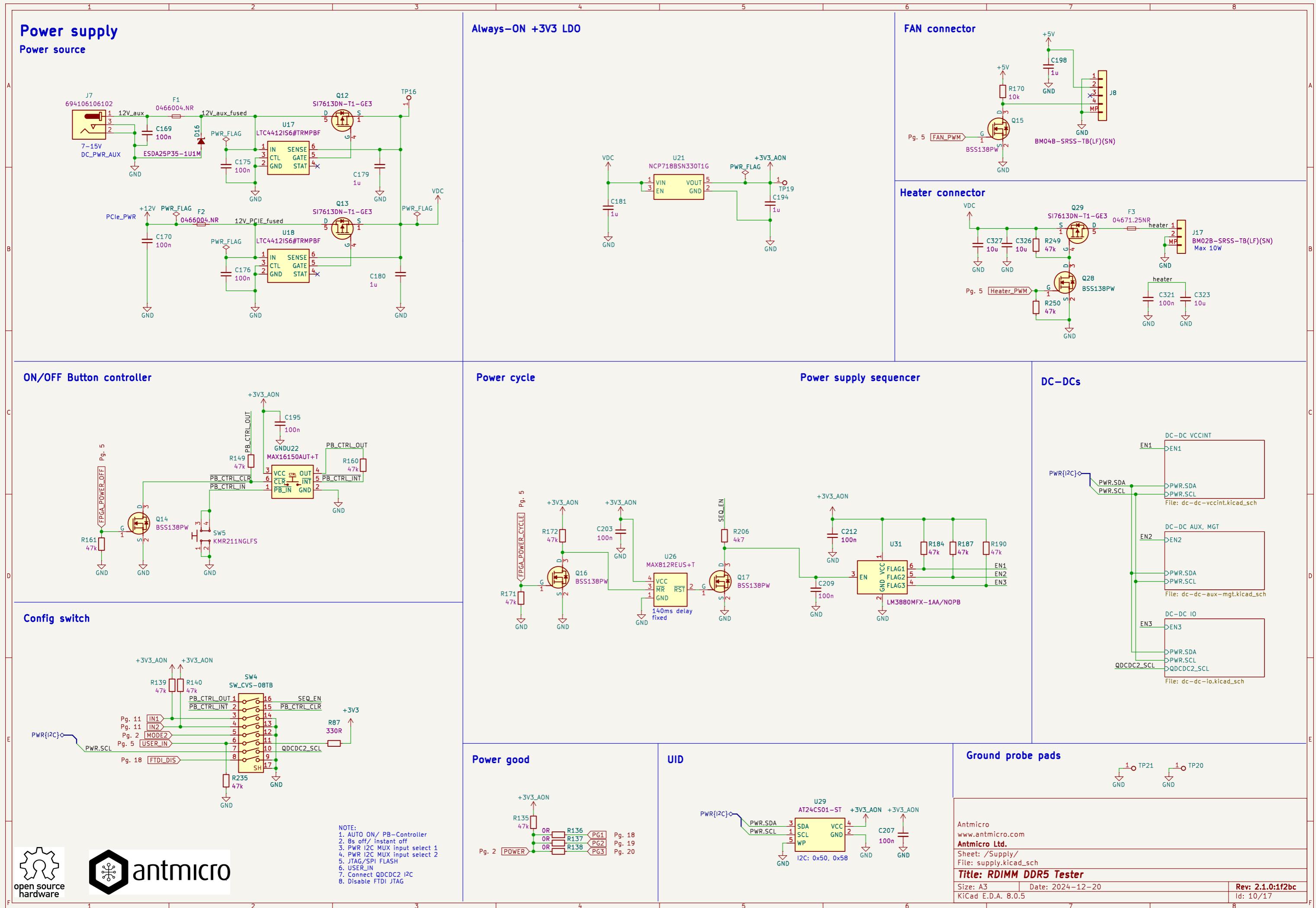
KiCad E.D.A. 8.0.5

7

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Digitized by srujanika@gmail.com

## Pinout 1.1.1



**MGT Interface**

PCIe 3.0 x8

A

U34I  
XCAU25P-2FFVB676I

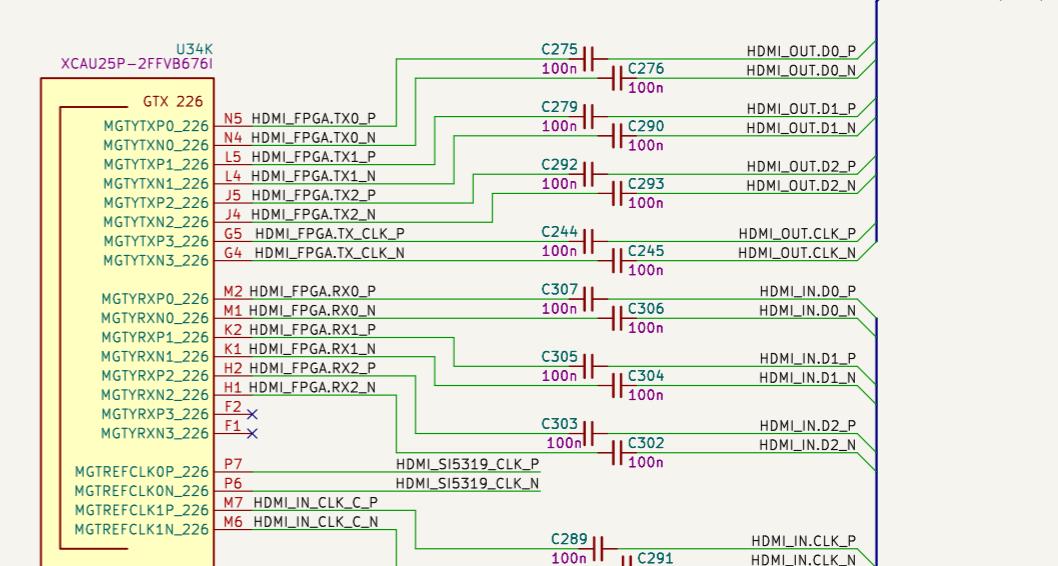
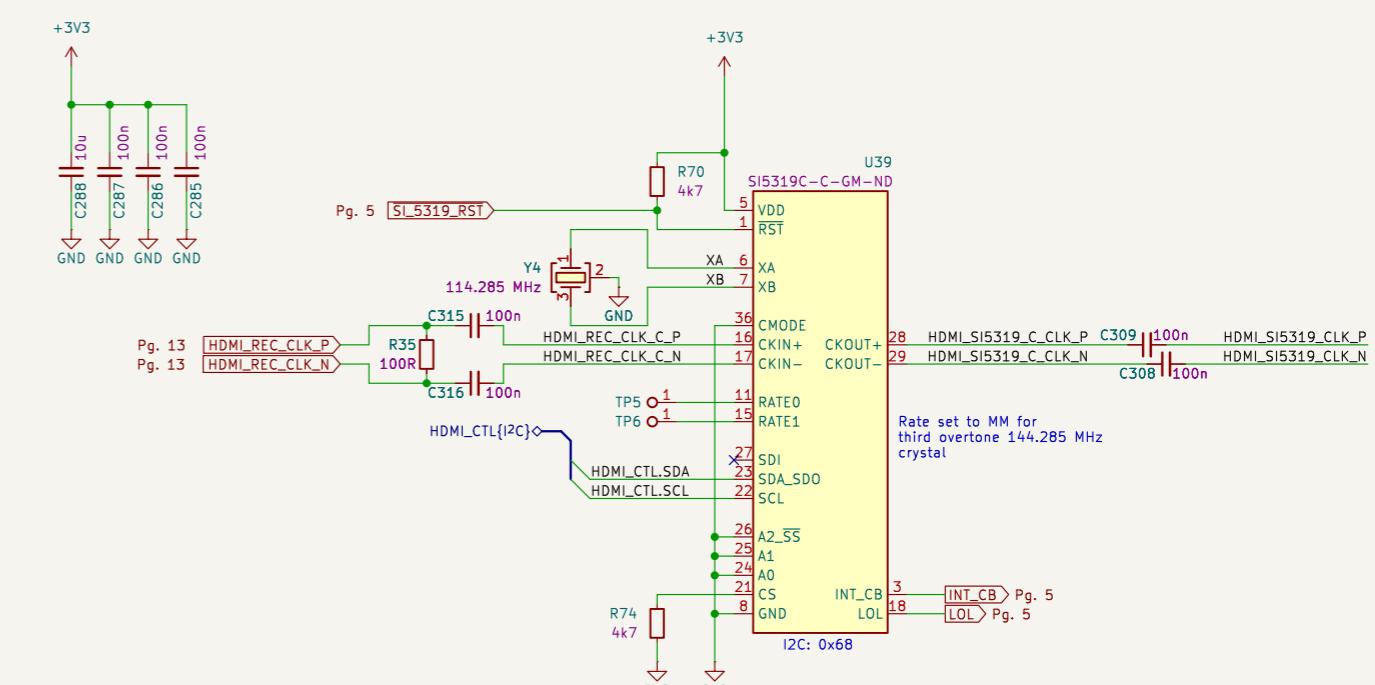
GTX 224  
 MGTYTXP0\_224  
 MGTYTXN0\_224  
 MGTYTXP1\_224  
 MGTYTXN1\_224  
 MGTYTXP2\_224  
 MGTYTXN2\_224  
 MGTYTXP3\_224  
 MGTYTXN3\_224  
 MGTYRXP0\_224  
 MGTYRXN0\_224  
 MGTYRXP1\_224  
 MGTYRXN1\_224  
 MGTYRXP2\_224  
 MGTYRXN2\_224  
 MGTYRXP3\_224  
 MGTYRXN3\_224  
 MGTRCLKOP\_224  
 MGTRCLKON\_224  
 MGTRCLK1P\_224  
 MGTRCLK1N\_224

U34J  
XCAU25P-2FFVB676I

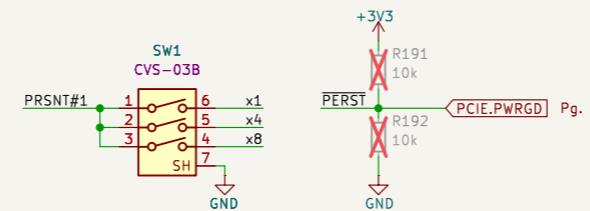
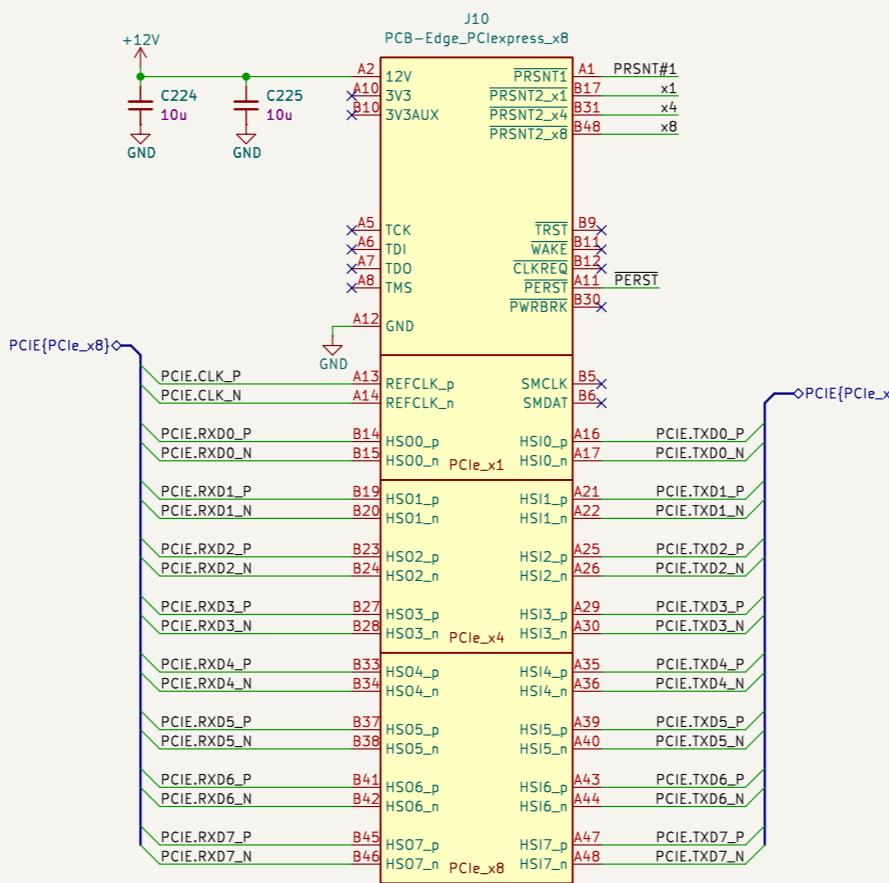
GTX 225  
 MGTYTXP0\_225  
 MGTYTXN0\_225  
 MGTYTXP1\_225  
 MGTYTXN1\_225  
 MGTYTXP2\_225  
 MGTYTXN2\_225  
 MGTYTXP3\_225  
 MGTYTXN3\_225  
 MGTYRXP0\_225  
 MGTYRXN0\_225  
 MGTYRXP1\_225  
 MGTYRXN1\_225  
 MGTYRXP2\_225  
 MGTYRXN2\_225  
 MGTYRXP3\_225  
 MGTYRXN3\_225  
 MGTRCLKOP\_225  
 MGTRCLKON\_225  
 MGTRCLK1P\_225  
 MGTRCLK1N\_225

Place capacitors close to connector

GTY\_224\_TX0\_P 100n C251 PCIE.TXD7\_P  
 GTY\_224\_TX0\_N 100n C252 PCIE.TXD7\_N  
 GTY\_224\_TX1\_P 100n C253 PCIE.TXD6\_P  
 GTY\_224\_TX1\_N 100n C254 PCIE.TXD6\_N  
 GTY\_224\_TX2\_P 100n C255 PCIE.TXD5\_P  
 GTY\_224\_TX2\_N 100n C250 PCIE.TXD5\_N  
 GTY\_224\_TX3\_P 100n C256 PCIE.TXD4\_P  
 GTY\_224\_TX3\_N 100n C257 PCIE.TXD4\_N  
 GTY\_225\_TX0\_P 100n C226 PCIE.TXD3\_P  
 GTY\_225\_TX0\_N 100n C230 PCIE.TXD3\_N  
 GTY\_225\_TX1\_P 100n C227 PCIE.TXD2\_P  
 GTY\_225\_TX1\_N 100n C231 PCIE.TXD2\_N  
 GTY\_225\_TX2\_P 100n C228 PCIE.TXD1\_P  
 GTY\_225\_TX2\_N 100n C233 PCIE.TXD1\_N  
 GTY\_225\_TX3\_P 100n C229 PCIE.TXD0\_P  
 GTY\_225\_TX3\_N 100n C232 PCIE.TXD0\_N  
 GTY\_224\_RX0\_P PCIE.RXD7\_P  
 GTY\_224\_RX0\_N PCIE.RXD7\_N  
 GTY\_224\_RX1\_P PCIE.RXD6\_P  
 GTY\_224\_RX1\_N PCIE.RXD6\_N  
 GTY\_224\_RX2\_P PCIE.RXD5\_P  
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 GTY\_224\_RX3\_N PCIE.RXD4\_N  
 GTY\_225\_RX0\_P PCIE.RXD3\_P  
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 GTY\_225\_RX1\_N PCIE.RXD2\_N  
 GTY\_225\_RX2\_P PCIE.RXD1\_P  
 GTY\_225\_RX2\_N PCIE.RXD1\_N  
 GTY\_225\_RX3\_P PCIE.RXD0\_P  
 GTY\_225\_RX3\_N PCIE.RXD0\_N  
 GTR\_REFCLK0\_P 10n C222 PCIE.CLK\_P  
 GTR\_REFCLK0\_N 10n C258 PCIE.CLK\_N

**HDMI****Clock multiplier**Antmicro  
www.antmicro.comSheet: /FPGA MGT Interface/  
File: fpga-mgt.kicad\_sch**Title: RDIMM DDR5 Tester**Size: A3 Date: 2024-12-20  
KiCad E.D.A. 8.0.5Rev: 2.1.0:1f2bc  
Id: 11/17

# PCIe



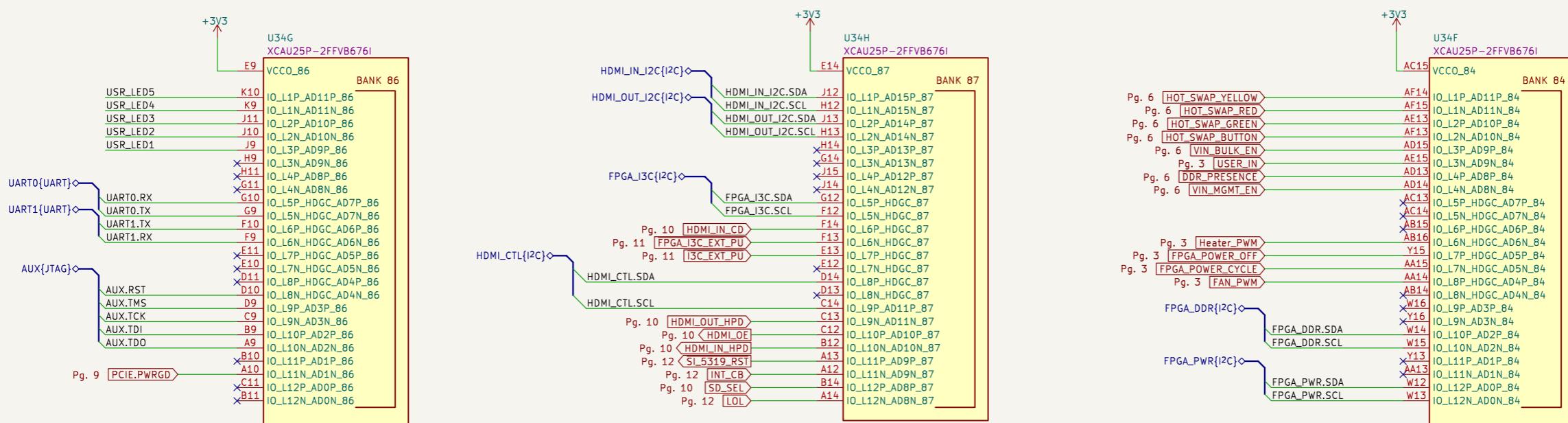
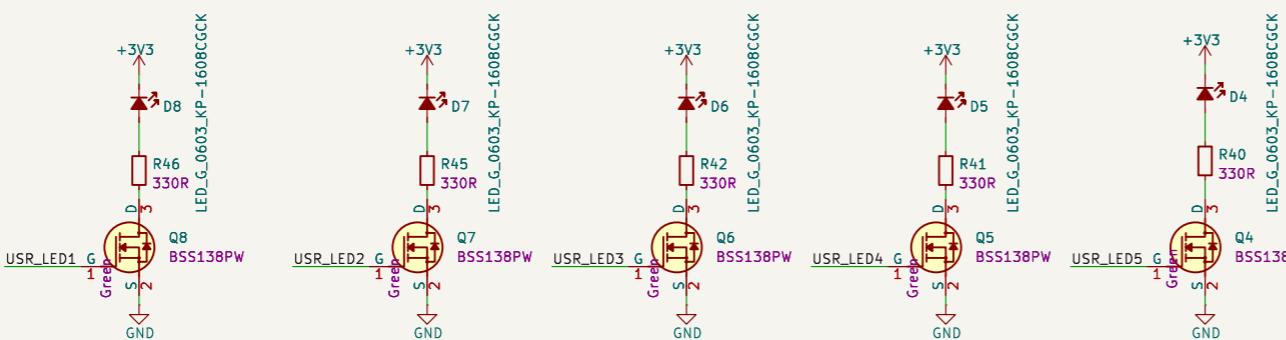
Antmicro  
www.antmicro.com

Sheet: /PCIe connector/  
File: pcie-connector.kicad\_sch

**Title: RDIMM DDR5 Tester**

Size: A3 | Date: 2024-12-20  
KiCad E.D.A. 8.0.5

Rev: 2.1.0:1f2bc | Id: 12/17

**BANKS HD****User LEDs**

Antmicro  
www.antmicro.com

Sheet: /FPGA banks HD/  
File: fpga-hd-banks.kicad\_sch

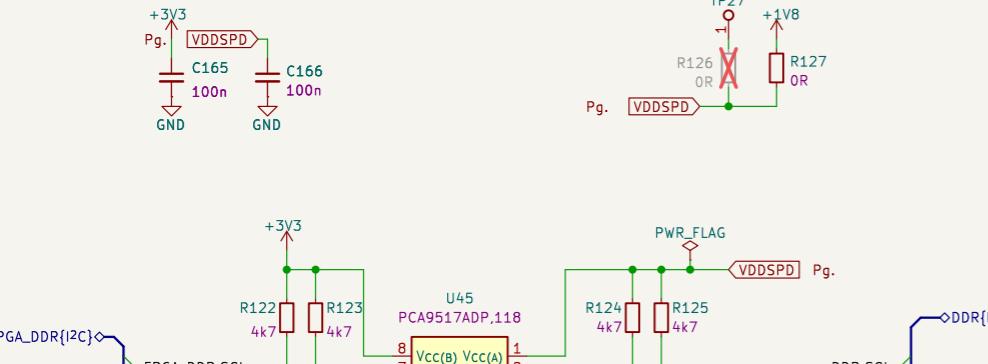
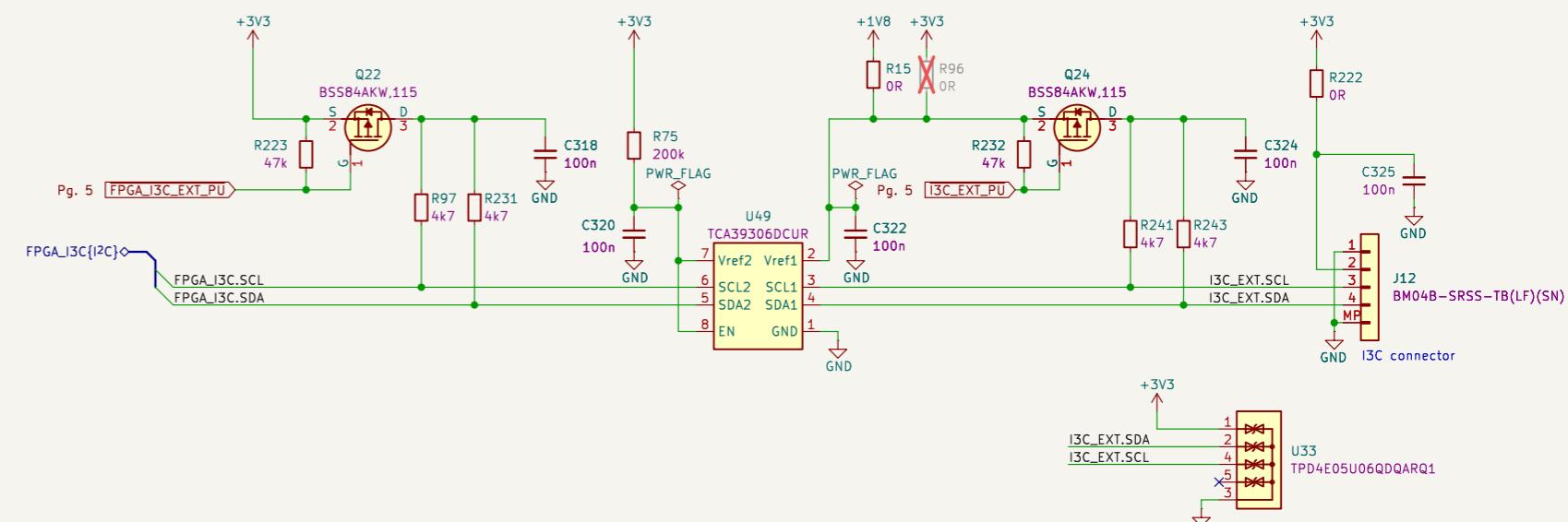
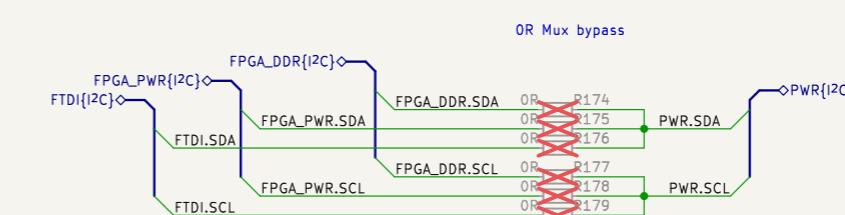
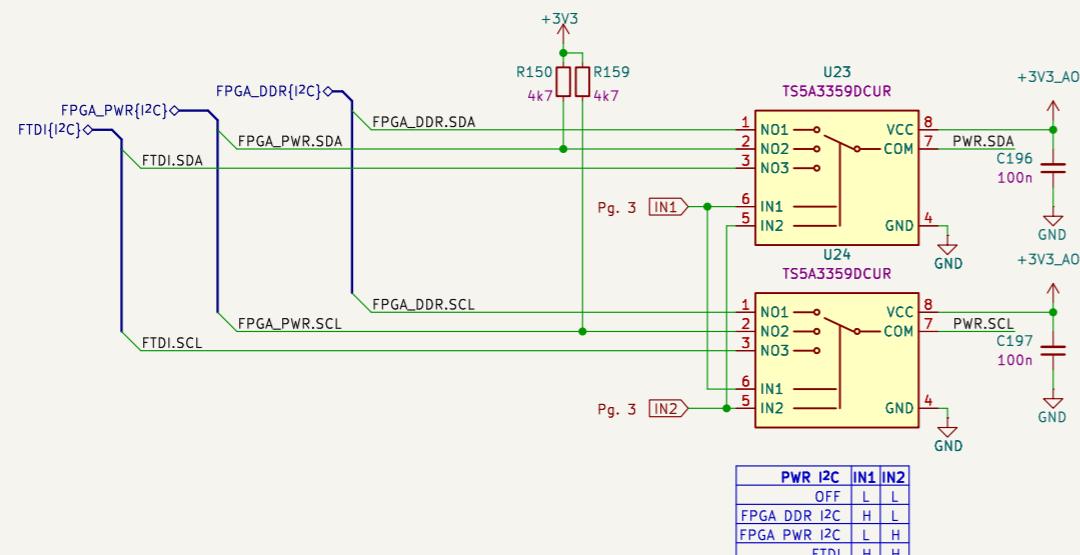
**Title: RDIMM DDR5 Tester**

Size: A3 Date: 2024-12-20

KiCad E.D.A. 8.0.5

Rev: 2.1.0:1f2bc

Id: 13/17

I<sup>2</sup>CI<sup>3</sup>CPWR I<sup>2</sup>C MUX

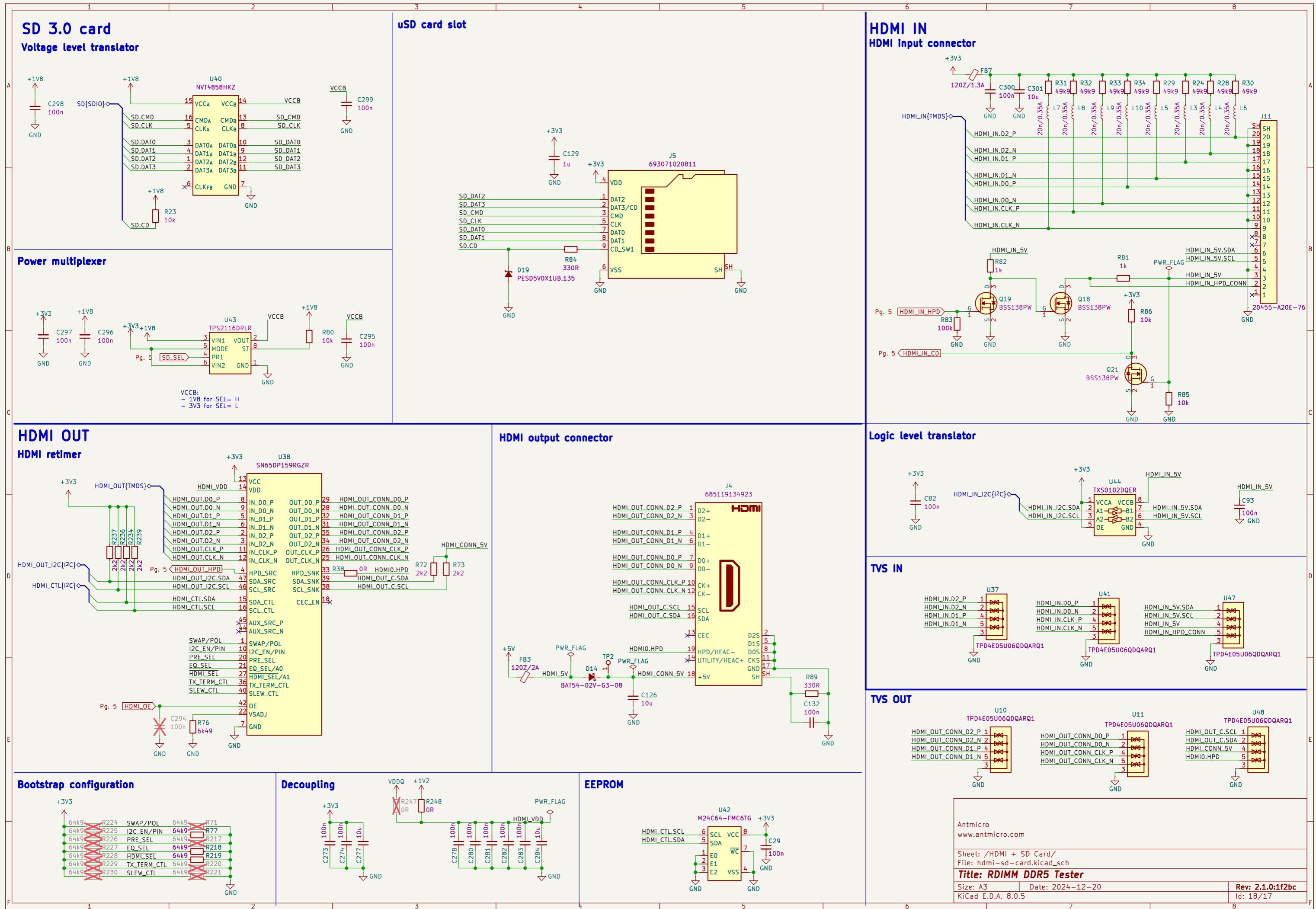
Antmicro  
www.antmicro.com

Sheet: /I<sup>2</sup>C + I<sup>3</sup>C/  
File: i2c.kicad\_sch

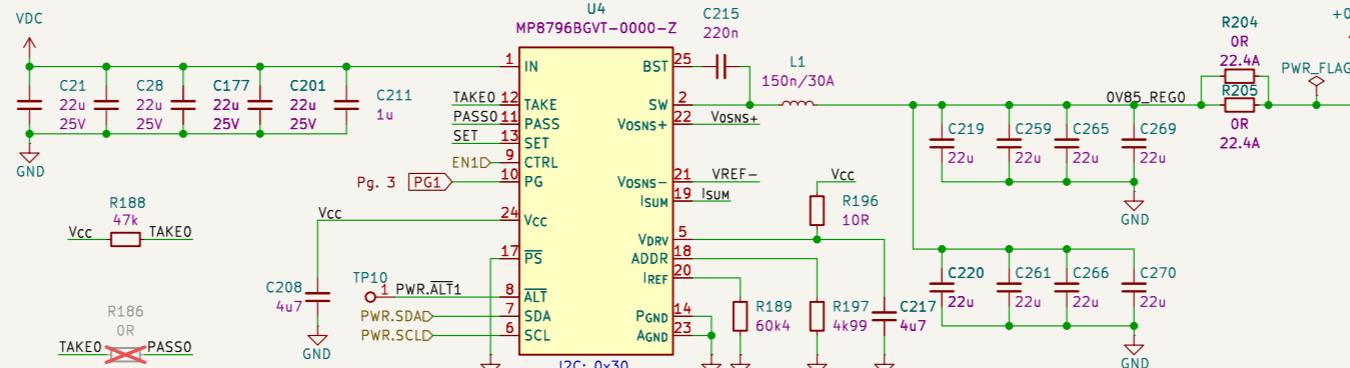
**Title: RDIMM DDR5 Tester**

Size: A3 | Date: 2024-12-20  
KiCad E.D.A. 8.0.5

Rev: 2.1.0:1f2bc | Id: 17/17



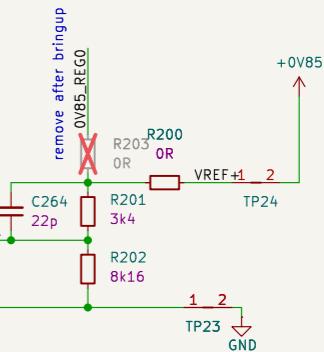
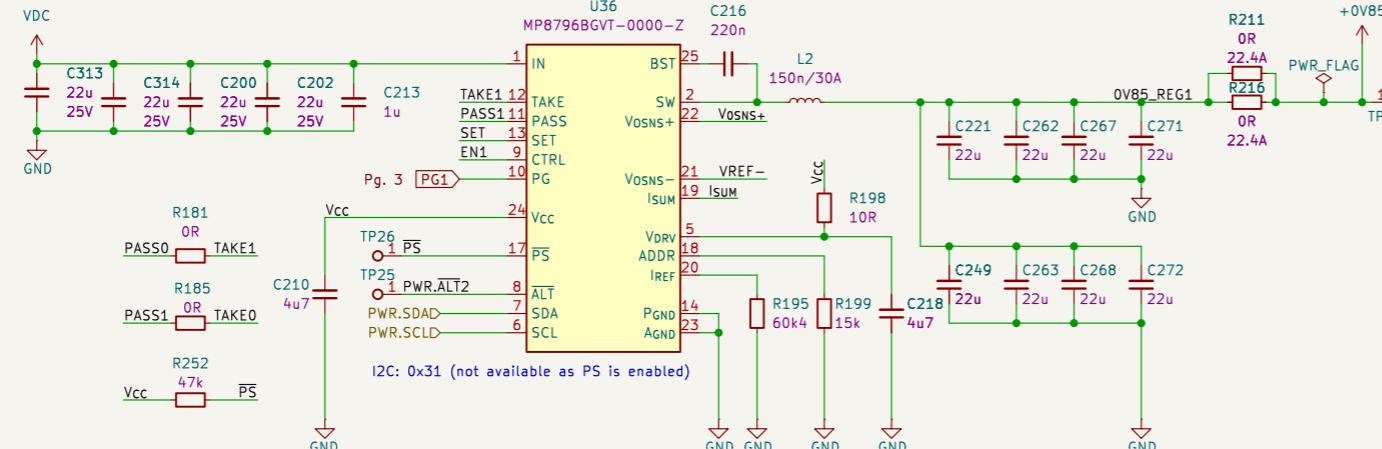
# DC-DC INT



MP8796BGVT-0000-Z selected due to its wide availability on the market  
Replace with MPQ8655GVT when it becomes available on the market

Pin compatible PN: MPQ8645P, MPQ8655GVT

Second phase is for VCCINT > 20A applications  
Do Not Populate if not required  
(place R188 instead)



Antmicro  
www.antmicro.com

Sheet: /Supply/DC-DC\_VCCINT/  
File: dc-dc-vccint.kicad\_sch

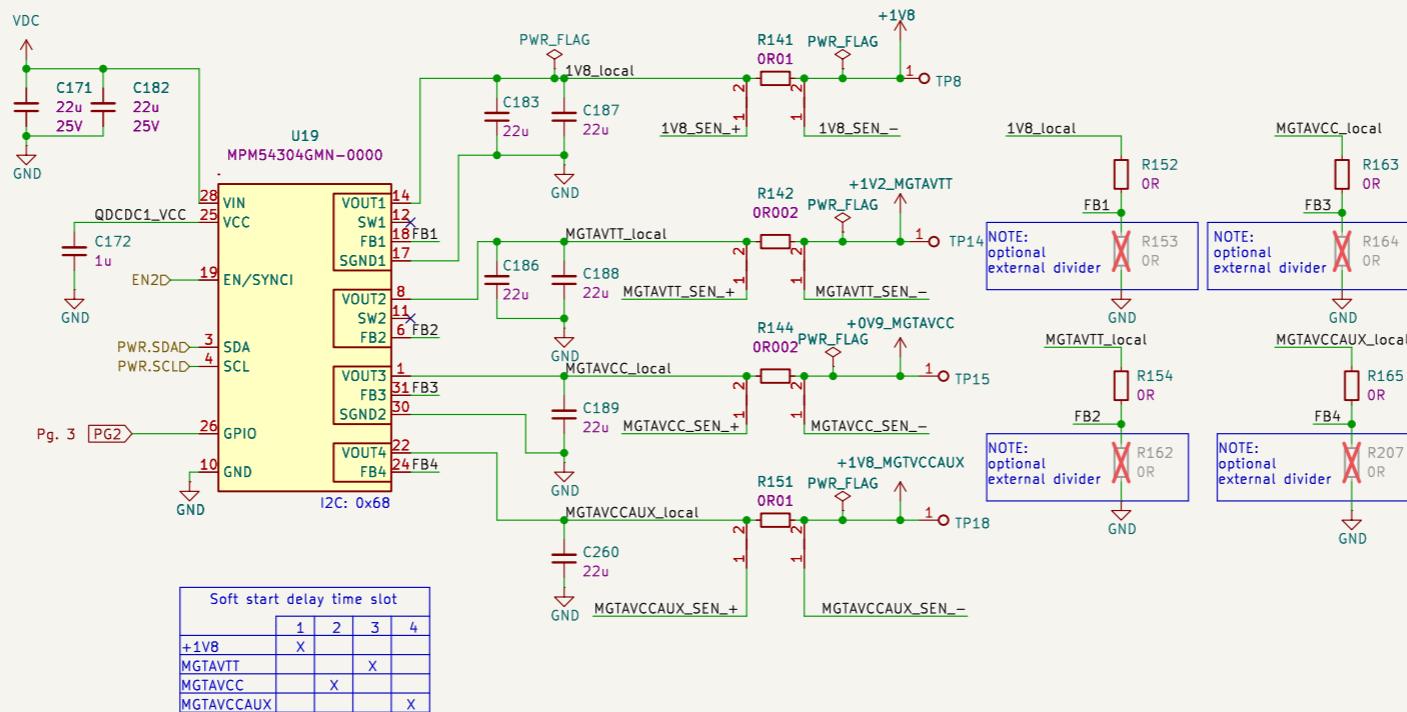
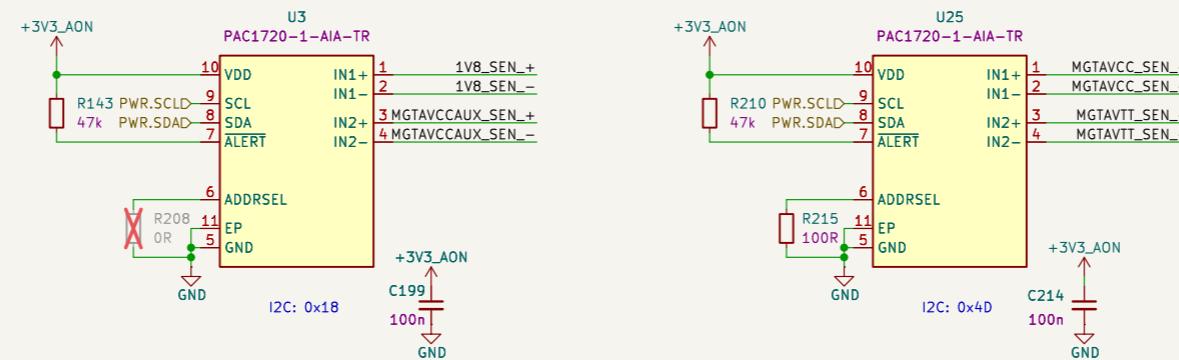
Title: RDIMM DDR5 Tester

Size: A3 Date: 2024-12-20

KiCad E.D.A. 8.0.5

Rev: 2.1.0:1f2bc

Id: 18/17

**DC-DC AUX, MGT****Current sense monitors**

Antmicro  
www.antmicro.com

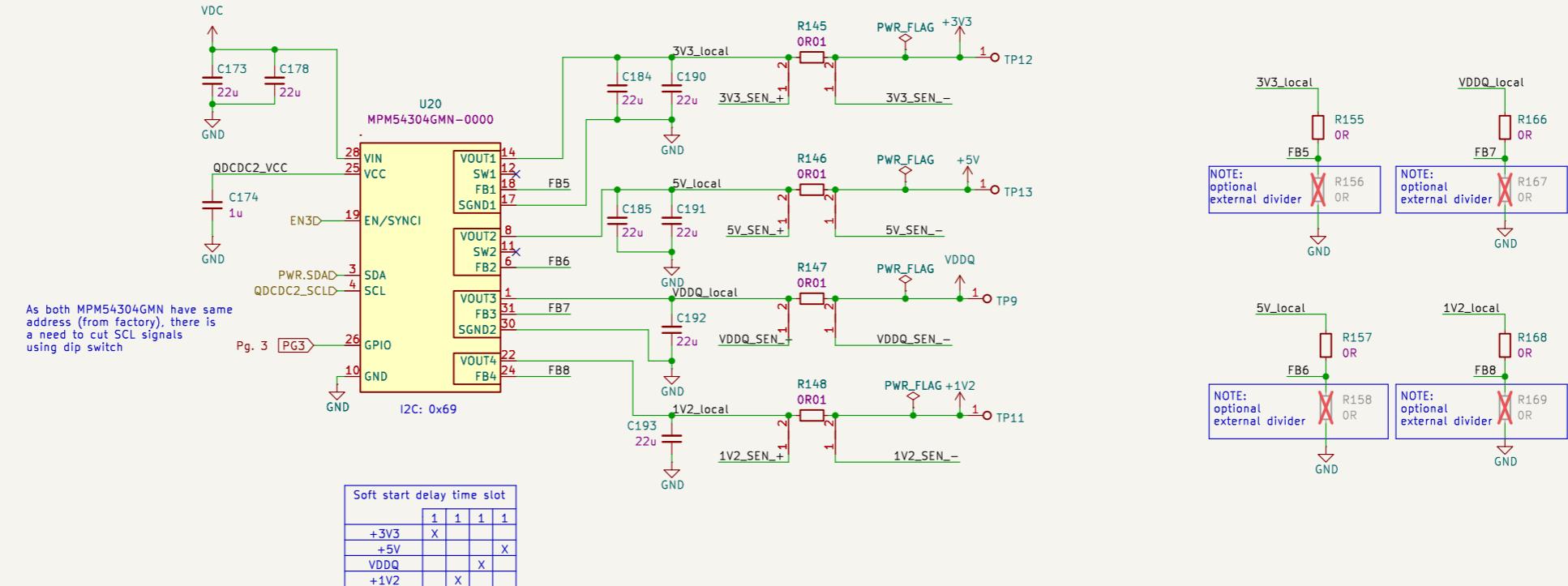
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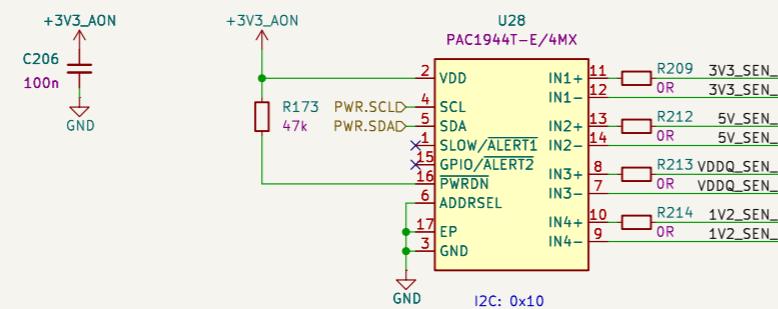
Size: A3 | Date: 2024-12-20  
KiCad E.D.A. 8.0.5

Rev: 2.1.0:1f2bc | Id: 19/17

## DC-DC IO



## Current sense monitor



Antmicro  
www.antmicro.com

Sheet: /Supply/DC-DC IO/  
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**Title: RDIMM DDR5 Tester**

Size: A3 | Date: 2024-12-20  
KiCad E.D.A. 8.0.5

Rev: 2.1.0:1f2bc | Id: 20/17