

31

220

0

controller_last_addr_3[20:0]

This diagram illustrates a 32-bit register structure. The register is divided into two main fields: 'controller_last_addr_3[20:0]' and 'controller_last_addr_4[1:0]'. The 'controller_last_addr_3[20:0]' field occupies the most significant 21 bits (from bit 31 down to bit 0), while the 'controller_last_addr_4[1:0]' field occupies the least significant 2 bits. Both fields are represented by vertical black bars on a white background, indicating their binary nature.

0