

**SDI deserializer**

U2A GS2971A Semtech

U2B GS2971A Semtech

U2C GS2971A Semtech

**Programming Interface**

J6 GRPB052VWVW-RC

**GS\_I2C**

J5 GRPB041VWVW-RC

**Logotypes**

N1 antimicro\_logo

N2 oshw\_logo

**SDI output**

U3 Semtech GS2988-INE3

**SDI input**

**Filtering**

**Place close to GS2971A**

**RESET**

**MIPI connector**

**I2C to SPI bridge**

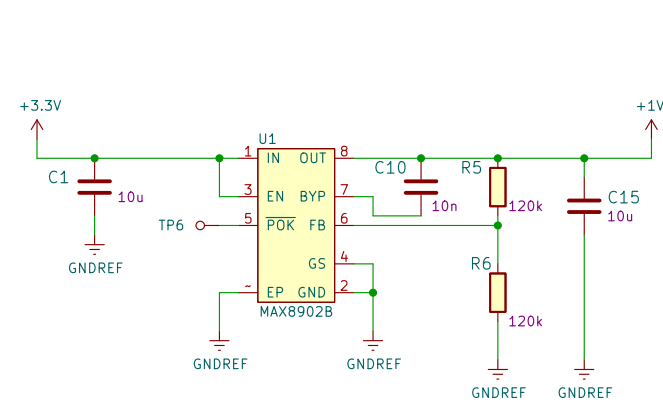
**I2S connector**

**Pull-up resistors**

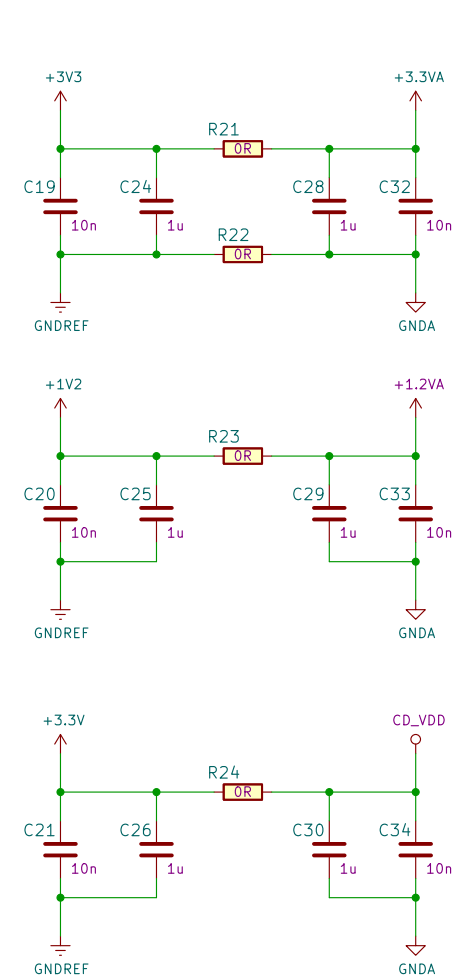
**BOM**

Ref	Value	Quantity	Part
R1	10k	1	RES
R2	10k	1	RES
R3	10k	1	RES
R4	10k	1	RES
R5	10k	1	RES
R6	10k	1	RES
R7	10k	1	RES
R8	10k	1	RES
R9	10k	1	RES
R10	10k	1	RES
R11	10k	1	RES
R12	10k	1	RES
R13	10k	1	RES
R14	10k	1	RES
R15	10k	1	RES
R16	10k	1	RES
R17	10k	1	RES
R18	10k	1	RES
R19	10k	1	RES
R20	10k	1	RES
R21	10k	1	RES
R22	10k	1	RES
R23	10k	1	RES
R24	10k	1	RES
R25	10k	1	RES
R26	10k	1	RES
R27	10k	1	RES
R28	10k	1	RES
R29	10k	1	RES
R30	10k	1	RES
R31	10k	1	RES
R32	10k	1	RES
R33	10k	1	RES
R34	10k	1	RES
R35	10k	1	RES
R36	10k	1	RES
R37	10k	1	RES
R38	10k	1	RES
R39	10k	1	RES
R40	10k	1	RES
R41	10k	1	RES
R42	10k	1	RES
R43	10k	1	RES
R44	10k	1	RES
R45	10k	1	RES
R46	10k	1	RES
R47	10k	1	RES
R48	10k	1	RES
R49	10k	1	RES
R50	10k	1	RES
R51	10k	1	RES
R52	10k	1	RES
R53	10k	1	RES
R54	10k	1	RES
R55	10k	1	RES
R56	10k	1	RES
R57	10k	1	RES
R58	10k	1	RES
R59	10k	1	RES
R60	10k	1	RES
R61	10k	1	RES
R62	10k	1	RES
R63	10k	1	RES
R64	10k	1	RES
R65	10k	1	RES
R66	10k	1	RES
R67	10k	1	RES
R68	10k	1	RES
R69	10k	1	RES
R70	10k	1	RES
R71	10k	1	RES
R72	10k	1	RES
R73	10k	1	RES
R74	10k	1	RES
R75	10k	1	RES
R76	10k	1	RES
R77	10k	1	RES
R78	10k	1	RES
R79	10k	1	RES
R80	10k	1	RES
R81	10k	1	RES
R82	10k	1	RES
R83	10k	1	RES
R84	10k	1</	

**Abstract**



The diagram illustrates a 4-stage Miller compensation network. A +1V2 input signal is applied to the first stage, which consists of a capacitor C2 in parallel with a 10nF resistor. This is followed by three more stages, each consisting of a capacitor (C4, C6, and C8 respectively) in parallel with a 10nF resistor. The output of the final stage is connected to GNDREF.



LOCKED

LOCKED\_CLR

CDONE

USER\_LED

DATA\_ERROR

R31 100R

R33 100R

D1

R88 100R

D2

R93 100R

D4

R64 100R

D5

LG\_L29K-G2J1-24-Z

LG\_L29K-G2J1-24-Z

LG\_L29K-G2J1-24-Z

LG\_L29K-G2J1-24-Z

GNDREF

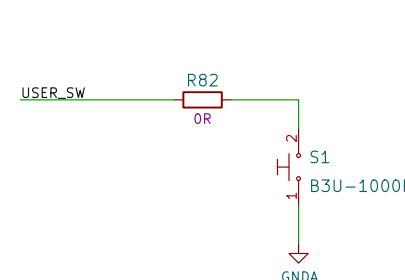
GNDREF

GNDREF

GNDREF

Figure 10: Pin connections for the board. The diagram shows two rows of pin headers. The top row (pins 1-10) includes connections for 10\_VDD, USER\_SW, 500\_EN\_DIS, Audio\_EN\_DIS, I2P0C\_EN\_DIS, 20bit\_T0B1, and SMPTE\_BYPASS. The bottom row (pins 11-20) includes connections for DVB\_ASI, SW\_EN, TIM\_B6, EC\_BYP, STANDBY, and JTAG\_HOST. Each pin is connected to a specific component or signal line, with some pins having a 10k resistor connected to GND.

Used as RESET button by default



Pinout diagram for the STM32F103C8T6 microcontroller. The diagram shows the 48 pins of the package, with pins 1-16 on the left and 17-48 on the right. A dashed blue box labeled "Crosslink and Semtech at same I2C Line" encloses pins 37-40, which are labeled SPI\_SCK(SDA) R37, SPI\_SS(SCL) R38, SDA\_GS R39, and SCL\_GS R40. Other pins are labeled with their functions: MIPI0\_D3\_N 1, MIPI0\_D3\_P 2, MIPI0\_D2\_N 3, MIPI0\_D2\_P 4, MIPI0\_D1\_N 5, MIPI0\_D1\_P 6, MIPI0\_D0\_N 7, MIPI0\_D0\_P 8, MIPI0\_CLK\_N 9, MIPI0\_CLK\_P 10, MIPI1\_D3\_N 19, MIPI1\_D3\_P 20, MIPI1\_D2\_N 21, MIPI1\_D2\_P 22, MIPI1\_D1\_N 23, MIPI1\_D1\_P 24, MIPI1\_D0\_N 25, MIPI1\_D0\_P 26, MIPI1\_CLK\_N 28, MIPI1\_CLK\_P 29, RST 31, SDA19 39, SCL14 40, SDA21 41, SCL2 42, and R92 47. The diagram also shows a +3.3V supply pin and a GND pin.

J4  
GRP052VWVN-RC

1	2
AUDIO_SERIAL_BIT_CLK	AUDIO_SERIAL_BIT_CLK
AUDIO_WORD_CLK	AUDIO_WORD_CLK
AUDIO_OUTPUT_CH1_2	AUDIO_OUTPUT_CH5_6
AUDIO_OUTPUT_CH3_4	AUDIO_OUTPUT_CH7_8
9	AUDIO_MASTER_CLK

Schematic diagram of the I2C bus connection for the ADXL345. The ADXL345 is shown with its I2C pins connected to the Raspberry Pi's I2C pins. The ADXL345 pins are SDA, SCL, GND, and VCC. The Raspberry Pi pins are SDA, SCL, GND, and VCC. The SDA pin is connected to the ADXL345 SDA pin. The SCL pin is connected to the ADXL345 SCL pin. The GND pin is connected to the ADXL345 GND pin. The VCC pin is connected to the ADXL345 VCC pin. A note indicates that the SDA pin should be DNP if one I2C device is used.