SA800U-WF

Hardware Design

Smart Module Series

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local office. For more information, please visit:
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The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2020-07-31	Light WANG/ Finley ZHANG	Creation of the document
1.0	2021-01-13	Light WANG/ Finley ZHANG	First official release

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1 Introduction

This document defines the SA800U-WF module and describes its air interfaces and hardware interfaces.

This document helps you quickly understand module interface specifications, electrical and mechanical details as well as other related information of the module. Associated with application notes and user guides, you can use the module to design and set up applications easily.

2 Product Concept

2.1. General Description

SA800U-WF is a smart module based on Qualcomm platform and Android operating system, which provides industrial grade performance. Its general features are listed below:

- Support short-range wireless communication via Wi-Fi 802.11a/b/g/n/ac and BT 5.0
- Support multiple audio and video codecs
- Built-in high performance Adreno™ 630 graphics processing unit
- Dedicated low-power Snapdragon sensor core DSP to support always-on use cases
- Provide multiple audio and video input/output interfaces as well as abundant GPIO interfaces

The following table shows the supported frequency bands of the module.

Table 1: SA800U-WF Frequency Bands

Type	Frequency Bands
802.11a/b/g/n/ac	2402–2482 MHz 5180–5825 MHz
BT 5.0	2402–2480 MHz
FM*	76–108 MHz

SA800U-WF is a 396-pin module, which supports B2B connection. With a compact profile of 60.0 mm × 37.0 mm × 6.55 mm, the module can meet almost all requirements for M2M applications such as smart meeting, smart home, security, routers, AR glasses, mobile computing devices, PDA phone, tablet PC, etc.

NOTE

"*" means under development.

2.2. Key Features

The following table describes the detailed features of the module.

Table 2: SA800U-WF Key Features

Features	Details
Applications Processor	64-bit Kryo 385 applications processor ● Quad high-performance Kyro cores at 2.649 GHz with 256 KB L2 cache per core ● Quad low-power Kyro cores at 1.766 GHz with 128 KB L2 cache per core
GPU	Adreno™ 630 graphics processing unit – 4K @ 60 fps or 2 × 2K @ 90 fps
Memory	● 64 GB UFS + 4 GB LPDDR4X (default) ● 256 GB UFS + 8 GB LPDDR4X (optional)
Operating System	Android 9.0/10.0
Power Supply	● VBAT Supply Voltage: 3.55–4.4 V ● Typ. 3.8 V
WLAN Features	● 2.4/5 GHz, 802.11a/b/g/n/ac ● Support 2 × 2 MIMO, maximally up to 866 Mbps ● Support AP and STA modes
Bluetooth Features	BT 2.1+EDR/3.0/4.1 LE/4.2 BLE/BT 5.0
LCM Interfaces	● Support two groups of 4-lane MIPI DSI ● Support dual LCDs ● Support 2560 × 1600 @ 60 fps VESA DSC 1.1 primary display with 4 lanes ● Support 4K @ 60 fps over DisplayPort ● Provide one high voltage output for powering strings of WLEDs and 29.6 V OVP ● Provide four drivers for sinking the current from WLED strings, and each sink current can reach up to 30 mA
Camera Interfaces	● Support three groups of 4-lane MIPI CSI and one 2-lane MIPI CSI [1], up to 2.5 Gbps/lane, ● Support 4 cameras (4-lane + 4-lane + 4-lane + 2-lane) ● Up to 32 MP with dual ISP
Video Codec	Video encoding and decoding up to 4K @ 60 fps
Audio Codec	QCELP, EVS, EVRC, EVRC-B, EVRC-WB, G.7Gen, G.729 A/AB

USB Interfaces	● 2 USB interfaces which comply with both USB 3.1 and USB 2.0 specifications ● Support up to 5 Gbps on USB 3.1 and 480 Mbps on USB 2.0 ● USB1 supports USB OTG and DisplayPort, and can be used for AT command communication, data transmission, software debugging and firmware upgrade ● USB2 only supports USB host mode
PCIe Interfaces	2 PCIe Interfaces: ● PCIe0 is a Gen 2 1-lane interface ● PCIe1 is a Gen 3 1-lane interface
UART Interface	One 2-wire debug UART interface used for debugging by default
Vibrator Drive Interface	Drive ERM/LRA vibrator
SDIO Interfaces	2 SDIO interfaces: ● The SDIO function of SDC4 is not supported by default ● As the SD card interface, SDC2 complies with SD 3.0 specifications
I2C Interfaces	6 I2C interfaces, used for peripherals such as TP, camera, sensor, etc.
I2S Interfaces	3 I2S interfaces
Flashlight Interfaces	3 high-current flash LED drivers, which supports both flash and torch modes ● Up to 1.5 A for FLASH_LED1/FLASH_LED2 in flash mode ● Up to 0.75 A for FLASH_LED3 in flash mode
ADC Interfaces	2 general-purpose ADC interfaces
SPI Interfaces	3 SPI interfaces, only support master mode
Charging Interface	Used for battery voltage detection, fuel gauge, battery temperature detection
Real Time Clock	Supported
Antenna Connection	4 antenna connectors: Wi-Fi/BT, Wi-Fi MIMO, BT*, FM*
Physical Characteristics	● Size: (60.0 ±0.15) mm × (37.0 ±0.15) mm × (6.55 ±0.2) mm ● Package: B2B ● Weight: approx. 15 g
Temperature Range	● Operating temperature range: -35 °C to +75 °C [2)] ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	Over USB interface or OTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1] The 2-lane MIPI CSI can only get data of RAW format. It can be used for ToF/3D camera modules but cannot be used for display.
2. [2] Within the operating temperature range, the module is IEEE compliant.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of SA800U-WF and illustrates the major functional parts.

- Power management
- Baseband
- LPDDR4X + UFS flash
- Peripheral interfaces
  -- USB interfaces
  -- PCIe interfaces
  -- UART interface
  -- I2C interfaces
  -- SPI interfaces
  -- SD card interface
  -- GPIO interfaces
  -- SLIMbus interface
  -- I2S interfaces
  -- ADC interfaces
  -- Vibrator drive interface
  -- LCM (MIPI) interfaces
  -- TP (touch panel) interface
  -- Camera (MIPI) interfaces
  -- Flashlight interfaces
  -- Sensor interfaces
  -- Emergency download interface

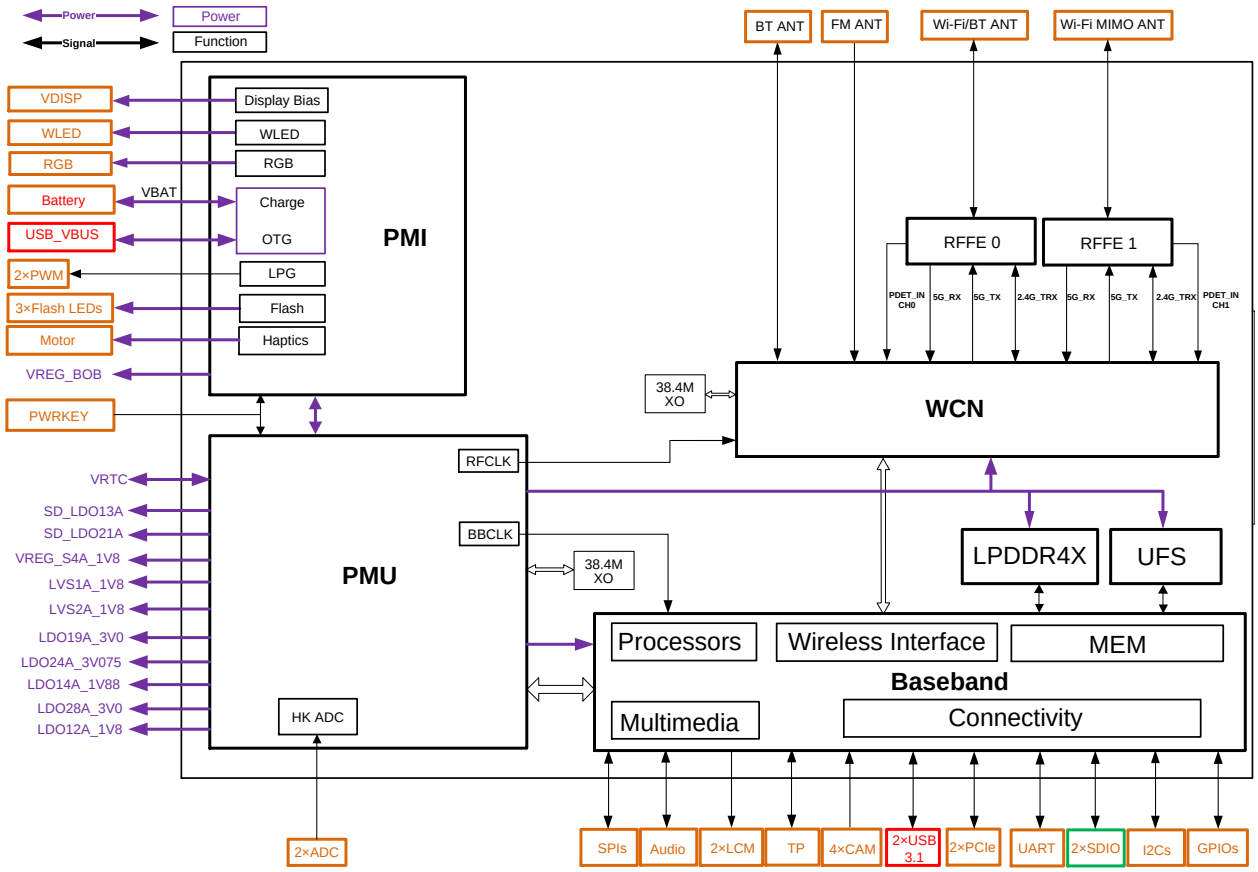


Figure 1: Functional Diagram

2.4. Evaluation Board

To help you develop applications with SA800U-WF conveniently, Quectel supplies the evaluation board, USB to RS-232 converter cable, USB Type-C data cable, power adapter, earphone, antenna and other peripherals to control or test the module. For more details, see ***document [1]***.

3 Application Interfaces

3.1. General Description

SA800U-WF is equipped with 396 pins that can be embedded into cellular application platform. The following chapters provide the detailed description of interfaces listed below.

- Power supply
- VRTC interface
- Charging interface
- USB interfaces
- UART interface
- PCIe interfaces
- SD card interface
- GPIO interfaces
- I2C interfaces
- SPI interfaces
- ADC interfaces
- Vibrator drive interface
- LCM interfaces
- TP interface
- Camera interfaces
- Flashlight interfaces
- Sensor interfaces
- Audio interfaces
- Emergency download interface

3.2. Pin Assignment

The following figure shows the pin assignment of SA800U-WF module.

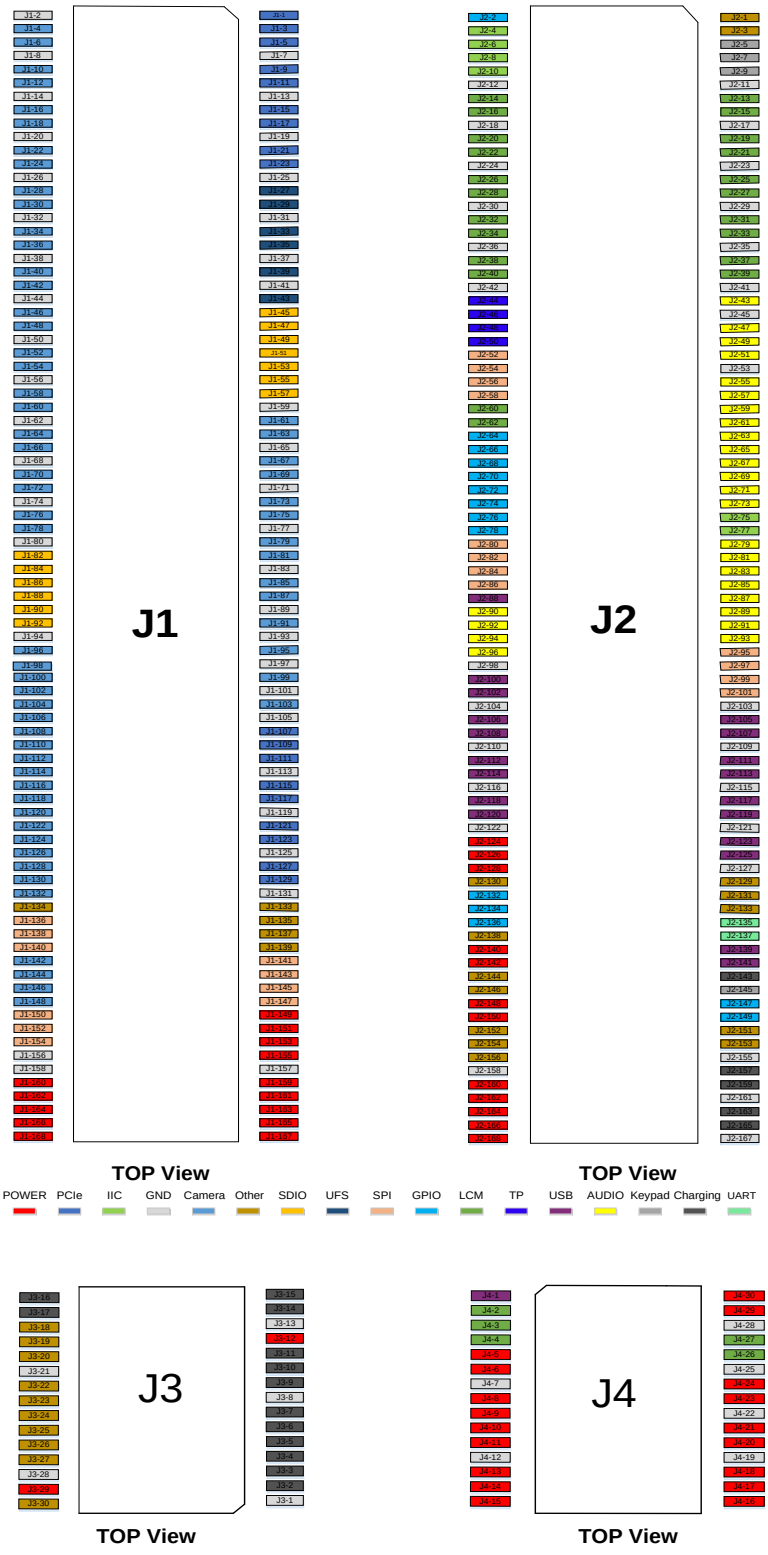


Figure 2: Pin Assignment (Top View)

3.3. Pin Description

Table 3: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

The following tables show the SA800U-WF's pin definitions and electrical characteristics.

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	J1-159, J1-160, J1-161, J1-162, J1-163, J1-164, J1-165, J1-166, J1-167, J1-168	PI/ PO	Power supply for the module	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V	Must be provided with sufficient current of up to 3 A. It is suggested to use a TVS to increase voltage surge withstand capability.
VREG_BOB	J2-140, J2-142	PO	BOB output	Vnom = 3.7 V $I_O$max = 2000 mA	Power supply for external LDOs.

VREG_S4A_1V8	J2-124, J2-126, J2-128	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 2000 mA	Power supply for external GPIO's pull-up circuit and level shift circuit.
LVS1A_1V8	J1-149	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 300 mA	Power supply for IOVDD of cameras. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LVS2A_1V8	J2-148	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 100 mA	Power supply for IOVDD or VDD of sensors. Add a 1.0–2.2 μF bypass capacitor if used. If unused, keep this pin open.
LDO12A_1V8	J3-12	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 300 mA	Connect this pin to SHDN of SMB1355 parallel charger to make the charger enter low power mode. If SMB1355 is unused, keep this pin open.
LDO14A_1V88	J4-9	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for IOVDD of TP and LCDs. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO19A_3V0	J2-150	PO	3.0 V output	Vnom = 3.0 V $I_O$max = 600 mA	Power supply for sensors Add a 1.0–2.2 μF bypass capacitor if used. If unused, keep this pin open.

LDO24A_3V075	J4-8	PO	3.075 V output	Vnom = 3.075 V $I_O$max = 150 mA	Power supply for DP's pull-up circuits. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO28A_3V0	J4-10	PO	3.0 V output	Vnom = 3.0 V $I_O$max = 150 mA	Power supply for VDD of TP. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
GND	J1-2, J1-7, J1-8, J1-13, J1-14, J1-19, J1-20, J1-25, J1-26, J1-31, J1-32, J1-37, J1-38, J1-41, J1-44, J1-50, J1-56, J1-59, J1-62, J1-65, J1-68, J1-71, J1-74, J1-77, J1-80, J1-83, J1-89, J1-93, J1-94, J1-97, J1-101, J1-105, J1-113, J1-119, J1-125, J1-131, J1-156, J1-157, J1-158, J2-11, J2-12, J2-17, J2-18, J2-23, J2-24, J2-29, J2-30, J2-35, J2-36, J2-41, J2-42, J2-45, J2-53, J2-98, J2-103, J2-104, J2-109, J2-110, J2-115, J2-116, J2-121, J2-122, J2-127, J2-155, J2-158, J2-161, J2-167, J3-1, J3-8, J3-13, J3-21, J3-28, J4-7, J4-12, J4-19, J4-22, J4-25, J4-28				

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	J2-160, J2-162, J2-164, J2-166, J2-168, J4-13, J4-14, J4-15, J4-16, J4-17, J4-18	PI/ PO	Charging power input. Power output for OTG device. USB/adaptor insertion detect.	Vmax = 14 V Vmin = 4.0 V Vnom = 5.0 V	
USB1_DM	J2-117	AIO	USB1 2.0 differential data (-)		90 Ω differential impedance. USB 2.0 standard compliant.
USB1_DP	J2-119	AIO	USB1 2.0 differential data (+)		

USB1_SS1_TX_M	J2-123	AO	USB1 3.1 channel 1 super-speed transmit (-)	90 Ω differential impedance. USB 3.1 standard compliant.
USB1_SS1_TX_P	J2-125	AO	USB1 3.1 channel 1 super-speed transmit (+)	
USB1_SS1_RX_M	J2-118	AI	USB1 3.1 channel 1 super-speed receive (-)	
USB1_SS1_RX_P	J2-120	AI	USB1 3.1 channel 1 super-speed receive (+)	
USB1_SS2_TX_M	J2-111	AO	USB1 3.1 channel 2 super-speed transmit (-)	
USB1_SS2_TX_P	J2-113	AO	USB1 3.1 channel 2 super-speed transmit (+)	
USB1_SS2_RX_M	J2-114	AI	USB1 3.1 channel 2 super-speed receive (-)	
USB1_SS2_RX_P	J2-112	AI	USB1 3.1 channel 2 super-speed receive (+)	
USB_CC1	J2-141	AI	USB Type-C configuration channel 1	
USB_CC2	J2-139	AI	USB Type-C configuration channel 2	
USB2_DP	J2-105	AIO	USB2 2.0 differential data (+)	90 Ω differential impedance. USB 2.0 standard

USB2_DM	J2-107	AIO	USB2 2.0 differential data (-)		compliant. Only support host mode.
USB2_SS_TX_M	J2-108	AO	USB2 3.1 channel 1 super-speed transmit (-)		90 Ω differential impedance. USB 3.1 standard compliant. Only support host mode.
USB2_SS_TX_P	J2-106	AO	USB2 3.1 channel 1 super-speed transmit (+)		
USB2_SS_RX_M	J2-100	AI	USB2 3.1 channel 1 super-speed receive (-)		
USB2_SS_RX_P	J2-102	AI	USB2 3.1 channel 1 super-speed receive (+)		
PCIe Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE0_RST_N	J1-1	DO	PCIe0 reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCIE0_WAKE_N	J1-3	DI	PCIe0 wake up host	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
PCIE0_CLKREQ_N	J1-5	DI	PCIe0 clock request	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
PCIE0_REFCLK_P	J1-15	AO	PCIe0 reference clock (+)		Control the characteristic impedance as 85 Ω.
PCIE0_REFCLK_M	J1-17	AO	PCIe0 reference clock (-)		
PCIE0_TX_P	J1-11	AO	PCIe0 transmit (+)		
PCIE0_TX_M	J1-9	AO	PCIe0 transmit (-)		
PCIE0_RX_P	J1-21	AI	PCIe0 receive (+)		
PCIE0_RX_M	J1-23	AI	PCIe0 receive (-)		
PCIE1_RST_N	J1-107	DO	PCIe1 reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

PCIE1_WAKE_N	J1-111	DI	PCIe1 wake up host	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
PCIE1_CLKREQ_N	J1-109	DI	PCIe1 clock request	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
PCIE1_REFCLK_P	J1-121	AO	PCIe1 reference clock (+)		Control the characteristic impedance as 85 Ω.
PCIE1_REFCLK_M	J1-123	AO	PCIe1 reference clock (-)		
PCIE1_TX_P	J1-129	AO	PCIe1 transmit (+)		
PCIE1_TX_M	J1-127	AO	PCIe1 transmit (-)		
PCIE1_RX_P	J1-115	AI	PCIe1 receive (+)		
PCIE1_RX_M	J1-117	AI	PCIe1 receive (-)		
SDIO Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDC4_CLK	J1-86	DO	SDIO clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	SDIO function is not supported by default. Can be multiplexed into GPIOs.
SDC4_CMD	J1-92	DO	SDIO command	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SDC4_DATA0	J1-82	DIO	SDIO data bit 0	V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SDC4_DATA1	J1-84	DIO	SDIO data bit 1		
SDC4_DATA2	J1-88	DIO	SDIO data bit 2		
SDC4_DATA3	J1-90	DIO	SDIO data bit 3		
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	J1-45	DO	SD card clock	**1.8 V SD card:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **2.95 V SD card:** V_{OL}max = 0.36 V V_{OH}min = 2.22 V	Control characteristic impedance as 45 Ω.
SD_CMD	J1-47	DO	SD card command		
SD_DATA0	J1-51	DIO	SDIO data bit 0	**1.8 V SD card:**	

SD_DATA1	J1-53	DIO	SDIO data bit 1	V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{OL}max = 0.45 V V_{OH}min = 1.4 V **2.95 V SD card:** V_{IL}max = 0.73 V V_{IH}min = 1.85 V V_{OL}max = 0.36 V V_{OH}min = 2.22 V	
SD_DATA2	J1-57	DIO	SDIO data bit 2		
SD_DATA3	J1-55	DIO	SDIO data bit 3		
SD_DET	J1-49	DI	SD card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Active low.
SD_LDO21A	J1-151, J1-153, J1-155	PO	SD card power supply	Vnom = 2.95 V $I_O$max = 800 mA	
SD_LDO13A	J4-11	PO	1.8/2.95 V output power for SD card pull-up circuits	Vnom = 1.8/2.95 V $I_O$max = 50 mA	
TP (Touch Panel) Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_INT	J2-48	DI	TP interrupt	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	1.8 V power domain.
TP_RST	J2-50	DO	TP reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
TP_I2C_SCL	J2-44	OD	TP I2C clock		
TP_I2C_SDA	J2-46	OD	TP I2C data		
LCM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_BL_A	J4-4	PO	Power output for LCD backlight		
LCD_BL_K1	J4-3	AI	Current sink 1 for LCD backlight		
LCD_BL_K2	J4-2	AI	Current sink 2 for LCD backlight		
LCD_BL_K3	J4-27	AI	Current sink 3 for LCD backlight		
LCD_BL_K4	J4-26	AI	Current sink 4 for LCD backlight		

VDISP_P	J4-29	PO	Display bias output (+)		
VDISP_M	J4-30	PO	Display bias output (-)		
LCD_RST	J2-62	DO	LCD reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Active low. 1.8 V power domain.
LCD_TE	J2-60	DI	LCD tearing effect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	1.8 V power domain.
DSI0_CLK_N	J2-26	AO	LCD0 MIPI clock (-)		100 Ω differential impedance.
DSI0_CLK_P	J2-28	AO	LCD0 MIPI clock (+)		
DSI0_LN0_N	J2-38	AO	LCD0 MIPI lane 0 data (-)		
DSI0_LN0_P	J2-40	AO	LCD0 MIPI lane 0 data (+)		
DSI0_LN1_N	J2-32	AO	LCD0 MIPI lane 1 data (-)		
DSI0_LN1_P	J2-34	AO	LCD0 MIPI lane 1 data (+)		
DSI0_LN2_N	J2-20	AO	LCD0 MIPI lane 2 data (-)		
DSI0_LN2_P	J2-22	AO	LCD0 MIPI lane 2 data (+)		
DSI0_LN3_N	J2-14	AO	LCD0 MIPI lane 3 data (-)		
DSI0_LN3_P	J2-16	AO	LCD0 MIPI lane 3 data (+)		
DSI1_CLK_N	J2-21	AO	LCD1 MIPI clock (-)		
DSI1_CLK_P	J2-19	AO	LCD1 MIPI clock (+)		
DSI1_LN0_N	J2-13	AO	LCD1 MIPI lane 0 data (-)		
DSI1_LN0_P	J2-15	AO	LCD1 MIPI lane 0 data (+)		
DSI1_LN1_N	J2-37	AO	LCD1 MIPI lane 1 data (-)		
DSI1_LN1_P	J2-39	AO	LCD1 MIPI lane 1 data (+)		

DSI1_LN2_N	J2-27	AO	LCD1 MIPI lane 2 data (-)		
DSI1_LN2_P	J2-25	AO	LCD1 MIPI lane 2 data (+)		
DSI1_LN3_N	J2-31	AO	LCD1 MIPI lane 3 data (-)		
DSI1_LN3_P	J2-33	AO	LCD1 MIPI lane 3 data (+)		
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI0_CLK_N	J1-30	AI	MIPI clock of camera 0 (-)		
CSI0_CLK_P	J1-28	AI	MIPI clock of camera 0 (+)		
CSI0_LN0_N	J1-22	AI	MIPI lane 0 data of camera 0 (-)		
CSI0_LN0_P	J1-24	AI	MIPI lane 0 data of camera 0 (+)		
CSI0_LN1_N	J1-16	AI	MIPI lane 1 data of camera 0 (-)		
CSI0_LN1_P	J1-18	AI	MIPI lane 1 data of camera 0 (+)		
CSI0_LN2_N	J1-10	AI	MIPI lane 2 data of camera 0 (-)		
CSI0_LN2_P	J1-12	AI	MIPI lane 2 data of camera 0 (+)		100 Ω differential impedance.
CSI0_LN3_N	J1-6	AI	MIPI lane 3 data of camera 0 (-)		
CSI0_LN3_P	J1-4	AI	MIPI lane 3 data of camera 0 (+)		
CSI1_CLK_N	J1-58	AI	MIPI clock of camera 1 (-)		
CSI1_CLK_P	J1-60	AI	MIPI clock of camera 1 (+)		
CSI1_LN0_N	J1-52	AI	MIPI lane 0 data of camera 1 (-)		
CSI1_LN0_P	J1-54	AI	MIPI lane 0 data of camera 1 (+)		
CSI1_LN1_N	J1-46	AI	MIPI lane 1 data of camera 1 (-)		

CSI1_LN1_P	J1-48	AI	MIPI lane 1 data of camera 1 (+)	
CSI1_LN2_N	J1-42	AI	MIPI lane 2 data of camera 1 (-)	
CSI1_LN2_P	J1-40	AI	MIPI lane 2 data of camera 1 (+)	
CSI1_LN3_N	J1-34	AI	MIPI lane 3 data of camera 1 (-)	
CSI1_LN3_P	J1-36	AI	MIPI lane 3 data of camera 1 (+)	
CSI2_CLK_N	J1-63	AI	MIPI clock of camera 2 (-)	
CSI2_CLK_P	J1-61	AI	MIPI clock of camera 2 (+)	
CSI2_LN0_N	J1-67	AI	MIPI lane 0 data of camera 2 (-)	
CSI2_LN0_P	J1-69	AI	MIPI lane 0 data of camera 2 (+)	
CSI2_LN1_N	J1-66	AI	MIPI lane 1 data of camera 2 (-)	
CSI2_LN1_P	J1-64	AI	MIPI lane 1 data of camera 2 (+)	
CSI2_LN2_N	J1-72	AI	MIPI lane 2 data of camera 2 (-)	
CSI2_LN2_P	J1-70	AI	MIPI lane 2 data of camera 2 (+)	
CSI2_LN3_N	J1-78	AI	MIPI lane 3 data of camera 2 (-)	
CSI2_LN3_P	J1-76	AI	MIPI lane 3 data of camera 2 (+)	
CSI3_CLK_N	J1-85	AI	MIPI clock of camera 3 (-)	100 Ω differential impedance. CSI3 can only receive data of RAW format. It can be used for ToF/3D camera modules but cannot be used for display.
CSI3_CLK_P	J1-87	AI	MIPI clock of camera 3 (+)	
CSI3_LN0_N	J1-81	AI	MIPI lane 0 data of camera 3 (-)	
CSI3_LN0_P	J1-79	AI	MIPI lane 0 data of camera 3 (+)	
CSI3_LN1_N	J1-73	AI	MIPI lane 1 data of camera 3 (-)	
CSI3_LN1_P	J1-75	AI	MIPI lane 1 data of camera 3 (+)	

CAM0_MCLK	J1-91	DO	Master clock of camera 0		
CAM1_MCLK	J1-95	DO	Master clock of camera 1		
CAM2_MCLK	J1-99	DO	Master clock of camera 2		
CAM3_MCLK	J1-103	DO	Master clock of camera 3		
CAM0_STROBE	J1-122	DO	Strobe of camera 0		
CAM1_STROBE	J1-116	DO	Strobe of camera 1		
CAM2_STROBE	J1-118	DO	Strobe of camera 2		
CAM0_RST	J1-100	DO	Reset of camera 0		
CAM1_RST	J1-96	DO	Reset of camera 1		
CAM2_RST	J1-124	DO	Reset of camera 2		
CAM3_RST	J1-126	DO	Reset of camera 3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
CAM0_PWDN	J1-114	DO	Power down of camera 0		
CAM1_PWDN	J1-120	DO	Power down of camera 1		
CAM2_PWDN	J1-106	DO	Power down of camera 2		
CAM3_PWDN	J1-112	DO	Power down of camera 3		
CAM0_AVDD_EN	J1-102	DO	AVDD enable of camera 0		
CAM1_AVDD_EN	J1-98	DO	AVDD enable of camera 1		
CAM2_AVDD_EN	J1-104	DO	AVDD enable of camera 2		
CAM3_AVDD_EN	J1-108	DO	AVDD enable of camera 3		
CAM0_DVDD_EN	J1-132	DO	DVDD enable of camera 0		
CAM1_DVDD_EN	J1-130	DO	DVDD enable of camera 1		

CAM2_DVDD_EN	J1-110	DO	DVDD enable of camera 2		
CAM3_DVDD_EN	J1-128	DO	DVDD enable of camera 3		
CCI0_I2C_SCL	J1-142	OD	CCI0 I2C clock		1.8 V power domain.
CCI0_I2C_SDA	J1-144	OD	CCI0 I2C data		
CCI1_I2C_SDA	J1-146	OD	CCI1 I2C data		
CCI1_I2C_SCL	J1-148	OD	CC1 I2C clock		
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	J2-5	DI	Turns on/off the module	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Pulled up to 1.8 V internally. Active low.
VOL_UP	J2-9	DI	Volume up		If unused, keep this pin open.
VOL_DOWN	J2-7	DI	Volume down		If unused, keep this pin open.
HOME_KEY	J2-145	DI	Home key		If unused, keep this pin open.
Sensor Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SSC_I2C1_SDA	J2-8	OD	Sensor core I2C1 data		1.8 V power domain.
SSC_I2C1_SCL	J2-10	OD	Sensor core I2C1 clock		
SSC_SPI1_CS0	J1-136	DO	Sensor core SPI1 chip select 0	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SSC_SPI1_CS1	J1-138	DO	Sensor core SPI1 chip select 1		
SSC_SPI1_CS2	J1-140	DO	Sensor core SPI1 chip select 2		
SSC_SPI1_CLK	J1-154	DO	Sensor core SPI1 clock		

SSC_SPI1_MOSI	J1-152	DO	Sensor core SPI1 master-out slave-in		
SSC_SPI1_MISO	J1-150	DI	Sensor core SPI1 master-in salve-out	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
SSC_SPI2_CS	J1-141	DO	Sensor core SPI2 chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SSC_SPI2_CLK	J1-145	DO	Sensor core SPI2 clock		
SSC_SPI2_MOSI	J1-143	DO	Sensor core SPI2 master-out slave-in		
SSC_SPI2_MISO	J1-147	DI	Sensor core SPI2 master-in salve-out	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
MAG_INT	J1-133	DI	Magnetic sensor interrupt		
MAG_DRDY_INT	J1-135	DI	Magnetic sensor DRDY interrupt		
GYRO_INT	J1-137	DI	Gyroscopic sensor interrupt		
ACCEL_INT	J1-139	DI	Acceleration sensor interrupt		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC_PMU_GPIO8	J2-153	AI	General-purpose ADC interface		Maximum input voltage: 1.8 V.
ADC_PMU_GPIO21	J2-151	AI	General-purpose ADC interface		Maximum input voltage: 4.5 V.
Charging Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

BAT_THERM	J2-143	AI	Battery temperature detect	Internally pulled up. Supports 47 kΩ NTC by default - externally connect BAT_THERM to 47 kΩ NTC to GND. If you need to connect 10 kΩ NTC, pull up BAT_THERM to BAT_RBIAS with a 12 kΩ resistor. If unused, pull BAT_THERM down to GND with a 47 kΩ resistor.
BAT_P	J2-163	AI	Battery voltage detect (+)	Must be connected.
BAT_M	J2-165	AI	Battery voltage detect (-)	
CS_P	J2-157	AI	Current sense (+)	
CS_M	J2-159	AI	Current sense (-)	
BAT_RBIAS	J3-11	PO	Power supply for NTC pull-up circuit	If NTC = 10 kΩ, pull BAT_THERM up to BAT_RBIAS with a 12 kΩ resistor. If NTC = 47 kΩ, keep BAT_RBIAS open.
BAT_ID	J3-16	AI	Battery type detect	
SMB_USB_IN	J3-2, J3-3, J3-4, J3-5, J3-6, J3-7	PO	Power output for SMB1355 parallel charging	Parallel charging is not supported by default and if it is needed please contact Quectel Technical Support.

SMB_EN_CHG	J3-9	DO	SMB1355 parallel charging enable		If unused, keep these pins open.
SMB_STAT	J3-10	DI	SMB1355 parallel charging status indicator		
SMB_THERM	J3-17	AI	SMB1355 parallel charging temperature detect		
SMB_CS_P	J3-15	AI	SMB1355 parallel charging current sense (+)		
SMB_CS_M	J3-14	AI	SMB1355 parallel charging current sense (-)		
Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CODEC_RST	J2-90	DO	Codec reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
CODEC_INT1	J2-91	DI	Codec interrupt 1	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
CODEC_INT2	J2-93	DI	Codec interrupt 2		
CODEC_SPI_CS	J2-96	DO	SPI chip select for codec	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
CODEC_SPI_CLK	J2-92	DO	SPI clock for codec		
CODEC_SPI_MOSI	J2-94	DO	SPI master-out slave-in for codec		
CODEC_SPI_MISO	J2-89	DI	SPI master-in salve-out for codec	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
WCD_CLK	J2-43	DO	WCD clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SLIMBUS_CLK	J2-51	DO	SLIMbus clock		
SLIMBUS_DATA0	J2-47	DIO	SLIMbus data bit 0	V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SLIMBUS_DATA1	J2-49	DIO	SLIMbus data bit 1		

I2S1_WS	J2-79	DO	I2S1 word select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2S1_MCLK	J2-81	DO	I2S1 master clock		
I2S1_SCK	J2-83	DO	I2S1 bit clock		
I2S1_DATA0	J2-87	DIO	I2S1 data channel 0	V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2S1_DATA1	J2-85	DIO	I2S1 data channel 1		
I2S2_WS	J2-55	DO	I2S2 word select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2S2_SCK	J2-57	DO	I2S2 bit clock		
I2S2_DATA0	J2-59	DIO	I2S2 data channel 0	V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2S2_DATA1	J2-61	DIO	I2S2 data channel 1		
I2S3_WS	J2-63	DO	I2S3 word select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2S3_SCK	J2-73	DO	I2S3 bit clock		
I2S3_DATA0	J2-69	DIO	I2S3 data channel 0	V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2S3_DATA1	J2-65	DIO	I2S3 data channel 1		
I2S3_DATA2	J2-67	DIO	I2S3 data channel 2		
I2S3_DATA3	J2-71	DIO	I2S3 data channel 3		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_25	J2-2	DIO	General-purpose input/output	V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
GPIO_42	J2-64	DIO	General-purpose input/output		
GPIO_44	J2-66	DIO	General-purpose input/output		
GPIO_49	J2-78	DIO	General-purpose input/output		
GPIO_50	J2-70	DIO	General-purpose input/output		

GPIO_52	J2-68	DIO	General-purpose input/output		
GPIO_122	J2-74	DIO	General-purpose input/output		
GPIO_124	J2-76	DIO	General-purpose input/output		
GPIO_128	J2-132	DIO	General-purpose input/output		
GPIO_129	J2-136	DIO	General-purpose input/output		
GPIO_134	J2-72	DIO	General-purpose input/output		
GPIO_135	J2-134	DIO	General-purpose input/output		
SPI Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI2_CLK	J2-52	DO	SPI2 clock		
SPI2_CS	J2-54	DO	SPI2 chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI2_MOSI	J2-58	DO	SPI2 master-out slave-in		
SPI2_MISO	J2-56	DI	SPI2 master-in salve-out	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
SPI0_CLK	J2-86	DO	SPI0 clock		
SPI0_CS	J2-80	DO	SPI0 chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
SPI0_MOSI	J2-82	DO	SPI0 master-out slave-in		
SPI0_MISO	J2-84	DI	SPI0 master-in salve-out	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
SPI11_CLK	J2-99	DO	SPI11 clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI11_CS	J2-101	DO	SPI11 chip select		
SPI11_MISO	J2-97	DI	SPI11 master-in salve-out	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
SPI11_MOSI	J2-95	DO	SPI11 master-out slave-in	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
RGB interfaces					

R_LED	J2-152	AO	Current source for red LED		
G_LED	J2-156	AO	Current source for green LED		
B_LED	J2-154	AO	Current source for blue LED		
DisplayPort Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
EDP_AUX_P	J2-129	AIO	DisplayPort auxiliary channel (+)		
EDP_AUX_N	J2-131	AIO	DisplayPort auxiliary channel (-)		
SBU_SW_OE	J2-1	DO	DisplayPort auxiliary channel switch output enable	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
SBU_SW_SEL	J2-3	DO	DisplayPort auxiliary channel switch select		
Vibrator Drive Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
HAP_PWM_IN	J3-18	DI	Haptic PWM input		
HAP_P	J3-20	AO	Haptic driver output (+)		
HAP_M	J3-19	AO	Haptic driver output (-)		
UFS Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UFS_DET	J1-43	DI	UFS card hot-plug detect		UFS is not supported by default.
UFS_CLK	J1-39	DO	UFS card clock		
UFS_TX_P	J1-33	AO	UFS card transmit (+)		
UFS_TX_M	J1-35	AO	UFS card transmit (-)		

UFS_RX_P	J1-29	AI	UFS card receive (+)		
UFS_RX_M	J1-27	AI	UFS card receive (-)		
PWM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWM_PMI_GPIO5	J2-146	DO	PWM output		1.8 V power domain.
PWM_PMI_GPIO8	J2-144	DO	PWM output		
Flashlight Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
FLASH_LED1	J4-23, J4-24	AO	Flash/torch driver output 1	I_{LED1} = 1.5 A	Support flash and torch modes.
FLASH_LED2	J4-20, J4-21	AO	Flash/torch driver output 2	I_{LED2} = 1.5 A	
FLASH_LED3	J4-5, J4-6	AO	Flash/torch driver output 3	I_{LED3} = 0.75 A	
VRTC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VRTC	J2-133	PI/PO	Power supply for RTC	Vnom = 3.2 V V_I = 2.5–3.2 V	
Emergency Download Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	J2-130	DI	Forces the module into emergency download mode		Pulling it up to VREG_S4A_1V8 during power-up will force the module to enter emergency download mode.
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C4_SDA	J2-4	OD	I2C4 data		1.8 V power domain.
I2C4_SCL	J2-6	OD	I2C4 clock		

I2C10_SCL	J2-75	OD	I2C10 clock		
I2C10_SDA	J2-77	OD	I2C10 data		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VCONN_EN	J3-30	DO	VCONN enable		
VCONN	J3-29	PI	Power supply for active cables		
CBL_PWR_N	J1-134	DI	Initiates power-on when grounded.		
DBG_TXD	J2-137	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
DBG_RXD	J2-135	DI	Debug UART receive	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
PMU_GPIO10	J2-147	DIO	General-purpose input/output	V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PMU_GPIO13	J2-149	DIO	General-purpose input/output		
Reserved Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	J2-88, J2-138, J3-22, J3-23, J3-24, J3-25, J3-26, J3-27, J4-1				Keep these pins open.

3.4. Power Supply

3.4.1. Power Supply Pins

SA800U-WF provides 10 VBAT pins, which are dedicated for connection with external power supply.

3.4.2. Decrease Voltage Drop

The power supply range of the module is from 3.55 V to 4.4 V, and the recommended value is 3.8 V. The power supply performance, such as load capacity, voltage ripple, etc. directly influences the module's performance and stability. Under ultimate conditions, the module may have a transient peak current up to 3 A. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.1 V, the module will be powered off automatically. Therefore, make sure the input voltage will never drop below 3.1 V.

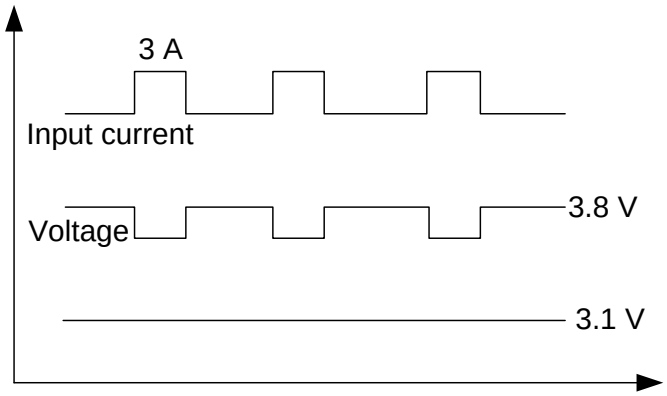


Figure 3: Voltage Drop Sample

To decrease voltage drop, a bypass capacitor of about 100 µF with low ESR (ESR = 0.7 Ω) should be used for the VBAT inputs, and a multi-layer ceramic chip capacitor (MLCC) array should also be used due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) to form the MLCC array, and place these capacitors close to the VBAT pins. The width of VBAT traces should be no less than 3 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, in order to get a stable power source, it is suggested to use a 2000 W TVS and place it as close to the VBAT pins as possible to increase voltage surge withstand capability.

The following figure shows the structure of the power supply.

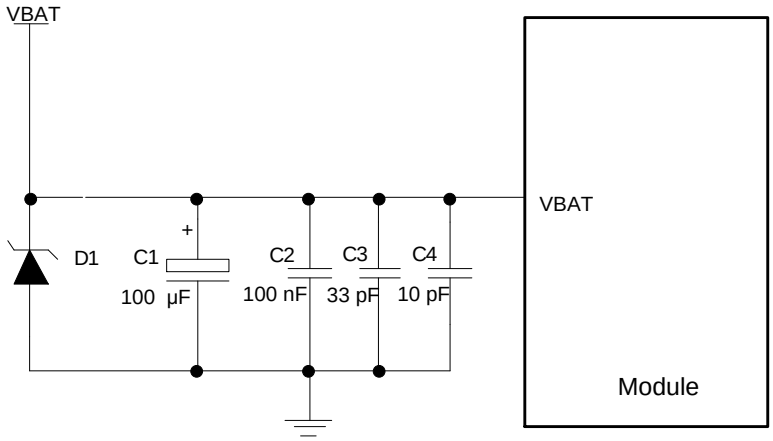


Figure 4: Star Structure of Power Supply

3.4.3. Reference Design for Power Supply

The power design for the module is important, as the performance of module largely depends on the power source. The power supply of SA800U-WF should be able to provide sufficient current of at least 3 A. By default, it is recommended to use a battery to supply power for the module. If battery is not used, it is recommended to use a regulator for the module. If the voltage difference between the input and output is not too high, it is suggested to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +12 V input power source which adopts a buck converter (TPS54428DDAR) from TI. The typical output voltage is 3.8 V and the maximum rated current is 5.3 A.

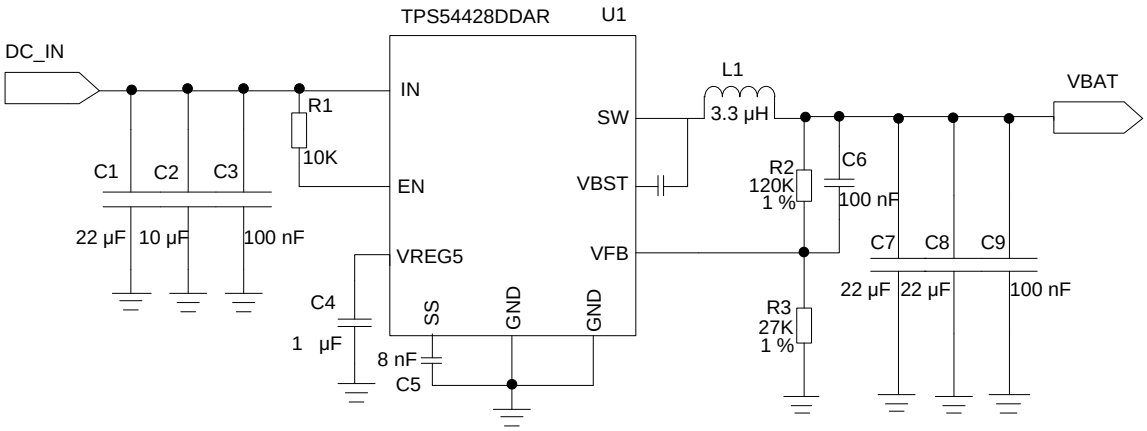


Figure 5: Reference Circuit of Power Supply

NOTES

1. It is recommended to switch off the power supply for the module in abnormal condition, and then switch on the power to restart the module.
2. The module supports battery charging function by default. If battery is not used and the above power supply design is adopted, make sure the charging function is disabled by software, or connect a Schottky diode with higher than 5 A average current capacity between the output of the inductor L1 and the VBAT pins of the module.
3. When the battery voltage is below 3.1 V, the system will trigger automatic shutdown, so the design of power supply should be consistent with the configuration of fuel gauge driver.

3.5. Turn on and off Scenarios

3.5.1. Turn on the Module Using PWRKEY

The module can be turned on by driving PWRKEY low for at least 1.6 s. PWRKEY is pulled up to 1.8 V internally. It is recommended to use an open drain/collector driver to control PWRKEY. A simple reference circuit is illustrated in the following figure.

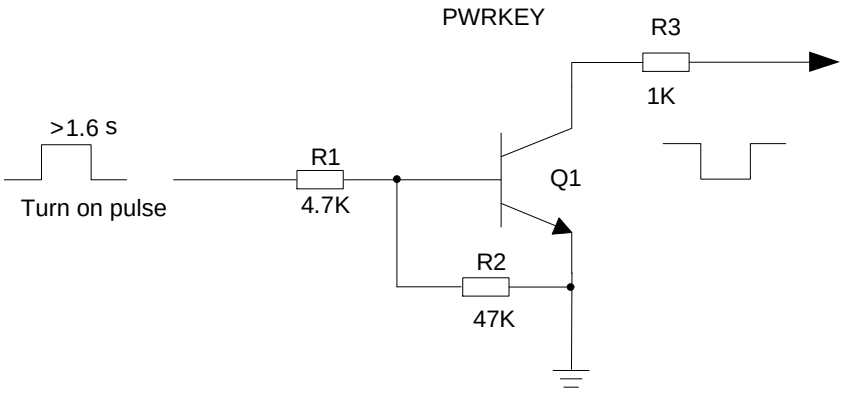


Figure 6: Turn on the Module Using Driving Circuit

Another way to control PWRKEY is using a button directly. A TVS component should be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

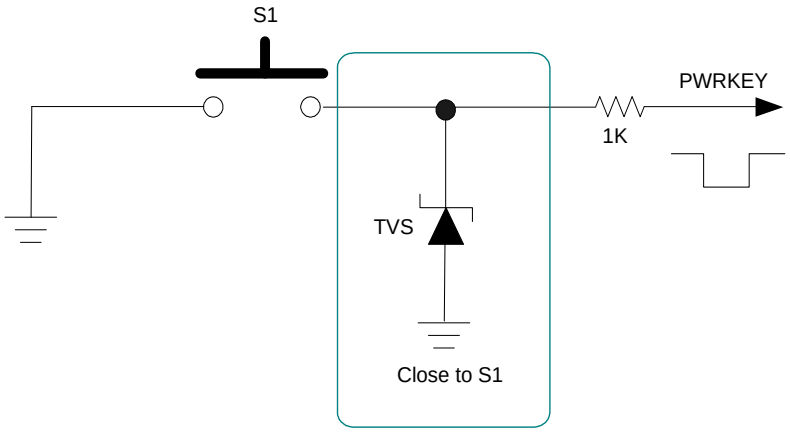


Figure 7: Turn on the Module Using Keystroke

The timing of turning on is illustrated in the following figure.

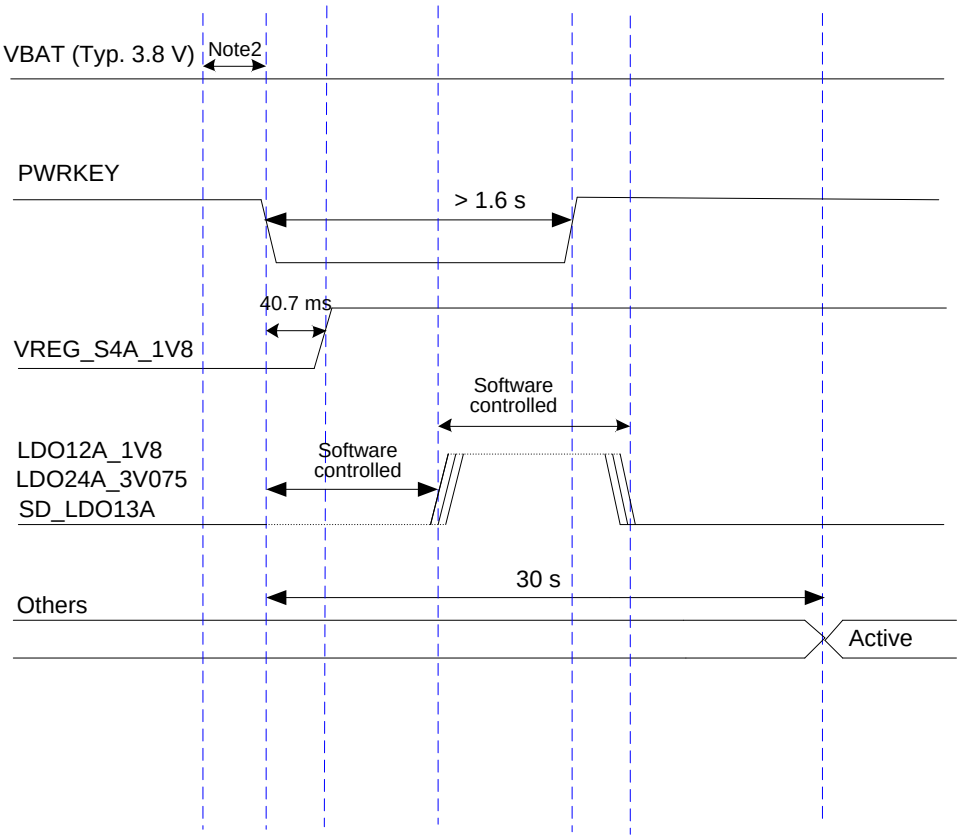


Figure 8: Timing of Turning on the Module

NOTES

1. The turn-on timing might be different from the above figure when the module powers on for the first time.
2. Make sure that VBAT is stable before pulling down PWRKEY. It is recommended to wait until VBAT to be stable for at least 30 ms before pulling down PWRKEY. Additionally, PWRKEY cannot be pulled down all the time.

3.5.2. Turn on the Module Automatically Using CBL_PWR_N

The module can be turned on automatically by driving the CBL_PWR_N pin to GND through a 1 kΩ resistor. CBL_PWR_N pin is pulled up internally. A simple reference circuit is illustrated in the following figure.

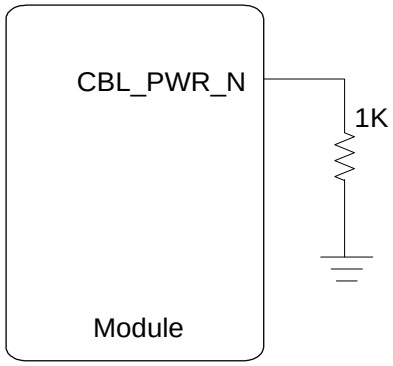


Figure 9: Turn on the Module Using CBL_PWR_N

NOTE

The module can be turned on automatically by driving CBL_PWR_N pin to GND, and cannot be turned off manually unless you shut down the VBAT.

3.5.3. Turn off/Restart the Module

Pull down PWRKEY for at least 1 s, and then choose to turn off the module when a prompt window comes up.

Another way to restart the module is to drive PWRKEY low for at least 8 s. The module will execute forced restart. The forced restart timing is illustrated in the following figure.

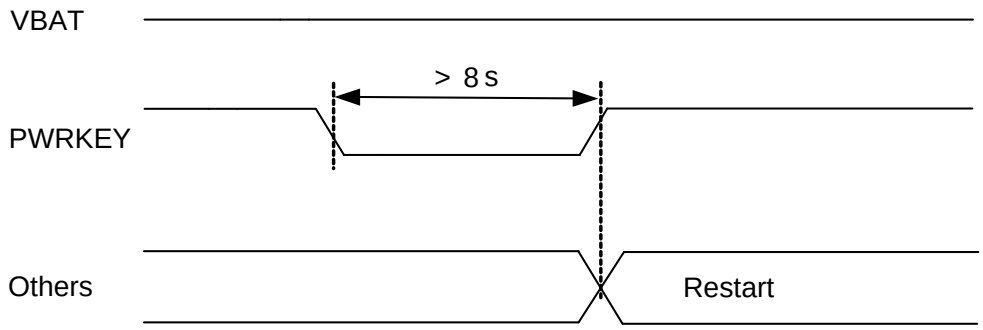


Figure 10: Timing of Restarting the Module

3.6. VRTC Interface

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supply for the VBAT. The external power source can be a rechargeable battery (such as coin cell) according to application demands. The following reference circuit design shows a design where an external battery is utilized to power RTC.

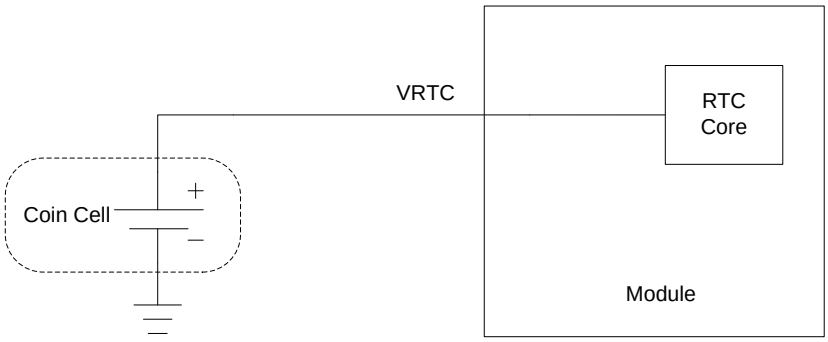


Figure 11: RTC Powered by Coin Cell

If RTC is ineffective, it can be synchronized through network after the module is powered on.

- 2.5–3.2 V input voltage range and 3.2 V typical value for VRTC, when VBAT is disconnected.
- When powered by VBAT, the RTC error is 50 ppm. When powered by VRTC, the RTC error is about 200 ppm.
- If rechargeable battery is used, the ESR of battery should be less than 2 kΩ, and it is recommended to use the MS621FE-FL11E of SEIKO.

3.7. Power Output

SA800U-WF supports output of regulated voltages for peripheral circuits. During application, it is recommended to use parallel capacitors (33 pF and 10 pF) in the circuit to suppress high-frequency noise.

Table 5: Power Description

Pin Name	Default Voltage (V)	Drive Current (mA)	Comment
VREG_S4A_1V8	1.8	2000	Keep
LVS1A_1V8	1.8	300	-
LVS2A_1V8	1.8	100	Keep
LDO12A_1V8	1.8	300	-
SD_LDO13A	1.8/2.95	50	-
LDO14A_1V88	1.8	50	-
LDO19A_3V0	3.0	600	-
SD_LDO21A	2.95	800	-
LDO24A_3V075	3.075	150	-
LDO28A_3V0	3.0	150	-
VREG_BOB	3.7	2000	Keep

3.8. Battery Charging and Management

SA800U-WF supports a fully programmable switch-mode Li-ion battery charging function. It can charge single-cell Li-ion and Li-polymer batteries. It supports QC 3.0 and QC 4.0 and the maximum charging current is up to 4.5 A. The battery charger of SA800U-WF supports trickle charging, pre-charge, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion and Li-polymer batteries.

- **Trickle charging:** When the battery voltage is below 2.1 V, a 45 mA trickle charging current is applied to the battery.
- **Pre-charge:** When the battery voltage is charged up and is between 2.1 V and 3.0 V (the maximum pre-charge voltage is 2.1–3.0 V programmable, 3.0 V by default), the system will enter the pre-charge mode. The charging current is 500 mA (0–1575 mA programmable).
- **Constant current mode (CC mode):** When the battery voltage is between the maximum pre-charge voltage and 4.35 V (3.0–4.35 V programmable, 4.35 V by default), the system will switch to CC mode. The charging current is programmable from 300–4500 mA. The default charging current is 500 mA for USB charging and 4000 mA for adapter.
- **Constant voltage mode (CV mode):** When the battery voltage reaches the final value 4.35 V, the system will switch to CV mode and the charging current will decrease gradually. When the charging current reduces to about 100 mA, the charging is completed.

Table 6: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	J2-160, J2-162, J2-164, J2-166, J2-168, J4-13, J4-14, J4-15, J4-16, J4-17, J4-18	PI/PO	Charging power input. Power output for OTG device. USB/adaptor insertion detect.	Vmax = 14 V Vmin = 4.0 V Vnom = 5.0 V
VBAT	J1-159, J1-160, J1-161, J1-162, J1-163, J1-164, J1-165, J1-166, J1-167, J1-168	PI/PO	Power supply for the module	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V
BAT_THERM	J2-143	AI	Battery temperature detect	Internally pulled up. Supports 47 kΩ NTC by default - externally connect BAT_THERM to 47 kΩ NTC to GND. If you need to connect 10 kΩ NTC, pull up

				BAT_THERM to BAT_RBIAS with a 12 kΩ resistor. If unused, pull BAT_THERM down to GND with a 47 kΩ resistor.
BAT_P	J2-163	AI	Battery voltage detect (+)	Must be connected.
BAT_M	J2-165	AI	Battery voltage detect (-)	
CS_P	J2-157	AI	Current sense (+)	
CS_M	J2-159	AI	Current sense (-)	
BAT_RBIAS	J3-11	PO	Power supply for NTC pull-up circuit	If NTC = 10 kΩ, pull BAT_THERM up to BAT_RBIAS with a 12 kΩ resistor. If NTC = 47 kΩ, keep BAT_RBIAS open.
BAT_ID	J3-16	AI	Battery type detect	
SMB_USB_IN	J3-2, J3-3, J3-4, J3-5, J3-6, J3-7	PO	Power output for SMB1355 parallel charging	Parallel charging is not supported by default and if it is needed please contact Quectel Technical Support. If unused, keep these pins open.
SMB_CS_P	J3-15	AI	SMB1355 parallel charging current sense (+)	
SMB_CS_M	J3-14	AI	SMB1355 parallel charging current sense (-)	
SMB_THERM	J3-17	AI	SMB1355 parallel charging temperature detect	
SMB_EN_CHG	J3-9	DO	SMB1355 parallel charging enable	
SMB_STAT	J3-10	DI	SMB1355 parallel charging status indicator	

SA800U-WF supports battery temperature detection in the condition that the battery integrates a thermistor (47 kΩ 1 % NTC thermistor with B-constant of 4050 K by default; SDNT1608X473F4050FTF of SUNLORD is recommended) and the thermistor is connected to the BAT_THERM pin. If BAT_THERM is not connected, there will be malfunctions such as boot error, battery charging failure, battery level display error, etc.

A reference design for battery charging circuit is shown below.

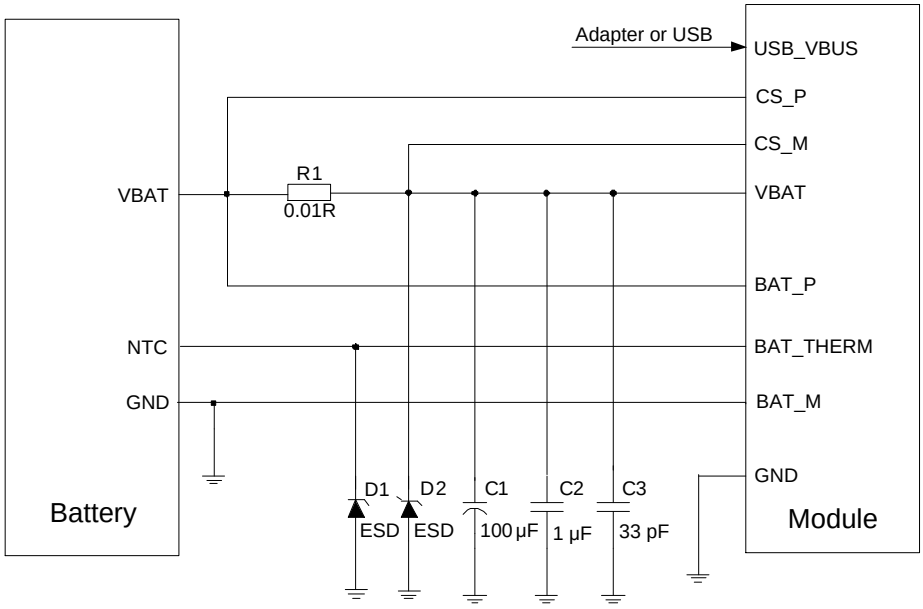


Figure 12: Reference Design for Battery Charging Circuit

SA800U-WF offers a fuel gauge algorithm which is able to accurately estimate the battery's health state by current and voltage monitoring techniques. Using precise measurements of battery voltage, current, and temperature, the fuel gauge provides a dependable state of charge estimate throughout the entire life of the battery and across a broad range of operating conditions. It effectively protects the battery from over-discharging, and also allows you to estimate the battery life based on the battery level to timely save important data before complete power-down.

Mobile devices such as mobile phone and game machine systems are powered by batteries. When different batteries are used, the charging and discharging curve has to be modified according to the battery type to achieve the best performance.

If thermistor is not available in the battery, or an adapter rather than a battery is used to power the module, BAT_THERM should be connected to GND with a 47 kΩ resistor. Otherwise the system may be unable to detect the battery, which will cause power-on failure. BAT_P and BAT_M must be connected, and also CS_P and CS_M must be connected, otherwise there may be abnormalities in using the module. BAT_P and BAT_M are used for battery level detection, and they should be routed as a differential pair to ensure accuracy. CS_P and CS_M are used for charging current sensing, and they should be routed as a differential pair to ensure accuracy.

3.9. USB Interfaces

SA800U-WF provides two USB interfaces which comply with both USB 3.1 and USB 2.0 specifications and support super speed (5 Gbps) on USB 3.1, high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0. USB1 can be used for AT command transmission, data transmission, software debugging and firmware upgrade. USB2 only supports host mode.

3.9.1. USB1 Interface

3.9.1.1. USB Type-C Mode

The USB1 interface has one USB 2.0 compliant high-speed differential channel (USB1_DP, USB1_DM) and two USB 3.1 compliant super-speed differential channels (USB1_SS1_RX_P/M, USB1_SS1_TX_P/M and USB1_SS2_RX_P/M, USB1_SS2_TX_P/M).

When Type-C is plugged in with one side up, USB_CC1 will detect the external device, and the data will be transmitted through USB_SS1; when it is plugged in with the other side up, USB_CC2 will detect the external device, and the data will be transmitted through USB_SS2. The following table shows the pin definition of USB Type-C interface.

The following table shows the pin definition of USB1 interface.

Table 7: Pin Definition of USB TYPE-C Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	J2-160, J2-162, J2-164, J2-166, J2-168, J4-13, J4-14, J4-15, J4-16, J4-17, J4-18	PI/PO	Charging power input. Power output for OTG device. USB/adaptor insertion detect.	Vmax = 14 V Vmin = 4.0 V Vnom = 5.0 V
USB1_DM	J2-117	AIO	USB1 2.0 differential data (-)	90 Ω differential impedance. USB 2.0 standard compliant.
USB1_DP	J2-119	AIO	USB1 2.0 differential data (+)	
USB1_SS1_TX_M	J2-123	AO	USB1 3.1 channel 1 super-speed transmit (-)	90 Ω differential impedance. USB 3.1 standard compliant.
USB1_SS1_TX_P	J2-125	AO	USB1 3.1 channel 1 super-speed transmit (+)	
USB1_SS1_RX_M	J2-118	AI	USB1 3.1 channel 1 super-speed receive (-)	
USB1_SS1_RX_P	J2-120	AI	USB1 3.1 channel 1 super-speed receive (+)	

USB1_SS2_TX_M	J2-111	AO	USB1 3.1 channel 2 super-speed transmit (-)
USB1_SS2_TX_P	J2-113	AO	USB1 3.1 channel 2 super-speed transmit (+)
USB1_SS2_RX_M	J2-114	AI	USB1 3.1 channel 2 super-speed receive (-)
USB1_SS2_RX_P	J2-112	AI	USB1 3.1 channel 2 super-speed receive (+)
USB_CC1	J2-141	AI	USB Type-C configuration channel 1
USB_CC2	J2-139	AI	USB Type-C configuration channel 2

The following is a reference design for USB Type-C interface:

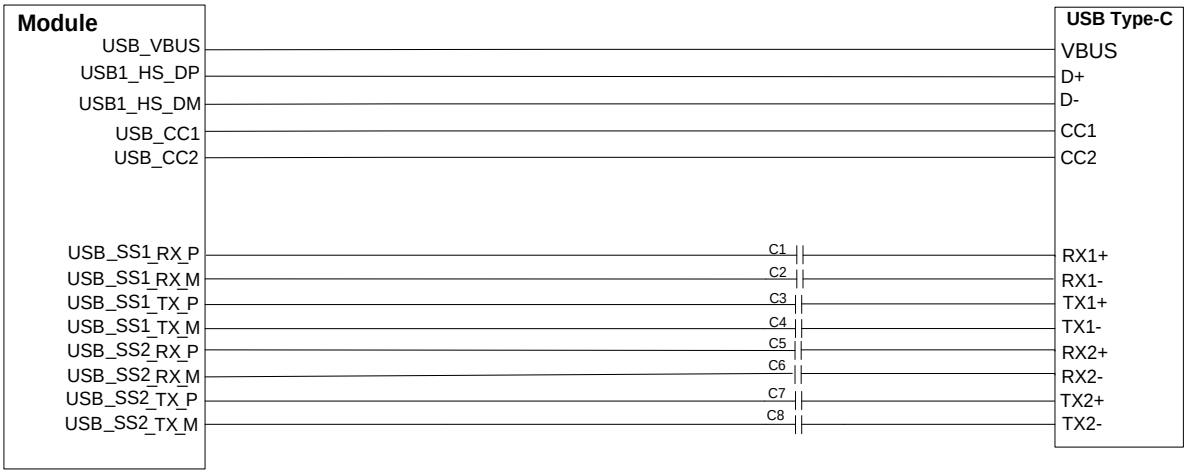


Figure 13: USB Type-C Interface Reference Design

SA800U-WF can support E-mark cable and active cable.

Table 8: Pin Definition of VCONN Circuit

Pin Name	Pin No.	I/O	Description
VCONN	J3-29	PI	Power supply for active cables
VCONN_EN	J3-30	DO	VCONN enable
SMB_USB_IN	J3-2, J3-3, J3-4, J3-5, J3-6, J3-7	PO	Power output for SMB1355 parallel charging

If you need to support E-mark cables or active cables, you need to add the following reference circuit:

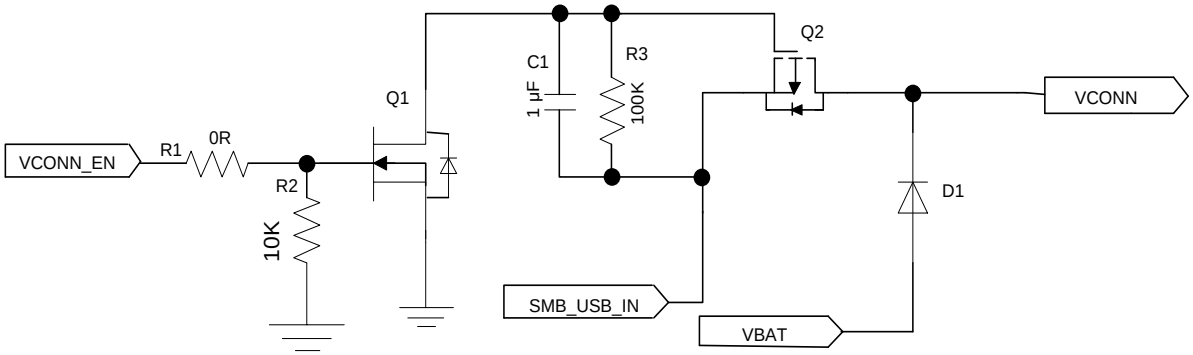


Figure 14: VCONN Reference Design

3.9.1.2. DisplayPort Mode

SA800U-WF supports DisplayPort mode with 4 lanes up to 4K @ 60 fps over USB Type-C. The pin definition of USB Type-C/DisplayPort mode is listed below:

Table 9: Pin Definition of USB Type-C/DisplayPort Mode

Pin Name	USB Type-C Mode	DisplayPort Mode
USB1_SS2_RX_P/M	USB1_SS2_RX_P/M	DP_LANE0_P/M
USB1_SS2_TX_P/M	USB1_SS2_TX_P/M	DP_LANE1_P/M
USB1_SS1_RX_P/M	USB1_SS1_RX_P/M	DP_LANE3_P/M
USB1_SS1_TX_P/M	USB1_SS1_TX_P/M	DP_LANE2_P/M
EDP_AUX_P/N	SBU1/2	DP_AUX_P/N
USB1_DP/M	USB1_DP/M	USB1_DP/M
USB_CC1/CC2	USB_CC1/CC2	HOTPLUG_DET/VCONN
USB_VBUS	USB_VBUS	USB_VBUS
GND	GND	GND

The reference design of DisplayPort is shown below:

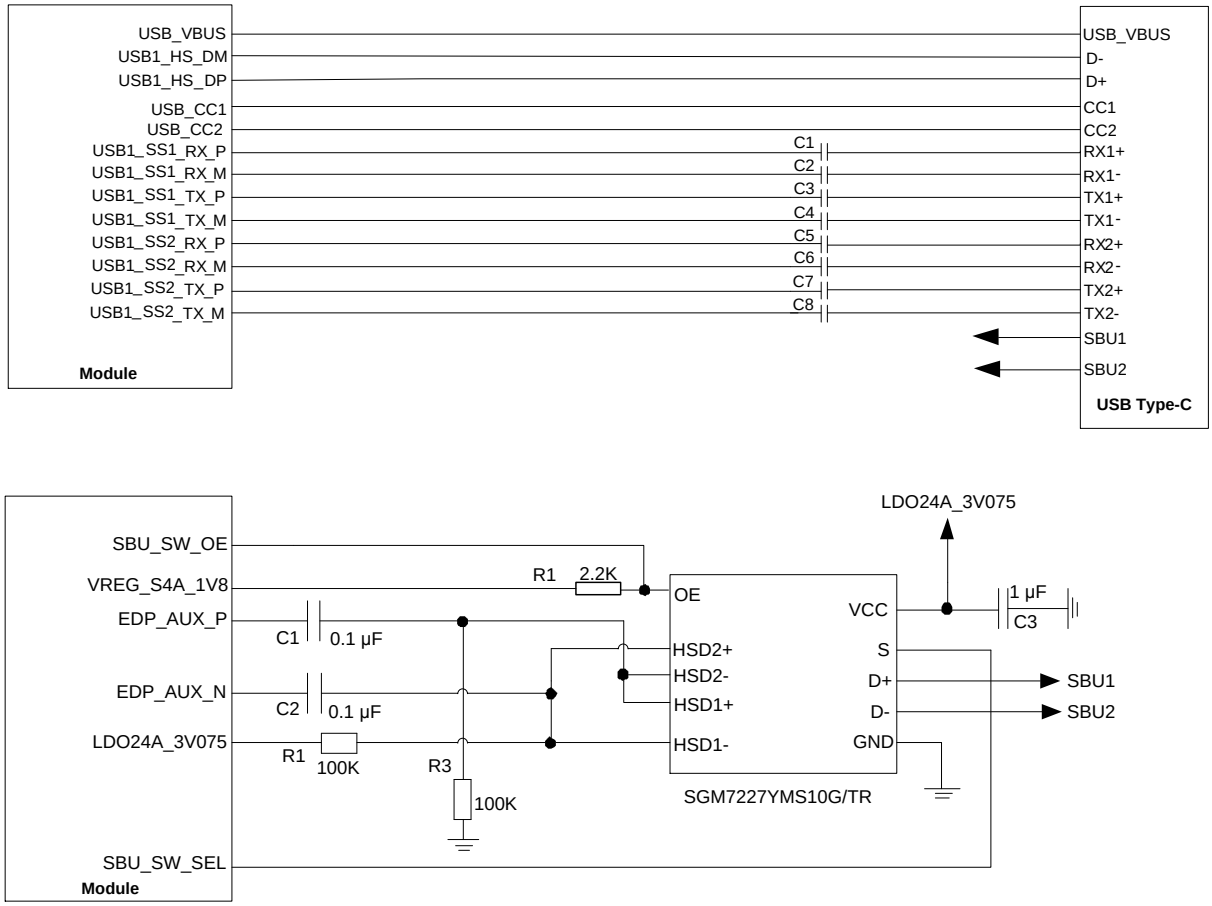


Figure 15: DisplayPort Reference Design

3.9.2. USB2 Interface

USB2 only supports host mode. The following table shows the pin definition of USB2 interface.

Table 10: Pin Definition of USB2

Pin Name	Pin No.	I/O	Description	Comment
USB2_DP	J2-105	AIO	USB2 2.0 differential data (+)	90 Ω differential impedance. USB 2.0 standard compliant. Only support host mode.
USB2_DM	J2-107	AIO	USB2 2.0 differential data (-)	
USB2_SS_TX_M	J2-108	AO	USB2 3.1 channel 1 super-speed transmit (-)	90 Ω differential impedance. USB 3.1 standard compliant. Only support host mode.
USB2_SS_TX_P	J2-106	AO	USB2 3.1 channel 1 super-speed transmit (+)	

USB2_SS_RX_M	J2-100	AI	USB2 3.1 channel 1 super-speed receive (-)
USB2_SS_RX_P	J2-102	AI	USB2 3.1 channel 1 super-speed receive (+)

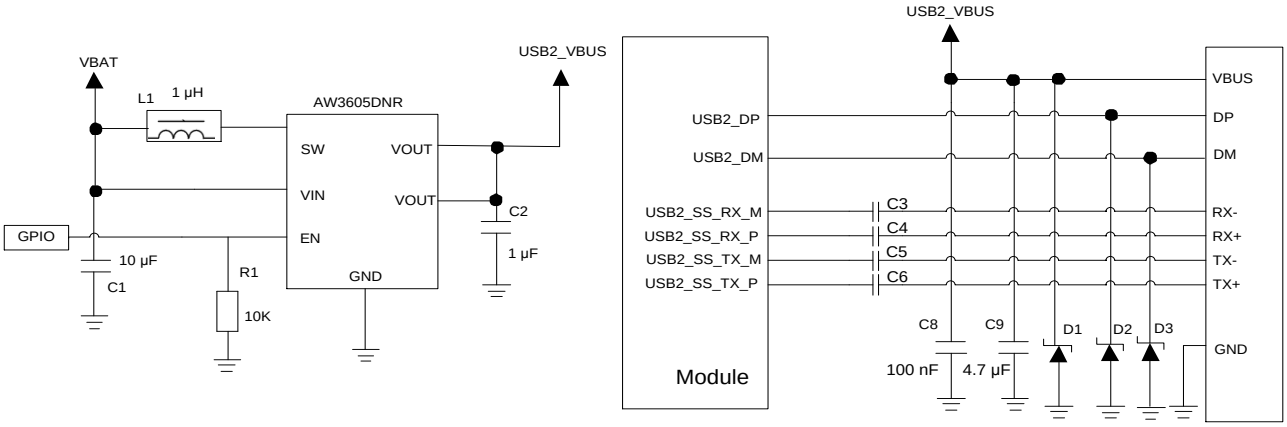


Figure 16: USB Type-A Interface Reference Design (USB2 for Host Mode)

3.9.3. Design Principles

Table 11: USB Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Length Difference (P - M)
J2-117	USB1_DM	39.59	-0.15
J2-119	USB1_DP	39.44	
J2-123	USB1_SS1_TX_M	22.37	0.90
J2-125	USB1_SS1_TX_P	23.27	
J2-118	USB1_SS1_RX_M	19.53	0.64
J2-120	USB1_SS1_RX_P	20.17	
J2-111	USB1_SS2_TX_M	19.65	0.31
J2-113	USB1_SS2_TX_P	19.96	
J2-114	USB1_SS2_RX_M	15.36	-0.50
J2-112	USB1_SS2_RX_P	14.86	

J2-131	EDP_AUX_N	26.00	-0.27
J2-129	EDP_AUX_P	25.73	
J2-107	USB2_DM	19.93	-0.03
J2-105	USB2_DP	19.90	
J2-108	USB2_SS_TX_M	15.93	-0.33
J2-106	USB2_SS_TX_P	15.60	
J2-100	USB2_SS_RX_M	11.58	0.41
J2-102	USB2_SS_RX_P	11.99	

To ensure USB performance, follow the following principles while designing USB interface.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential traces is 90 Ω.
- Pay attention to the influence of junction capacitance of ESD protection devices on USB data lines. Typically, the capacitance value should be less than 2 pF for USB 2.0 and less than 0.5 pF for USB 3.1.
- Do not route signal traces under crystal oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Do not route USB 3.1 signal lines under RF signal lines. Crossing or parallel with RF signal lines is forbidden. Isolation between USB 3.1 signals and RF signals should be more than 90 dB. Otherwise, the RF signals will be seriously affected.
- Keep the ESD protection devices as close as possible to the USB connector.
- Make sure the intra-pair length difference within USB 2.0 differential pair and that within USB 3.1 RX or TX differential pair does not exceed 0.7 mm.
- The spacing between USB signals and all other signals should be at least 4 times the trace width while that between RX and TX should be at least 3 times the trace width.
- For DisplayPort, the routing length difference between EDP_AUX_N and EDP_AUX_P should be less than 7 mm.

3.10. UART Interface

The module provides one debug UART used for debugging by default. The following table shows the pin definition of debug UART interface.

Table 12: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	J2-137	DO	Debug UART transmit	1.8 V power domain.
DBG_RXD	J2-135	DI	Debug UART receive	

Debug UART is a 2-wire UART interface of 1.8 V power domain. A level translator chip should be used if your application is equipped with a 3.3 V UART interface. The level translator chip TXS0102DCUR provided by Texas Instruments is recommended. The following figure shows a reference design.

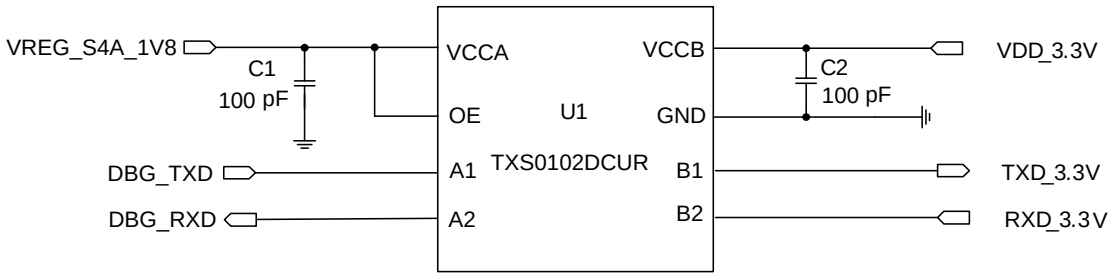


Figure 17: Reference Circuit with Level Translator Chip

The following figure is an example of connection between SA800U-WF and PC. A level translator and an RS-232 level translator chip is recommended to be added between the module and PC, as shown below.

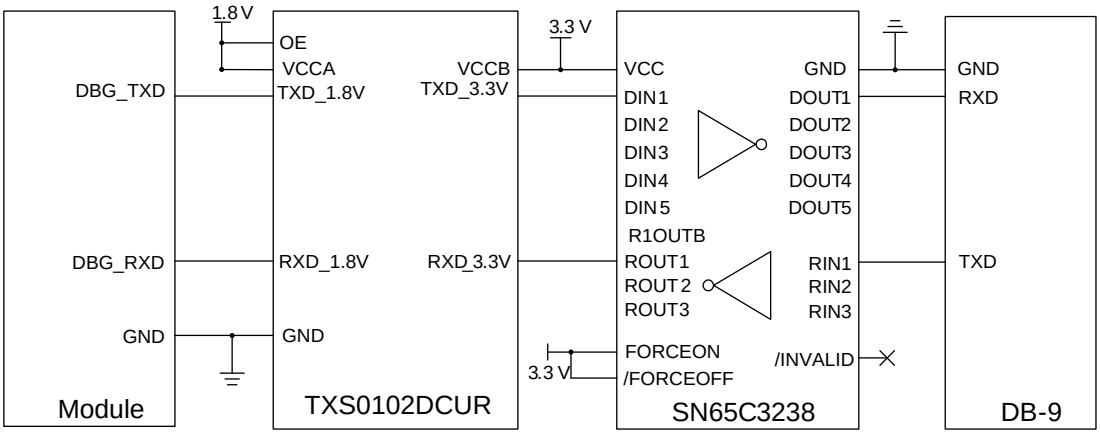


Figure 18: RS-232 Level Match Circuit

3.11. PCIe Interfaces

SA800U-WF provides two PCIe interfaces. PCIe0 is a Gen 2 1-lane interface that transmits up to 5 Gbps/lane. PCIe1 is a Gen 3 1-lane interface that transmits up to 8 Gbps/lane.

Table 13: Pin Definition of PCIe Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCIE0_RST_N	J1-1	DO	PCIe0 reset	
PCIE0_WAKE_N	J1-3	DI	PCIe0 wakes up host	
PCIE0_CLKREQ_N	J1-5	DI	PCIe0 clock request	
PCIE0_REFCLK_P	J1-15	AO	PCIe0 reference clock (+)	
PCIE0_REFCLK_M	J1-17	AO	PCIe0 reference clock (-)	
PCIE0_TX_P	J1-11	AO	PCIe0 transmit (+)	Control the characteristic impedance as 85 Ω.
PCIE0_TX_M	J1-9	AO	PCIe0 transmit (-)	
PCIE0_RX_P	J1-21	AI	PCIe0 receive (+)	
PCIE0_RX_M	J1-23	AI	PCIe0 receive (-)	
PCIE1_RST_N	J1-107	DO	PCIe1 reset	
PCIE1_WAKE_N	J1-111	DI	PCIe1 wakes up host	
PCIE1_CLKREQ_N	J1-109	DI	PCIe1 clock request	
PCIE1_REFCLK_P	J1-121	AO	PCIe1 reference clock (+)	
PCIE1_REFCLK_M	J1-123	AO	PCIe1 reference clock (-)	
PCIE1_TX_P	J1-129	AO	PCIe1 transmit (+)	Control the characteristic impedance as 85 Ω.
PCIE1_TX_M	J1-127	AO	PCIe1 transmit (-)	
PCIE1_RX_P	J1-115	AI	PCIe1 receive (+)	
PCIE1_RX_M	J1-117	AI	PCIe1 receive (-)	

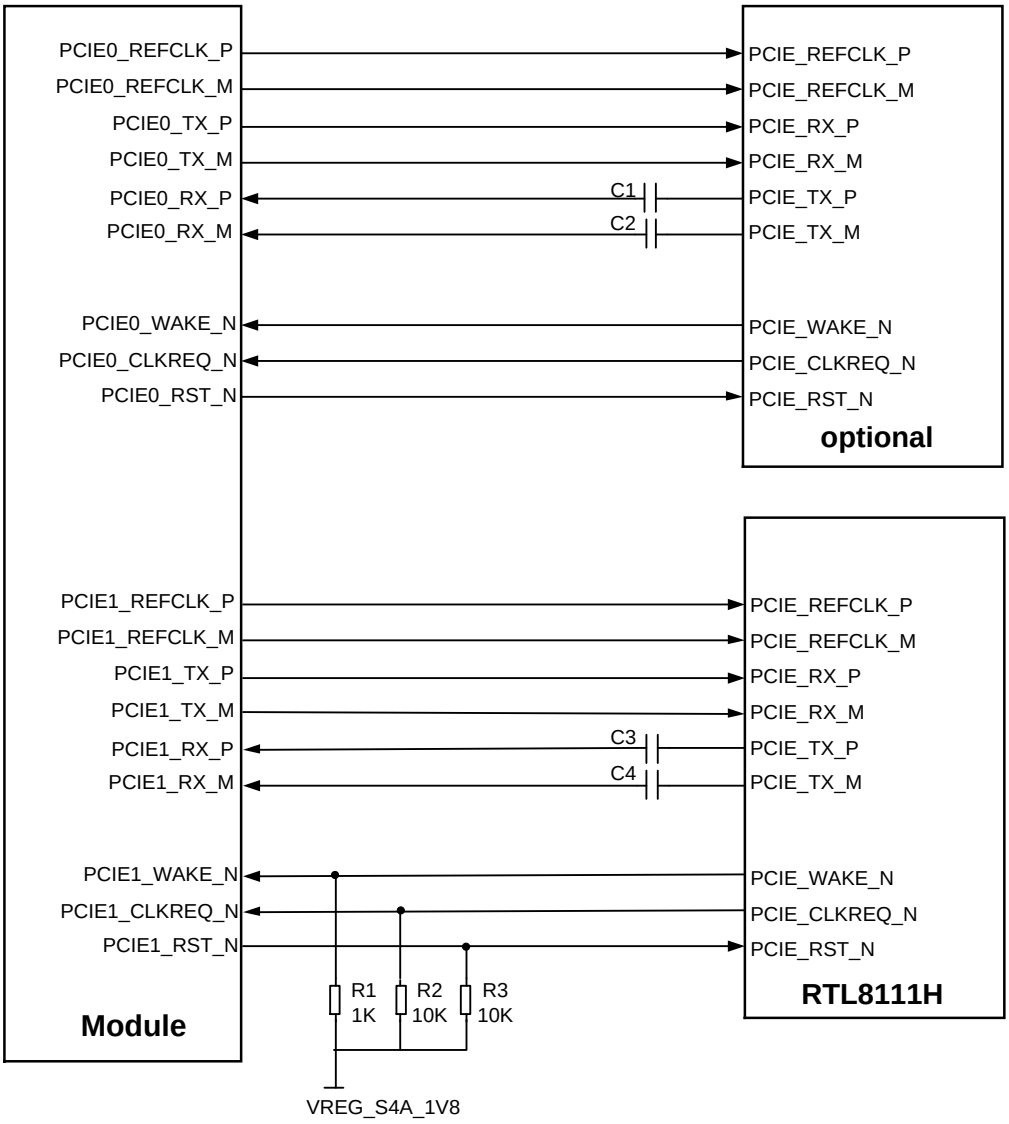


Figure 19: PCIe Interfaces Reference Circuit

To enhance the reliability and availability in applications, follow the criteria below in the circuit design of PCIe interfaces:

- Keep the PCIe signals away from noisy signals, such as clock signals, SMPS, and so forth.
- It is recommended to place the AC coupling capacitors (C1/C2/C3/C4) close to the TX side to ensure signal integrity of trace routing on PCB.
- Keep the intra-pair length difference within each differential data pair less than 0.7 mm during PCIe trace routing. Trace length matching between the reference clock, TX, and RX pairs is not required.
- Keep the impedance of PCIe differential traces as 85 Ω ±10 %.
- You must not route PCIe data traces under components or cross them with other traces.
- The spacing between PCIe signals and all other signals and that between RX and TX should be at least 4 times the trace width.

3.12. SD Card Interface

SA800U-WF supports two SDIO interfaces (SDC2 and SDC4). The SDIO function of SDC4 is not supported by default. As the SD card interface, SDC2 complies with SD 3.0 specifications. The pin definition is shown below.

Table 14: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_LDO21A	J1-151, J1-153, J1-155	PO	SD card power supply	Vnom = 2.95 V $I_O$max = 800 mA
SD_LDO13A	J4-11	PO	1.8/2.95 V output power for SD card pull-up circuits	Vnom = 1.8/2.95 V $I_O$max = 50 mA
SD_CLK	J1-45	DO	SD card clock	Control characteristic impedance as 45 Ω.
SD_CMD	J1-47	DO	SD card command	
SD_DATA0	J1-51	DIO	SDIO data bit 0	
SD_DATA1	J1-53	DIO	SDIO data bit 1	
SD_DATA2	J1-57	DIO	SDIO data bit 2	
SD_DATA3	J1-55	DIO	SDIO data bit 3	
SD_DET	J1-49	DI	SD card hot-plug detect	Active low.
SDC4_CLK	J1-86	DO	SDIO clock	SDIO function is not supported by default. Can be multiplexed into GPIOs.
SDC4_CMD	J1-92	DO	SDIO command	
SDC4_DATA0	J1-82	DIO	SDIO data bit 0	
SDC4_DATA1	J1-84	DIO	SDIO data bit 1	
SDC4_DATA2	J1-88	DIO	SDIO data bit 2	
SDC4_DATA3	J1-90	DIO	SDIO data bit 3	

A reference circuit for SD card interface is shown as below.

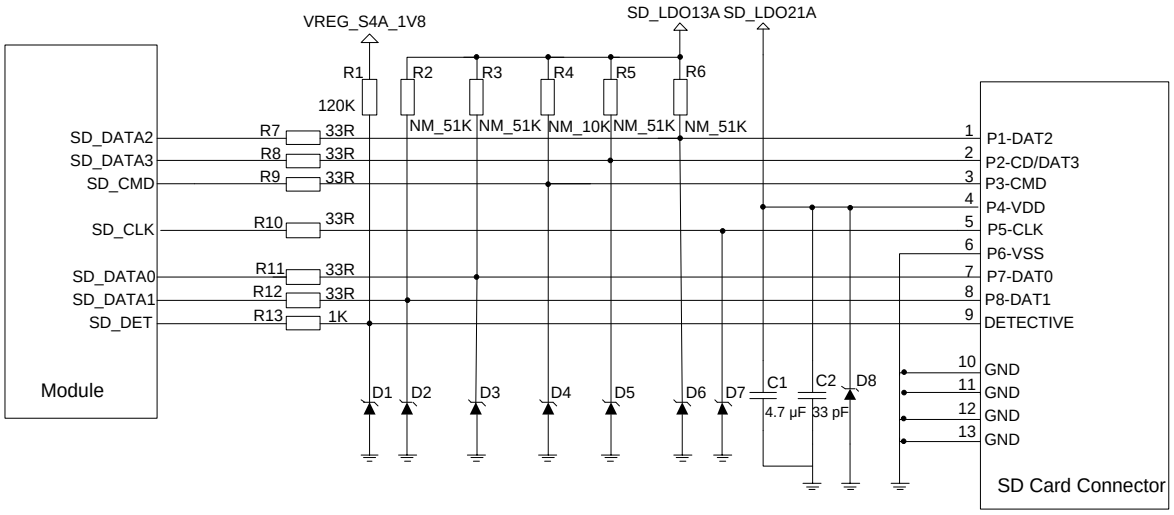


Figure 20: Reference Circuit for SD Card Interface

SD_LDO21A is a peripheral power supply driver for SD card. The maximum drive current is about 800 mA. Because of the high drive current, it is recommended that the trace width should be 0.8 mm or above. To ensure the stability of drive power, a 4.7 µF and a 33 pF capacitor should be added in parallel near the SD card connector.

SD_CMD, SD_CLK, SD_DATA0, SD_DATA1, SD_DATA2 and SD_DATA3 are all high speed signal lines. In PCB design, control the characteristic impedance of them to 45 Ω, and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB, and keep them of the same trace length. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control characteristic impedance to 45 Ω ±10 %, and add ground shielding.
- The length difference between SD_CLK and SD_DATA should be less than 2 mm.
- The spacing between SDIO signals and all other signals and that between different SDIO signals should be at least 1.5 times the trace width.
- For SDR104 mode, the total routing length recommended is less than 50 mm, and the total capacitance should be less than 5 pF
- For SDR50 and DDR50 modes, the total routing length recommended is less than 150 mm, and the total capacitance should be less than 10 pF

Table 15: SD Card Signal Trace Length Inside the Module

Pin No.	Signal	Length (mm)
J1-45	SD_CLK	16.07
J1-47	SD_CMD	14.78
J1-51	SD_DATA0	15.32
J1-53	SD_DATA1	14.61
J1-57	SD_DATA2	14.43
J1-55	SD_DATA3	14.10

3.13. GPIO Interfaces

SA800U-WF has abundant GPIO pins with power domain of 1.8 V. The pin definition is listed below.

Table 16: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GPIO_25	J2-2	DIO	General-purpose input/output	
GPIO_42	J2-64	DIO	General-purpose input/output	
GPIO_44	J2-66	DIO	General-purpose input/output	Wakeup [1)]
GPIO_49	J2-78	DIO	General-purpose input/output	Wakeup
GPIO_50	J2-70	DIO	General-purpose input/output	
GPIO_52	J2-68	DIO	General-purpose input/output	Wakeup
GPIO_122	J2-74	DIO	General-purpose input/output	Wakeup
GPIO_124	J2-76	DIO	General-purpose input/output	Wakeup
GPIO_128	J2-132	DIO	General-purpose input/output	Wakeup
GPIO_129	J2-136	DIO	General-purpose input/output	Wakeup
GPIO_134	J2-72	DIO	General-purpose input/output	

GPIO_135	J2-134	DIO	General-purpose input/output

NOTES

1. [1)] Wakeup: Interrupt pins that can wake up the system.
2. For more details about GPIO configuration, see ***document [2]***.

3.14. I2C Interfaces

SA800U-WF provides six groups of I2C interfaces. As an open drain output, each I2C interface should be pulled up to 1.8 V. CCI_I2C bus is controlled by Linux Kernel code and supports connection to video output related devices. SSC_I2C only supports connection to sensor which is dedicated to support low-power and always-on use cases.

Table 17: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
TP_I2C_SCL	J2-44	OD	TP I2C clock	Used for touch panel.
TP_I2C_SDA	J2-46	OD	TP I2C data	
I2C4_SDA	J2-4	OD	I2C4 data	
I2C4_SCL	J2-6	OD	I2C4 clock	
I2C10_SCL	J2-75	OD	I2C10 clock	
I2C10_SDA	J2-77	OD	I2C10 data	
CCI0_I2C_SCL	J1-142	OD	CCI0 I2C clock	Used for video output devices.
CCI0_I2C_SDA	J1-144	OD	CCI0 I2C data	
CCI1_I2C_SDA	J1-146	OD	CCI1 I2C data	
CCI1_I2C_SCL	J1-148	OD	CC1 I2C clock	
SSC_I2C1_SDA	J2-8	OD	Sensor core I2C1 data	Used for external sensors.
SSC_I2C1_SCL	J2-10	OD	Sensor core I2C1 clock	

3.15. SPI Interfaces

SA800U-WF provides three SPI interfaces which only support master mode.

Table 18: Pin Definition of SPI Interfaces

Pin Name	Pin No	I/O	Description	Comment
SPI2_CLK	J2-52	DO	SPI2 clock	1.8 V power domain.
SPI2_CS	J2-54	DO	SPI2 chip select	
SPI2_MISO	J2-56	DI	SPI2 master-in salve-out	
SPI2_MOSI	J2-58	DO	SPI2 master-out slave-in	
SPI0_CLK	J2-86	DO	SPI0 clock	
SPI0_CS	J2-80	DO	SPI0 chip select	
SPI0_MISO	J2-84	DI	SPI0 master-in salve-out	
SPI0_MOSI	J2-82	DO	SPI0 master-out slave-in	
SPI11_CLK	J2-99	DO	SPI11 clock	
SPI11_CS	J2-101	DO	SPI11 chip select	
SPI11_MISO	J2-97	DI	SPI11 master-in salve-out	
SPI11_MOSI	J2-95	DO	SPI11 master-out slave-in	

3.16. ADC Interfaces

SA800U-WF provides two analog-to-digital converter (ADC) interfaces, and the pin definition is shown below.

Table 19: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC_PMU_GPIO8	J2-153	AI	General-purpose ADC interface	Maximum input voltage: 1.8 V.
ADC_PMU_GPIO21	J2-151	AI	General-purpose ADC interface	Maximum input voltage: 4.5 V.

The accuracy for ADC_PMU_GPIO8 is 6 mV typically, while that for ADC_PMU_GPIO21 is 10 mV typically.

3.17. Vibrator Drive Interface

SA800U-WF supports eccentric rotating mass (ERM) motor and linear resonant actuator (LRA). The pin definition of vibrator drive interface is listed below.

Table 20: Pin Definition of Vibrator Drive Interface

Pin Name	Pin No.	I/O	Description
HAP_PWM_IN	J3-18	DI	Haptic PWM input
HAP_P	J3-20	AO	Haptic driver output (+)
HAP_M	J3-19	AO	Haptic driver output (-)

The vibrator is driven by an exclusive circuit, and a reference circuit design is shown below.

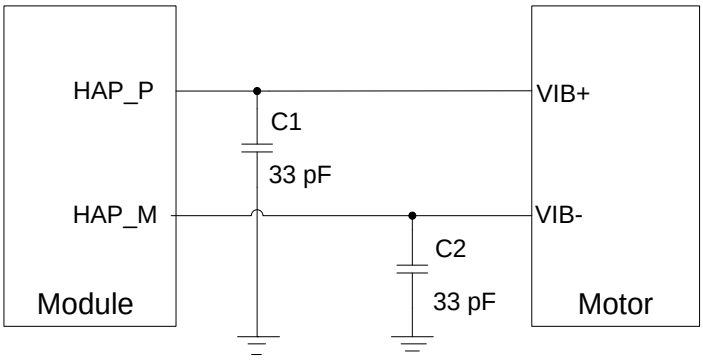


Figure 21: Reference Circuit for Vibrator Connection

3.18. LCM Interfaces

Based on MIPI DSI standard, the video output interfaces (LCM interfaces) of SA800U-WF support 2560 × 1600 @ 60 fps VESA DSC 1.1 primary display with 4 lanes. Additionally, with a MIPI to HDMI converter (LT9611 is recommended), its 8 lanes can support QUXGA display (resolution: 3840 × 2160). The module supports dual-LCD independent display: default - DSI + DP (over USB Type-C), optional - DSI0 + DSI1. Please note that DSI1 does not support screens with command mode.

Table 21: Pin Definition of LCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
LDO14A_1V88	J4-9	PO	1.8 V output for IOVDD of LCDs	Vnom = 1.8 V $I_O$max = 50 mA
LCD_RST	J2-62	DO	LCD reset	Active low. 1.8 V power domain.
LCD_TE	J2-60	DI	LCD tearing effect	1.8 V power domain.
DSI0_CLK_N	J2-26	AO	LCD0 MIPI clock (-)	100 Ω differential impedance.
DSI0_CLK_P	J2-28	AO	LCD0 MIPI clock (+)	
DSI0_LN0_N	J2-38	AO	LCD0 MIPI lane 0 data (-)	
DSI0_LN0_P	J2-40	AO	LCD0 MIPI lane 0 data (+)	
DSI0_LN1_N	J2-32	AO	LCD0 MIPI lane 1 data (-)	

DSI0_LN1_P	J2-34	AO	LCD0 MIPI lane 1 data (+)	
DSI0_LN2_N	J2-20	AO	LCD0 MIPI lane 2 data (-)	
DSI0_LN2_P	J2-22	AO	LCD0 MIPI lane 2 data (+)	
DSI0_LN3_N	J2-14	AO	LCD0 MIPI lane 3 data (-)	
DSI0_LN3_P	J2-16	AO	LCD0 MIPI lane 3 data (+)	
DSI1_CLK_N	J2-21	AO	LCD1 MIPI clock (-)	
DSI1_CLK_P	J2-19	AO	LCD1 MIPI clock (+)	
DSI1_LN0_N	J2-13	AO	LCD1 MIPI lane 0 data (-)	
DSI1_LN0_P	J2-15	AO	LCD1 MIPI lane 0 data (+)	
DSI1_LN1_N	J2-37	AO	LCD1 MIPI lane 1 data (-)	
DSI1_LN1_P	J2-39	AO	LCD10 MIPI lane 1 data (+)	
DSI1_LN2_N	J2-27	AO	LCD1 MIPI lane 2 data (-)	
DSI1_LN2_P	J2-25	AO	LCD1 MIPI lane 2 data (+)	
DSI1_LN3_N	J2-31	AO	LCD1 MIPI lane 3 data (-)	
DSI1_LN3_P	J2-33	AO	LCD1 MIPI lane 3 data (+)	
LCD_BL_A	J4-4	PO	Power output for LCD backlight	
LCD_BL_K1	J4-3	AI	Current sink 1 for LCD backlight	
LCD_BL_K2	J4-2	AI	Current sink 2 for LCD backlight	
LCD_BL_K3	J4-27	AI	Current sink 3 for LCD backlight	
LCD_BL_K4	J4-26	AI	Current sink 4 for LCD backlight	
VDISP_P	J4-29	PO	Display bias output (+)	
VDISP_M	J4-30	PO	Display bias output (-)	
PWM_PMI_GPIO5	J2-146	DO	PWM output	1.8 V power domain.
PWM_PMI_GPIO8	J2-144	DO	PWM output	

The following are the reference designs for LCM interfaces.

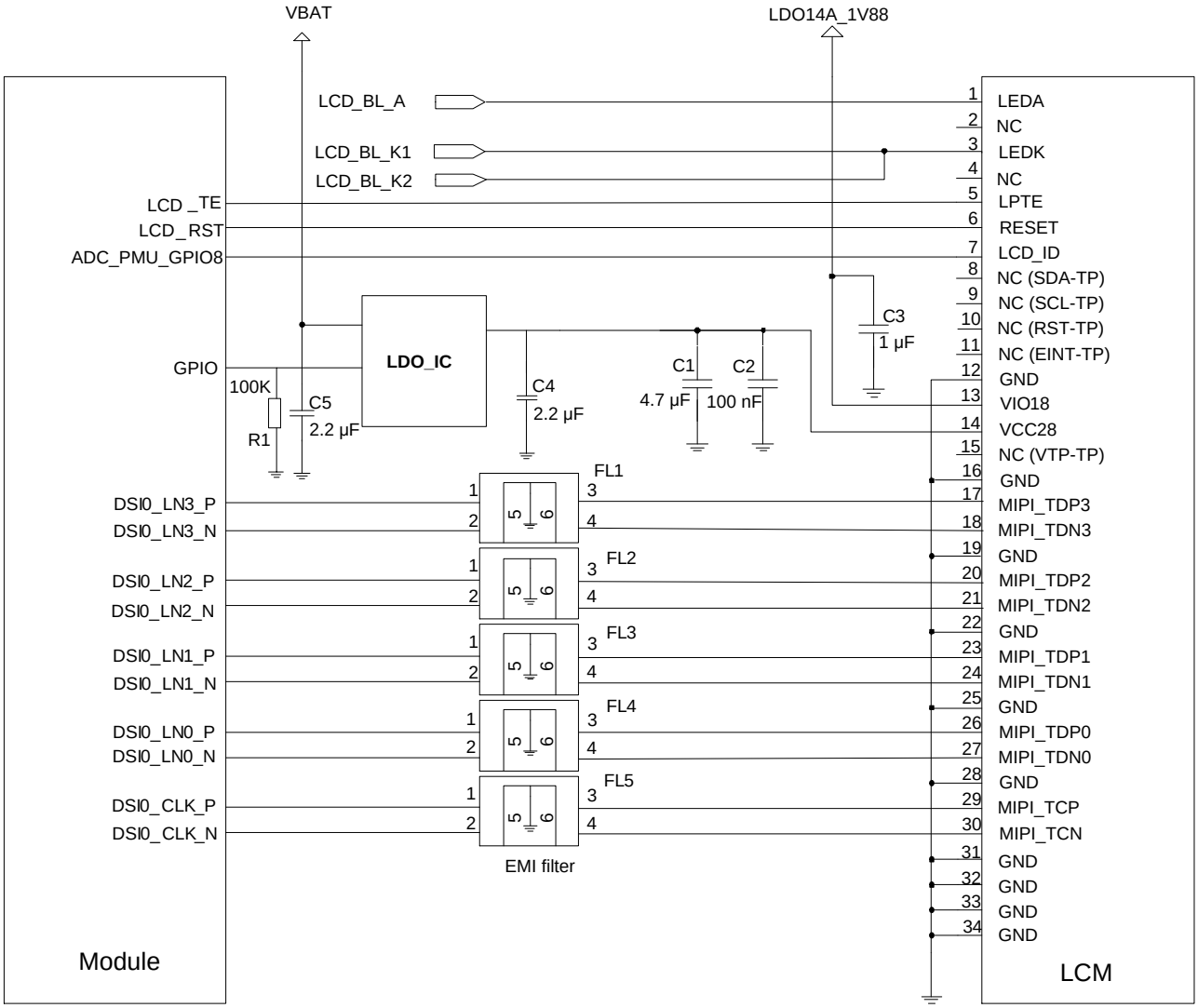


Figure 22: Reference Circuit Design for LCM0 Interface

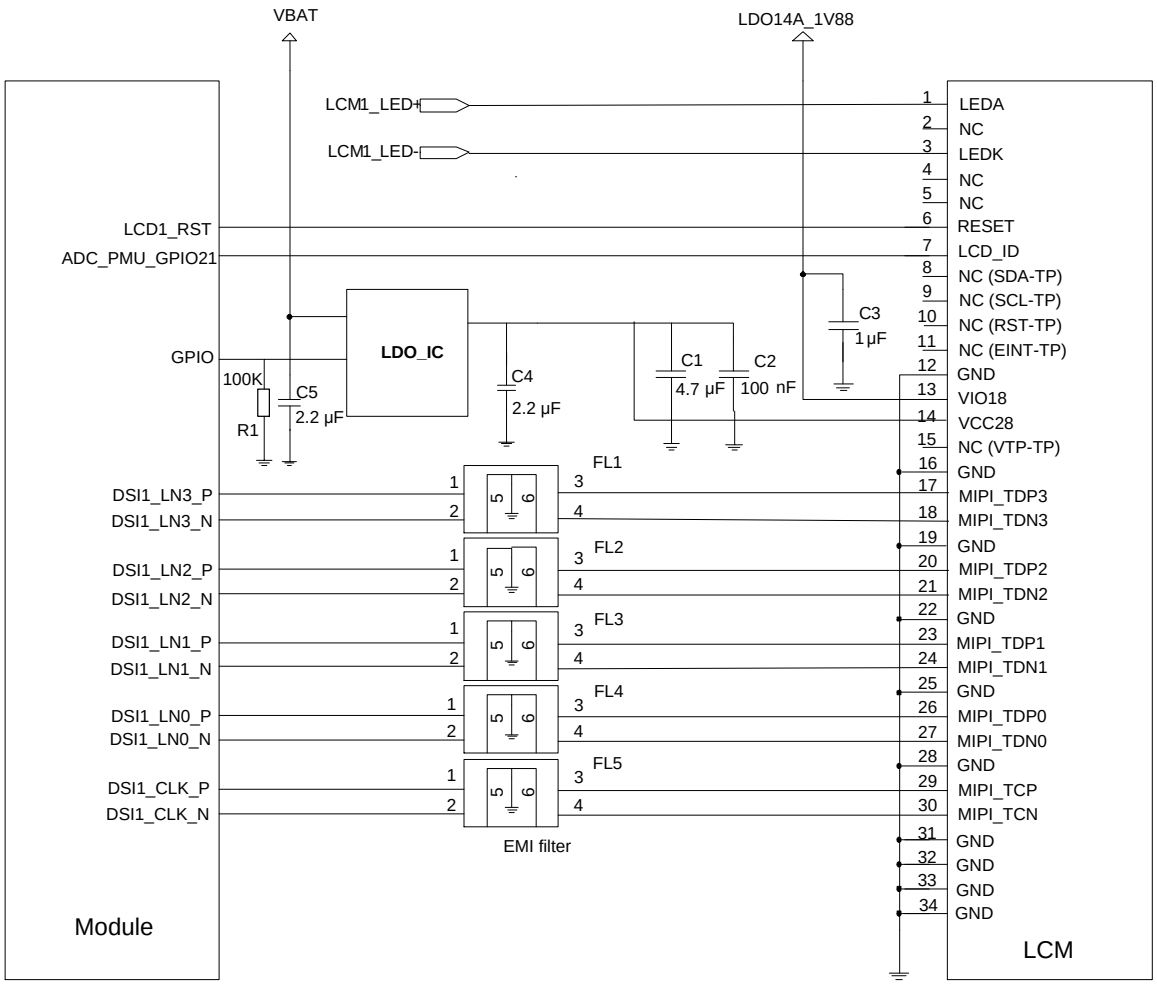


Figure 23: Reference Circuit Design for LCM1 Interface

MIPI are high-speed signals. It is recommended that common-mode filters should be added in series near the LCM connector, so as to improve protection against electromagnetic radiation interference. ICMEF112P900MFR is recommended.

When compatible design with other displays is required, connect the LCD_ID pin of LCM to the module's ADC pin, and please note that the output voltage of LCD_ID cannot exceed the voltage range of the ADC pin.

SA800U-WF provides a backlight driving output which can be used to drive LCM backlight WLEDs directly. The features are listed below:

- Use the high voltage output (LCD_BL_A) for powering WLED strings, and the OVP voltage output is 29.6 V.
- Support 4 current sink drivers (LCD_BL_K1, LCD_BL_K2, LCD_BL_K3, LCD_BL_K4), with maximum sink current of up to 30 mA for each. 2 of them can be connected in parallel for powering 16 WLEDs and 4 of them for 32 WLEDs.

- To adjust the backlight brightness, you can configure the sink current of the four current sink drivers via software.

For LCM0, use the internal backlight driving circuit provided by SA800U-WF by default. For LCM1, you can use the internal circuit or an external backlight driving circuit according to your demand. The following is a reference design for LCM1 external backlight driving circuit where PWM_PMI_GPIO5 is used to adjust the backlight brightness.

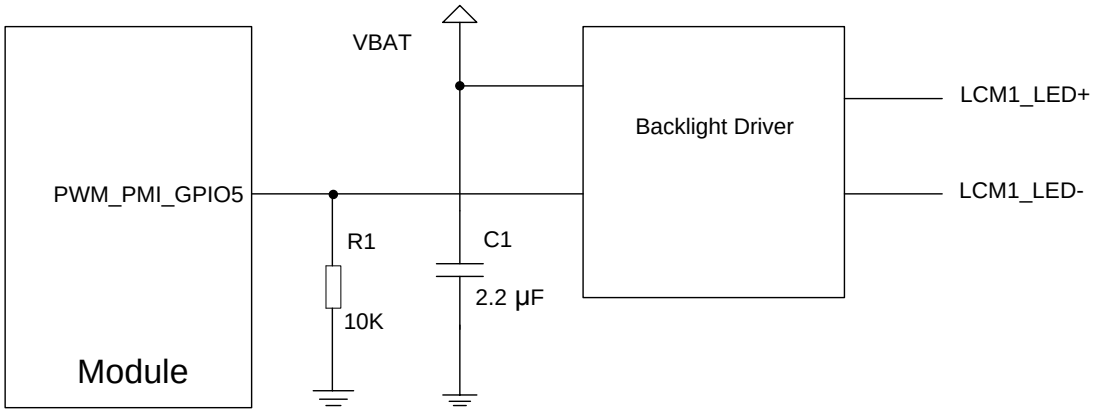


Figure 24: Reference Design of LCM1 External Backlight Driving Circuit

3.19. Touch Panel Interface

SA800U-WF provides one I2C interface to connect with touch panel, and also provides the corresponding power supply and interrupt pins. The pin definition of touch panel interfaces is illustrated below.

Table 22: Pin Definition of Touch Panel Interface

Pin Name	Pin No	I/O	Description	Comment
LDO28A_3V0	J4-10	PO	3.0 V output for VDD of TP	Vnom = 3.0 V $I_O$max = 150 mA
LDO14A_1V88	J4-9	PO	1.8 V output for TP I2C pull-up circuit	Vnom = 1.8 V $I_O$max = 50 mA
TP_INT	J2-48	DI	TP interrupt	1.8 V power domain.
TP_RST	J2-50	DO	TP reset	
TP_I2C_SCL	J2-44	OD	TP I2C clock	
TP_I2C_SDA	J2-46	OD	TP I2C data	

A reference design for touch panel interface is shown below.

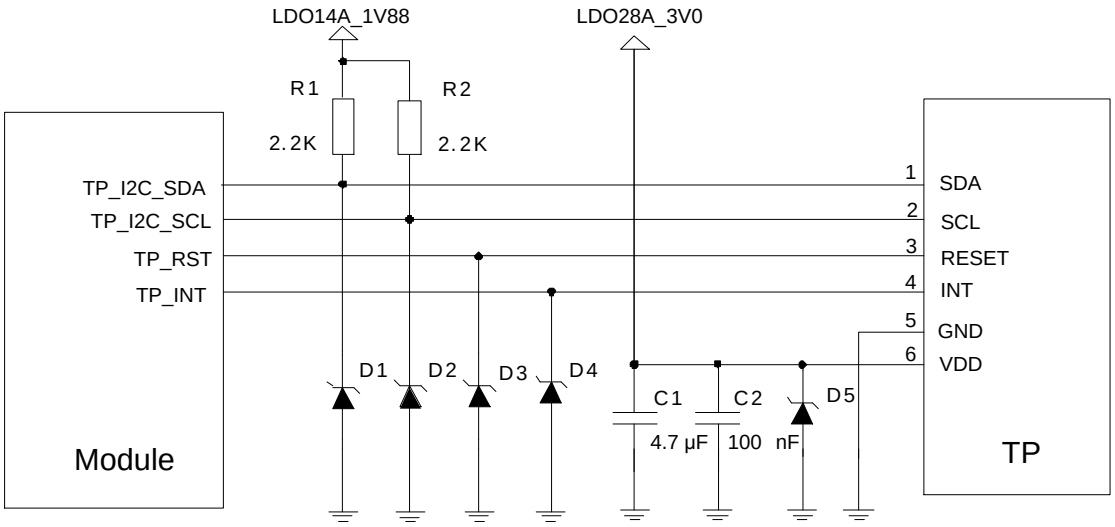


Figure 25: Reference Circuit Design for Touch Panel Interface

3.20. Camera Interfaces

Based on standard MIPI CSI input interface, SA800U-WF supports 4 cameras (4-lane + 4-lane + 4-lane + 2-lane), with maximum pixels up to 32 MP. The 2-lane MIPI CSI can only receive data of RAW format. It can be used for ToF/3D camera modules and cannot be used for display. The video and photo quality are determined by various factors such as camera sensor, camera lens quality, etc.

Table 23: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
LVS1A_1V8	J1-149	PO	1.8 V output for IOVDD of cameras	Vnom = 1.8 V $I_O$max = 300 mA
CSI0_CLK_N	J1-30	AI	MIPI clock of camera 0 (-)	100 Ω differential impedance.
CSI0_CLK_P	J1-28	AI	MIPI clock of camera 0 (+)	
CSI0_LN0_N	J1-22	AI	MIPI lane 0 data of camera 0 (-)	
CSI0_LN0_P	J1-24	AI	MIPI lane 0 data of camera 0 (+)	
CSI0_LN1_N	J1-16	AI	MIPI lane 1 data of camera 0 (-)	
CSI0_LN1_P	J1-18	AI	MIPI lane 1 data of camera 0 (+)	

CSI0_LN2_N	J1-10	AI	MIPI lane 2 data of camera 0 (-)	
CSI0_LN2_P	J1-12	AI	MIPI lane 2 data of camera 0 (+)	
CSI0_LN3_N	J1-6	AI	MIPI lane 3 data of camera 0 (-)	
CSI0_LN3_P	J1-4	AI	MIPI lane 3 data of camera 0 (+)	
CSI1_CLK_N	J1-58	AI	MIPI clock of camera 1 (-)	
CSI1_CLK_P	J1-60	AI	MIPI clock of camera 1 (+)	
CSI1_LN0_N	J1-52	AI	MIPI lane 0 data of camera 1 (-)	
CSI1_LN0_P	J1-54	AI	MIPI lane 0 data of camera 1 (+)	
CSI1_LN1_N	J1-46	AI	MIPI lane 1 data of camera 1 (-)	
CSI1_LN1_P	J1-48	AI	MIPI lane 1 data of camera 1 (+)	
CSI1_LN2_N	J1-42	AI	MIPI lane 2 data of camera 1 (-)	
CSI1_LN2_P	J1-40	AI	MIPI lane 2 data of camera 1 (+)	
CSI1_LN3_N	J1-34	AI	MIPI lane 3 data of camera 1 (-)	
CSI1_LN3_P	J1-36	AI	MIPI lane 3 data of camera 1 (+)	
CSI2_CLK_N	J1-63	AI	MIPI clock of camera 2 (-)	
CSI2_CLK_P	J1-61	AI	MIPI clock of camera 2 (+)	
CSI2_LN0_N	J1-67	AI	MIPI lane 0 data of camera 2 (-)	
CSI2_LN0_P	J1-69	AI	MIPI lane 0 data of camera 2 (+)	
CSI2_LN1_N	J1-66	AI	MIPI lane 1 data of camera 2 (-)	
CSI2_LN1_P	J1-64	AI	MIPI lane 1 data of camera 2 (+)	
CSI2_LN2_N	J1-72	AI	MIPI lane 2 data of camera 2 (-)	
CSI2_LN2_P	J1-70	AI	MIPI lane 2 data of camera 2 (+)	
CSI2_LN3_N	J1-78	AI	MIPI lane 3 data of camera 2 (-)	
CSI2_LN3_P	J1-76	AI	MIPI lane 3 data of camera 2 (+)	
CSI3_CLK_N	J1-85	AI	MIPI clock of camera 3 (-)	100 Ω differential

CSI3_CLK_P	J1-87	AI	MIPI clock of camera 3 (+)	impedance. CSI3 can only receive data of RAW format. It can be used for ToF/3D camera modules but cannot be used for display.
CSI3_LN0_N	J1-81	AI	MIPI lane 0 data of camera 3 (-)	
CSI3_LN0_P	J1-79	AI	MIPI lane 0 data of camera 3 (+)	
CSI3_LN1_N	J1-73	AI	MIPI lane 1 data of camera 3 (-)	
CSI3_LN1_P	J1-75	AI	MIPI lane 1 data of camera 3 (+)	
CAM0_STROBE	J1-122	DO	Strobe of camera 0	1.8 V power domain.
CAM1_STROBE	J1-116	DO	Strobe of camera 1	
CAM2_STROBE	J1-118	DO	Strobe of camera 2	
CAM0_MCLK	J1-91	DO	Master clock of camera 0	
CAM1_MCLK	J1-95	DO	Master clock of camera 1	
CAM2_MCLK	J1-99	DO	Master clock of camera 2	
CAM3_MCLK	J1-103	DO	Master clock of camera 3	
CAM0_RST	J1-100	DO	Reset of camera 0	
CAM1_RST	J1-96	DO	Reset of camera 1	
CAM2_RST	J1-124	DO	Reset of camera 2	
CAM3_RST	J1-126	DO	Reset of camera 3	
CAM0_PWDN	J1-114	DO	Power down of camera 0	
CAM1_PWDN	J1-120	DO	Power down of camera 1	
CAM2_PWDN	J1-106	DO	Power down of camera 2	
CAM3_PWDN	J1-112	DO	Power down of camera 3	
CAM0_AVDD_EN	J1-102	DO	AVDD enable of camera 0	
CAM1_AVDD_EN	J1-98	DO	AVDD enable of camera 1	
CAM2_AVDD_EN	J1-104	DO	AVDD enable of camera 2	
CAM3_AVDD_EN	J1-108	DO	AVDD enable of camera 3	
CAM0_DVDD_EN	J1-132	DO	DVDD enable of camera 0	

CAM1_DVDD_EN	J1-130	DO	DVDD enable of camera 1
CAM2_DVDD_EN	J1-110	DO	DVDD enable of camera 2
CAM3_DVDD_EN	J1-128	DO	DVDD enable of camera 3
CCI0_I2C_SCL	J1-142	OD	CCI0 I2C clock
CCI0_I2C_SDA	J1-144	OD	CCI0 I2C data
CCI1_I2C_SDA	J1-146	OD	CCI1 I2C data
CCI1_I2C_SCL	J1-148	OD	CC1 I2C clock

The following is a reference circuit design for camera applications.

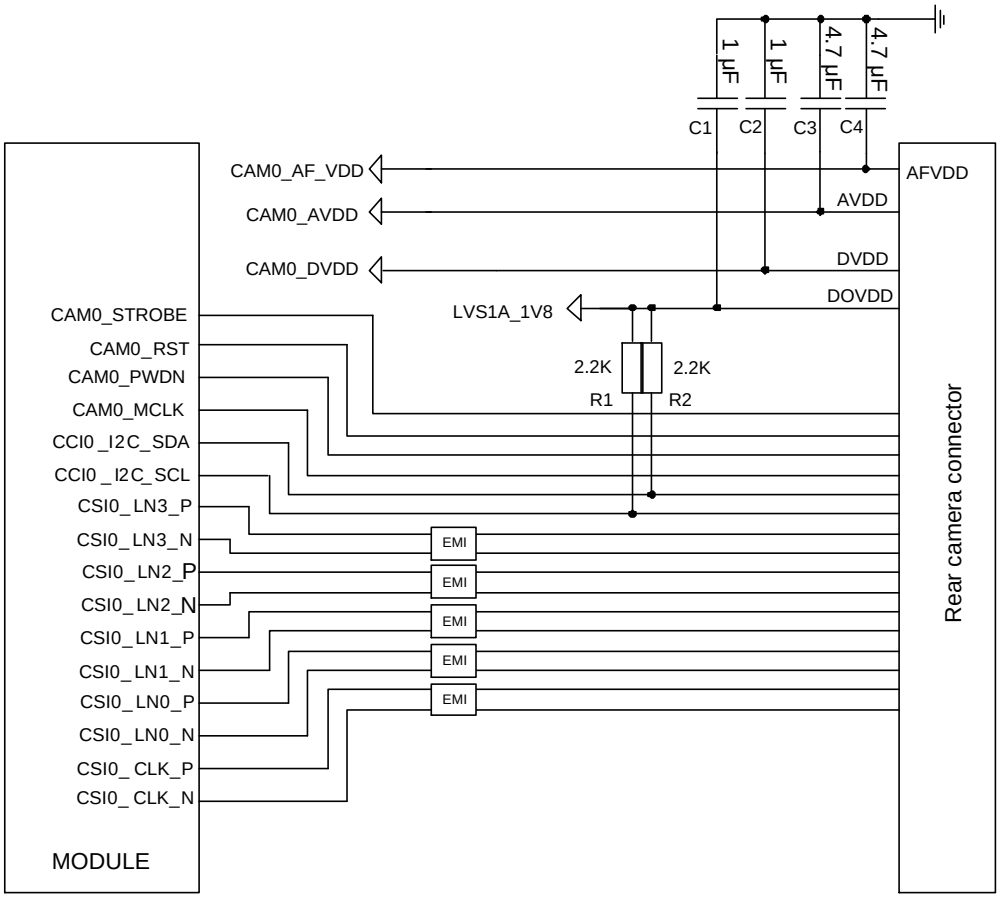


Figure 26: Reference Circuit Design for CSI0

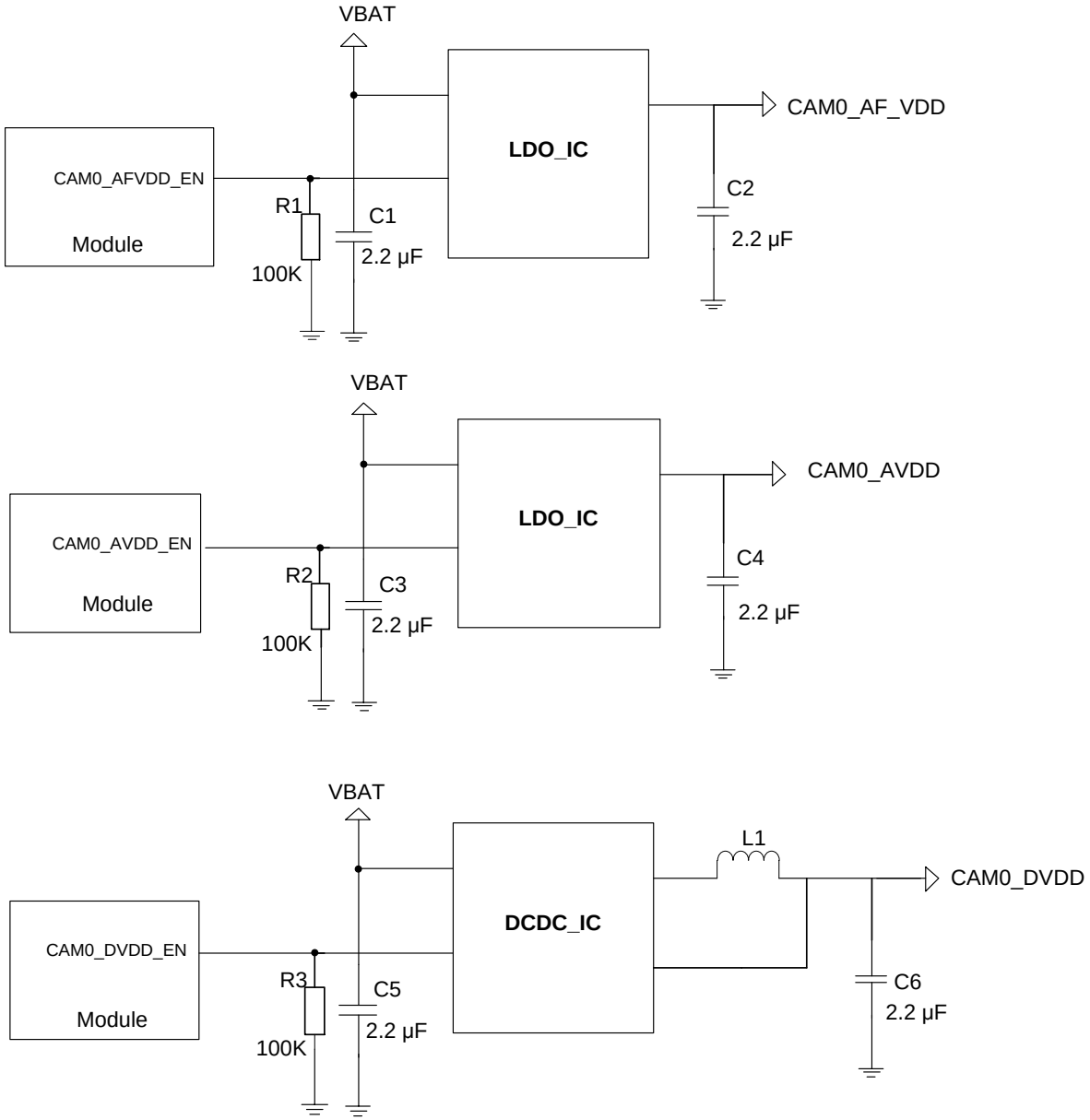


Figure 27: Reference Circuit Design for Power of CSI0

NOTE

CSI3 can only receive data of RAW format. It can be used for ToF/3D camera modules but cannot be used for display.

3.20.1. Design Considerations

- Special attention should be paid to the pin definition of LCM/camera connectors. Ensure the SA800U-WF module and the connectors are correctly connected.
- MIPI are high-speed signals, supporting maximum data rate of up to 2.5 Gbps. The differential impedance should be controlled as 100 Ω. Additionally, it is recommended to route the trace on the inner layer of PCB, and do not cross it with other traces. Any cut or hole on GND reference plane under MIPI signals should be avoided. For the same group of DSI or CSI signals, keep all the MIPI traces of the same length.
- Route the CAM_MCLK signals in the inner layer of the PCB and surround them with ground.
- Spacing for the lanes should comply with the following rules:
  a) Intra-lane P to N: 1 × trace width
  b) Lane to lane: 1.5 × trace width
  c) Lanes to all other signals: 2.5 × trace width
- Route MIPI traces according to the following rules:
  a) Control the differential impedance to 100 Ω ±10 %;
  b) Control intra-lane length difference within 0.7 mm;
  c) Control inter-lane length difference within 1.4 mm.

Table 24: CSI Data Rate and PCB Maximum Trace Length (D-PHY)

Data Rate	Flex Cable Length (inch)	Cable Insertion Loss (dB)	Maximum PCB Trace Length (mm)
500 Mbps/lane	3	-0.5	< 260
	6	-1	< 190
750 Mbps/lane	3	-0.7	< 210
	6	-1.15	< 155
1.0 Gbps/lane	3	-0.75	< 200
	6	-1.4	< 125
1.5 Gbps/lane	3	-0.9	< 145
	6	-1.8	< 60
2.1 Gbps/lane	3	-1.3	< 170
	6	-2.3	< 90

Table 25: DSI Data Rate and PCB Maximum Trace Length (D-PHY)

Data Rate	Flex Cable Length (inch)	Cable Insertion Loss (dB)	Maximum PCB Trace Length (mm)
500 Mbps/lane	3	-0.8	< 280
	6	-1.4	< 210
750 Mbps/lane	3	-1	< 210
	6	-1.5	< 150
1.0 Gbps/lane	3	-1.1	< 200
	6	-1.7	< 100
1.5 Gbps/lane	3	-1.2	< 135
	6	-2.2	< 40
2.1 Gbps/lane	3	-1.6	< 110
	6	-2.8	0

NOTES

1. The flex cable length used in this table is an example with specified insertion loss.
2. The flex cable insertion loss can be measured using a vector signal analyzer or obtained from the flex cable datasheet. Cable insertion loss on the design should be no worse than what is listed above.
3. The maximum PCB trace length listed above includes the length routed inside the module.

Table 26: MIPI Trace Length Inside the Module

Pin No.	Pin Name	Length (mm)	Length Difference (P - N)
J2-26	DSI0_CLK_N	13.12	0.15
J2-28	DSI0_CLK_P	13.27	
J2-38	DSI0_LN0_N	13.41	-0.52
J2-40	DSI0_LN0_P	12.89	
J2-32	DSI0_LN1_N	13.21	-0.43
J2-34	DSI0_LN1_P	12.78	

J2-20	DSI0_LN2_N	13.35	-0.54
J2-22	DSI0_LN2_P	12.81	
J2-14	DSI0_LN3_N	13.67	-0.57
J2-16	DSI0_LN3_P	13.10	
J2-21	DSI1_CLK_N	24.35	-0.40
J2-19	DSI1_CLK_P	23.95	
J2-13	DSI1_LN0_N	22.42	0.29
J2-15	DSI1_LN0_P	22.71	
J2-37	DSI1_LN1_N	23.35	0.67
J2-39	DSI1_LN1_P	24.02	
J2-27	DSI1_LN2_N	22.45	0.54
J2-25	DSI1_LN2_P	22.99	
J2-31	DSI1_LN3_N	23.73	-0.46
J2-33	DSI1_LN3_P	23.27	
J1-30	CSI0_CLK_N	23.90	-0.36
J1-28	CSI0_CLK_P	23.54	
J1-22	CSI0_LN0_N	24.31	-0.12
J1-24	CSI0_LN0_P	24.19	
J1-16	CSI0_LN1_N	23.33	-0.34
J1-18	CSI0_LN1_P	22.99	
J1-10	CSI0_LN2_N	24.53	0.42
J1-12	CSI0_LN2_P	24.95	
J1-6	CSI0_LN3_N	23.61	-0.26
J1-4	CSI0_LN3_P	23.35	
J1-58	CSI1_CLK_N	15.49	0.16

J1-60	CSI1_CLK_P	15.65	
J1-52	CSI1_LN0_N	14.99	-0.28
J1-54	CSI1_LN0_P	14.71	
J1-46	CSI1_LN1_N	14.93	-0.12
J1-48	CSI1_LN1_P	14.81	
J1-42	CSI1_LN2_N	14.74	0.54
J1-40	CSI1_LN2_P	15.28	
J1-34	CSI1_LN3_N	15.61	-0.30
J1-36	CSI1_LN3_P	15.31	
J1-63	CSI2_CLK_N	16.36	0.36
J1-61	CSI2_CLK_P	16.72	
J1-67	CSI2_LN0_N	15.84	0.25
J1-69	CSI2_LN0_P	16.09	
J1-66	CSI2_LN1_N	15.71	0.40
J1-64	CSI2_LN1_P	16.11	
J1-72	CSI2_LN2_N	14.90	0.49
J1-70	CSI2_LN2_P	15.39	
J1-78	CSI2_LN3_N	15.98	0.49
J1-76	CSI2_LN3_P	16.47	
J1-85	CSI3_CLK_N	10.27	0.08
J1-87	CSI3_CLK_P	10.35	
J1-81	CSI3_LN0_N	9.57	0.11
J1-79	CSI3_LN0_P	9.68	
J1-73	CSI3_LN1_N	11.20	-0.65
J1-75	CSI3_LN1_P	10.55	

3.20.2. Flashlight Interfaces

SA800U-WF supports 3 flash LED drivers with 2 × 1.5 A + 1 × 0.75 A, and supports both flash and torch modes. As for FLASH_LED1 and FLASH_LED2, in flash mode, the maximum output current is 0.75 A for each when the two LEDs work together and 1.5 A for each when they work separately. In torch mode, the maximum output current is 500 mA for each whether the two LEDs work together or separately. As for FLASH_LED3, in flash mode, the maximum output current is 0.75 A and in torch mode, the maximum output current is 500 mA.

Table 27: Pin Definition of Flashlight Interfaces

Pin Name	Pin No.	I/O	Description	Comment
FLASH_LED1	J4-23, J4-24	AO	Flash/torch driver output 1	I_{LED1} = 1.5 A
FLASH_LED2	J4-20, J4-21	AO	Flash/torch driver output 2	I_{LED2} = 1.5 A
FLASH_LED3	J4-5, J4-6	AO	Flash/torch driver output 3	I_{LED3} = 0.75 A

A reference circuit design is shown below.

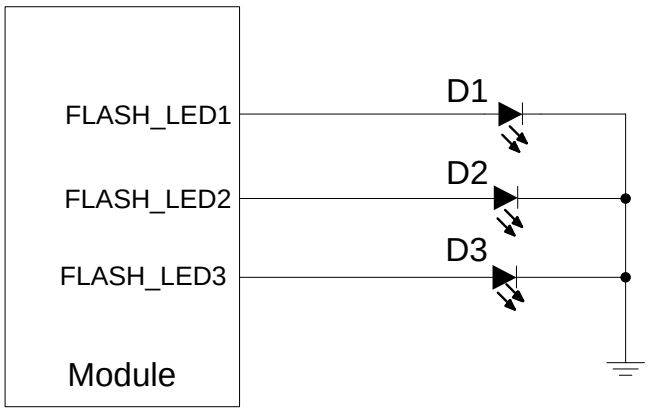


Figure 28: Reference Circuit Design for Flashlight Interfaces

3.21. Sensor Interfaces

SA800U-WF has an integrated sensor subsystem called the Snapdragon sensor core, which is dedicated to support low-power, always-on use cases. Snapdragon sensor core supports communication with sensors via I2C interface and SPI interface, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, optical sensor, temperature sensor. Snapdragon sensor core pins cannot be used for non-Snapdragon sensor core cases. They are dedicated for Snapdragon sensor core DSP.

Table 28: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SSC_SPI1_CS0	J1-136	DO	Sensor core SPI1 chip select 0	1.8 V power domain.
SSC_SPI1_CS1	J1-138	DO	Sensor core SPI1 chip select 1	
SSC_SPI1_CS2	J1-140	DO	Sensor core SPI1 chip select 2	
SSC_SPI1_CLK	J1-154	DO	Sensor core SPI1 clock	
SSC_SPI1_MOSI	J1-152	DO	Sensor core SPI1 master-out slave-in	
SSC_SPI1_MISO	J1-150	DI	Sensor core SPI1 master-in salve-out	
SSC_SPI2_CS	J1-141	DO	Sensor core SPI2 chip select	
SSC_SPI2_CLK	J1-145	DO	Sensor core SPI2 clock	
SSC_SPI2_MOSI	J1-143	DO	Sensor core SPI2 master-out slave-in	
SSC_SPI2_MISO	J1-147	DI	Sensor core SPI2 master-in salve-out	
SSC_I2C1_SDA	J2-8	OD	Sensor core I2C1 data	
SSC_I2C1_SCL	J2-10	OD	Sensor core I2C1 clock	
MAG_INT	J1-133	DI	Magnetic sensor interrupt	
MAG_DRDY_INT	J1-135	DI	Magnetic sensor DRDY interrupt	
GYRO_INT	J1-137	DI	Gyroscopic sensor interrupt	
ACCEL_INT	J1-139	DI	Acceleration sensor interrupt	

3.22. Audio Interfaces

SA800U-WF provides one SPI interface which is dedicated for the control of WCD934x audio codec, one 2-lane SLIMbus interface dedicated for data transmission between SA800U-WF and WCD934x, three I2S interfaces which can support TDM function. The following table shows the pin definition.

Table 29: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
CODEC_RST	J2-90	DO	Codec reset	
CODEC_SPI_CLK	J2-92	DO	SPI clock for codec	
CODEC_SPI_MOSI	J2-94	DO	SPI master-out slave-in for codec	
CODEC_SPI_CS	J2-96	DO	SPI chip select for codec	
CODEC_SPI_MISO	J2-89	DI	SPI master-in salve-out for codec	
CODEC_INT1	J2-91	DI	Codec interrupt 1	
CODEC_INT2	J2-93	DI	Codec interrupt 2	
WCD_CLK	J2-43	DO	WCD clock	
SLIMBUS_CLK	J2-51	DO	SLIMbus clock	
SLIMBUS_DATA0	J2-47	DIO	SLIMbus data bit 0	1.8 V power domain.
SLIMBUS_DATA1	J2-49	DIO	SLIMbus data bit 1	
I2S1_WS	J2-79	DO	I2S1 word select	
I2S1_MCLK	J2-81	DO	I2S1 master clock	
I2S1_SCK	J2-83	DO	I2S1 bit clock	
I2S1_DATA1	J2-85	DIO	I2S1 data channel 1	
I2S1_DATA0	J2-87	DIO	I2S1 data channel 0	
I2S2_WS	J2-55	DO	I2S2 word select	
I2S2_SCK	J2-57	DO	I2S2 bit clock	
I2S2_DATA0	J2-59	DIO	I2S2 data channel 0	

I2S2_DATA1	J2-61	DIO	I2S2 data channel 1
I2S3_WS	J2-63	DO	I2S3 word select
I2S3_DATA1	J2-65	DIO	I2S3 data channel 1
I2S3_DATA2	J2-67	DIO	I2S3 data channel 2
I2S3_DATA0	J2-69	DIO	I2S3 data channel 0
I2S3_DATA3	J2-71	DIO	I2S3 data channel 3
I2S3_SCK	J2-73	DO	I2S3 bit clock

3.23. Emergency Download Interface

USB_BOOT is an emergency download interface. Pulling it up to VREG_S4A_1V8 during power-up will force the module into emergency download mode. This is an emergency option when there are failures such as abnormal startup or operation. For convenient firmware upgrade and debugging in the future, please reserve the reference circuit design shown as below.

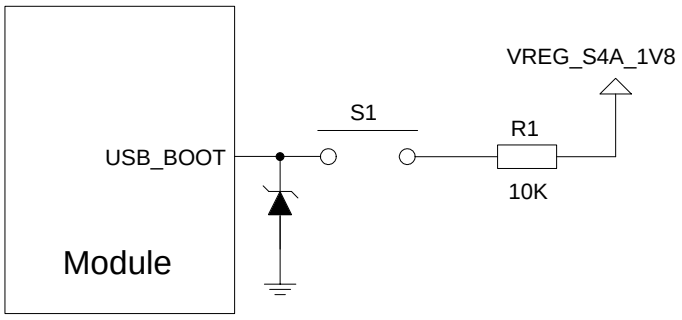


Figure 29: Reference Circuit Design for Emergency Download Interface

4 Wi-Fi and BT

SA800U-WF provides a shared antenna connector ANT-CH0 for Wi-Fi and Bluetooth functions, a Wi-Fi MIMO antenna connector ANT-CH1 for better Wi-Fi performance and a Bluetooth antenna connector BT*. The interface impedance is 50 Ω. External antennas such as PCB antenna, sucker antenna and ceramic antenna can be connected to the module via these connectors, so as to achieve Wi-Fi and BT functions.

NOTE

"*" means under development.

4.1. Wi-Fi Overview

SA800U-WF supports 2.4 GHz and 5 GHz dual-band WLAN wireless communication based on IEEE 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 866 Mbps.

The features are as below:

- Support 2 × 2 MIMO
- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI SMS4 hardware encryption
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0–7 for HT20 and HT40
- Support MCS 0–8 for VHT20
- Support MCS 0–9 for VHT40 and VHT80

4.1.1. Wi-Fi Performance

The following table lists the Wi-Fi transmitting and receiving performance of SA800U-WF module.

Table 30: Wi-Fi Transmitting Performance

	Standard	Rate	Output Power
2.4 GHz	802.11b	1 Mbps	17 dBm ±2.5 dB
	802.11b	11 Mbps	17 dBm ±2.5 dB
	802.11g	6 Mbps	17 dBm ±2.5 dB
	802.11g	54 Mbps	14 dBm ±2.5 dB
	802.11n HT20	MCS0	16 dBm ±2.5 dB
	802.11n HT20	MCS7	13 dBm ±2.5 dB
	802.11n HT40	MCS0	16 dBm ±2.5 dB
	802.11n HT40	MCS7	13 dBm ±2.5 dB
5 GHz	802.11a	6 Mbps	17 dBm ±2.5 dB
	802.11a	54 Mbps	15 dBm ±2.5 dB
	802.11n HT20	MCS0	16 dBm ±2.5 dB
	802.11n HT20	MCS7	14 dBm ±2.5 dB
	802.11n HT40	MCS0	16 dBm ±2.5 dB
	802.11n HT40	MCS7	14 dBm ±2.5 dB
	802.11ac VHT20	MCS0	16 dBm ±2.5 dB
	802.11ac VHT20	MCS8	14 dBm ±2.5 dB
	802.11ac VHT40	MCS0	16 dBm ±2.5 dB
	802.11ac VHT40	MCS9	14 dBm ±2.5 dB
	802.11ac VHT80	MCS0	16 dBm ±2.5 dB
	802.11ac VHT80	MCS9	13.5 dBm ±2.5 dB

Table 31: Wi-Fi Receiving Performance

	Standard	Rate	Sensitivity
2.4 GHz	802.11b	1 Mbps	-96 dBm
	802.11b	11 Mbps	-87 dBm
	802.11g	6 Mbps	-90 dBm
	802.11g	54 Mbps	-74 dBm
	802.11n HT20	MCS0	-90 dBm
	802.11n HT20	MCS7	-72 dBm
	802.11n HT40	MCS0	-87 dBm
	802.11n HT40	MCS7	-70 dBm
5 GHz	802.11a	6 Mbps	-91 dBm
	802.11a	54 Mbps	-75 dBm
	802.11n HT20	MCS0	-91 dBm
	802.11n HT20	MCS7	-72 dBm
	802.11n HT40	MCS0	-87 dBm
	802.11n HT40	MCS7	-70 dBm
	802.11ac VHT20	MCS8	-68 dBm
	802.11ac VHT40	MCS9	-64 dBm
	802.11ac VHT80	MCS9	-59 dBm

Reference specifications: IEEE 802.11a/b/g/n/ac.

4.2. BT Overview

SA800U-WF supports BT 5.0 (BR/EDR + BLE) specifications, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally support up to 7 wireless connections
- Maximally support up to 3.5 piconets at the same time
- Support one SCO or eSCO (Extended Synchronous Connection Oriented) connection

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 32: BT Data Rate and Versions

Version	Data rate	Maximum Application Throughput
1.2	1 Mbit/s	> 80 kbit/s
2.0 + EDR	3 Mbit/s	> 80 kbit/s
3.0 + HS	24 Mbit/s	Reference to 3.0 + HS
4.0	24 Mbit/s	Reference to 4.0 LE
5.0	48 Mbit/s	Reference to 5.0 LE

Reference specifications are listed below:

- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth 5.0 RF-PHY Cover Standard：RF-PHY.TS.5.0.0, December 06, 2016

4.2.1. BT Performance

The following table lists the BT transmitting and receiving performance of SA800U-WF module.

Table 33: BT Transmitting and Receiving Performance

Transmitter Performance			
Packet Types	DH5	2-DH5	3-DH5
Transmitting Power	7.5 dBm ±2.5 dB	7.5 dBm ±2.5 dB	8 dBm ±2.5 dB
Receiver Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	-92 dBm	-93 dBm	-86 dBm

5 Antenna Connection

5.1. Antenna Connectors

SA800U-WF is mounted with four antenna connectors: ANT-CH0 (Wi-Fi/BT antenna connector), ANT-CH1 (Wi-Fi MIMO antenna connector), BT* (BT antenna connector), and FM* (FM antenna connector) respectively. The impedance of the antenna connectors is 50 Ω.

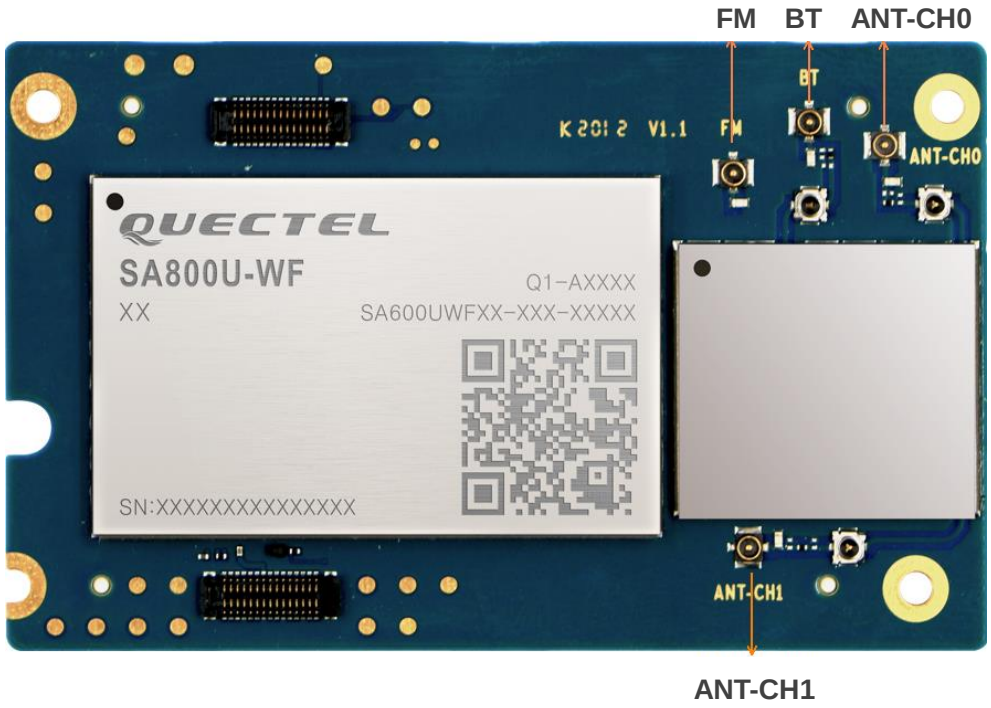


Figure 30: Antenna Connectors

Table 34: Definition of Antenna Connectors

Antenna Connector Name	I/O	Description	Comment
ANT-CH0	AIO	Wi-Fi/BT antenna connector	50 Ω impedance
ANT-CH1	AIO	Wi-Fi MIMO antenna connector	50 Ω impedance

BT*	AIO	BT antenna connector	50 Ω impedance
FM*	AI	FM antenna connector	50 Ω impedance

Table 35: Operating Frequency

Type	Frequency	Unit
802.11a/b/g/n/ac	2402–2482 5180–5825	MHz
BT 5.0	2402–2480	MHz
FM*	76–108	MHz

NOTE

"*" means under development.

5.2. Antenna Installation

5.2.1. Antenna Requirements

The following table shows the requirements for Wi-Fi/BT/FM antennas.

Table 36: Antenna Requirements

Antenna Type	Requirements
Wi-Fi/BT/FM	VSWR: ≤ 2 Gain: 1 dBi Max Input Power: 50 W Input Impedance: 50 Ω Polarization Type: Vertical Cable Insertion Loss: <1 dB

5.2.2. Recommended Mating Plug for Antenna Connection

SA800U-WF is mounted with RF connectors (receptacles) for convenient antenna connection. The connector being used is 818000500 from ECT and its dimensions are shown as below.

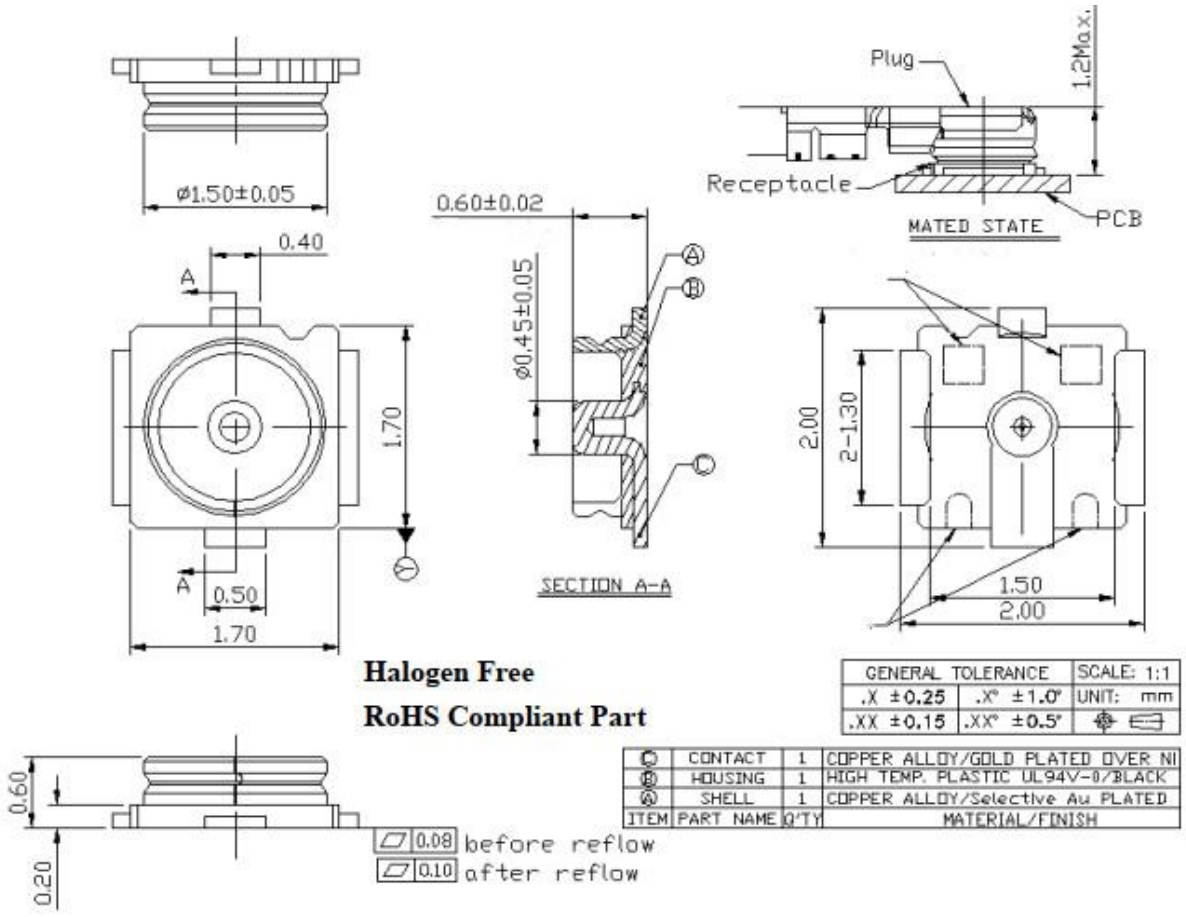
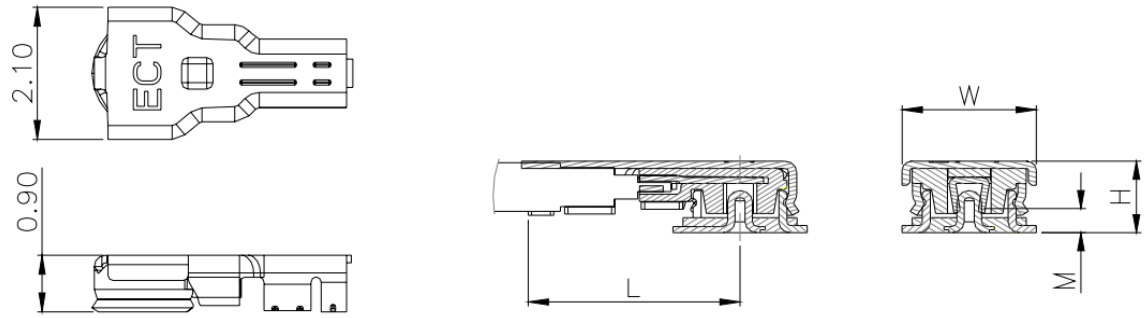


Figure 31: Dimensions of the ECT 818000500 Connector (Unit: mm)

The mating plug listed in the following figure can be used to match the receptacles.



Mating Dimension (mm)				
Item	L	H	W	M
DIA=0.81mm Coaxial Cable Assembly	3.20±0.2	1.2 Max.	2.1±0.2	0.4±0.2

Figure 32: Mechanicals of the Mating Plug (Unit: mm)

6 Reliability, Radio and Electrical Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 37: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	6	V
USB_VBUS	-0.3	28	V
Voltage on Digital Pins	-0.5	2.3	V

6.2. Power Supply Ratings

Table 38: SA800U-WF Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltages must fall between the minimum and maximum values	3.55	3.8	4.4	V
	Voltage drop during power-on	Maximum power control level during power-on	-	-	400	mV
I_{VBAT}	Peak supply current (during power-on)	Maximum power control level during power-on	-	3.0	5.0	A

USB_VBUS	Charging power input. Power output for OTG device. USB/charger insertion detection.	-	4.0	5.0	14	V
VRTC	Power supply voltage of backup battery	-	2.5	3.2	3.2	V

6.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 39: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating temperature range [1)]	-35	+25	+75	°C
Storage temperature range	-40	-	+90	°C

NOTE

[1)] Within the operating temperature range, the module is IEEE compliant.

6.4. Current Consumption

The current consumption of different conditions is listed in the following table.

Table 40: SA800U-WF Current Consumption (2 × 2 MIMO)

Description	Conditions	Typ.	Unit
OFF	Power down	80	μA
Airplane Mode	RF sleep	5.5	mA
Wi-Fi 802.11a Tx	@ 6 Mbps	210	mA

	@ 54 Mbps	190	mA
Wi-Fi 802.11b Tx	@ 1 Mbps	305	mA
	@ 11 Mbps	175	mA
Wi-Fi 802.11g Tx	@ 6 Mbps	170	mA
	@ 54 Mbps	150	mA
Wi-Fi 802.11n Tx	@ 14.4 Mbps, 20 MHz	750	mA
	@ 144.4 Mbps, 20 MHz	625	mA
	@ 30 Mbps, 40 MHz	770	mA
	@ 300 Mbps, 40 MHz	615	mA
Wi-Fi 802.11ac Tx	@ 14.4 Mbps, 20 MHz	760	mA
	@ 173.2 Mbps, 20 MHz	655	mA
	@ 30 Mbps, 40 MHz	740	mA
	@ 400 Mbps, 40 MHz	610	mA
	@ 65 Mbps, 80 MHz	685	mA
	@ 866.6 Mbps, 80 MHz	565	mA
Wi-Fi 802.11a Rx	@ 54 Mbps	160	mA
Wi-Fi 802.11b Rx	@ 11 Mbps	175	mA
Wi-Fi 802.11g Rx	@ 54 Mbps	155	mA
Wi-Fi 802.11n Rx	@ 300 Mbps, 40 MHz	615	mA
Wi-Fi 802.11ac Rx	@ 866.6 Mbps, 80 MHz	550	mA
BT Tx Channel 0	-	110	mA
BT Tx Channel 38	-	112	mA
BT Tx Channel 78	-	113	mA
BT Rx Channel 38	-	109	mA

6.5. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it should be subject to ESD handling precautions that are typically applied to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the electrostatic discharge characteristics of SA800U-WF module.

Table 41: ESD Characteristics (Temperature: 25 °C, Humidity: 45 %)

Test Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	+/-8	+/-12	kV
FM Antenna Interface	+/-4	+/-8	kV
BT Antenna Interface	+/-3	+/-6	kV
Other Antenna Interfaces	+/-4	+/-8	kV
Other Interfaces	+/-0.5	+/-1	kV

6.6. Thermal Dissipation

To achieve a maximum performance while working under extended temperatures or extreme conditions (such as with maximum power) for a long time, it is strongly recommended to apply thermal conductive gap fillers to the gaps between the shielding cover and heat-generating components in the module for better thermal dissipation.

There are other measures to enhance thermal dissipation:

- Place the module away from other heat sources.
- Select a suitable mechanical enclosure for the terminal product integrating the SA800U-WF module, and apply special treatment to the surface of the enclosure to enhance its heat radiation capability.
- Forced convection cooling scheme is highly recommended for the module to decrease the temperature rise, such as attaching an active heat sink with adequate cooling capacity to the top of the shielding cover.

The following figure shows the thermal dissipation area:

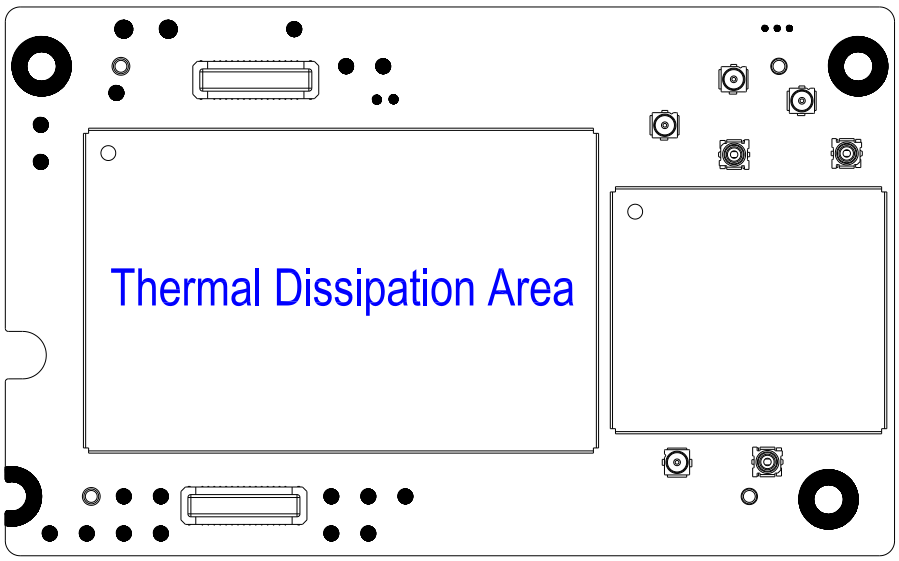


Figure 33: Thermal Dissipation

NOTE

If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimension tolerances are ±0.05 mm unless otherwise specified.

7.1. Mechanical Dimensions of the Module

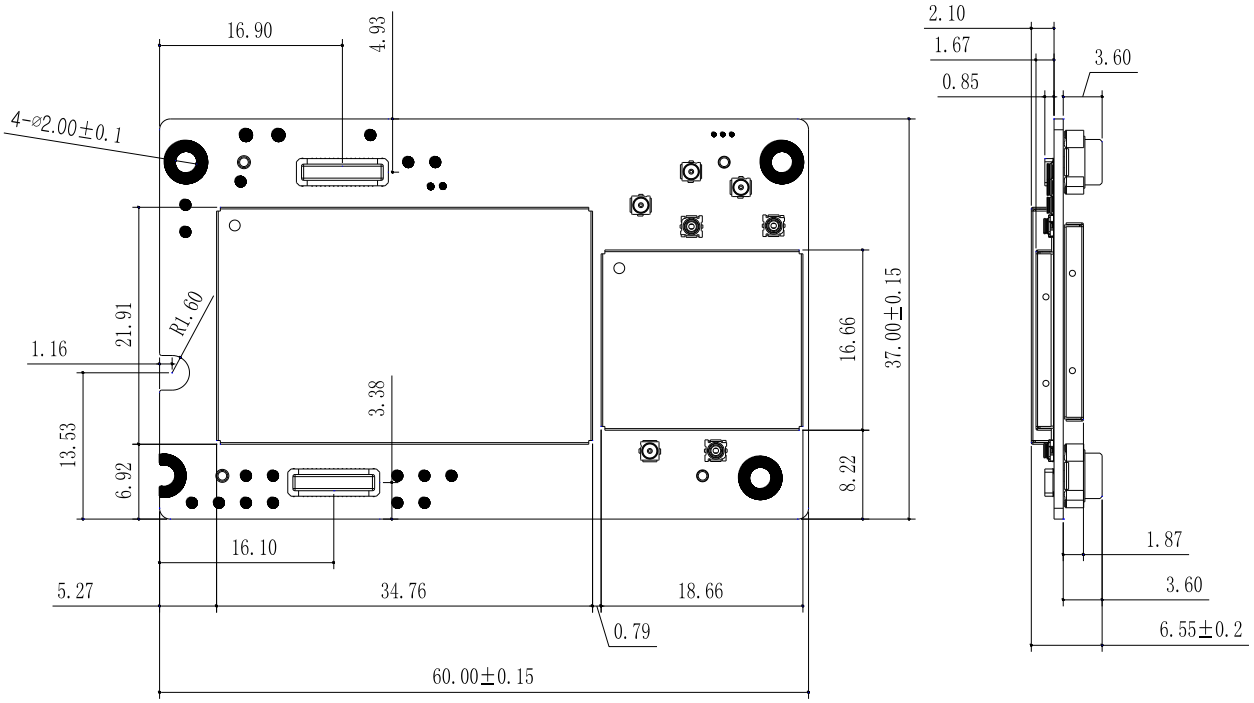


Figure 34: Module Top and Side Dimensions

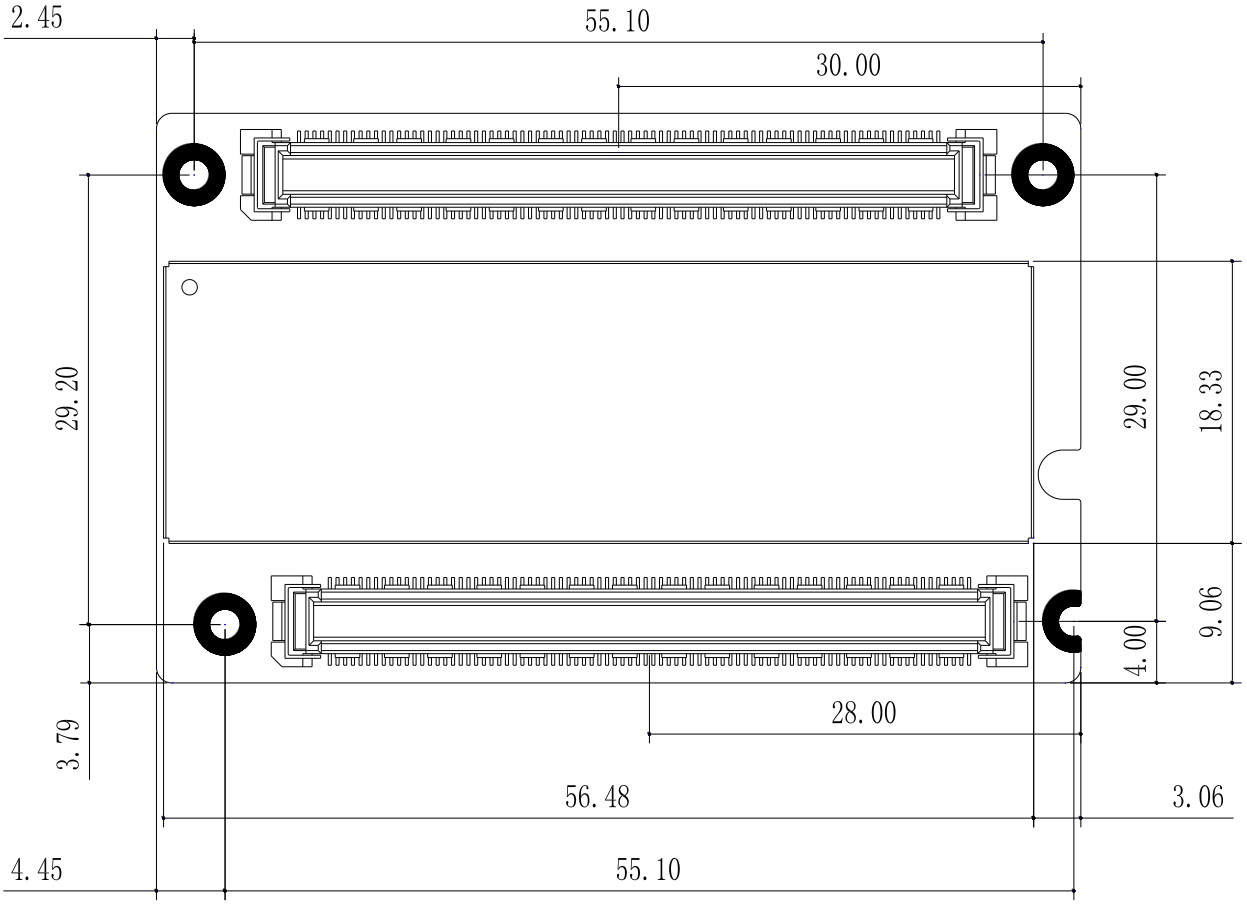


Figure 35: Module Bottom Dimensions (Bottom View)

7.2. Recommended Footprint

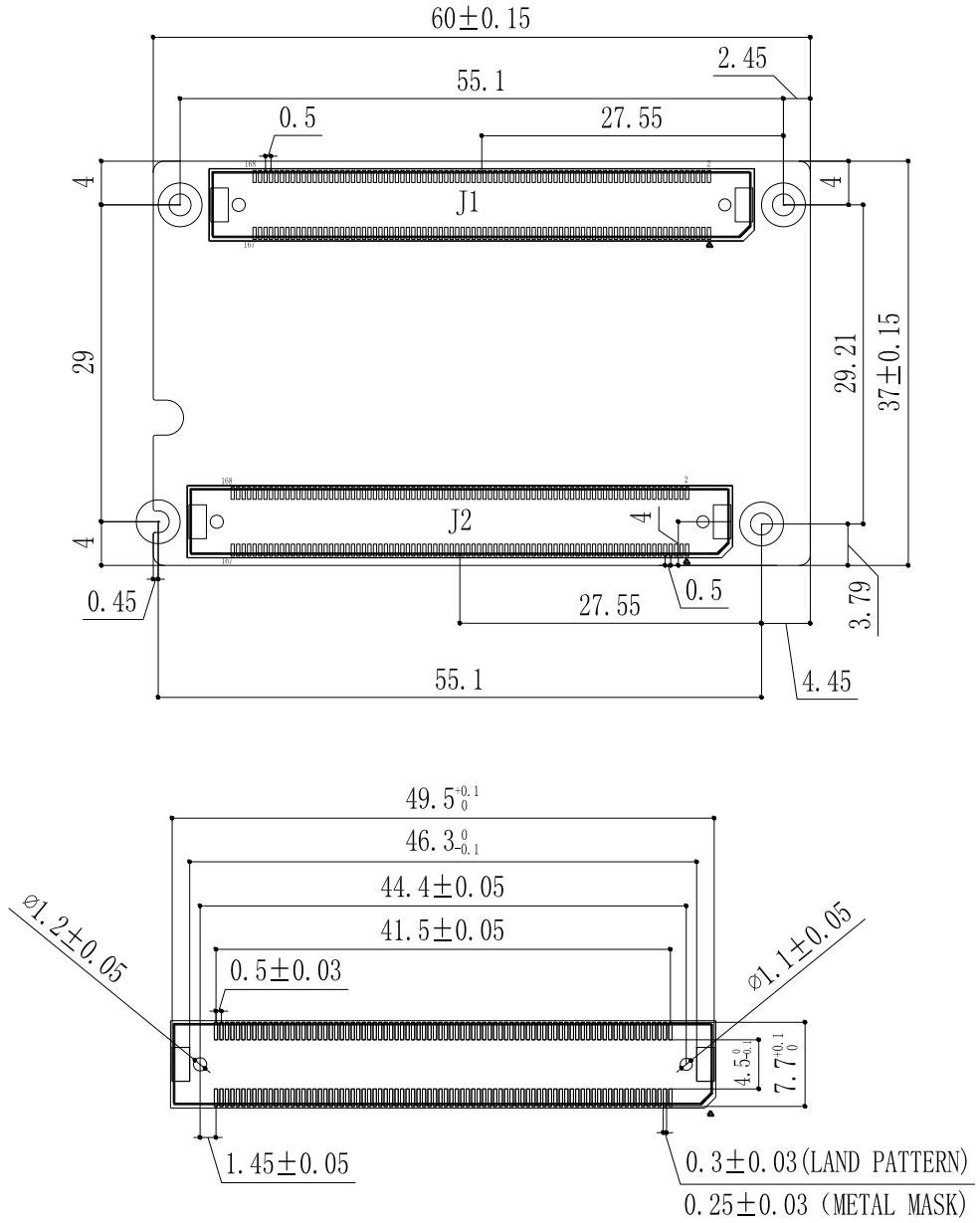


Figure 36: Recommended Footprint (Top View)

NOTES

1. For easy maintenance of the module, keep about 5 mm between the module and other components on the host PCB.
2. All RESERVED pins should be kept open and MUST NOT be connected to ground.
3. The 168-pin connector FX10A-168S-SV(21) of HIROSE should be used for connection with the module.

7.3. Top and Bottom View of the Module

Figure 37: Top View of SA800U-WF Module

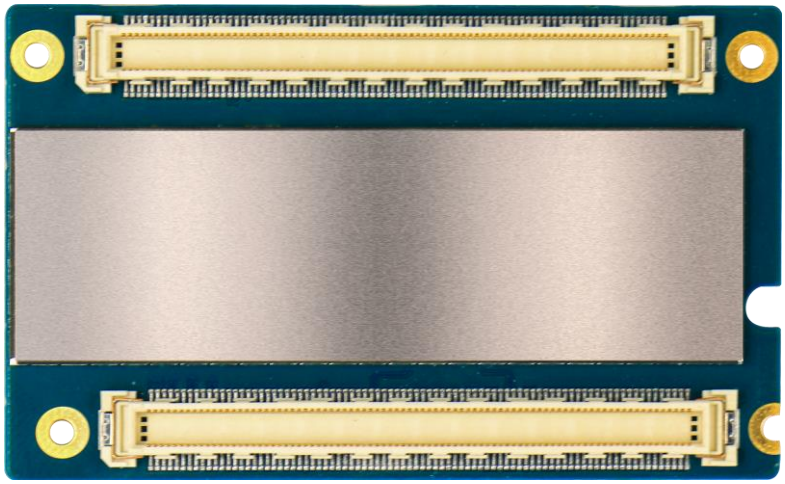


Figure 38: Bottom View of SA800U-WF Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage and Packaging

8.1. Storage

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be installed within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

NOTE

[1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.

8.2. Packaging

SA800U-WF is packaged in tray carriers. Each tray is 350 mm × 245 mm × 15.8 mm and contains 18 modules. The following figures show the package details, measured in mm.

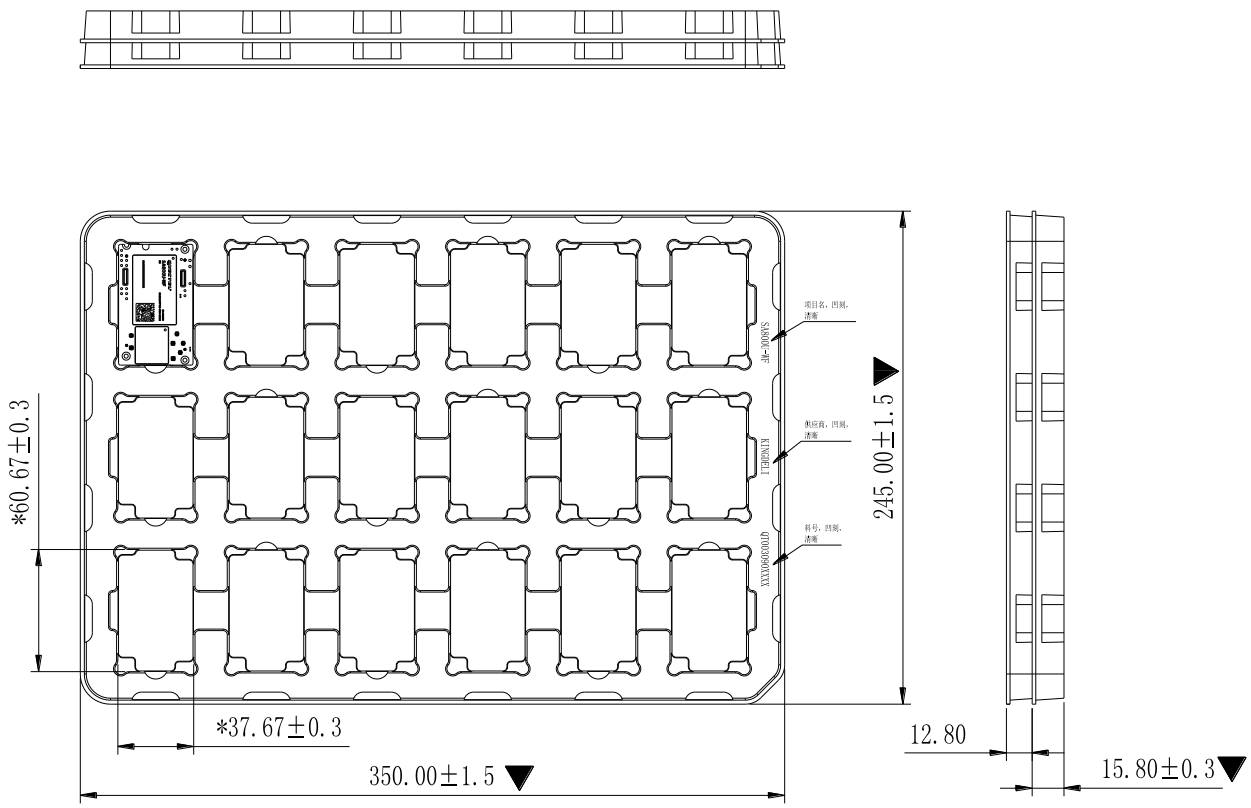


Figure 39: Tray Dimensions

10 trays are overlaid in one vacuum-sealed package. The package details are shown below.

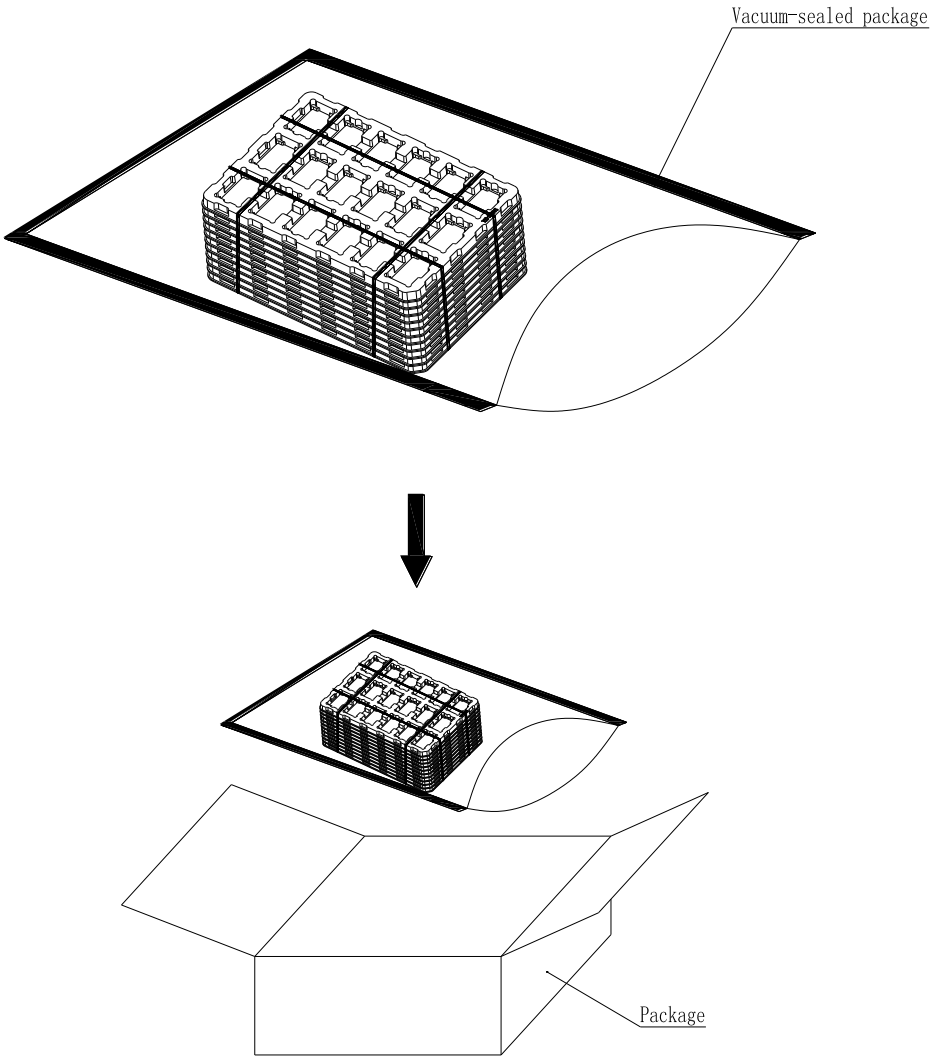


Figure 40: Package Details

Table 42: Tray Package

Model Name	MOQ for MP	Minimum Package: 180 pcs
SA800U-WF	180 pcs	N.W.: 4.67 kg G.W.: 5.07 kg

9 Appendix References

Table 43: Related Documents

SN	Document Name	Description
[1]	Quectel_SA800U-WF_EVB_User_Guide	EVB User Guide for SA800U-WF
[2]	Quectel_SA800U-WF_Pin_Description_and_GPIO_Configuration	Pin Description and GPIO Configuration of SA800U-WF
[3]	Quectel_SA800U-WF_Reference_Design	Reference Design for SA800U-WF

Table 44: Terms and Abbreviations

Abbreviation	Description
3D	3-Dimensional
ADC	Analog-to-Digital Converter
AP	Access Point
B2B	Board-to-Board
BOB	Buck or Boost
bps	Bits per Second
BT	Bluetooth
CS	Coding Scheme
CSI	Camera Serial Interface
CTS	Clear to Send
DP	DisplayPort
DRDY	Data Ready

DSC	Display Stream Compression
DSI	Display Serial Interface
DSP	Digital Signal Processor
DTE	Data Terminal Equipment (typically computer, external controller)
DTR	Data Terminal Ready
ERM	Eccentric Rotating Mass
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
EVRC	Enhanced Variable Rate Codec
EVS	Enhanced Voice Services
FM	Frequency Modulation
GPIO	General Purpose Input/Output
GPU	Graphics Processing Unit
HK ADC	Housekeeping ADC
HT	High Throughput
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IEEE	Institute of Electrical and Electronics Engineers
Imax	Maximum Load Current
I/O	Input/Output
ISP	Image Signal Processor
LCD	Liquid Crystal Display
LCM	LCD Module
LE	Low Energy
LED	Light Emitting Diode

LPDDR	Low-Power Double Data Rate
LPG	Light Pulse Generator
LRA	Linear Resonant Actuator
MCS	Modulation and Coding Scheme
MIMO	Multiple Input Multiple Output
MIPI	Mobile Industry Processor Interface
MLCC	Multi-layer Ceramic Capacitor
NTC	Negative Temperature Coefficient
OTG	On-The-Go
OVP	Over Voltage Protection
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PHY	Physical Layer
PMU	Power Management Unit
PWM	Pulse Width Modulation
QC	Quick Charge
QCELP	Qualcomm Code-Excited Linear Prediction
QUXGA	Quad Ultra Extended Graphics Array
RF	Radio Frequency
RFFE	RF Front End
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
RX	Receive
SD	Secure Digital

SDIO	Secure Digital Input Output
SLIMbus	Serial Low-power Inter-chip Media Bus
SMPS	Switched-Mode Power Supply
SPI	Serial Peripheral Interface
SSC	Snapdragon Sensor Core
TDM	Time-Division Multiplexing
ToF	Time-of-Flight
TP	Touch Panel
TX	Transmitting Direction
UART	Universal Asynchronous Receiver & Transmitter
UFS	Universal Flash Storage
USB	Universal Serial Bus
VESA	Video Electronics Standards Association
VHT	Very High Throughput
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
V_I	Voltage Input
$V_{IH}max$	Maximum Input High Level Voltage Value
$V_{IH}min$	Minimum Input High Level Voltage Value
$V_{IL}max$	Maximum Input Low Level Voltage Value
$V_{IL}min$	Minimum Input Low Level Voltage Value
V_Imax	Absolute Maximum Input Voltage Value
V_Imin	Absolute Minimum Input Voltage Value
V_O	Voltage Output

V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
WAPI	WLAN Authentication and Privacy Infrastructure
WLAN	Wireless Local Area Network
WLED	White LED
XO	Crystal Oscillator