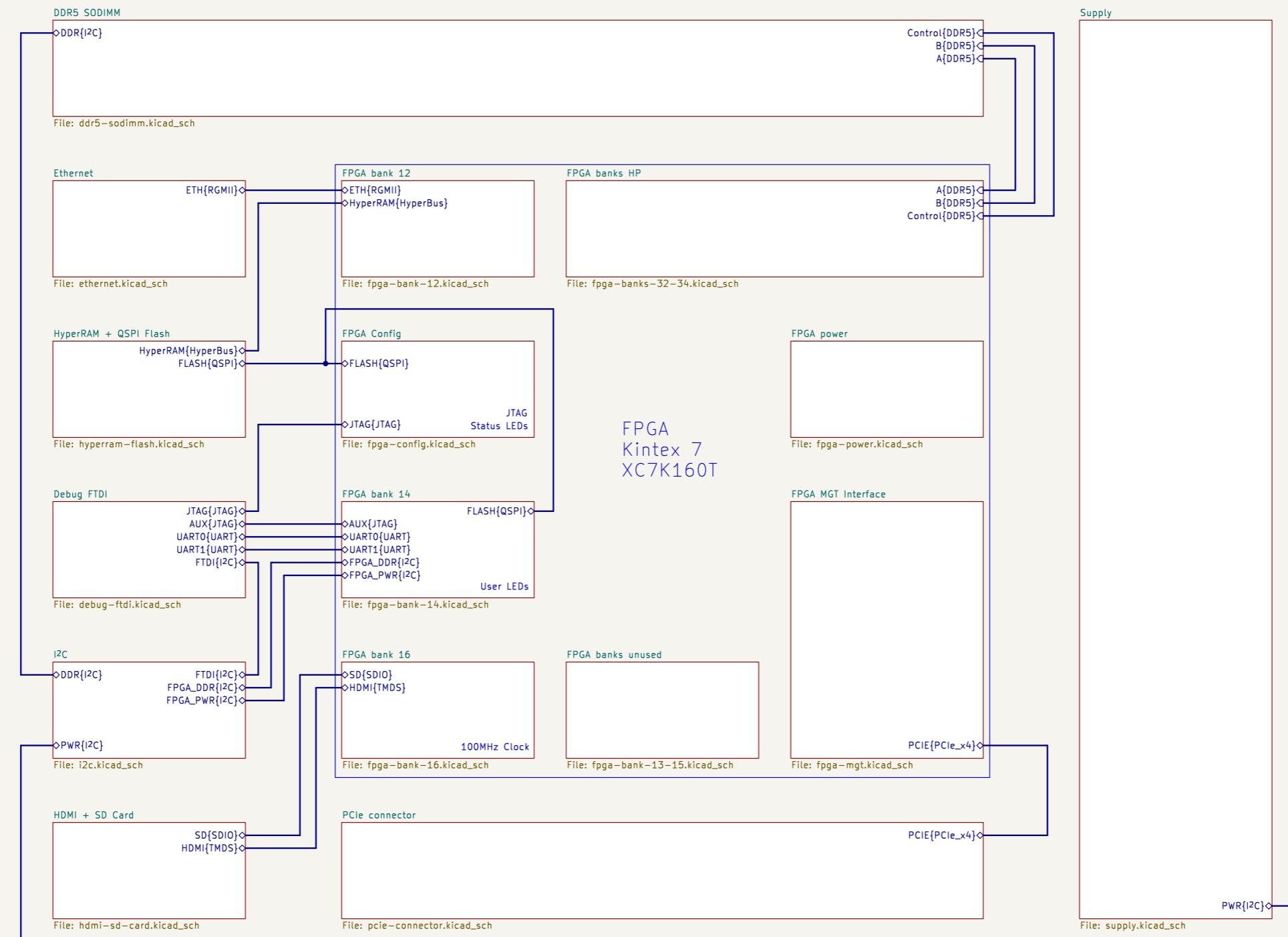
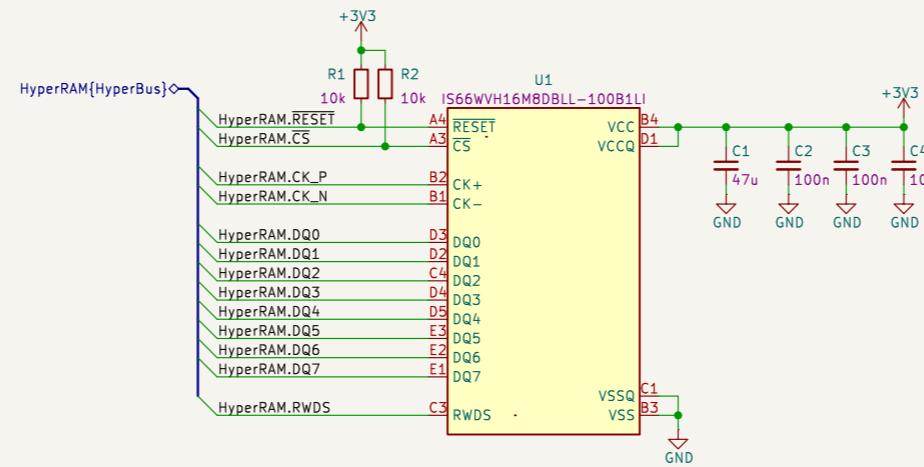


# SO-DIMM DDR5 Tester

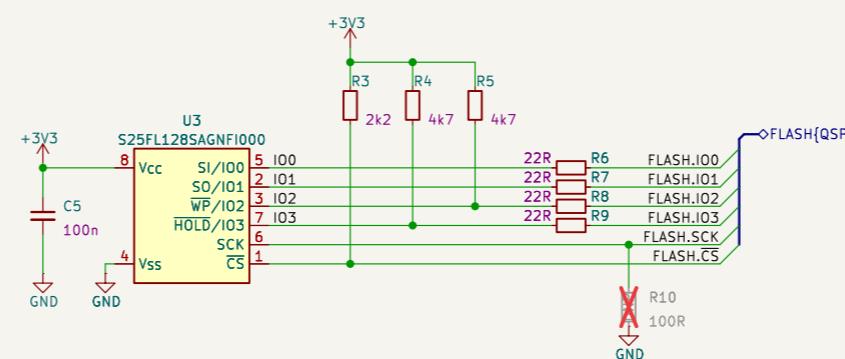


# HyperRAM

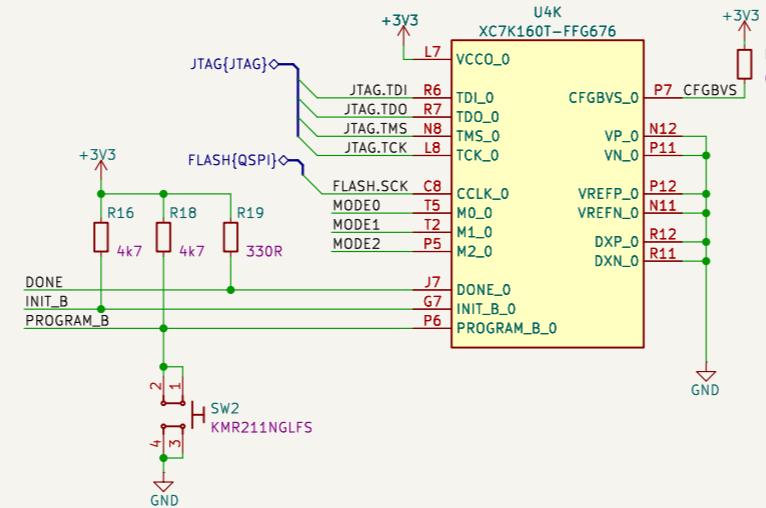


## (Q)SPI flash

Master SPI Quad (x4) configuration scheme  
Follows Figure 2-14 7 Series FPGAs Configuration User Guide  
UG470 (v1.13.1)

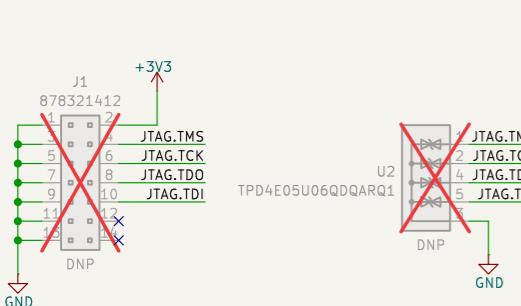


# FPGA BANK 0

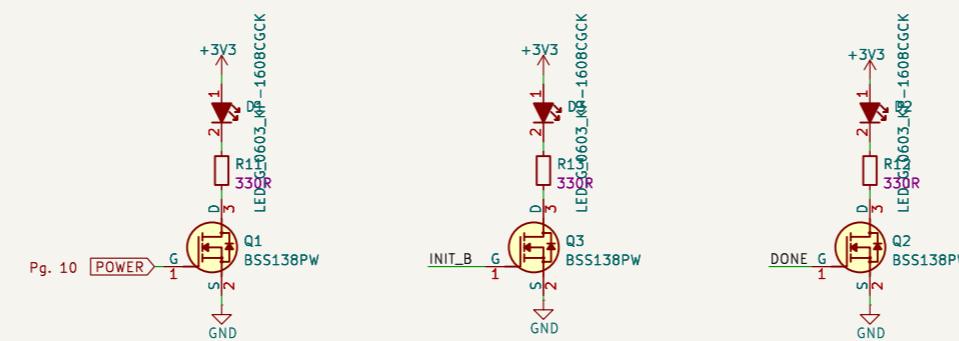


## JTAG Connector

Compatible with Xilinx Platform Cable

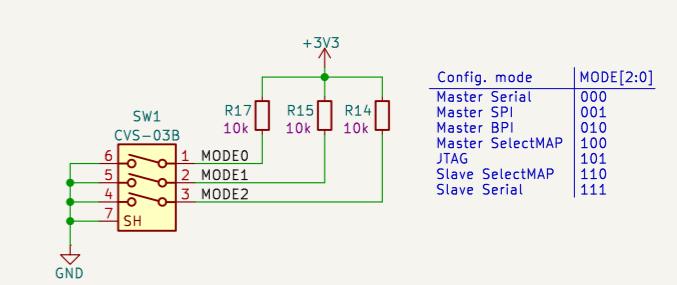


## STATUS LEDs



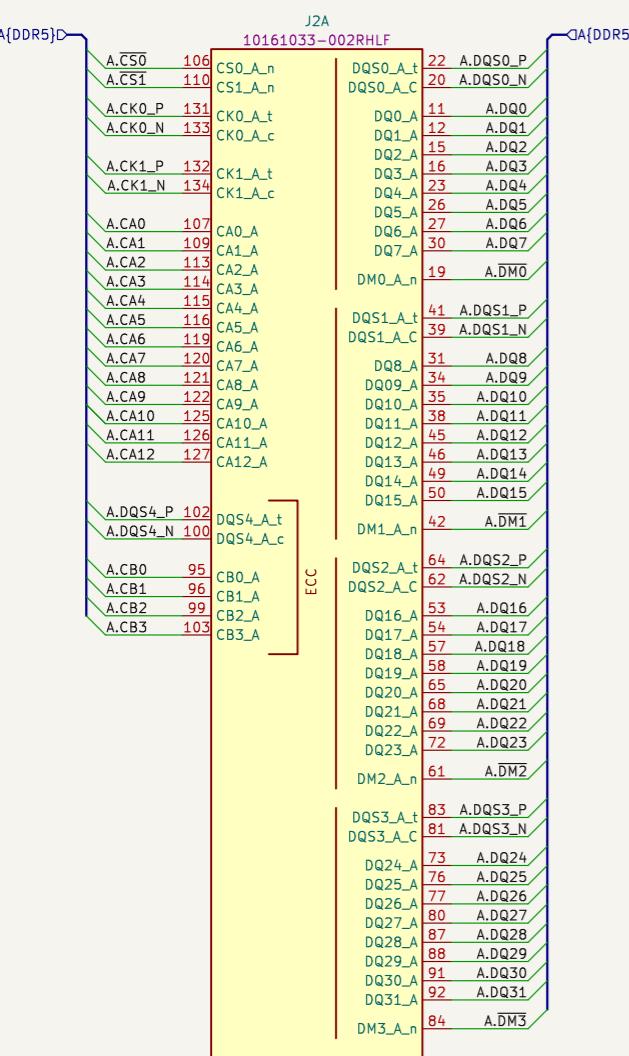
## Configuration Modes

For details, see UG470 p. 21

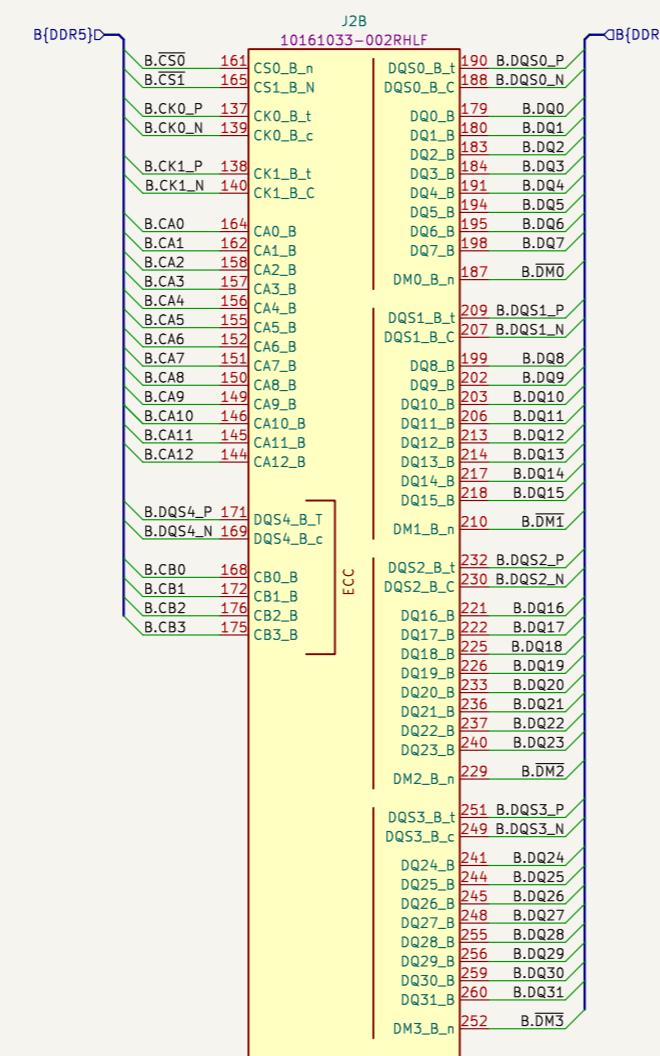


# DDR5 SODIMM connector

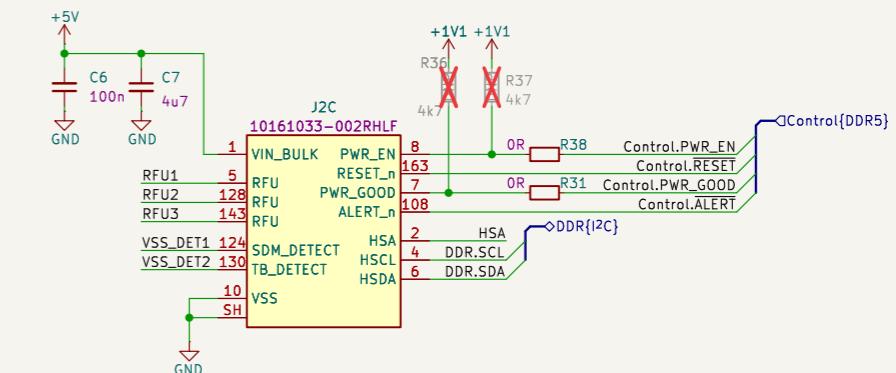
Subchannel A



Subchannel B

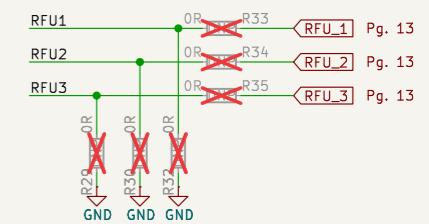
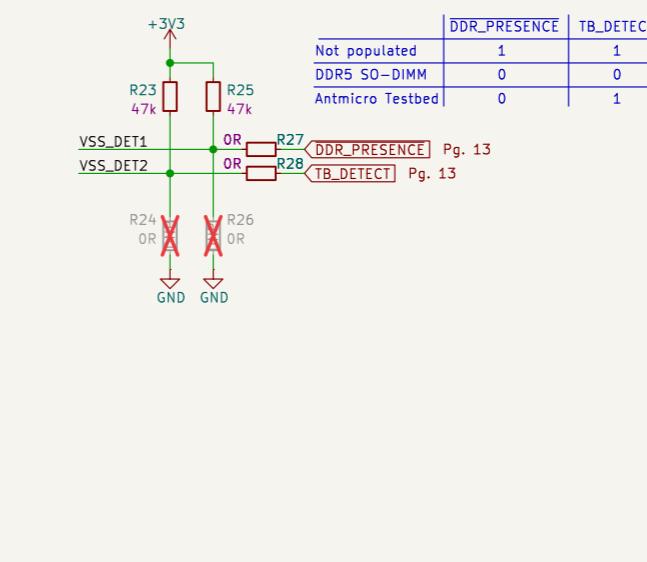


Power and control

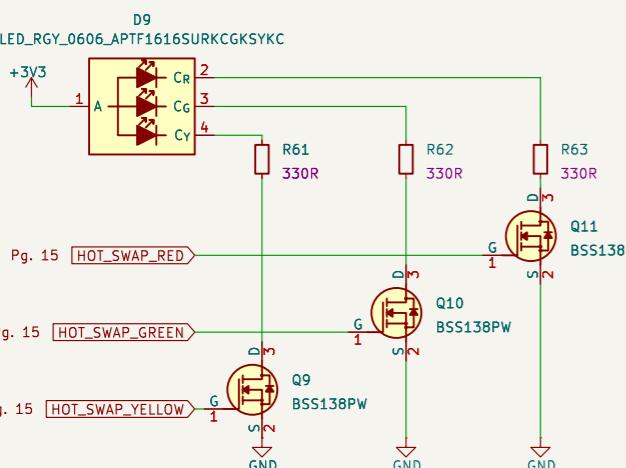


Optional RFU

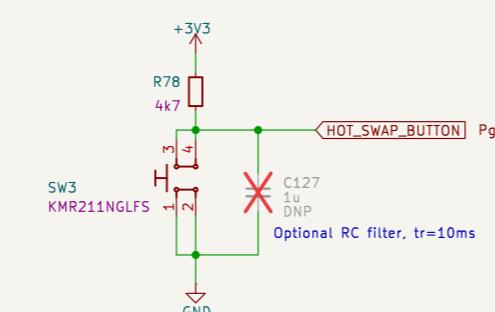
SO-DIMM type detect



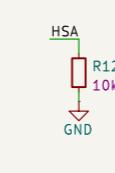
HOT SWAP status LED



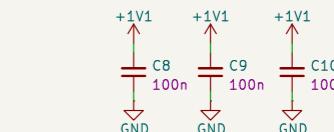
HOT SWAP eject button



Serial address select  
Default 000



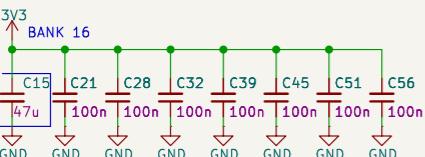
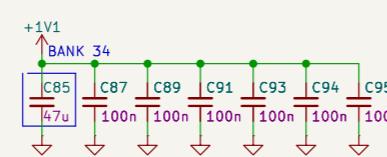
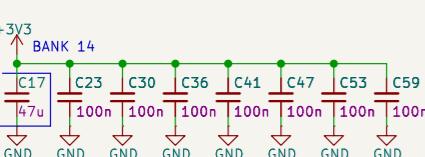
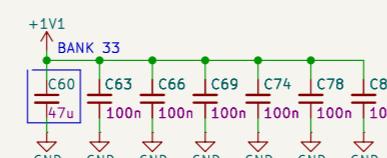
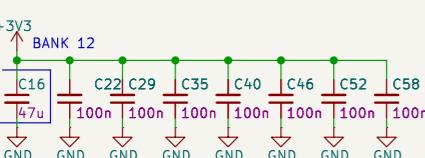
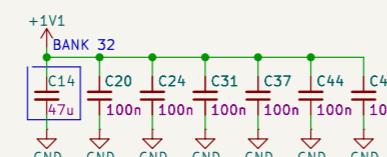
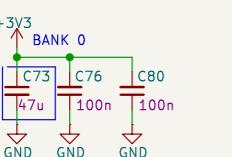
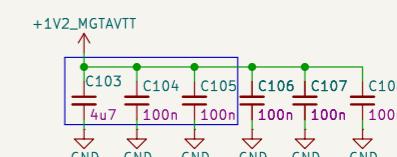
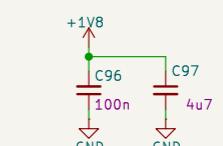
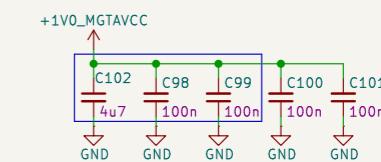
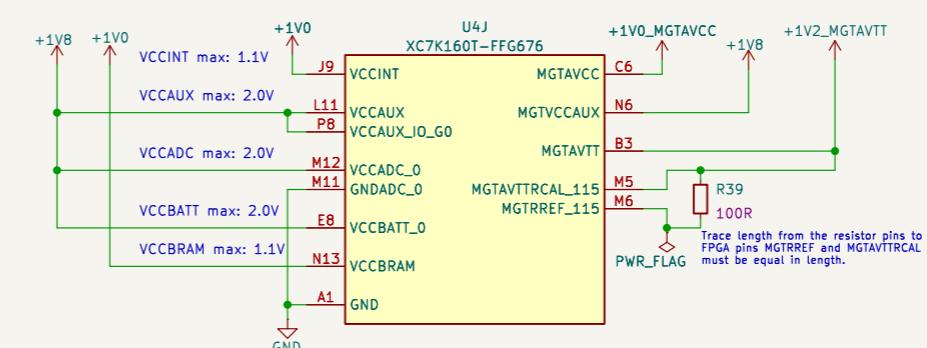
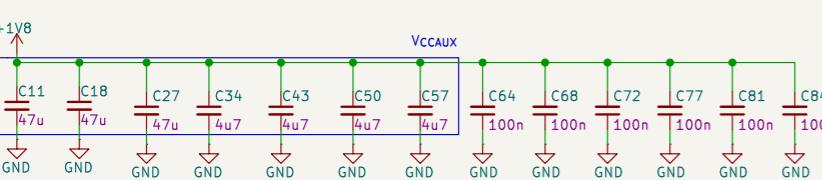
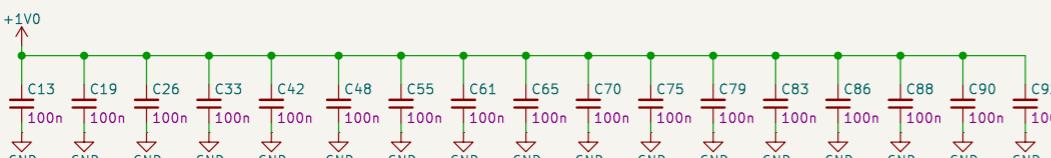
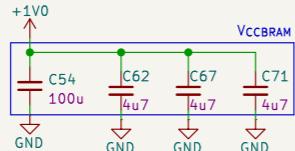
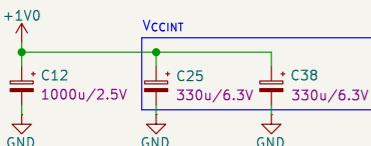
Plane decoupling



**FPGA Power rails**

Bank marked by dashed line  
referenced from 7 Series FPGAs  
PCB Design Guide UG483  
(FFG+FBG Package worst case)  
MGT decoupling marked by dashed line  
referenced from 7 Series FPGAs  
PCB Design Guide UG482  
(FFG+FBG Package worst case)

A



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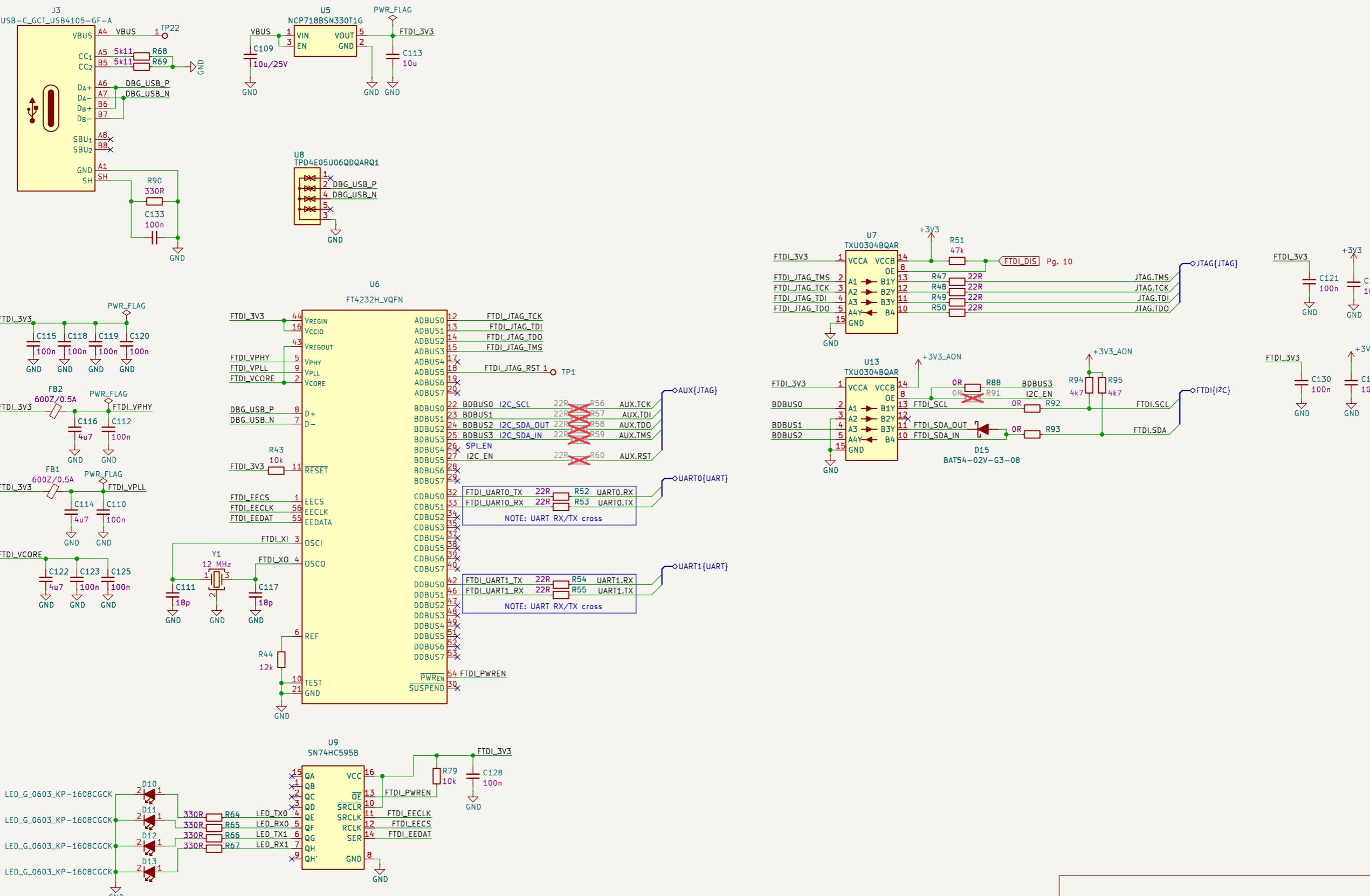
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File: fpga-power.kicad\_sch

**Title: SO-DIMM DDR5 Tester**

Size: A3 Date: 2024-01-18  
KiCad E.D.A. kicad-cliv 7.0.11

Rev: 1.1.1:89245  
Id: 5/17

# Debug FTDI



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Sheet: /Debug\_FTDI/  
File: debug-ftdi.kicad\_sch

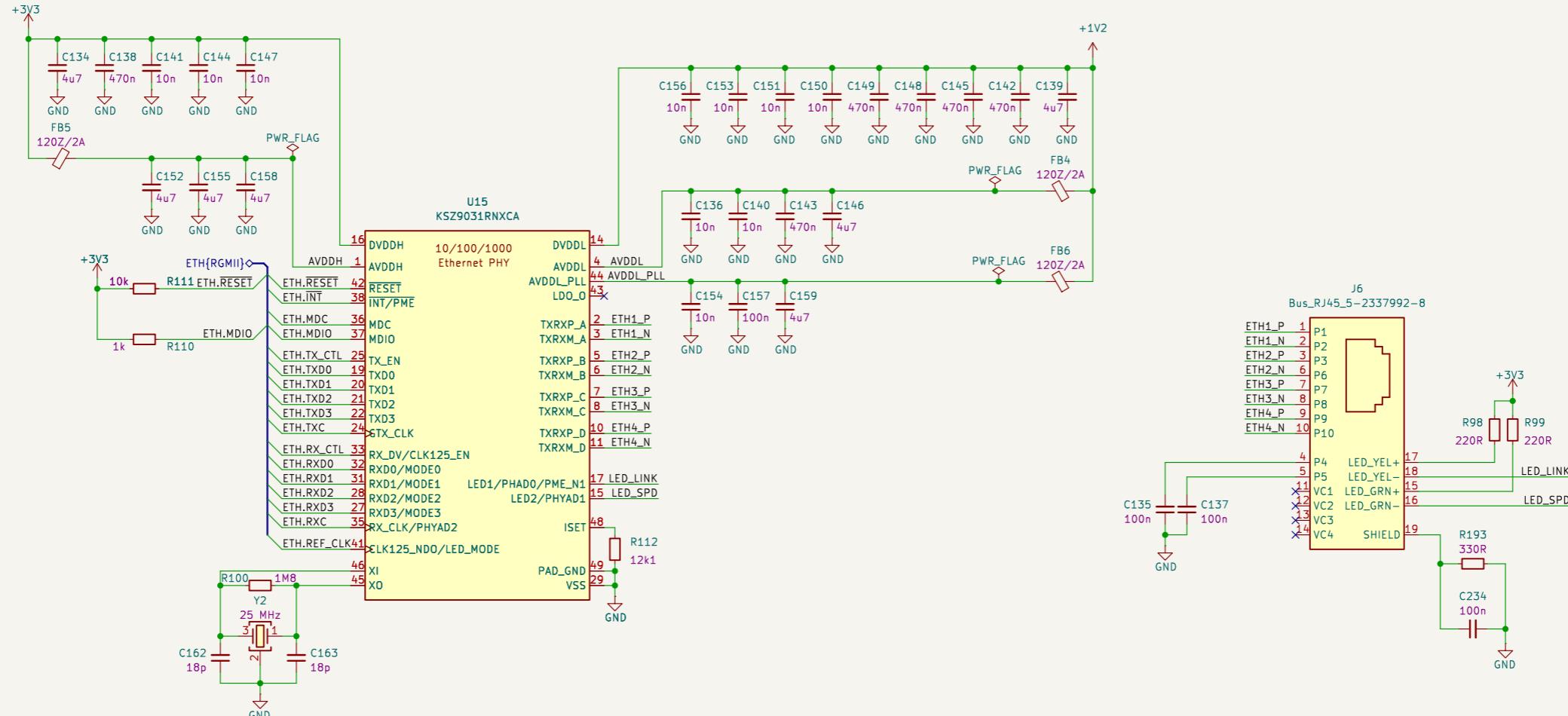
Title: SO-DIMM DDR5 Tester

Size: A3 Date: 2024-01-18  
KiCad E.D.A. kicad-cli 7.0.11

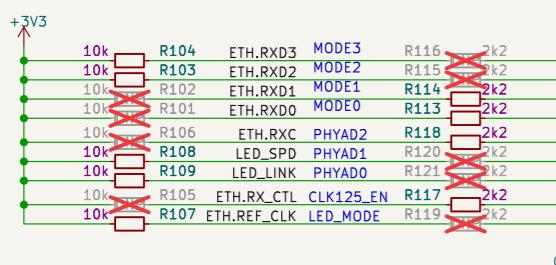
Rev: 1.1.1:89245  
Id: 6/17



# Gigabit Ethernet

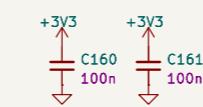


## Bootstrap configuration



MODE[3:0] : 1100 (RGMII mode – Advertise 1000BASE-T full-duplex only)  
PHYAD[4:0] : 00011  
CLK125\_EN: 0, disabled  
LED\_MODE: 1, Single-LED mode

## Reference plane decoupling



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Sheet: /Ethernet/

File: ethernet.kicad\_sch

Title: SO-DIMM DDR5 Tester

Size: A3 Date: 2024-01-18

KiCad E.D.A. kicad-cliv 7.0.11

Rev: 1.1.1:89245

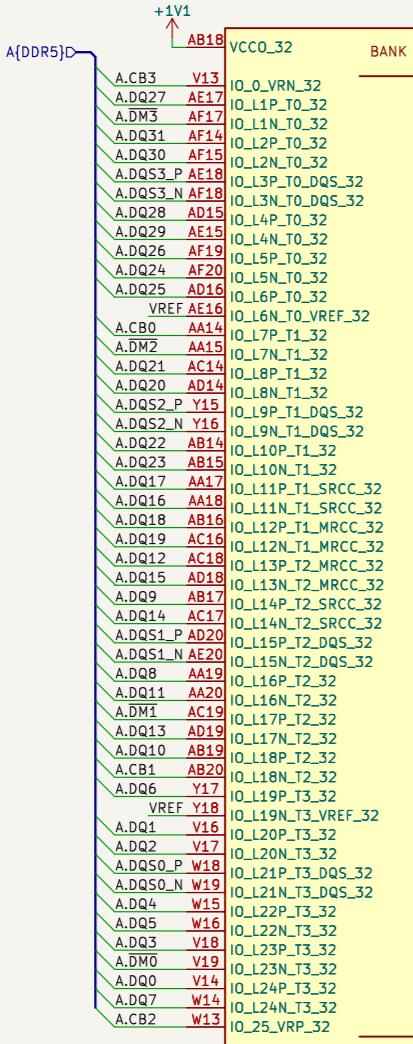
Id: 8/17

**HP Banks**

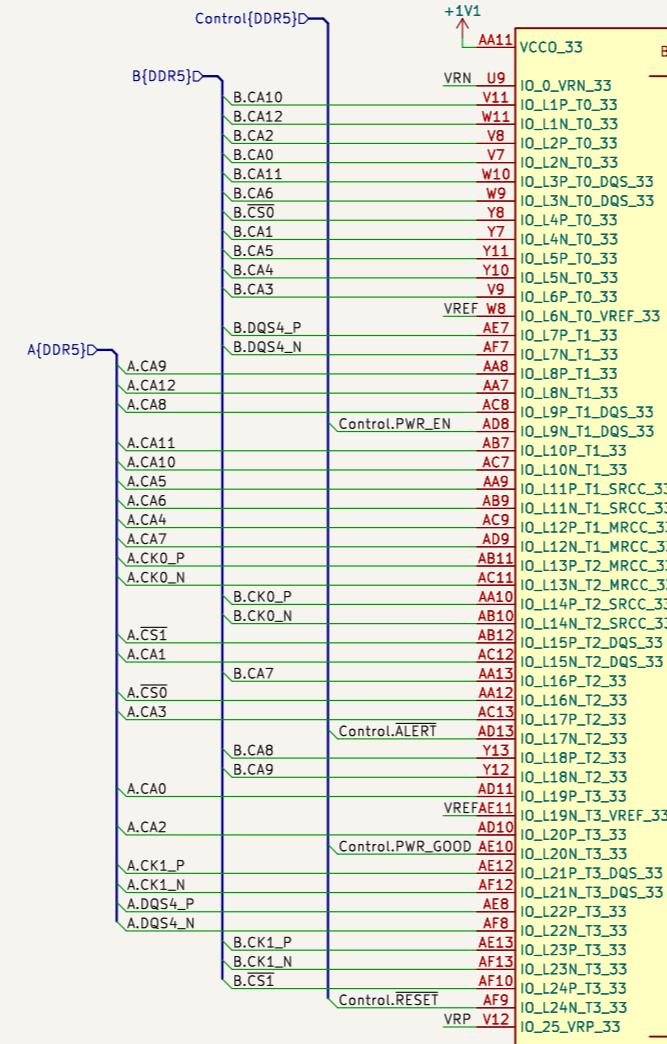
VCCO (HP banks) max: 2.0V

A

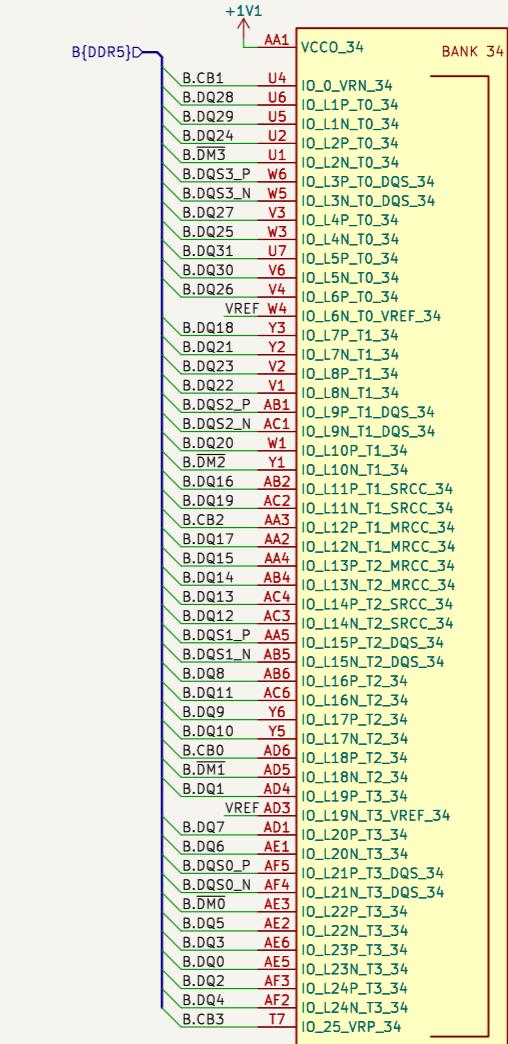
BANK 32



BANK 33



BANK 34



B

C

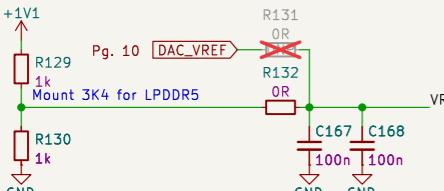
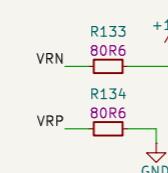
D

A

B

C

D

**VREF****Reference termination**

**open source  
hardware**

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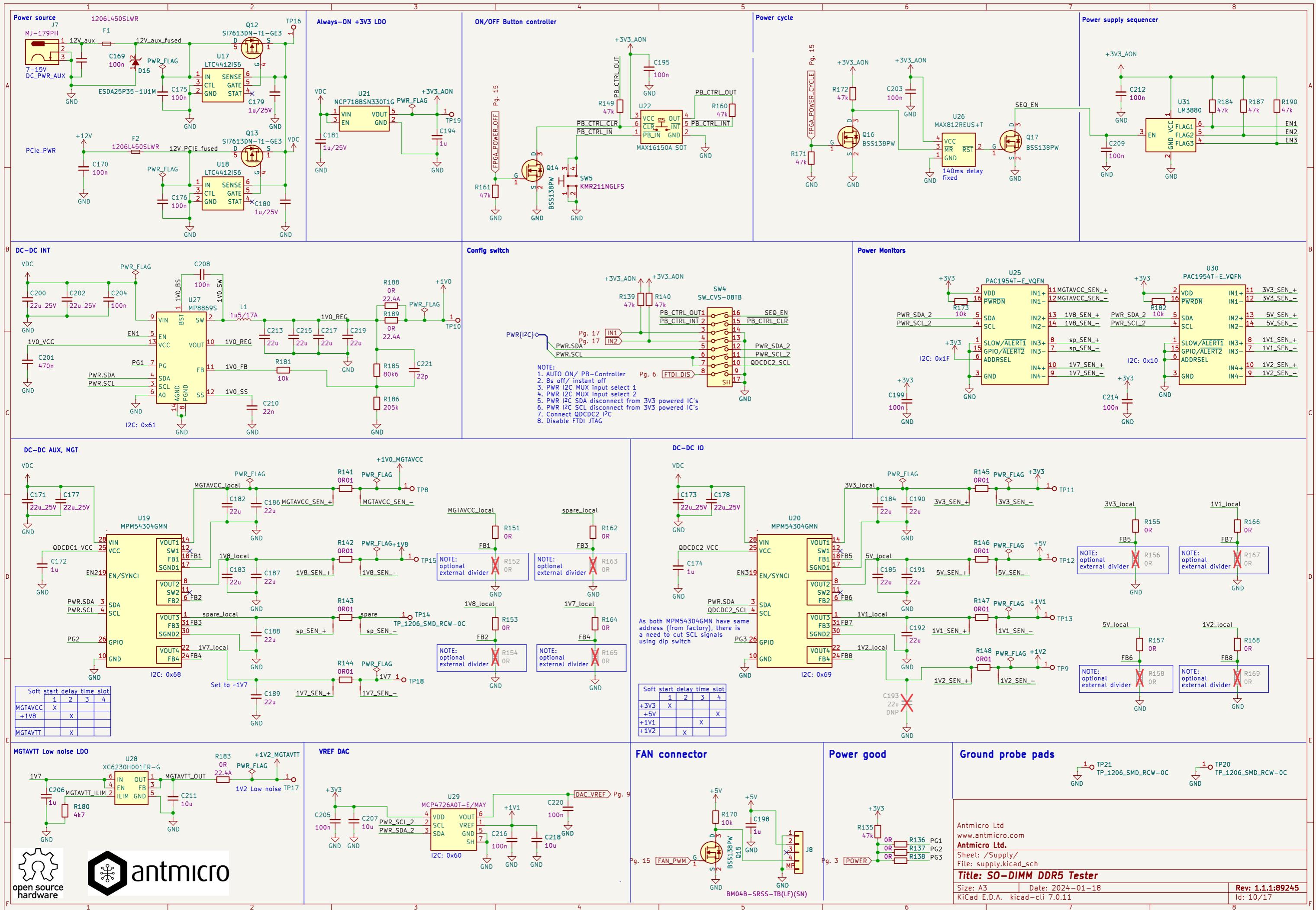
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File: fpga-banks-32-34.kicad\_sch

Title: SO-DIMM DDR5 Tester

Size: A3 Date: 2024-01-18  
KiCad E.D.A. kicad-cl 7.0.11

Pinout D.1.1

Rev: 1.1.1:89245  
Id: 9/17



**MGT Interface**

A

A

B

B

C

C

D

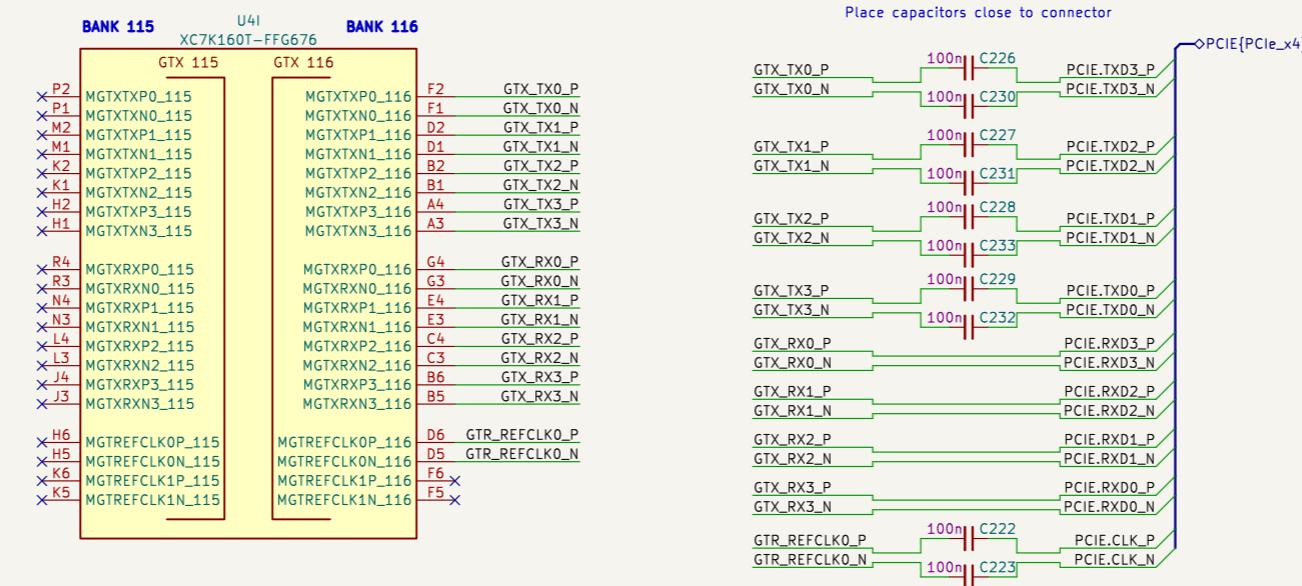
D

E

E

F

F



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Sheet: /FPGA MGT Interface/  
File: fpga-mgt.kicad\_sch

**Title: SO-DIMM DDR5 Tester**

Size: A3 | Date: 2024-01-18  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 1.1.1:89245  
Id: 11/17

PCIe

A

B

C

D

E

F

A

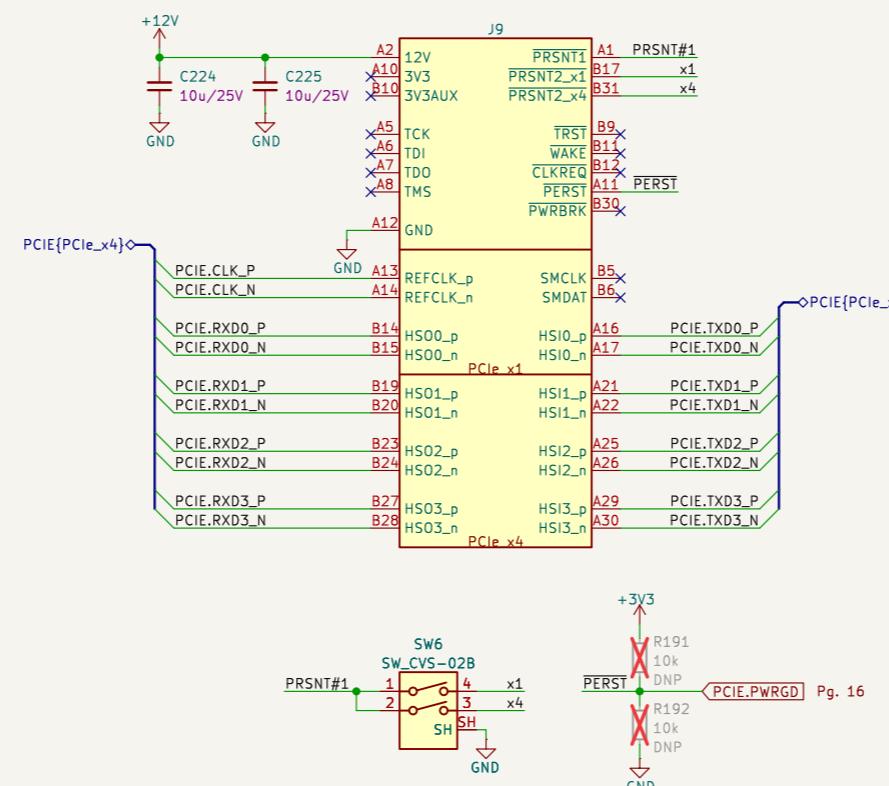
B

C

D

E

F



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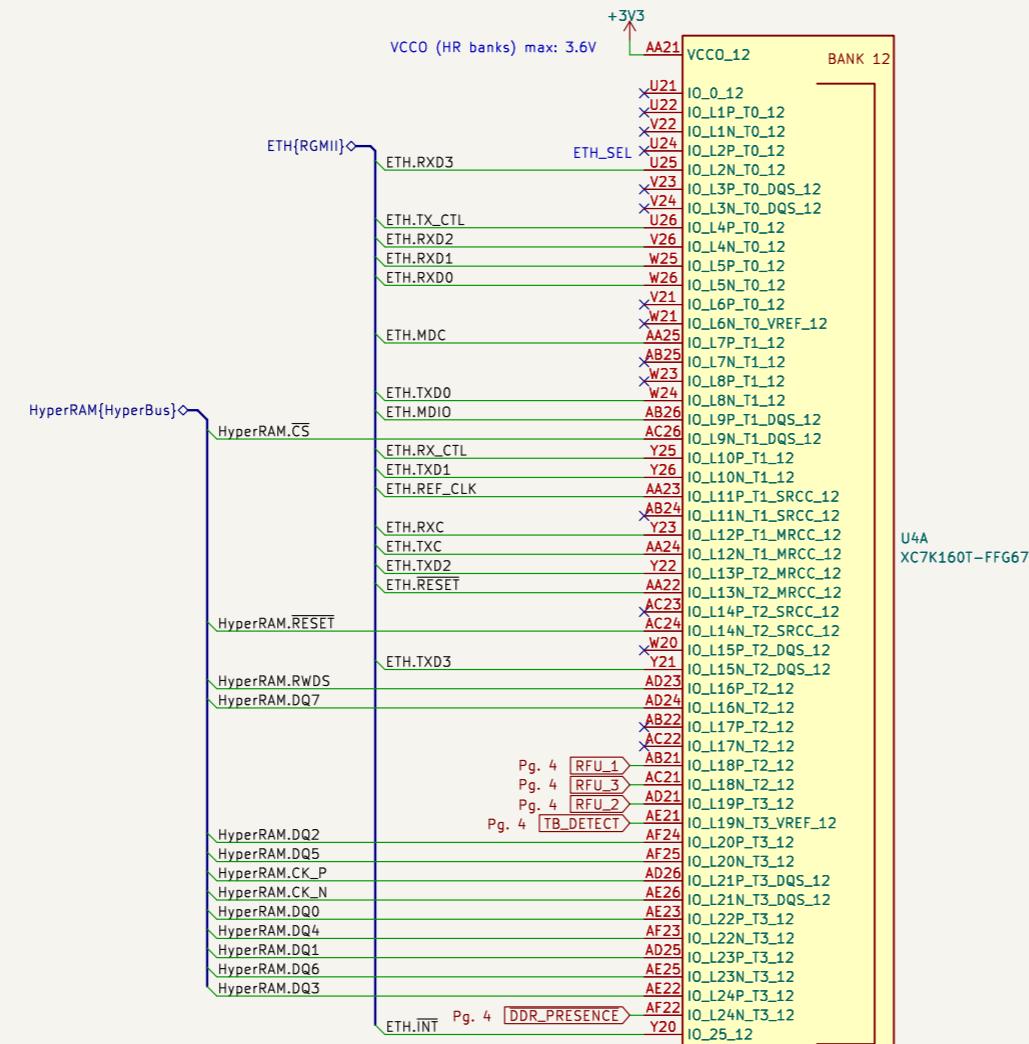
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File: pcie-connector.kicad\_sch

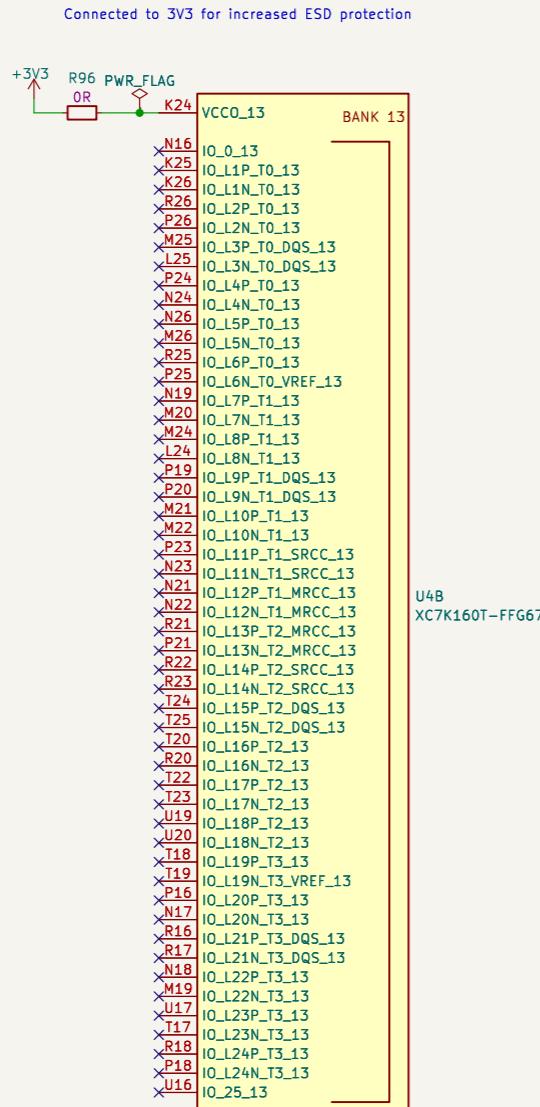
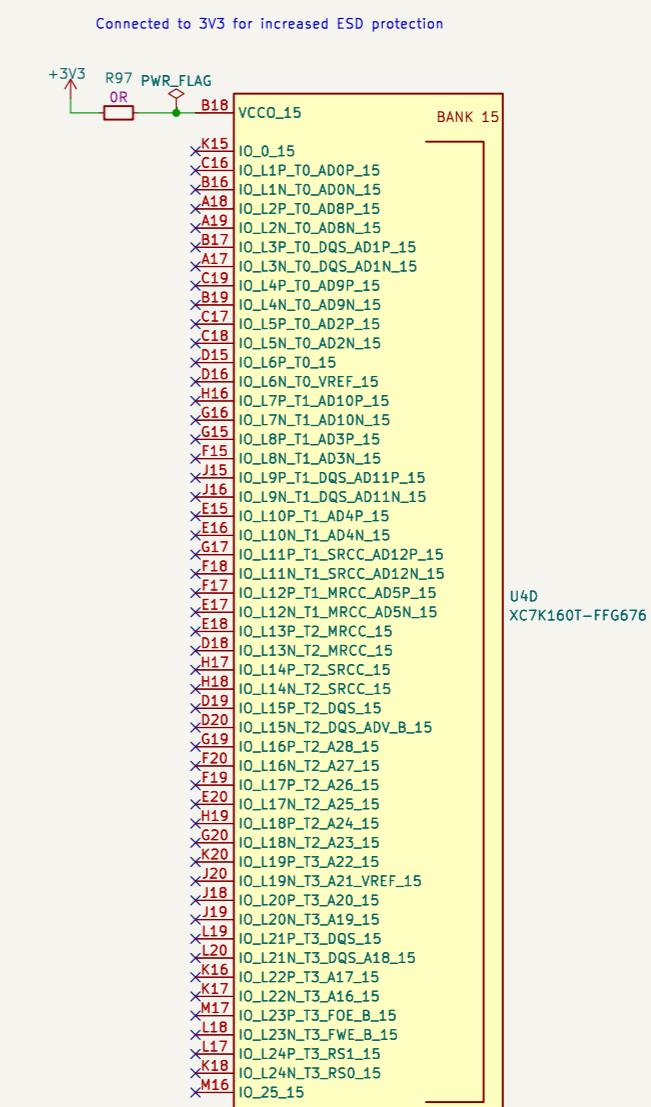
**Title: SO-DIMM DDR5 Tester**

Size: A3 | Date: 2024-01-18  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 1.1.1:89245  
Id: 12/17

BANK 12



**BANK 13****BANK 15**

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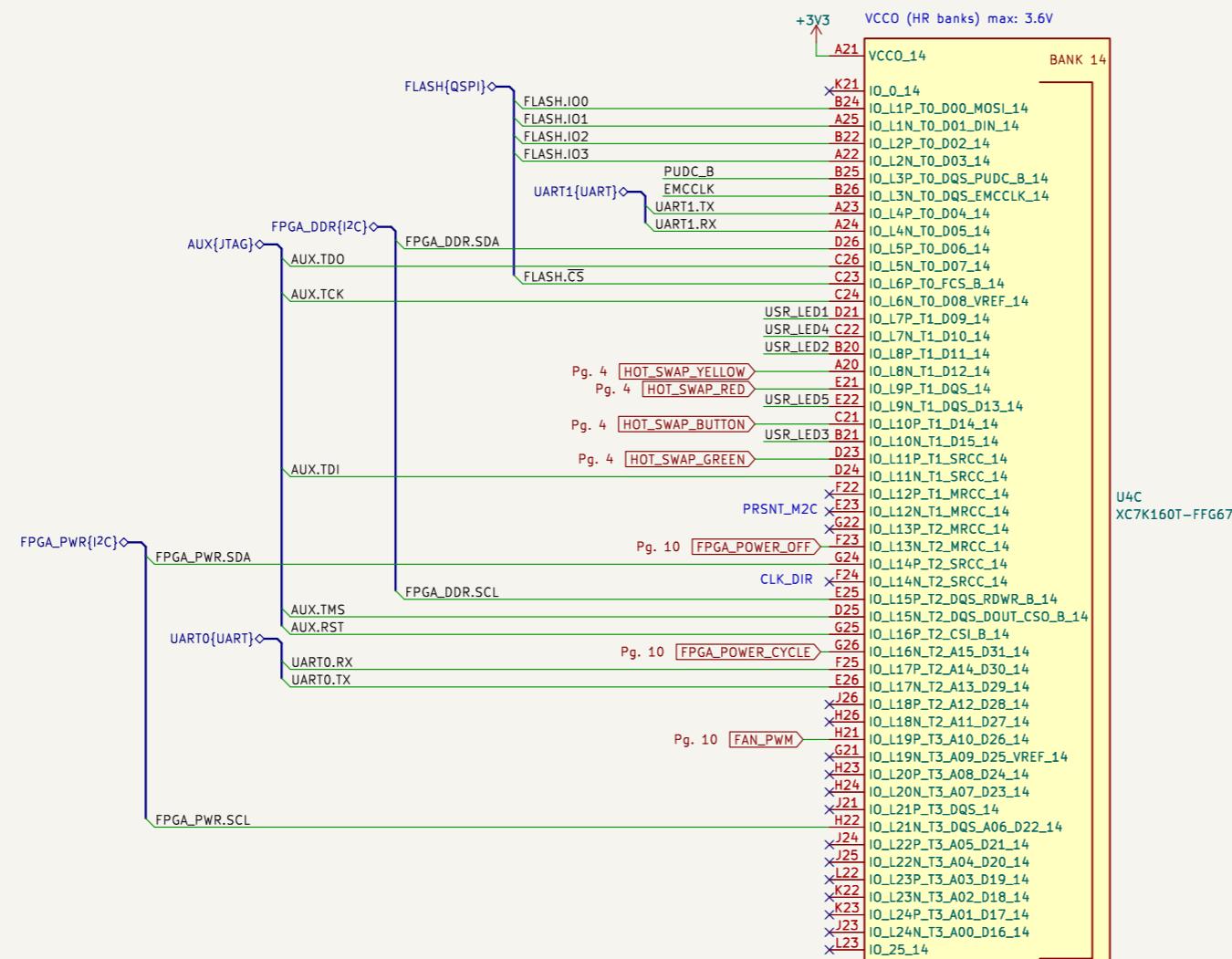
Sheet: /FPGA banks unused/  
File: fpga-bank-13-15.kicad\_sch

**Title: SO-DIMM DDR5 Tester**

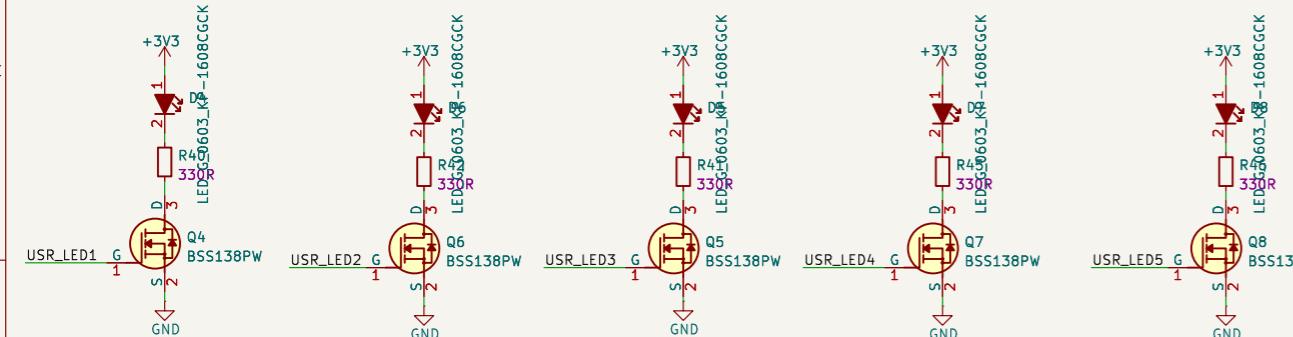
Size: A3 Date: 2024-01-18  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 1.1.1:89245  
Id: 14/17

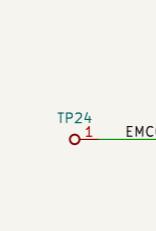
BANK 14



## User LEDs



## Probe



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Sheet: /FPGA bank 14/  
File: fpga-bank-14.kicad\_sch

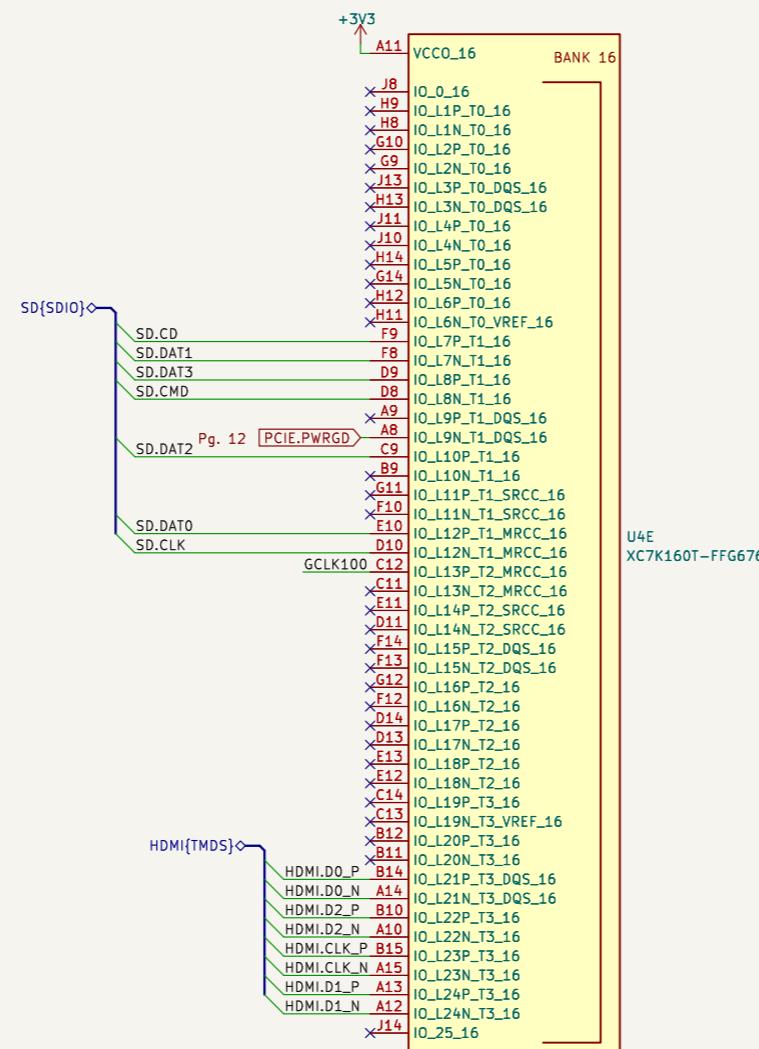
## Title: SO-DIMM DDR5 Tester

Size: A3 Date: 2024-01-18  
KiCad E.D.A. kicad-cli 7.0.11

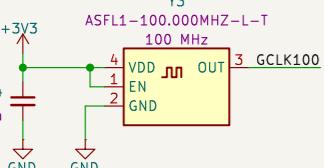
7

BANK 16

VCCO (HR banks) max: 3.6V



## Clock source



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Sheet: /FPGA bank 16/  
File: fpga-bank-16.kicad\_sch

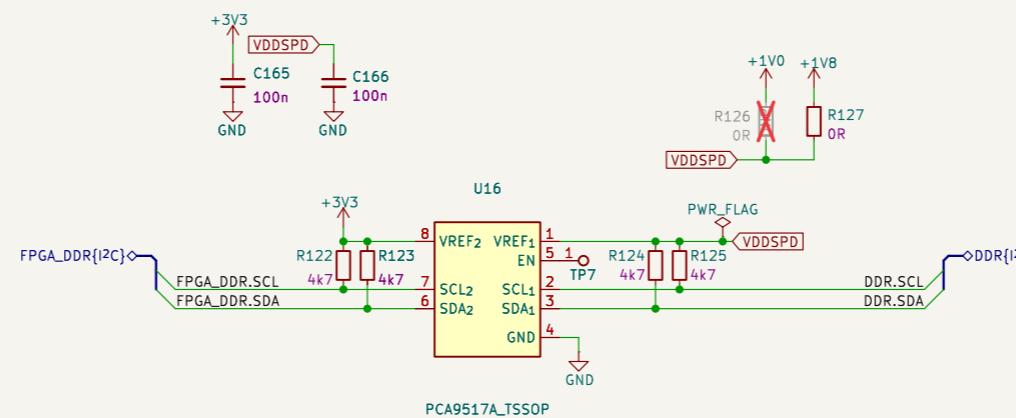
Title: SO-DIMM DDR5 Tester

Size: A3 Date: 2024-01-18  
KiCad E.D.A. kicad-cli 7.0.11

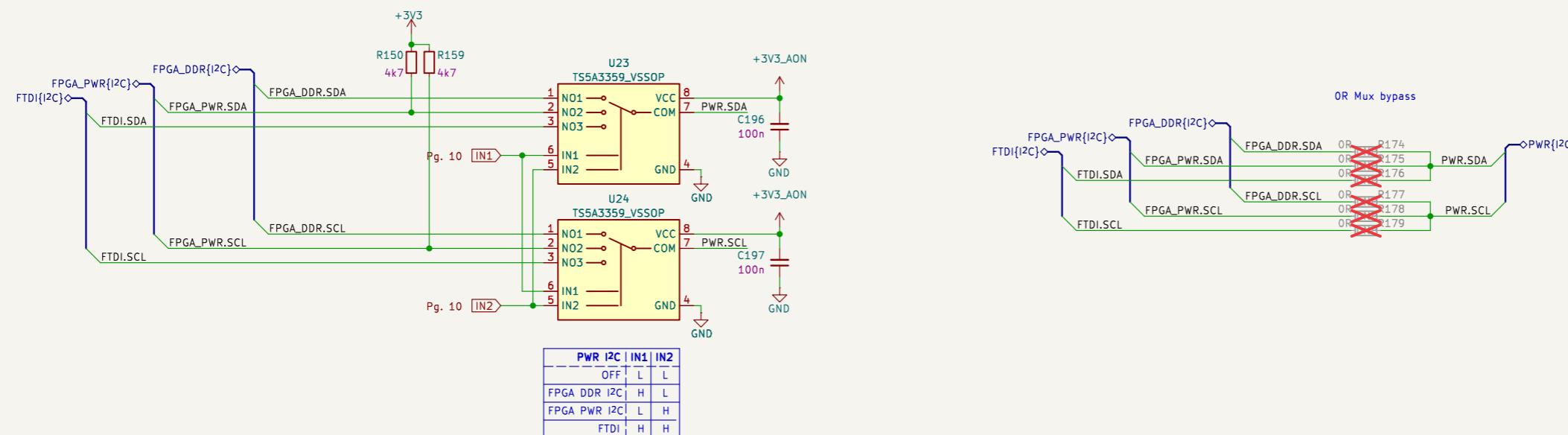
7

Rev: 1.1.1:89245  
Id: 16/17

## I2C logic translator



## PWR I2C MUX



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Sheet: /I2C/  
File: i2c.kicad\_sch

**Title: SO-DIMM DDR5 Tester**

Size: A3 | Date: 2024-01-18  
KiCad E.D.A. kicad-cli 7.0.11

Rev: 1.1.1:89245  
Id: 17/17

