Microfabrication Work Description

Devrim Kilinc

This document describes the microfluidic devices we are intending to develop and the method for their fabrication. Two-layer photolithography in a standard clean room environment is required.

Material and equipment required:

- Photomask containing microchannels features (Photomask # 1)
- o Photomask containing chamber features (Photomask # 2)
- o Photoresist SU8-2002 or similar
- o Photoresist SU8-2100 or similar
- o Spin coater
- o Developer for the photoresist
- o Hot plate and/or oven
- o Mask aligner Suss MicroTec MA/BA6 or similar
- o Dicer (optional)

Fabrication process: The fabrication of these devices requires two-step photolithography. ¹⁻² Major steps of the process are as follows:

- 1. Spin-coat 1st layer of photoresist (SU8-2002) on silicon wafer (4" or 5")
- 2. Pre-bake
- 3. Expose to UV using photomask #1
- 4. Post-bake
- 5. Develop 1st layer
- 6. Spin-coat 2nd layer of photoresist (SU8-2100)
- 7. Pre-bake
- 8. Expose to UV using photomask #2 on a mask aligner
- 9. Post-bake
- 10. Develop 2nd layer
- 11. Dice the wafer if possible

Quantities: Ideally, we would test as many design options and parameters by fabricating a small number of devices (2-3 copies of 4" silicon wafer) and later replicate successful designs using another set of photomasks to obtain multiple copies (3-4 additional master devices) of desired devices. We would like to fabricate the first master as soon as possible, but we will be more flexible regarding the second part of the work. The total amount of the final products will depend on the costs incurred.

Feasibility: I will provide the mask designs, i.e., the drawing files for mask production. I would be happy to get input regarding the mask design. If the IEMN Centrale de Micro et Nano Fabrication has the capacity to print their own masks (chrome-on-glass is preferred for Photomask #1), I would be happy to

work with them to this end. Standard (or custom) alignment markers will be included according to the requirements of the facility/technician.

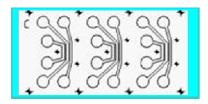
It is preferred to let the skilled staff at the IEMN Centrale to conduct the clean room work. I would be happy to provide them with technical documentation and a detailed workflow, if required. If such a service cannot be provided within a reasonable time period (such that the overall project is delayed), then I can conduct the clean room work. I have over 8 years of experience in designing and testing similar microfluidic devices ³⁻⁶ and over 4 years of hands-on microfabrication experience in a Class 100 clean room environment (School of Chemistry, University College Dublin, Ireland) creating similar microfluidic devices. ⁷ If my access requires training and/or supervision, I would be happy to conform to the requirements of the facility.

Description of the devices: The devices requested consist of three parallel channels (75-100 μ m high; products of photomask #2) that are interconnected with two sets of narrowing microchannels (3-4 μ m high; products of photomask #1) to guarantee unidirectional neurite growth. The minimum feature sizes for photomasks #1 and #2 are typically 1 and 5 μ m, respectively. Draft technical drawings of two particular device designs are provided below.

The distances between pre-synaptic and synaptic chamber and between synaptic and post-synaptic chambers determine the microchannel lengths, which are adjusted to guarantee axonal/dendritic growth from pre- and post-synaptic chambers, respectively. The density of microchannels defines how quickly the chamber is populated by neurites. The synaptic chamber bifurcates into two inlet channels, both of which are controlled by simple pin-valves with approximately 1.5 mm in diameter. One of the inlet channels connects to a simple medium reservoir, whereas the other connects to an additional cell chamber, reserved co-culture. The latter connection may occur through direct contact or through a third set of parallel microchannels that would act as a filter for motile cells.

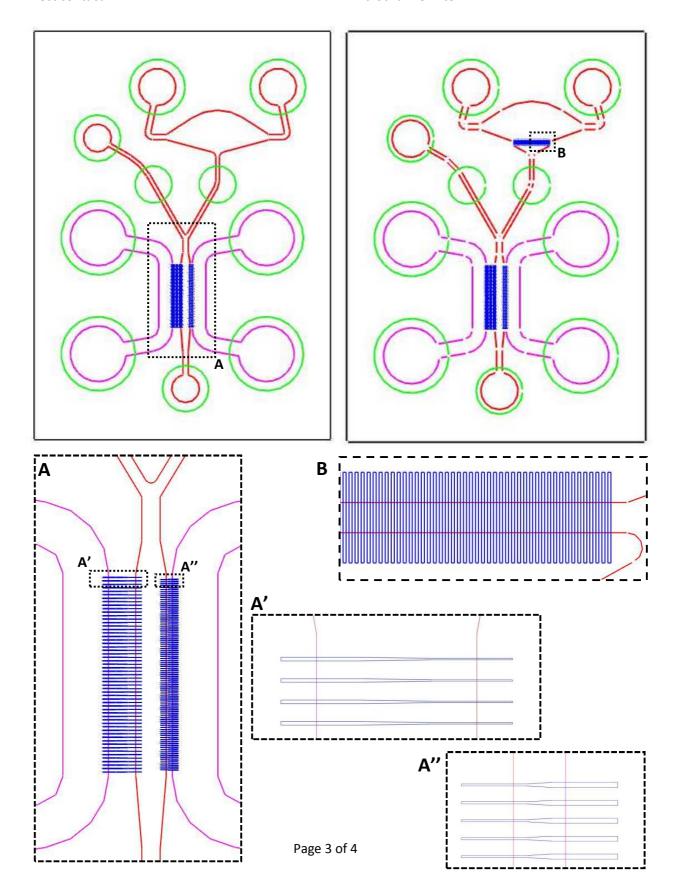
Photomask design:

The draft design fits to 16×22 mm area with sufficient margins. This is suitable for 24×24 mm square coverslips (single circuit) and 50×24 mm rectangular coverslips (triple circuit format as shown below).



Four such "triple"s can fit in a 4" silicon wafer.

Design alternatives for glass-bottom multiwell format will be developed.



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