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Experiment Title	Silicon oxide etching by HF vapor

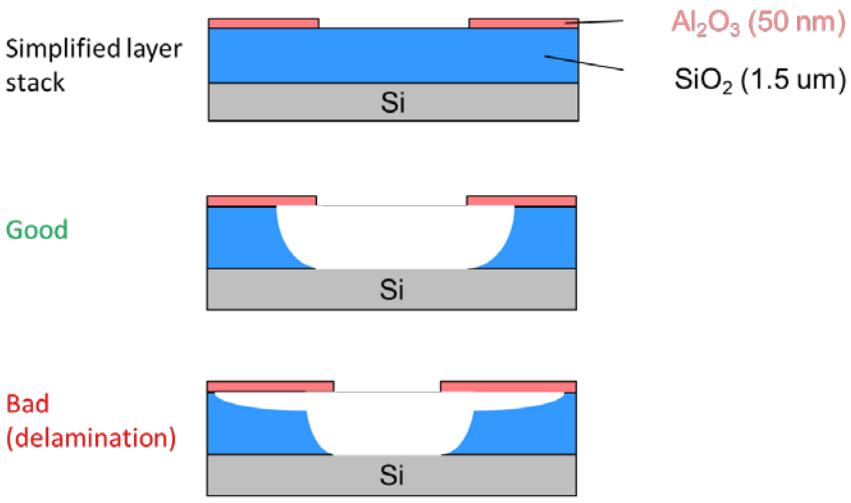
Objectives

Etching of samples (layers from bottom to top) by Primaxx HF vapor etcher with EtOH:

- Si substrate 500 um
- Thermal SiO_2 1.5 um (layer to be etched)
- Al_2O_3 25 nm (hard mask)
- Different materials depending on sample (see sample types below)
- Al_2O_3 25 nm (hard mask)

- Target:
  - Etching of 1.5 um silicon dioxide with Al_2O_3 hard mask
  - No excessive undercut or delamination
  - No damage of hard mask
  - No adverse interaction with materials used on samples

Example for successful and non-successful etch (layer stack simplified)



Pretest by PTA staff: 2 etching runs (all analysis will be performed at ETH)

- Determine if delamination free etching can be achieved with Primaxx Monarch 3 HF vapor etcher using a standard recipe by SPTS (see below)
- Test if dummy structures give results close to real structures
- Test how SU-8 on Al_2O_3 reacts in HF vapor with EtOH
- Test if samples are compatible with process or if incompatibilities occur
- Determination of etching results: Analysis will be performed by ETH staff at ETH

Etching experiments by ETH staff at PTA

- Optimization of etching recipe if required (est. 5 runs + 5x analysis)
- Etching of real devices (test run + analysis + real run), estimate of 6x in 2014

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Method

Recipe for pretest by PTA staff:

- Bake at 200°C for 2 min
- Vapor HF with EtOH on Primaxx etcher
  - Conditions 125 torr, 310 HF , 350 EtOH, 1250 N_2
  - Run #1: 3 x 16.25 minutes etching time (3 step process), the etching times do not include stabilization times
  - Run #2: 4 x 16.25 minutes etching time (4 step process), the etching times do not include stabilization times
    (see Figure below for image of samples)

Etching of real devices by ETH staff at PTA

- Recipe depends on results of pretest
- Analysis by SEM/ profilometer/ AFM

Sample description

Sample types

- Type 1: Dummy chip in package
  - Dummy test chip in CLCC 32 ceramic package (11 mm x 14 mm)
  - Chip (6 mm x 6 mm) glued into package with PMMA
  - Layer stack from bottom to top: Si 500 um, SiO_2 1.5 um, ALD Al_2O_3 50 nm
  - May contain residues of Au, Cr, Al, PMMA, LOR, AZ5214E, CNTs
  - Substances the chip was in contact with: LOR, blue tape, DI-water, DMSO, acetone, IPA, RCA SC-1, RCA SC-2, Cr, PMMA, MIBK, Cr etchant, H_3PO_4, HCl, NMP

- Type 2: Dummy chip w/o package
  - Dummy test chip w/o package
  - Chip (6 mm x 6 mm)
  - Layer stack from bottom to top: Si 500 um, SiO_2 1.5 um, ALD Al_2O_3 50 nm
  - May contain residues of Au, Cr, Pd, PMMA, LOR, AZ5214E, CNTs
  - Substances the chip was in contact with: LOR, blue tape, DI-water, DMSO, acetone, IPA, RCA SC-1, RCA SC-2, Cr, PMMA, MIBK, Cr etchant, H_3PO_4, HCl, NMP

- Type 3: Dummy chip with SU-8
  - Dummy test chip w/ SU-8 structures
  - Chip (6 mm x 6 mm)
  - Layer stack from bottom to top: Si 500 um, SiO_2 1.5 um, ALD Al_2O_3 50 nm, SU-8 pillars
  - SU-8 pillars: approx. 2 um high, 800 nm diameter
  - May contain residues of Au, Cr, Pd LOR, CNTs, PMMA, AZ5214E
  - Substances the chip was in contact with: LOR, blue tape, DI-water, DMSO, acetone, IPA, RCA SC-1, RCA SC-2, SU-8 developer

- Type 4: Realistic device structure containing also CNTs
  - Chip in CLCC 32 ceramic package (11 mm x 14 mm)
  - Chip (6 mm x 6 mm) glued into package with PMMA, bonded with Al wire
  - Layer stack from bottom to top: Si 500 um, SiO_2 1.5 um, ALD Al_2O_3 25 nm, single-walled carbon nanotubes, Cr 2nm, Au 40-60 nm, ALD Al_2O_3 25 nm
  - May contain residues of LOR, AZ5214E, PMMA, Nitto Denko Revalpha thermal transfer tape type 3198M, iron oxide, Pd

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- Substances the chip was in contact with: LOR, blue tape, DI-water, DMSO, acetone, IPA, RCA SC-1, RCA SC-2, Cr, AZ5214E, TMAH, NMP, PMMA, MIBK, Cr etchant, H_3PO_4, HCl

Samples in sample box for pre-test at PTA by PTA staff: