Etapes technologiques prévues pour la fabrication du composant de doublage de fréquence

TASK 2 : Wafer Fabrication

Task 2 corresponds to the fabrication of the hybrid wafer. A mask to pole the LiNb3 wafer with the proper period defined in task 1 will be fabricated.

A three steps process will be pursued as described in figure 2. 4" diameter commercial z-cut $LiNbO_3$ wafers will be periodically poled. Then, the poled (PPLN) wafer will be bonded to a substrate. Typical substrates are silicon wafers. Either thermal bonding with an appropriate buffer layer or dielectric adhesive can be employed. Then the fabricated hybrid wafer will be ground and polished to obtain a thin and uniform LiNbO3 layer whose thickness corresponds to the design of task 1.

Several rounds may be necessary to reach the desired layer uniformity and thickness.

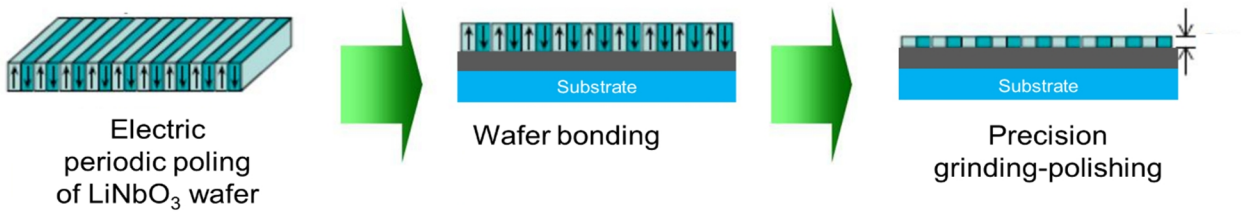

Figure 2 : schematic description of the hybrid wafer fabrication process

TASK 3 : Chip fabrication and characterization

Task 3 concerns the fabrication and characterization of the PPLN waveguides. The wafer from task 2 will be diced to give waveguides of different lengths by a Disco precision saw equipped with a diamond blade. Waveguides will be first analyzed by visual inspection and selected waveguides will be individually characterized. Conversion efficiency will be measured first. Waveguides with appropriate characteristics according to table 1 will be sorted for further characterization (power handling, long term stability).

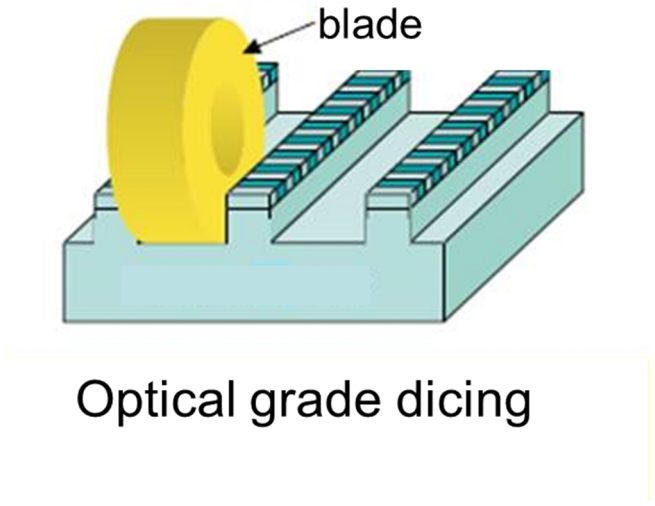

Figure 3 : schematic description of the dicing of PPLN waveguides