StarFive
赛昉科技

JH7110 Boot User Guide

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VisionFive 2

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Important legal notice before reading this documentation.

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Contact Us

Address: Room 502, Building 2, No. 61 Shengxia Rd., China (Shanghai) Pilot Free Trade Zone, Shanghai, 201203, China

Website: http://www.starfivetech.com

Email:

- Sales: sales@starfivetech.com
- Support: support@starfivetech.com

Preface

About this guide and technical support information.

About this document

This document mainly provides the StarFive JH7110 users and partners with a high-level understanding of how their SoC JH7110 and single board computer VisionFive 2 are boot up.

Revision History

Table 0-1 Revision History

Version	Released	Revision
1.1.3	2023/05/10	Updated Boot Mode Settings *(on page 15)*.
1.1.2	2022/02/02	Minor change. Corrected a typo in the offset value in Boot Address Allocation *(on page 7)*.
1.1.1	2022/01/19	Minor change. Removed duplicate sections delivered also in other documents.
1.1	2022/01/18	Refined the boot process and republish.
1.0	2022/01/16	First official release.

Notes and notices

The following notes and notices might appear in this guide:

- **Tip:**
  Suggests how to apply the information in a topic or step.
- **Note:**
  Explains a special case or expands on an important point.
- **Important:**
  Points out critical information concerning a topic or step.
- **CAUTION:**
  Indicates that an action or step can cause loss of data, security problems, or performance issues.
- **Warning:**
  Indicates that an action or step can result in physical harm or cause damage to hardware.

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1. Introduction

1.1. Overview

This document is intended to:

- Introduce all the boot stages of booting a Linux operating system on JH7110.
- Provide instructions for how an image package is generated and where it is located.
- Provide instructions for how to write different media and where to boot.

The code sources referenced in this document are based on the following conditions:

- SDK version: 2.4.5
- OpenSBI v1.0
- U-Boot version: 2021.10
- Linux Kernel version: 5.15
- Hardware Board: VisionFive 2

Note:
For different U-Boot or Linux Kernel versions, these references may be slightly different.

File Locations

Locate the JH7110 *Software Development Kit (SDK)* with the following information.

- **Repository**: https://github.com/starfive-tech/VisionFive2
- **Branch**: JH7110_VisionFive2_devel
- **Tag**: Select the newest tag. For example, VF2_v2.11.5 is newer than VF2_v2.10.10.

1.2. Boot Sources

The power domain **AON_GPIO** is used to select the boot vector and BootLoader source and offer multiple methods to obtain the BootLoader image.

The JH7110 SoC can boot from one of the sources listed in the following table, as selected by the AON_GPIO[1,0] (0x1702002c).

Table 1-1 PAD_AON_GPIO Values for Boot Source Selection

Processor	BootROM	Boot Vector	Source List
U74	0x00_2A00_0000	0x00_1301_0000	Quad SPI NOR flash memory
		0x00_1601_0000	SDIO0 (eMMC)
		0x00_1602_0000	SDIO1 (SD card)
		0x00_1000_0000	UART0

1.3. Boot Address Allocation

The following table shows the boot allocation for 16 M Flash.

Table 1-2 16 M Flash Boot Address Allocation

Offset	Length	Description
0x0	0x80000	SPL
0xF0000	0x10000	U-Boot environment variables
0x100000	0x400000	`fw_payload.img` (OpenSBI + U-Boot)
0x600000	0x1000000	Reseved

The following table shows the boot allocation for SD Card or eMMC.

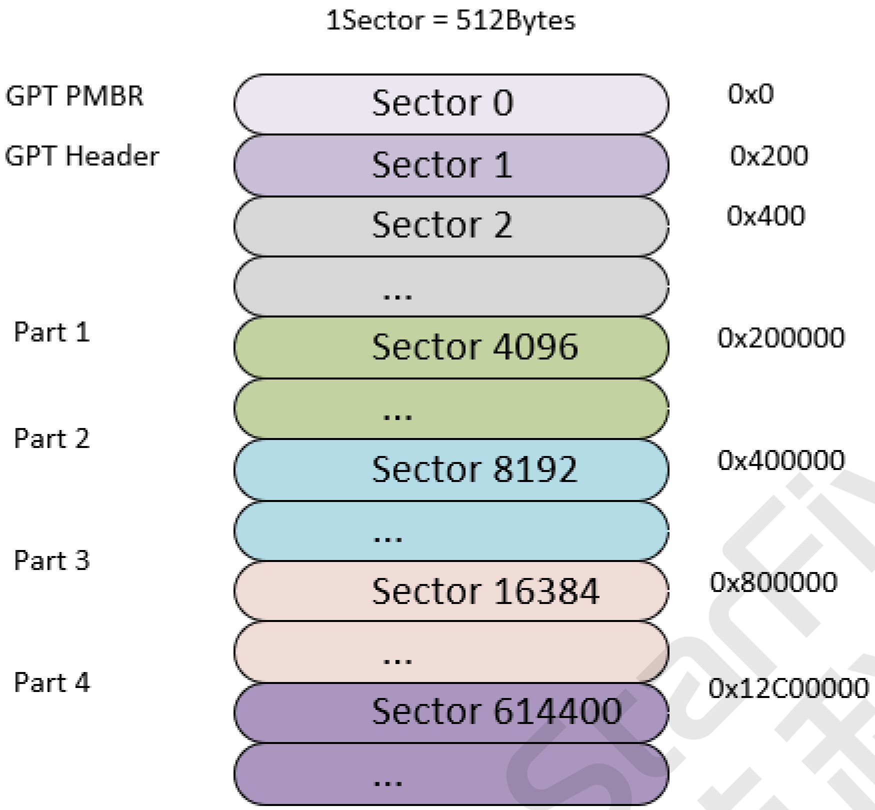
Table 1-3 SD/eMMC Boot Address Allocation

Offset	Length	Description	Comment
0x0	0x200	GPT PMBR	0x4: Backup address
0x200	0x200	GPT Header	
0x400	0x1F_FC00	Reserved	
0x20_0000	0x20_0000	SPL	Partition 1
0x40_0000	0x40_0000	`Fw_payload.img` (OpenSBI + U-Boot)	Partition 2
0x80_0000	0x1240_0000	Initramfs + `UEnv.txt`	Partition 3
0x12C0_0000	End of disk	System rootfs	Partition 4

1.4. BootROM

BootROM is a hard-coded boot program written in the address offset of 0x2A00_0000 on JH7110. The program is basically used to load and execute the Secondary Program Loader (SPL).

Figure 1-1 SD/eMMC Boot Address Partitions



BootROM enables developers to insert programs from different media accesses, including flash, eMMC, SD card and UART, by reading SPL to SRAM (0x8000000).

By using the bit of AON_GPIO[1,0] (0x1702002c), developers can confirm their boot mode.

The following table explains the procedure of how BootROM loads resources.

Table 1-4 How BootROM loads resources

GPIO1	GPIO0	Boot Source	Comments
0x0	0x0	Quad SPI NOR flash memory	Read SPL from Sector 0.
0x1	0x0	SDIO0 (eMMC)	Read SPL from Sector 0. If the CRC validation failed, the system will re-direct to a backup address. For compatibility, the pointer is usually set to the start of Sector 1.

0x0	0x1	SDIO1 (SD card)	Same as the above. The following code blocks provide an example.
			`second boot"--typecode=1:2E54B353-1271-4842-806F-E436D6AF6985`
			`second boot bak"--typecode=2:2E54B353-1271-4842-806F-E436D6AF6984`

0x1	0x1	UART0	When the system detects the boot-mode of UART has been chosen, it will enter Xmode Receiver Mode. Users can then import ELF files in Xmode mode using serial cable connections. Once the files are confirmed with transmission complete BootROM will run the ELF file automatically.

Note:
Besides in the BootROM, you can also change the backup address in the `spl_tool`.

For eMMC Boot

Make sure you know this before starting an eMMC boot.

1. Because the eMMC boot reads directly from the boot sector, which has an impact against the partition table. As a result, to boot up your JH7110 SoC on eMMC, you need to put an invalid SPL file in sector 0, to trigger the CRC validation failure.
2. Then, the system will re-direct to the start of Sector 1 and load the correct SPL file.

1.5. SPL

SPL is a boot program based on U-Boot. The primary use of SPL is to facilitate DDR initialization and to load the image file `fw_payload.img` (U-Boot + OpenSBI). SPL reads `fw_payload.img` from Partition 2 of the eMMC or SD card and then loads it to the address 0x40000000 of the DDR for operation.

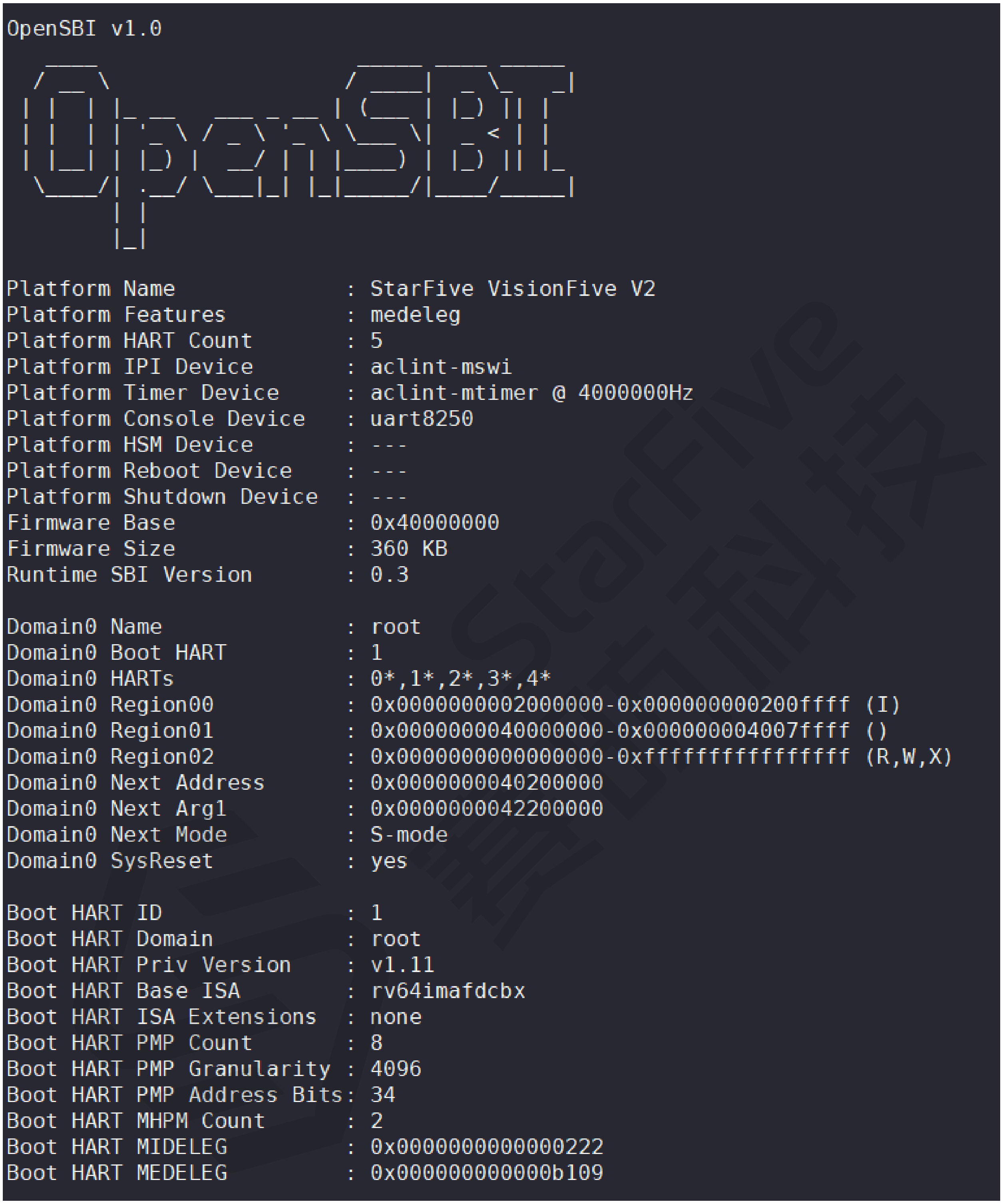
1.6. OpenSBI

The binary of OpenSBI is packaged with the binary compiled by U-Boot in the way of payload to generate the final `fw_payload.bin`. The main functions of OpenSBI are:

- Provide basic system calls for Linux
- Switch the mode from M mode to S mode
- Jump to 0x4020_0000 (located in DDR) to execute U-Boot

The normal output information is illustrated in the following figure.

Figure 1-2 OpenSBI Output Example

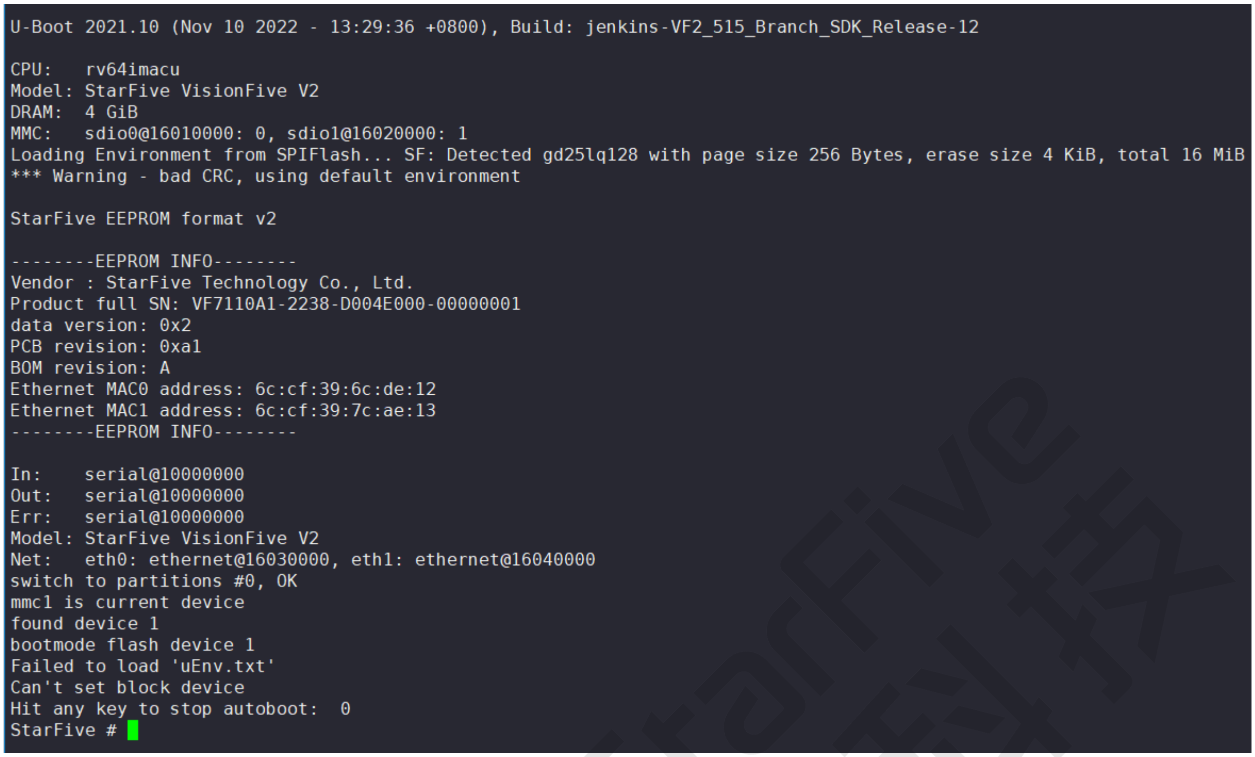


```
OpenSBI v1.0
   ____                    _____ ____ _____
  / __ \                  / ____|  _ \_   _|
 | |  | |_ __   ___ _ __ | (___ | |_) || |
 | |  | | '_ \ / _ \ '_ \ \___ \|  _ < | |
 | |__| | |_) |  __/ | | |____) | |_) || |_
  \____/| .__/ \___|_| |_|_____/|____/_____|
        | |
        |_|

Platform Name             : StarFive VisionFive V2
Platform Features         : medeleg
Platform HART Count       : 5
Platform IPI Device       : aclint-mswi
Platform Timer Device     : aclint-mtimer @ 4000000Hz
Platform Console Device   : uart8250
Platform HSM Device       : ---
Platform Reboot Device    : ---
Platform Shutdown Device  : ---
Firmware Base             : 0x40000000
Firmware Size             : 360 KB
Runtime SBI Version       : 0.3

Domain0 Name              : root
Domain0 Boot HART         : 1
Domain0 HARTs             : 0*,1*,2*,3*,4*
Domain0 Region00          : 0x0000000002000000-0x000000000200ffff (I)
Domain0 Region01          : 0x0000000040000000-0x000000004007ffff ()
Domain0 Region02          : 0x0000000000000000-0xffffffffffffffff (R,W,X)
Domain0 Next Address      : 0x0000000040200000
Domain0 Next Arg1         : 0x0000000042200000
Domain0 Next Mode         : S-mode
Domain0 SysReset          : yes

Boot HART ID              : 1
Boot HART Domain          : root
Boot HART Priv Version    : v1.11
Boot HART Base ISA        : rv64imafdcbx
Boot HART ISA Extensions  : none
Boot HART PMP Count       : 8
Boot HART PMP Granularity : 4096
Boot HART PMP Address Bits: 34
Boot HART MHPM Count      : 2
Boot HART MIDELEG         : 0x0000000000000222
Boot HART MEDELEG         : 0x000000000000b109
```

1.7. U-Boot

U-Boot runs at 0x4020_0000 and works in S mode. It contains basic file system and commonly used peripheral drivers (such as GMAC, UART, QSPI, USB, SDIO etc.). U-Boot can load the kernel image through ETH, UART, QSPI, SDIO or USB.

Figure 1-3 U-Boot Screen



```
U-Boot 2021.10 (Nov 10 2022 - 13:29:36 +0800), Build: jenkins-VF2_515_Branch_SDK_Release-12

CPU:   rv64imacu
Model: StarFive VisionFive V2
DRAM:  4 GiB
MMC:   sdio0@16010000: 0, sdio1@16020000: 1
Loading Environment from SPIFlash... SF: Detected gd25lq128 with page size 256 Bytes, erase size 4 KiB, total 16 MiB
*** Warning - bad CRC, using default environment

StarFive EEPROM format v2

--------EEPROM INFO--------
Vendor : StarFive Technology Co., Ltd.
Product full SN: VF7110A1-2238-D004E000-00000001
data version: 0x2
PCB revision: 0xa1
BOM revision: A
Ethernet MAC0 address: 6c:cf:39:6c:de:12
Ethernet MAC1 address: 6c:cf:39:7c:ae:13
--------EEPROM INFO--------

In:    serial@10000000
Out:   serial@10000000
Err:   serial@10000000
Model: StarFive VisionFive V2
Net:   eth0: ethernet@16030000, eth1: ethernet@16040000
switch to partitions #0, OK
mmc1 is current device
found device 1
bootmode flash device 1
Failed to load 'uEnv.txt'
Can't set block device
Hit any key to stop autoboot:  0
StarFive #
```

Note:
Visit RVspace to make sure you have the most updated files and installation packages from StarFive. Press **Enter** to confirm the operation or for the next command.

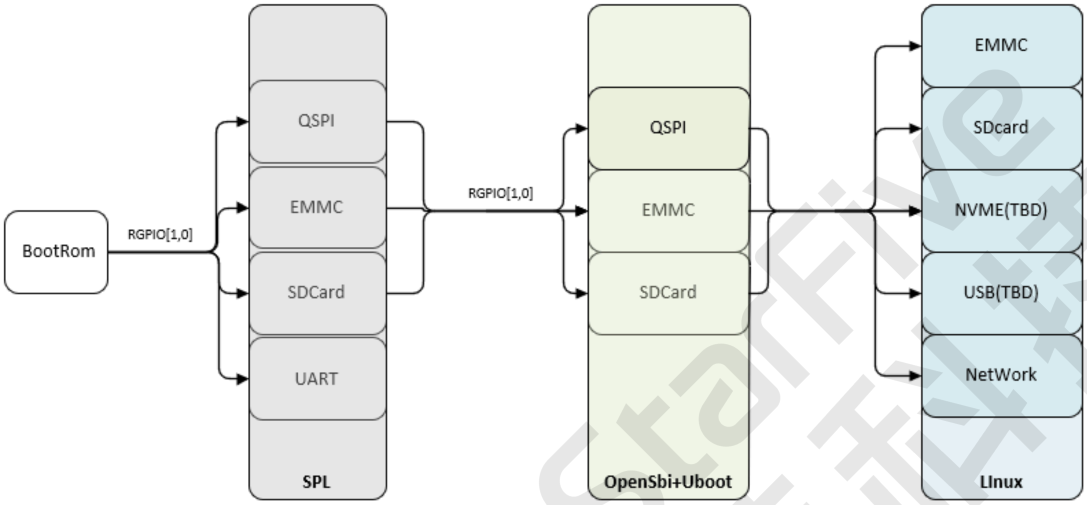
2. Boot Flow

This chapter introduces the general boot-up process of the JH7110 SoC including the image used for boot path, etc.

You can boot from the U-Boot TPL/SPL from StarFive U-Boot, which is the image source code.

The following menu-cascade shows typical JH7110 boot flow: **BootROM > SPL > U-Boot > Linux**.

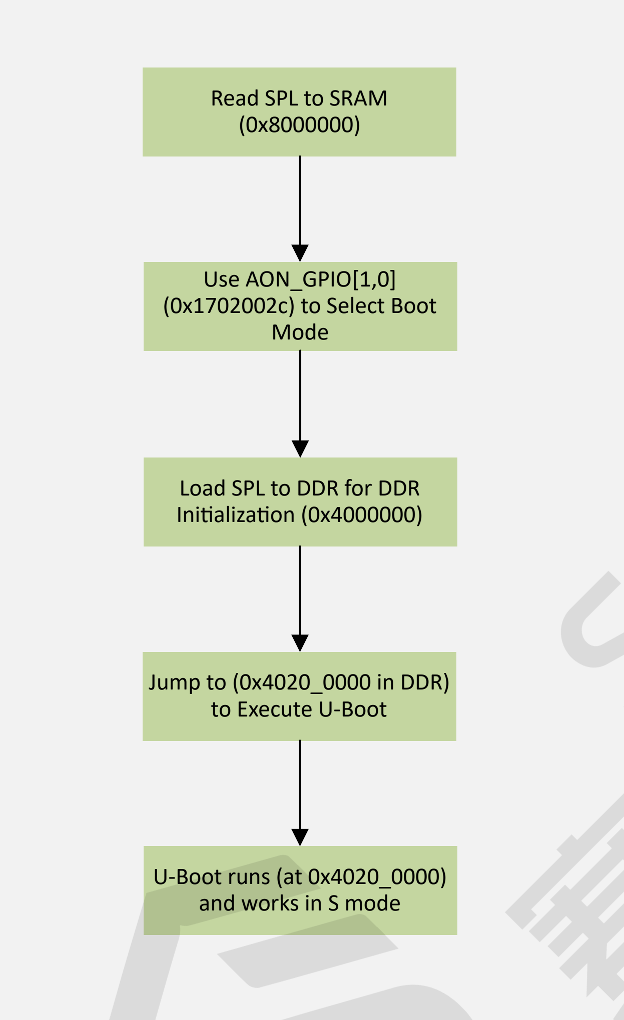
Figure 2-1 Boot Flow



3. Boot Process Memory Map

The following diagram shows the memory map of boot process for JH7110 on VisionFive 2.

Figure 3-1 Boot Process Memory Map


Read SPL to SRAM (0x8000000)
Use AON_GPIO[1,0] (0x1702002c) to Select Boot Mode
Load SPL to DDR for DDR Initialization (0x4000000)
Jump to (0x4020_0000 in DDR) to Execute U-Boot
U-Boot runs (at 0x4020_0000) and works in S mode

4. Boot Mode Settings

VisionFive 2 provides pins to determine the boot mode before it is powered up. The following are the available boot modes and details.

Table 4-1 Boot Mode Settings

Boot Mode	RGPIO_1	RGPIO_0
1-bit QSPI Nor Flash	0 (L)	0 (L)
SDIO3.0	0 (L)	1(H)
eMMC	1(H)	0 (L)
UART	1(H)	1(H)

The following figure displays the location and the pin definitions of the boot mode settings.

Figure 4-1 Boot Mode Setting Location

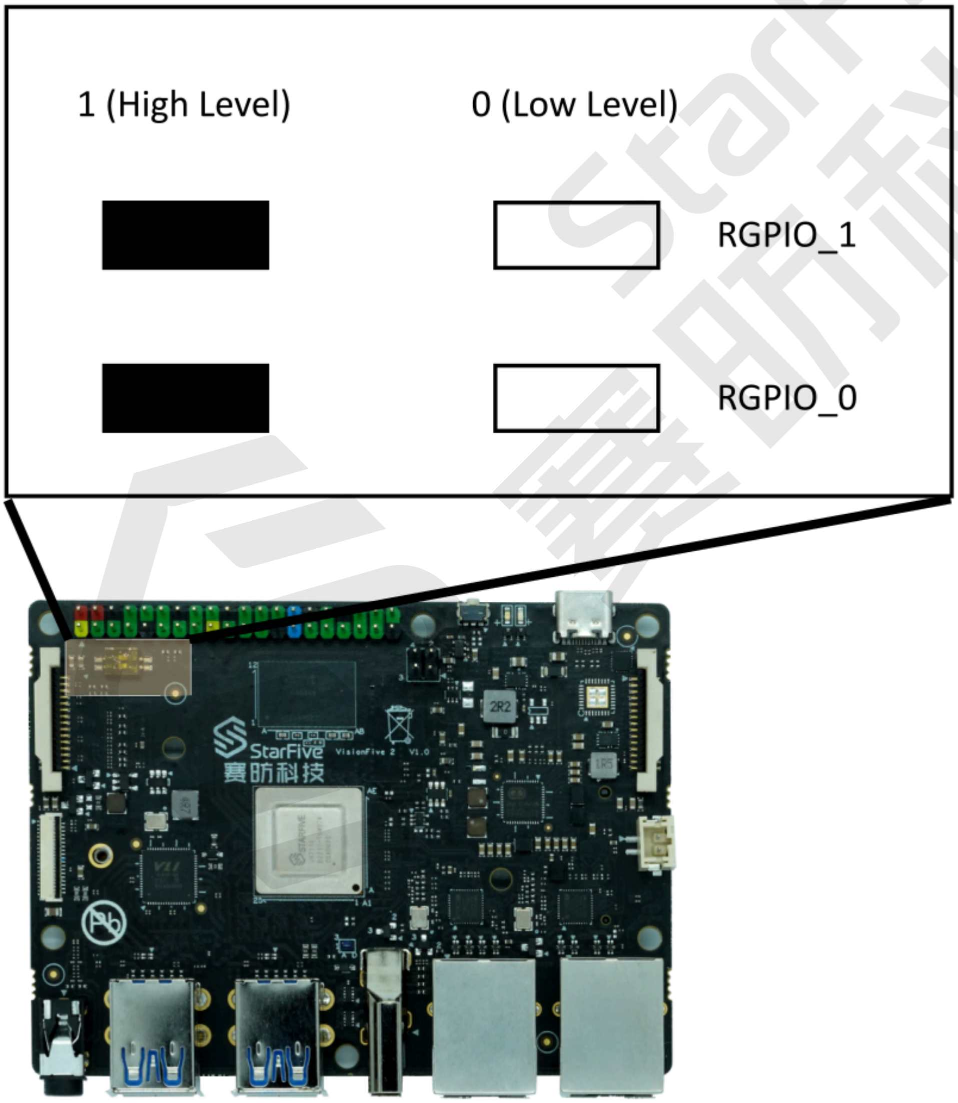
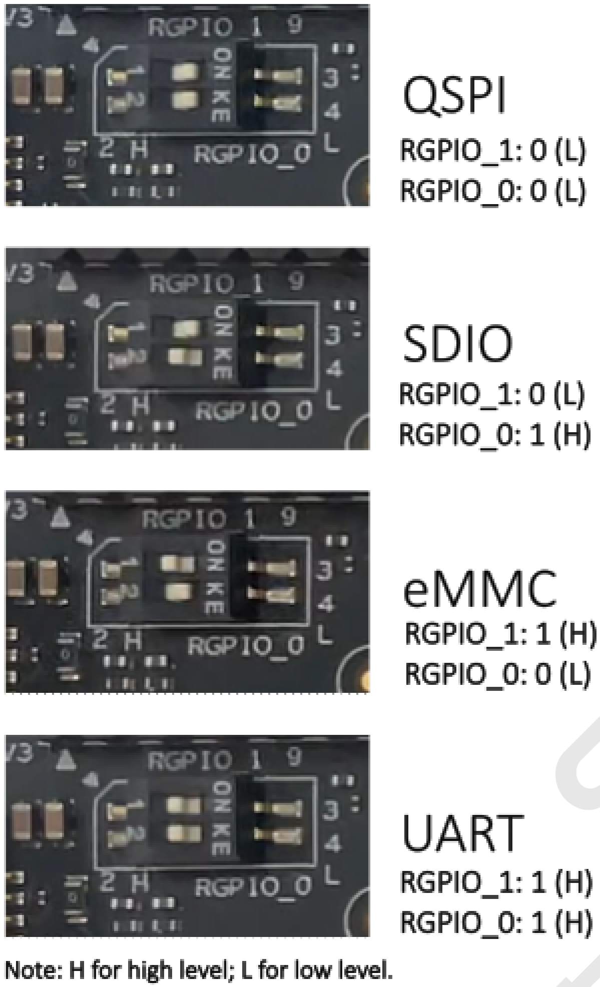


Figure 4-2 Boot Mode Settings



QSPI

RGPIO_1: 0 (L)
RGPIO_0: 0 (L)

SDIO

RGPIO_1: 0 (L)
RGPIO_0: 1 (H)

eMMC

RGPIO_1: 1 (H)
RGPIO_0: 0 (L)

UART

RGPIO_1: 1 (H)
RGPIO_0: 1 (H)

Note: H for high level; L for low level.

Note:
The silk prints may vary with different versions of boards.