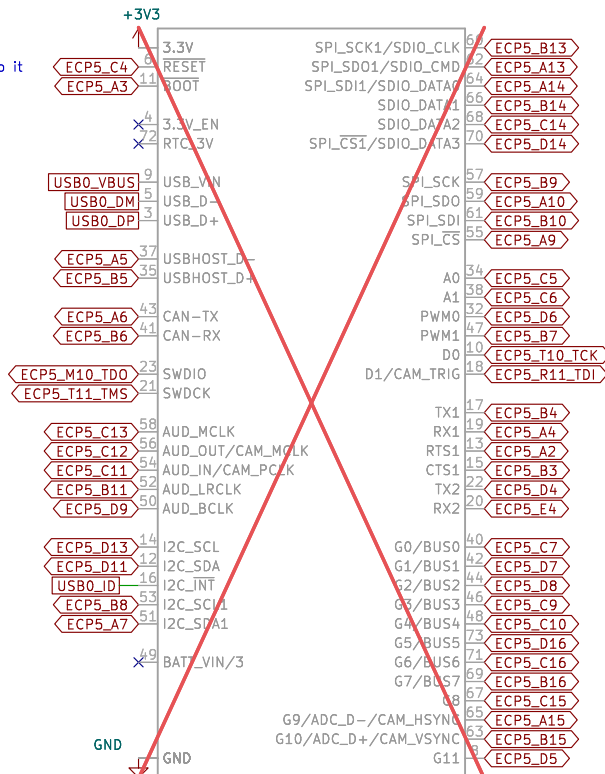


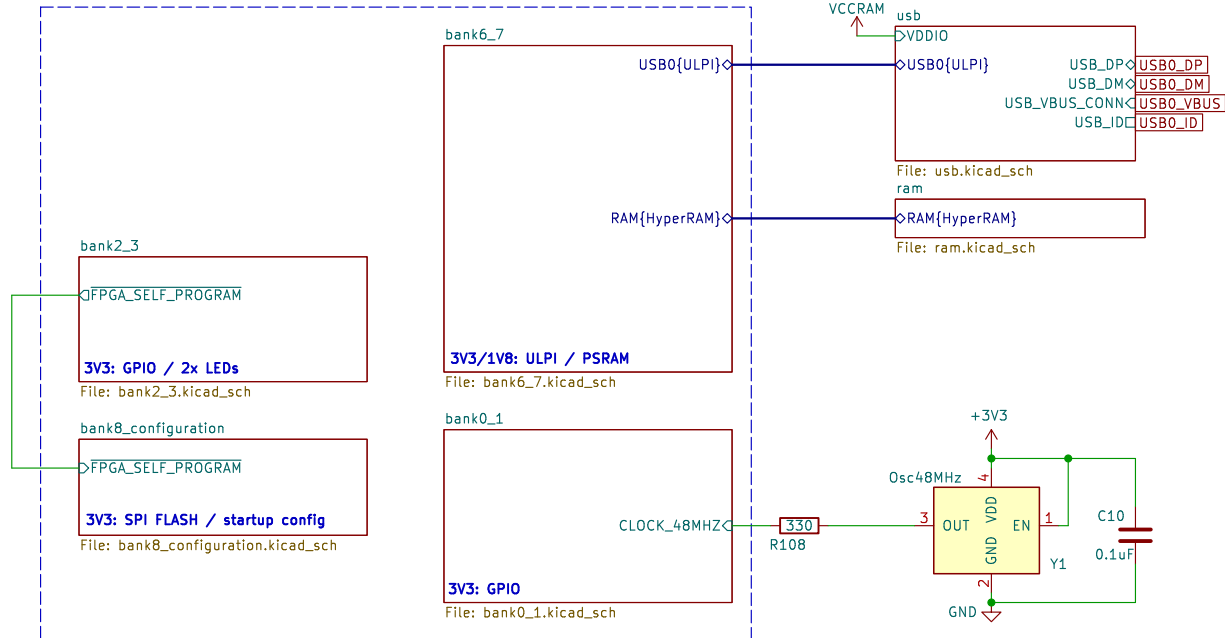
M.2 CARD EDGE

GPIOs here are all 3V3 from banks 0–3



NOPOP, this part just represents the card edge

LFE5U FPGA



power_supplies

File: power_supplies.kicad_sch

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Sheet: /
File: soldiercrab.kicad_sch

Title: SoldierCrab

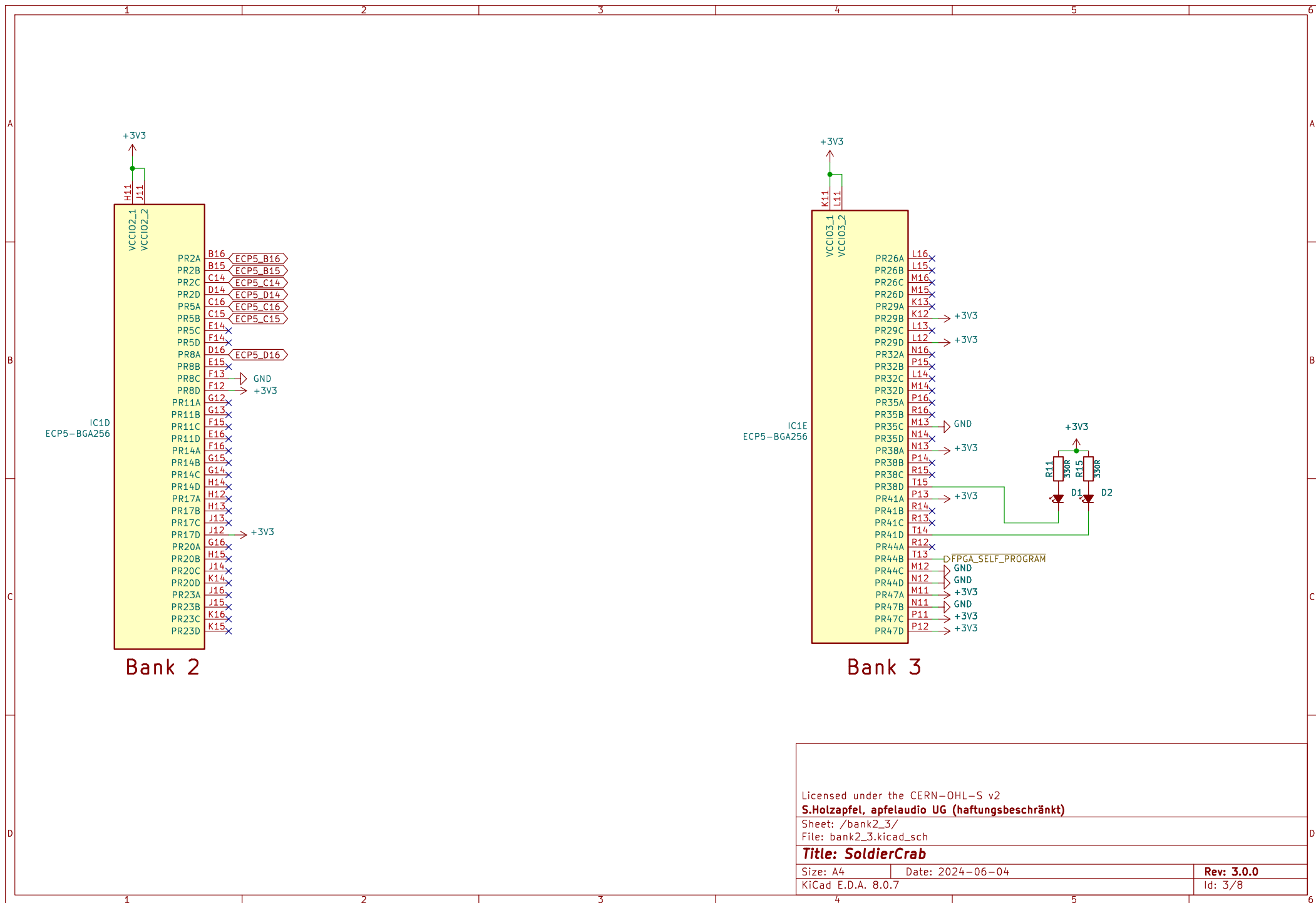
Size: A4 Date: 2024-06-04

KiCad E.D.A. 8.0.7

Rev: 3.0.0

Id: 1/8





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Sheet: /bank2_3/
File: bank2_3.kicad_sch

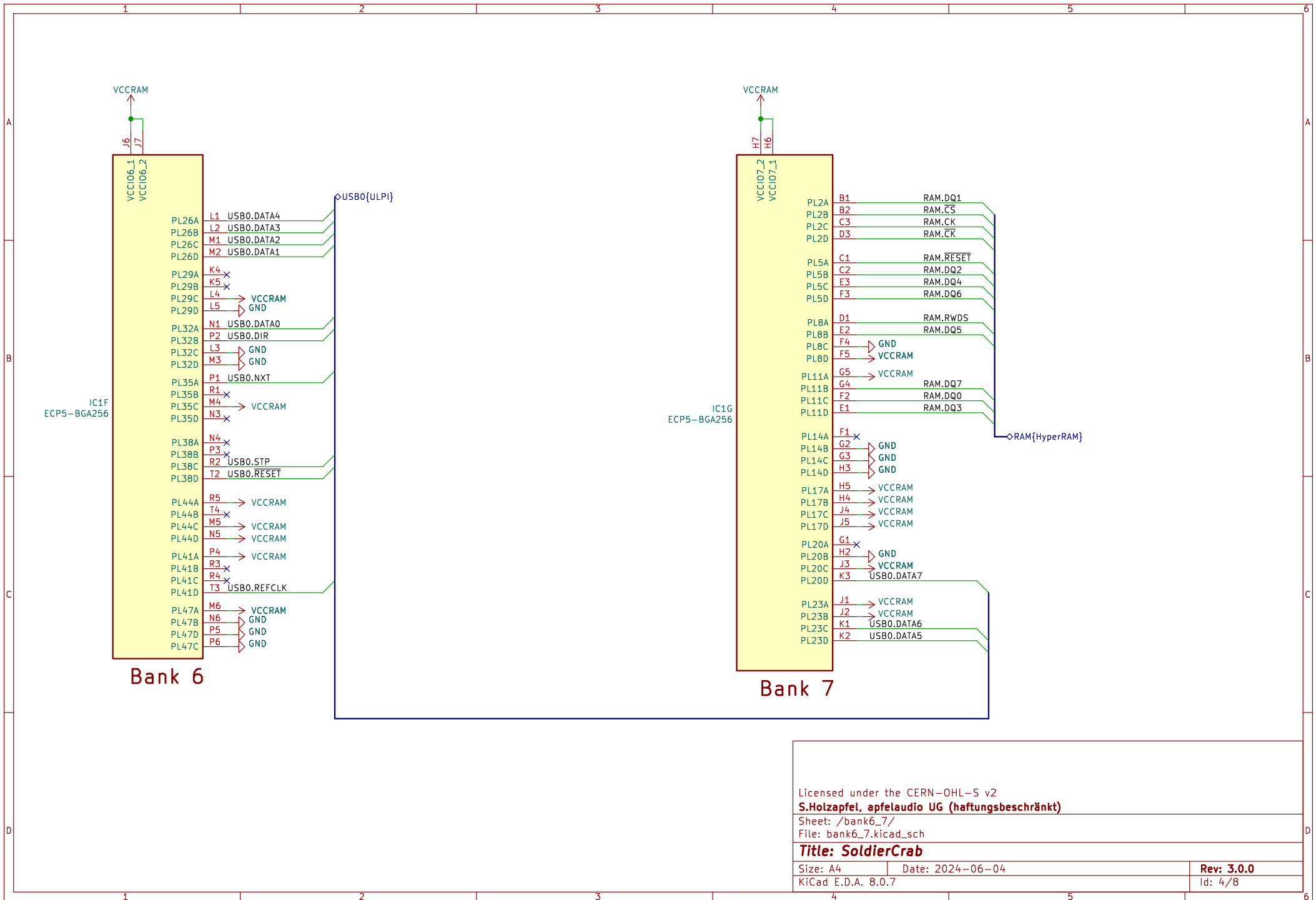
Title: SoldierCrab

Size: A4 Date: 2024-06-04

KiCad E.D.A. 8.0.7

Rev: 3.0.0

Id: 3/8



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Sheet: /bank6_7/

File: bank6_7.kicad_sch

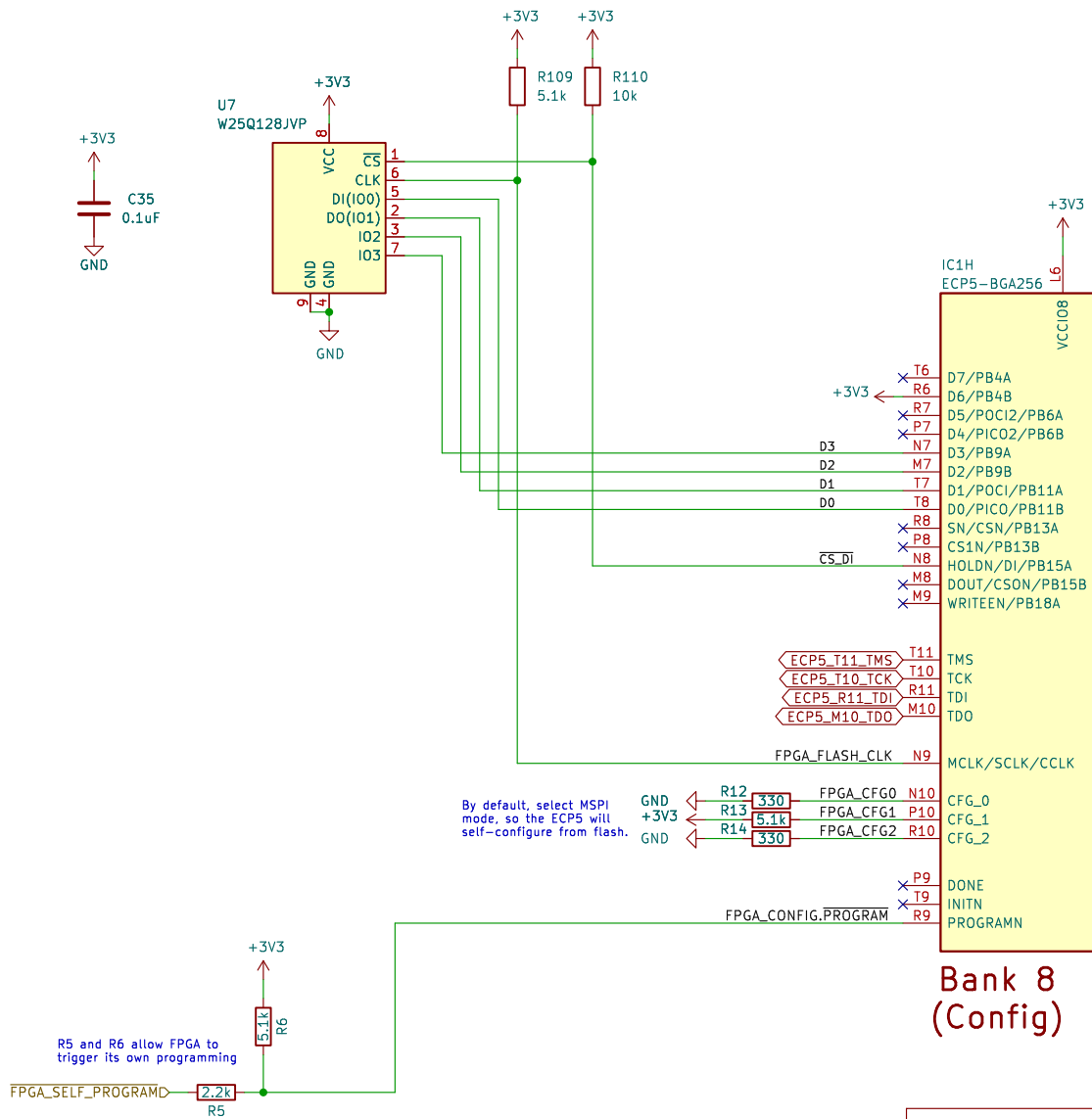
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Size: A4 Date: 2024-06-04

KiCad E.D.A. 8.0.7

Rev: 3.0.0

Id: 4/8



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Sheet: /bank8_configuration/
File: bank8_configuration.kicad_sch

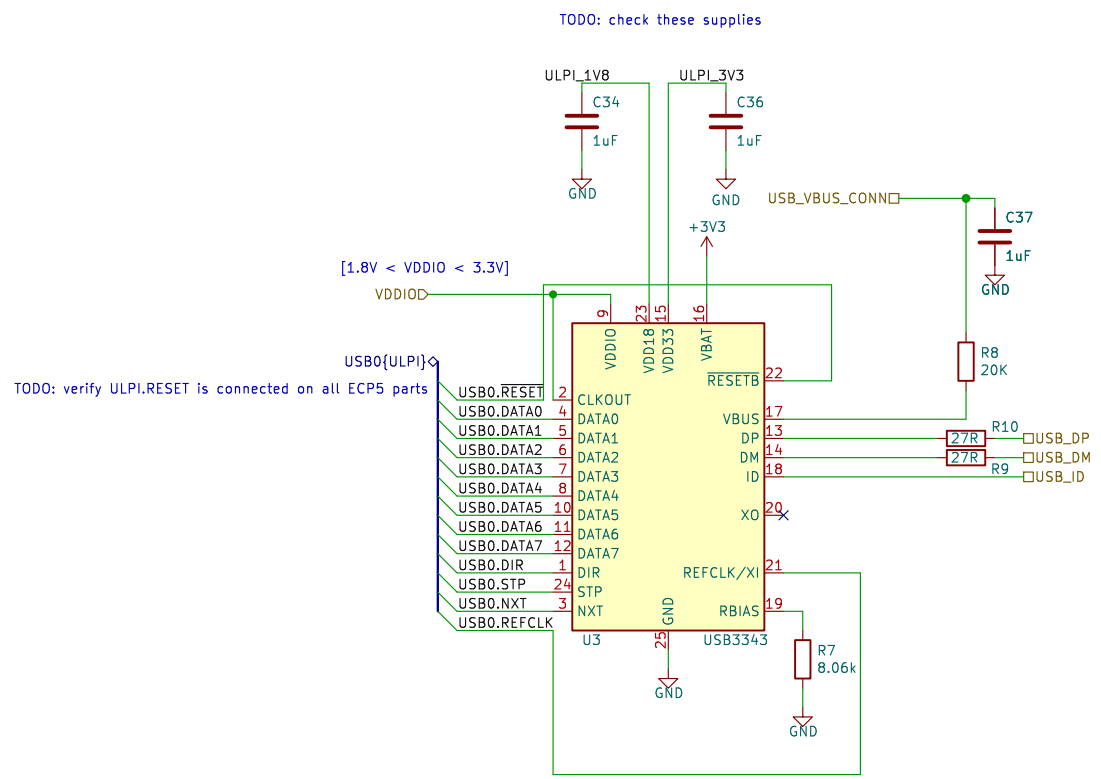
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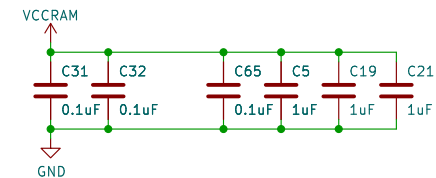
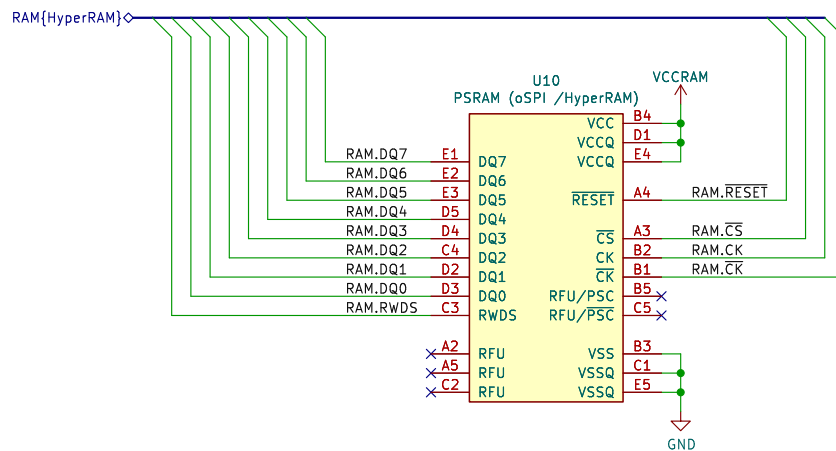
Size: A4 Date: 2024-06-04

KiCad E.D.A. 8.0.7

Rev: 3.0.0

Id: 5/8





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Sheet: /ram/
File: ram.kicad_sch

Title: SoldierCrab

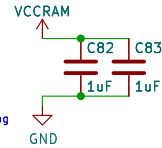
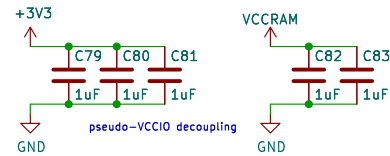
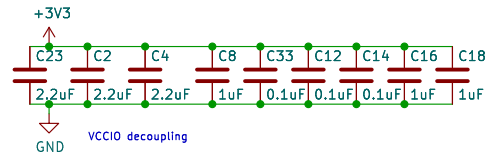
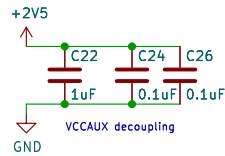
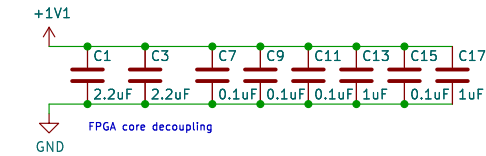
Size: A4 Date: 2024-06-04

KiCad E.D.A. 8.0.7

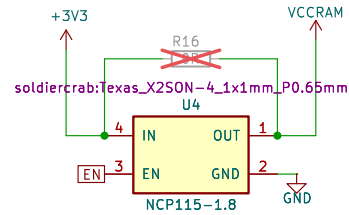
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decoupling under ECP5

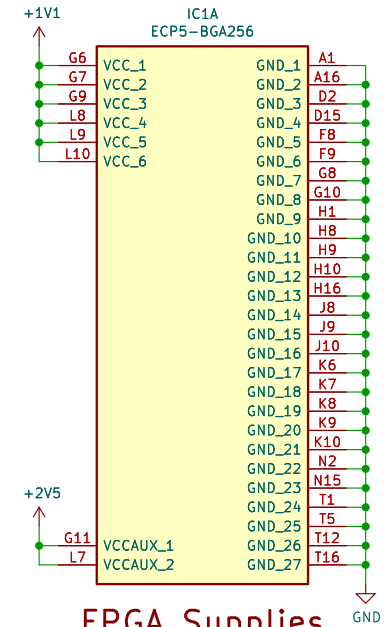
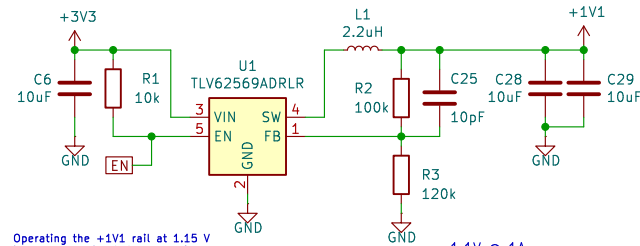


RAM VCC / ULPI VCCIO

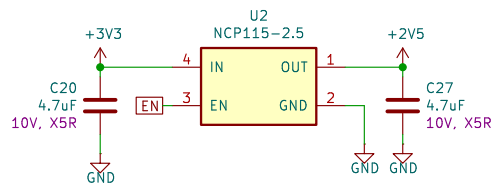


USB3343: fine with VCCIO at 1V8 or 3V3.
PSRAM: depends on the RAM chip chosen
Both ULPI VCCIO and RAM VCC are fed by this net,
as the associated ECP5 pins are on the same bank.

1V1 / VCORE



2V5 / VCCAUX



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Sheet: /power_supplies/
File: power_supplies.kicad_sch

Title: SoldierCrab

Size: A4 Date: 2024-06-04

KiCad E.D.A. 8.0.7

Rev: 3.0.0

Id: 8/8