ΠΑΡΑΔΟΤΕΟ 1ου ΕΡΓΑΣΤΗΡΙΟΥ (Πρώτο Μέρος)

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1. Από το αρχείο starter_se.py οι αρχικές παράμετροι που έχουν περάσει στον gem5 για το σύστημα προς εξομοίωση είναι:

   - **Cache line size**: 64
   - **Voltage:** "3.3V"
   - **CPU model to use:** "minor" (κατά την εκτέλεση της εντολής ($ ./build/ARM/gem5.opt -d hello_result configs/example/arm/starter_se.py --cpu="minor" "tests/test-progs/hello/bin/arm/linux/hello") υπάρχει το flag --cpu="minor".)
   - **CPU frequency :** 1GHz"

   Default:

   - **Number of CPU cores:** 1
   - **Type of memory to use:** "DDR3_1600_8x8"
   - **Number of memory channels:** 2
   - **Number of memory ranks per channel:** None
   - **Specify the physical memory size:** "2GB"

2. Ανοίγοντας τα αρχεία config.json και config.ini επαληθεύεται η απάντηση του πρώτου ερωτήματος, καθώς τα στοιχεία αντιστοιχούν μεταξύ τους.

Κομμάτι κώδικα από το starter_se.py:

```
87      # Use a fixed cache line size of 64 bytes
88      cache_line_size = 64
89
90      def __init__(self, args, **kwargs):
91          super(SimpleSeSystem, self).__init__(**kwargs)
92
93          # Setup book keeping to be able to use CpuClusters from the
94          # devices module.
95          self._clusters = []
96          self._num_cpus = 0
97
98          # Create a voltage and clock domain for system components
99          self.voltage_domain = VoltageDomain(voltage="3.3V")
100         self.clk_domain = SrcClockDomain(clock="1GHz",
101                                          voltage_domain=self.voltage_domain)
102
103         # Create the off-chip memory bus.
104         self.membus = SystemXBar()
105
106         # Wire up the system port that gem5 uses to load the kernel
107         # and to perform debug accesses.
108         self.system_port = self.membus.slave
109
110
111         # Add CPUs to the system. A cluster of CPUs typically have
112         # private L1 caches and a shared L2 cache.
113         self.cpu_cluster = devices.CpuCluster(self,
114                                               args.num_cores,
115                                               args.cpu_freq, "1.2V",
116                                               *cpu_types[args.cpu])
117
```

```
186 def main():
187     parser = argparse.ArgumentParser(epilog=__doc__)
188
189     parser.add_argument("commands_to_run", metavar="command(s)", nargs='*',
190                         help="Command(s) to run")
191     parser.add_argument("--cpu", type=str, choices=cpu_types.keys(),
192                         default="atomic",
193                         help="CPU model to use")
194     parser.add_argument("--cpu-freq", type=str, default="4GHz")
195     parser.add_argument("--num-cores", type=int, default=1,
196                         help="Number of CPU cores")
197     parser.add_argument("--mem-type", default="DDR3_1600_8x8",
198                         choices=ObjectList.mem_list.get_names(),
199                         help = "type of memory to use")
200     parser.add_argument("--mem-channels", type=int, default=2,
201                         help = "number of memory channels")
202     parser.add_argument("--mem-ranks", type=int, default=None,
203                         help = "number of memory ranks per channel")
204     parser.add_argument("--mem-size", action="store", type=str,
205                         default="2GB",
206                         help="Specify the physical memory size")
```

Κομμάτι κώδικα από το config.json:

```
111         },
112         "cache line size": 64,
```

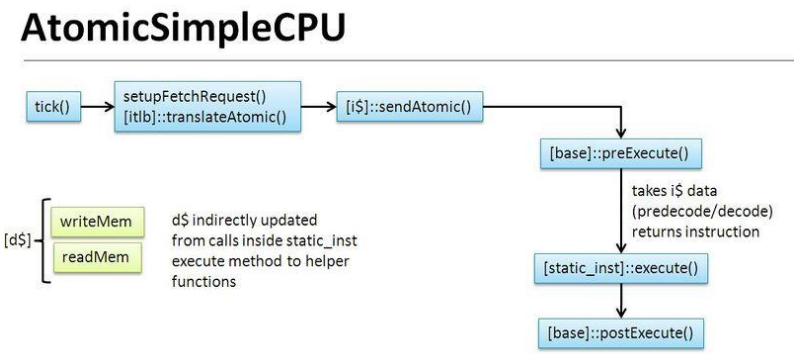
Κομμάτια κώδικα από το config.ini

```
cache_line_size=64
eventq_index=0
exit_on_work_items=false
init_param=0

[system.voltage_domain]
type=VoltageDomain
eventq_index=0
voltage=3.3
```

3. In-order CPU types supported by gem5

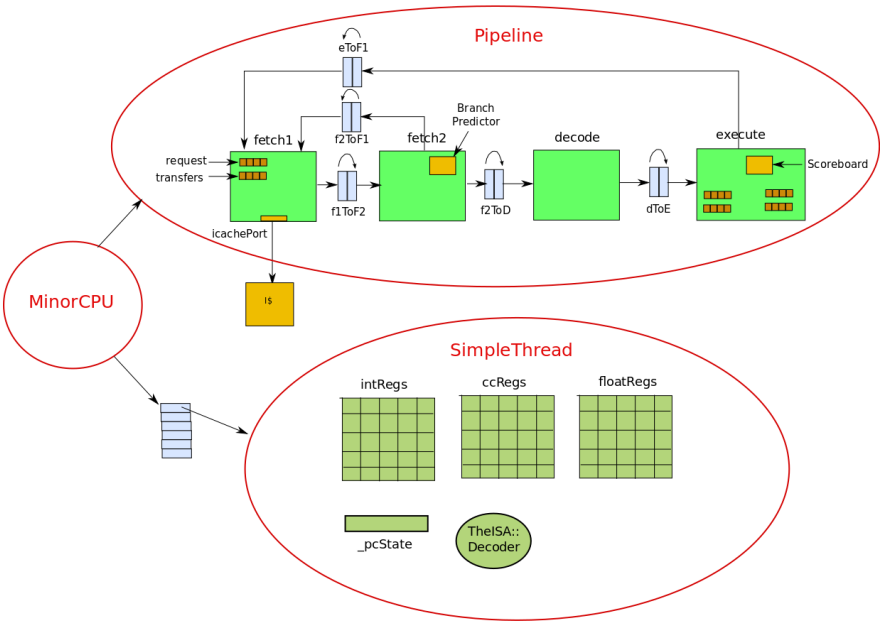
```
66  # Pre-defined CPU configurations. Each tuple must be ordered as : (cpu_class,
67  # l1_icache_class, l1_dcache_class, walk_cache_class, l2_Cache_class). Any of
68  # the cache class may be 'None' if the particular cache is not present.
69  cpu_types = {
70      "atomic" : ( AtomicSimpleCPU, None, None, None, None),
71      "minor" : (MinorCPU,
72                 devices.L1I, devices.L1D,
73                 devices.WalkCache,
74                 devices.L2),
75      "hpi" : ( HPI.HPI,
76                HPI.HPI_ICache, HPI.HPI_DCache,
77                HPI.HPI_WalkCache,
78                HPI.HPI_L2)
79  }
```

atomic:
Ο Atomic είναι επεξεργαστής που χρησιμοποιεί ατομική πρόσβαση στη μνήμη. Χρησιμοποιεί τα latency estimates από τις ατομικές προσβάσεις για να υπολογίσει το συνολικό χρόνο πρόσβασης στη κρυφή μνήμη (cache). Ο Atomic CPU προέρχεται από τον BaseSimpleCPU και υλοποιεί λειτουργίες ανάγνωσης και εγγραφής στη μνήμη, καθώς επίσης και tick (ορίζει δηλαδή το τι συμβαίνει σε κάθε κύκλο του ρολογιού). Ορίζει τη θύρα που χρησιμοποιείται για να συνδέσει τη μνήμη και συνδέει τη CPU με την cache.



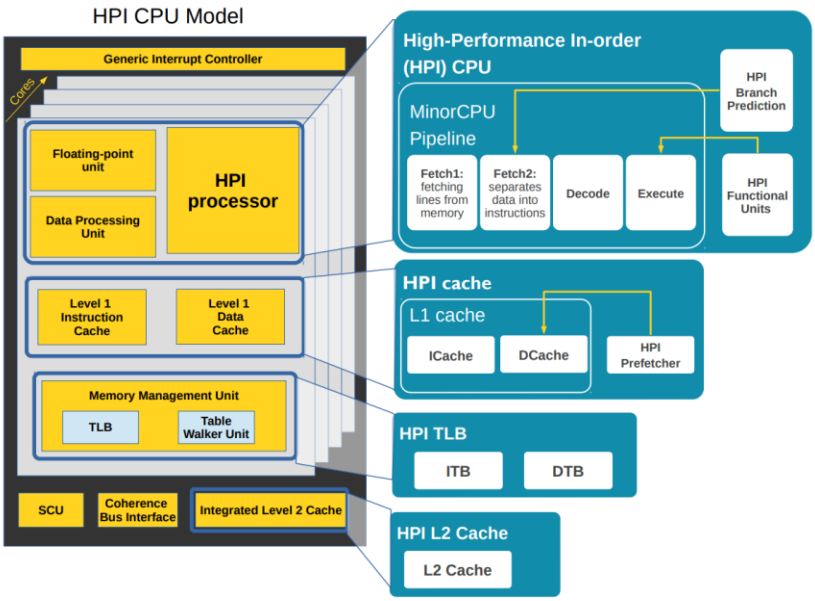
minor:
Πρόκειται για έναν επεξεργαστή με 4 στάδια pipelining. Τα τέσσερα στάδια είναι η fetch1, η fetch2, η decode και η execute. Η πρόσβαση ITLB και η λήψη της εντολής από την κύρια μνήμη γίνεται στο fetch1. Το fetch2 είναι υπεύθυνο για την αποκωδικοποίηση της εντολής, η decode είναι υπεύθυνη για book-keeping και η execute υλοποιεί το logic for issue, την εκτέλεση, τη μνήμη, το writeback και το commit. Όλα αυτά τα στάδια ορίζονται ως SimObjects στην κλάση Pipeline, η οποία υλοποιεί ολόκληρο το pipelining. Τα διαφορετικά στάδια του pipeline συνδέονται μεταξύ τους με Latches.

```
class Pipeline {
    /* Latches to connect the stages */
    Latch<ForwardLineData> f1ToF2;
    Latch<BranchData> f2ToF1;
    Latch<ForwardInstData> f2ToD;
    Latch<ForwardInstData> dToE;
    Latch<BranchData> eToF1;

    /* Pipeline Stages */
    Execute execute;
    Decode decode;
    Fetch2 fetch2;
    Fetch1 fetch1

    /* Action to be performed at each cycle (tick) */
    void evaluate();
}
```



hpi:

Ο HPI επεξεργαστής είναι βασισμένος στην αρχιτεκτονική βραχίονα. Το μοντέλο χρονισμού του HPI επεξεργαστή αντιπροσωπεύει μια πραγματική in-order υλοποίηση του Armv8-A. Ο pipeline του HPI CPU χρησιμοποιεί το ίδιο μοντέλο τεσσάρων σταδίων με το Minor CPU.



Building blocks of the Arm High-performance In-order CPU in gem5

3.a.

Atomic:

```
---------- Begin Simulation Statistics ----------
final_tick                                   57592750                       # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
host_inst_rate                                 567557                       # Simulator instruction rate (inst/s)
host_mem_usage                                2234256                       # Number of bytes of host memory used
host_op_rate                                   672257                       # Simulator op (including micro ops) rate (op/s)
host_seconds                                     0.31                       # Real time elapsed on the host
host_tick_rate                               187533356                       # Simulator tick rate (ticks/s)
sim_freq                                  1000000000000                       # Frequency of simulated ticks
sim_insts                                      174212                       # Number of instructions simulated
sim_ops                                        206435                       # Number of ops (including micro ops) simulated
sim_seconds                                  0.000058                       # Number of seconds simulated
sim_ticks                                    57592750                       # Number of ticks simulated
system.cpu_cluster.cpus.Branches               36890                       # Number of branches fetched
system.cpu_cluster.cpus.committedInsts         174212                       # Number of instructions committed
system.cpu_cluster.cpus.committedOps           206435                       # Number of ops (including micro ops) committed
system.cpu_cluster.cpus.dtb.accesses                0                       # DTB accesses
system.cpu_cluster.cpus.dtb.align_faults            0                       # Number of TLB faults due to alignment restrictions
system.cpu_cluster.cpus.dtb.domain_faults            0                       # Number of TLB faults due to domain restrictions
system.cpu_cluster.cpus.dtb.flush_entries            0                       # Number of entries that have been flushed from TLB
```

Minor:

```
---------- Begin Simulation Statistics ----------
final_tick                                   79542750                       # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
host_inst_rate                                 252324                       # Simulator instruction rate (inst/s)
host_mem_usage                                2248584                       # Number of bytes of host memory used
host_op_rate                                   298883                       # Simulator op (including micro ops) rate (op/s)
host_seconds                                     0.69                       # Real time elapsed on the host
host_tick_rate                               115040564                       # Simulator tick rate (ticks/s)
sim_freq                                  1000000000000                       # Frequency of simulated ticks
sim_insts                                      174425                       # Number of instructions simulated
sim_ops                                        206649                       # Number of ops (including micro ops) simulated
sim_seconds                                  0.000080                       # Number of seconds simulated
sim_ticks                                    79542750                       # Number of ticks simulated
system.cpu_cluster.cpus.branchPred.BTBCorrect            0                       # Number of correct BTB predictions (this stat may not work properly.
system.cpu_cluster.cpus.branchPred.BTBHitPct    47.324754                       # BTB Hit Percentage
system.cpu_cluster.cpus.branchPred.BTBHits        15629                       # Number of BTB hits
system.cpu_cluster.cpus.branchPred.BTBLookups        33025                       # Number of BTB lookups
system.cpu_cluster.cpus.branchPred.RASInCorrect            8                       # Number of incorrect RAS predictions.
system.cpu_cluster.cpus.branchPred.condIncorrect         1718                       # Number of conditional branches incorrect
system.cpu_cluster.cpus.branchPred.condPredicted        26806                       # Number of conditional branches predicted
system.cpu_cluster.cpus.branchPred.indirectHits         1794                       # Number of indirect target hits.
system.cpu_cluster.cpus.branchPred.indirectLookups         2971                       # Number of indirect predictor lookups.
system.cpu_cluster.cpus.branchPred.indirectMisses         1177                       # Number of indirect misses.
system.cpu_cluster.cpus.branchPred.lookups        40496                       # Number of BP lookups
system.cpu_cluster.cpus.branchPred.usedRAS         4332                       # Number of times the RAS was used to get a target.
system.cpu_cluster.cpus.branchPredindirectMispredicted          290                       # Number of mispredicted indirect branches.
system.cpu_cluster.cpus.committedInsts         174425                       # Number of instructions committed
system.cpu_cluster.cpus.committedOps           206649                       # Number of ops (including micro ops) committed
system.cpu_cluster.cpus.cpi                  1.824114                       # CPI: cycles per instruction
system.cpu_cluster.cpus.discardedOps             4682                       # Number of ops (including micro ops) which were discarded before commit
```

HPI:

```
---------- Begin Simulation Statistics ----------
final_tick                                   86826750                       # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
host_inst_rate                                 226716                       # Simulator instruction rate (inst/s)
host_mem_usage                                2253788                       # Number of bytes of host memory used
host_op_rate                                   268538                       # Simulator op (including micro ops) rate (op/s)
host_seconds                                     0.77                       # Real time elapsed on the host
host_tick_rate                               112825078                       # Simulator tick rate (ticks/s)
sim_freq                                  1000000000000                       # Frequency of simulated ticks
sim_insts                                      174425                       # Number of instructions simulated
sim_ops                                        206649                       # Number of ops (including micro ops) simulated
sim_seconds                                  0.000087                       # Number of seconds simulated
sim_ticks                                    86826750                       # Number of ticks simulated
system.cpu_cluster.cpus.branchPred.BTBCorrect            0                       # Number of correct BTB predictions (this stat may not work properly.
system.cpu_cluster.cpus.branchPred.BTBHitPct    24.088155                       # BTB Hit Percentage
system.cpu_cluster.cpus.branchPred.BTBHits        11531                       # Number of BTB hits
system.cpu_cluster.cpus.branchPred.BTBLookups        47870                       # Number of BTB lookups
system.cpu_cluster.cpus.branchPred.RASInCorrect            9                       # Number of incorrect RAS predictions.
system.cpu_cluster.cpus.branchPred.condIncorrect         6596                       # Number of conditional branches incorrect
system.cpu_cluster.cpus.branchPred.condPredicted        34912                       # Number of conditional branches predicted
system.cpu_cluster.cpus.branchPred.indirectHits         1786                       # Number of indirect target hits.
system.cpu_cluster.cpus.branchPred.indirectLookups         3931                       # Number of indirect predictor lookups.
system.cpu_cluster.cpus.branchPred.indirectMisses         2145                       # Number of indirect misses.
system.cpu_cluster.cpus.branchPred.lookups        57356                       # Number of BP lookups
system.cpu_cluster.cpus.branchPred.usedRAS         6022                       # Number of times the RAS was used to get a target.
system.cpu_cluster.cpus.branchPredindirectMispredicted          289                       # Number of mispredicted indirect branches.
system.cpu_cluster.cpus.committedInsts         174425                       # Number of instructions committed
system.cpu_cluster.cpus.committedOps           206649                       # Number of ops (including micro ops) committed
system.cpu_cluster.cpus.cpi                  1.991154                       # CPI: cycles per instruction
system.cpu_cluster.cpus.dcache.prefetcher.num_hwpf_issued            5                       # number of hwpf issued
system.cpu_cluster.cpus.dcache.prefetcher.pfBufferHit            2                       # number of redundant prefetches already in prefetch queue
system.cpu_cluster.cpus.dcache.prefetcher.pfIdentified            8                       # number of prefetch candidates identified
system.cpu_cluster.cpus.dcache.prefetcher.pfInCache            0                       # number of redundant prefetches already in cache/mshr dropped
system.cpu_cluster.cpus.dcache.prefetcher.pfRemovedFull            0                       # number of prefetches dropped due to prefetch queue size
system.cpu_cluster.cpus.dcache.prefetcher.pfSpanPage            0                       # number of prefetches that crossed the page
system.cpu_cluster.cpus.discardedOps            22113                       # Number of ops (including micro ops) which were discarded before commit
```

3.b.

Χρησιμοποιώντας διαφορετικά μοντέλα CPU παρατηρούμε διαφορά στο instruction rate, στον χρόνο εκτέλεσης αλλά και στο tick rate. Αυτό συμβαίνει επειδή το pipelining σε κάθε μοντέλο είναι διαφορετικό και κατά συνέπεια αλλάζει ο αριθμός των εντολών που εκτελούνται σε κάθε κύκλο ρολογιού.

3.c.

Frequency 1GHz→2GHz

Atomic:

```
---------- Begin Simulation Statistics ----------
final_tick                                 57592750                       # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
host_inst_rate                               846366                       # Simulator instruction rate (inst/s)
host_mem_usage                              2234256                       # Number of bytes of host memory used
host_op_rate                                1002272                       # Simulator op (including micro ops) rate (op/s)
host_seconds                                   0.21                       # Real time elapsed on the host
host_tick_rate                            279577542                       # Simulator tick rate (ticks/s)
sim_freq                                1000000000000                       # Frequency of simulated ticks
sim_insts                                    174212                       # Number of instructions simulated
sim_ops                                      206435                       # Number of ops (including micro ops) simulated
sim_seconds                                  0.000058                       # Number of seconds simulated
sim_ticks                                  57592750                       # Number of ticks simulated
system.cpu_cluster.cpus.Branches             36890                       # Number of branches fetched
system.cpu_cluster.cpus.committedInsts       174212                       # Number of instructions committed
system.cpu_cluster.cpus.committedOps         206435                       # Number of ops (including micro ops) committed
```

Minor:

```
---------- Begin Simulation Statistics ----------
final_tick                                 77626250                       # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
host_inst_rate                               270799                       # Simulator instruction rate (inst/s)
host_mem_usage                              2248584                       # Number of bytes of host memory used
host_op_rate                                 320748                       # Simulator op (including micro ops) rate (op/s)
host_seconds                                   0.64                       # Real time elapsed on the host
host_tick_rate                             120480464                       # Simulator tick rate (ticks/s)
sim_freq                                1000000000000                       # Frequency of simulated ticks
sim_insts                                    174425                       # Number of instructions simulated
sim_ops                                      206649                       # Number of ops (including micro ops) simulated
sim_seconds                                  0.000078                       # Number of seconds simulated
sim_ticks                                  77626250                       # Number of ticks simulated
system.cpu_cluster.cpus.branchPred.BTBCorrect            0                       # Number of correct BTB predictions (this stat may not work properly.
system.cpu_cluster.cpus.branchPred.BTBHitPct    47.329215                       # BTB Hit Percentage
system.cpu_cluster.cpus.branchPred.BTBHits        15630                       # Number of BTB hits
system.cpu_cluster.cpus.branchPred.BTBLookups        33024                       # Number of BTB lookups
system.cpu_cluster.cpus.branchPred.RASInCorrect            8                       # Number of incorrect RAS predictions.
system.cpu_cluster.cpus.branchPred.condIncorrect         1718                       # Number of conditional branches incorrect
system.cpu_cluster.cpus.branchPred.condPredicted        26806                       # Number of conditional branches predicted
system.cpu_cluster.cpus.branchPred.indirectHits         1794                       # Number of indirect target hits.
system.cpu_cluster.cpus.branchPred.indirectLookups         2971                       # Number of indirect predictor lookups.
system.cpu_cluster.cpus.branchPred.indirectMisses         1177                       # Number of indirect misses.
system.cpu_cluster.cpus.branchPred.lookups        40495                       # Number of BP lookups
system.cpu_cluster.cpus.branchPred.usedRAS         4332                       # Number of times the RAS was used to get a target.
system.cpu_cluster.cpus.branchPredindirectMispredicted          290                       # Number of mispredicted indirect branches.
system.cpu_cluster.cpus.committedInsts         174425                       # Number of instructions committed
system.cpu_cluster.cpus.committedOps           206649                       # Number of ops (including micro ops) committed
```

HPI:

```
|
---------- Begin Simulation Statistics ----------
final_tick                                 85611750                       # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
host_inst_rate                               235929                       # Simulator instruction rate (inst/s)
host_mem_usage                              2253788                       # Number of bytes of host memory used
host_op_rate                                 279465                       # Simulator op (including micro ops) rate (op/s)
host_seconds                                   0.74                       # Real time elapsed on the host
host_tick_rate                             115773691                       # Simulator tick rate (ticks/s)
sim_freq                                1000000000000                       # Frequency of simulated ticks
sim_insts                                    174425                       # Number of instructions simulated
sim_ops                                      206649                       # Number of ops (including micro ops) simulated
sim_seconds                                  0.000086                       # Number of seconds simulated
sim_ticks                                  85611750                       # Number of ticks simulated
system.cpu_cluster.cpus.branchPred.BTBCorrect            0                       # Number of correct BTB predictions (this stat may not work properly.
system.cpu_cluster.cpus.branchPred.BTBHitPct    24.089741                       # BTB Hit Percentage
system.cpu_cluster.cpus.branchPred.BTBHits        11532                       # Number of BTB hits
system.cpu_cluster.cpus.branchPred.BTBLookups        47871                       # Number of BTB lookups
system.cpu_cluster.cpus.branchPred.RASInCorrect            9                       # Number of incorrect RAS predictions.
system.cpu_cluster.cpus.branchPred.condIncorrect         6596                       # Number of conditional branches incorrect
system.cpu_cluster.cpus.branchPred.condPredicted        34913                       # Number of conditional branches predicted
system.cpu_cluster.cpus.branchPred.indirectHits         1786                       # Number of indirect target hits.
system.cpu_cluster.cpus.branchPred.indirectLookups         3931                       # Number of indirect predictor lookups.
system.cpu_cluster.cpus.branchPred.indirectMisses         2145                       # Number of indirect misses.
system.cpu_cluster.cpus.branchPred.lookups        57357                       # Number of BP lookups
system.cpu_cluster.cpus.branchPred.usedRAS         6022                       # Number of times the RAS was used to get a target.
system.cpu_cluster.cpus.branchPredindirectMispredicted          289                       # Number of mispredicted indirect branches.
system.cpu_cluster.cpus.committedInsts         174425                       # Number of instructions committed
system.cpu_cluster.cpus.committedOps           206649                       # Number of ops (including micro ops) committed
```

Timing→ O3CPU

Atomic:

```
---------- Begin Simulation Statistics ----------
final_tick                                   57592750                       # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
host_inst_rate                                 531099                       # Simulator instruction rate (inst/s)
host_mem_usage                                2234260                       # Number of bytes of host memory used
host_op_rate                                   629094                       # Simulator op (including micro ops) rate (op/s)
host_seconds                                     0.33                       # Real time elapsed on the host
host_tick_rate                               175493753                       # Simulator tick rate (ticks/s)
sim_freq                                  1000000000000                       # Frequency of simulated ticks
sim_insts                                      174212                       # Number of instructions simulated
sim_ops                                        206435                       # Number of ops (including micro ops) simulated
sim_seconds                                  0.000058                       # Number of seconds simulated
sim_ticks                                    57592750                       # Number of ticks simulated
system.cpu_cluster.cpus.Branches               36890                       # Number of branches fetched
system.cpu_cluster.cpus.committedInsts         174212                       # Number of instructions committed
system.cpu_cluster.cpus.committedOps           206435                       # Number of ops (including micro ops) committed
```

Minor:

```
---------- Begin Simulation Statistics ----------
final_tick                                 3008974500                       # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
host_inst_rate                                 147454                       # Simulator instruction rate (inst/s)
host_mem_usage                                2239632                       # Number of bytes of host memory used
host_op_rate                                   173873                       # Simulator op (including micro ops) rate (op/s)
host_seconds                                     1.19                       # Real time elapsed on the host
host_tick_rate                             2531647332                       # Simulator tick rate (ticks/s)
sim_freq                                  1000000000000                       # Frequency of simulated ticks
sim_insts                                      174425                       # Number of instructions simulated
sim_ops                                        206649                       # Number of ops (including micro ops) simulated
sim_seconds                                  0.003009                       # Number of seconds simulated
sim_ticks                                  3008974500                       # Number of ticks simulated
system.cpu_cluster.cpus.branchPred.BTBCorrect            0                       # Number of correct BTB predictions (this stat may not work properly.
system.cpu_cluster.cpus.branchPred.BTBHitPct    46.197742                       # BTB Hit Percentage
system.cpu_cluster.cpus.branchPred.BTBHits        15139                       # Number of BTB hits
system.cpu_cluster.cpus.branchPred.BTBLookups        32770                       # Number of BTB lookups
system.cpu_cluster.cpus.branchPred.RASInCorrect            8                       # Number of incorrect RAS predictions.
system.cpu_cluster.cpus.branchPred.condIncorrect         1722                       # Number of conditional branches incorrect
system.cpu_cluster.cpus.branchPred.condPredicted        27718                       # Number of conditional branches predicted
system.cpu_cluster.cpus.branchPred.indirectHits         1791                       # Number of indirect target hits.
system.cpu_cluster.cpus.branchPred.indirectLookups         3830                       # Number of indirect predictor lookups.
system.cpu_cluster.cpus.branchPred.indirectMisses         2039                       # Number of indirect misses.
system.cpu_cluster.cpus.branchPred.lookups        40736                       # Number of BP lookups
system.cpu_cluster.cpus.branchPred.usedRAS         4120                       # Number of times the RAS was used to get a target.
system.cpu_cluster.cpus.branchPredindirectMispredicted          289                       # Number of mispredicted indirect branches.
system.cpu_cluster.cpus.committedInsts         174425                       # Number of instructions committed
system.cpu_cluster.cpus.committedOps           206649                       # Number of ops (including micro ops) committed
system.cpu_cluster.cpus.cpi                  69.003285                       # CPI: cycles per instruction
system.cpu_cluster.cpus.discardedOps             3889                       # Number of ops (including micro ops) which were discarded before commit
```

HPI:

```
---------- Begin Simulation Statistics ----------
final_tick                                 3335436500                       # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
host_inst_rate                                 128176                       # Simulator instruction rate (inst/s)
host_mem_usage                                2243480                       # Number of bytes of host memory used
host_op_rate                                   151837                       # Simulator op (including micro ops) rate (op/s)
host_seconds                                     1.36                       # Real time elapsed on the host
host_tick_rate                             2450689002                       # Simulator tick rate (ticks/s)
sim_freq                                  1000000000000                       # Frequency of simulated ticks
sim_insts                                      174425                       # Number of instructions simulated
sim_ops                                        206649                       # Number of ops (including micro ops) simulated
sim_seconds                                  0.003335                       # Number of seconds simulated
sim_ticks                                  3335436500                       # Number of ticks simulated
system.cpu_cluster.cpus.branchPred.BTBCorrect            0                       # Number of correct BTB predictions (this stat may not work properly.
system.cpu_cluster.cpus.branchPred.BTBHitPct    22.992201                       # BTB Hit Percentage
system.cpu_cluster.cpus.branchPred.BTBHits        11586                       # Number of BTB hits
system.cpu_cluster.cpus.branchPred.BTBLookups        50391                       # Number of BTB lookups
system.cpu_cluster.cpus.branchPred.RASInCorrect            7                       # Number of incorrect RAS predictions.
system.cpu_cluster.cpus.branchPred.condIncorrect         6800                       # Number of conditional branches incorrect
system.cpu_cluster.cpus.branchPred.condPredicted        37452                       # Number of conditional branches predicted
system.cpu_cluster.cpus.branchPred.indirectHits         1779                       # Number of indirect target hits.
system.cpu_cluster.cpus.branchPred.indirectLookups         5383                       # Number of indirect predictor lookups.
system.cpu_cluster.cpus.branchPred.indirectMisses         3604                       # Number of indirect misses.
system.cpu_cluster.cpus.branchPred.lookups        60416                       # Number of BP lookups
system.cpu_cluster.cpus.branchPred.usedRAS         5796                       # Number of times the RAS was used to get a target.
system.cpu_cluster.cpus.branchPredindirectMispredicted          297                       # Number of mispredicted indirect branches.
system.cpu_cluster.cpus.committedInsts         174425                       # Number of instructions committed
system.cpu_cluster.cpus.committedOps           206649                       # Number of ops (including micro ops) committed
```

Πηγές:

- http://www.gem5.org/Main_Page
- https://nitish2112.github.io/post/gem5-minor-cpu/
- http://www.m5sim.org/SimpleCPU
- https://raw.githubusercontent.com/arm-university/arm-gem5-rsk/master/gem5_rsk.pdf