PWM controller design with Zynq SoC

Antonio Minighin

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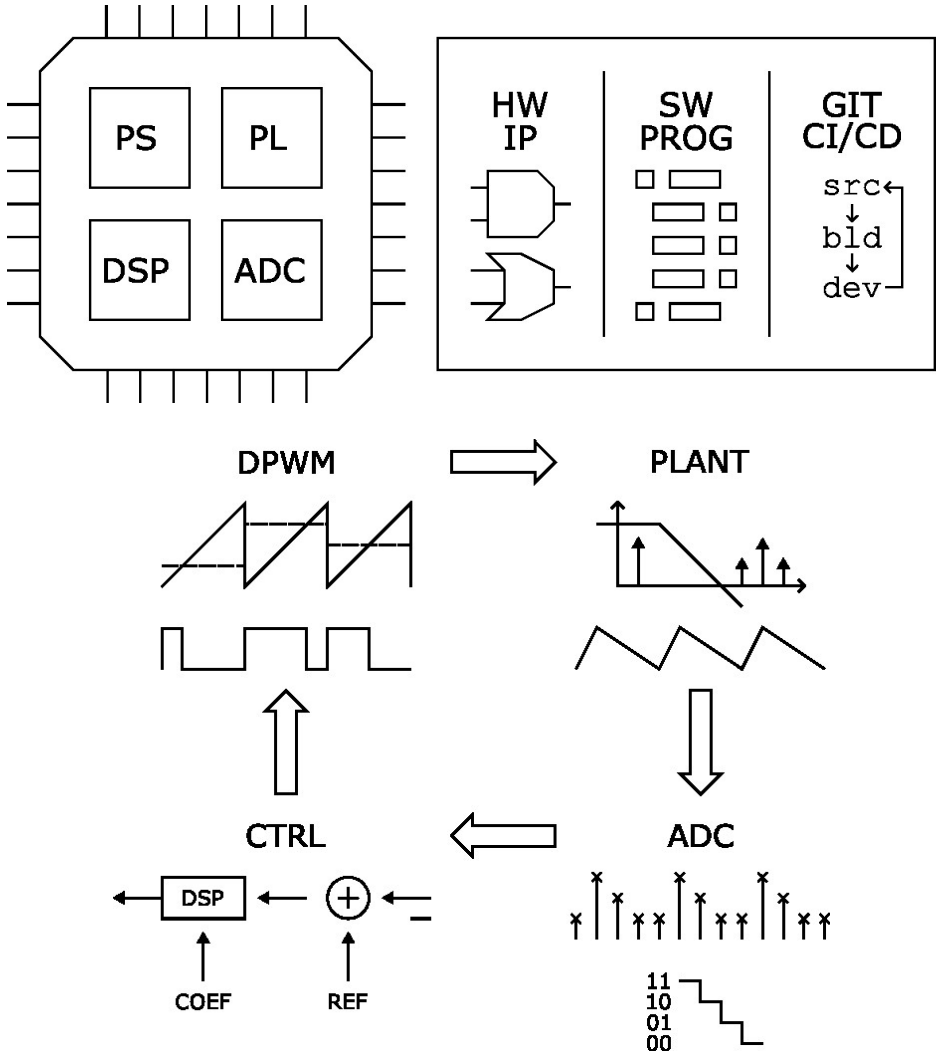
Outline

Topics

- Embedded SoC + FPGA
  - CPU timing
  - DSP acceleration
- DPWM Control System
  - PWM technique
  - PID controller

Final

- Zynq DPWM controller
  - SAW-TRI modulation
  - HW-SW processing



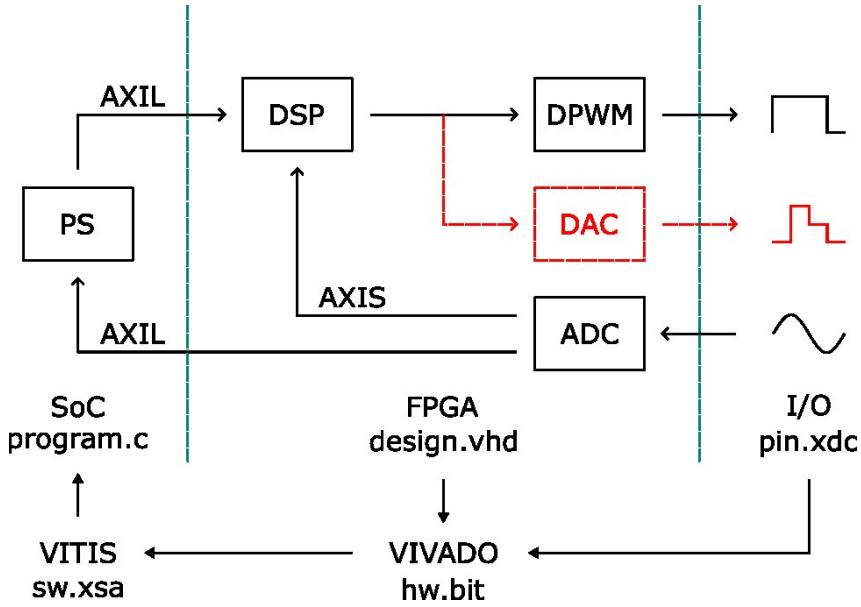
Block Diagram

design.vhd

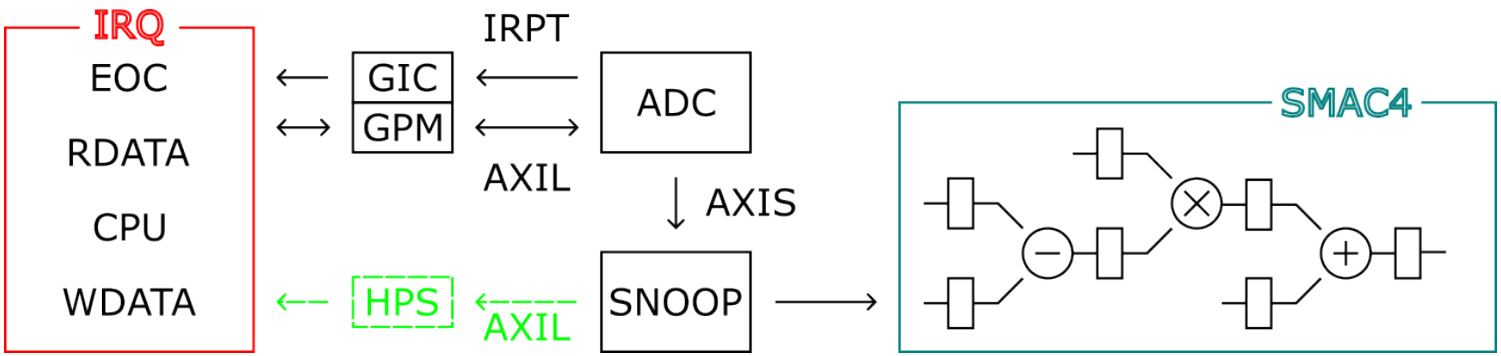
- DSP pipeline SMAC4
- ADC axis router
- DPWM timer comparator

program.c

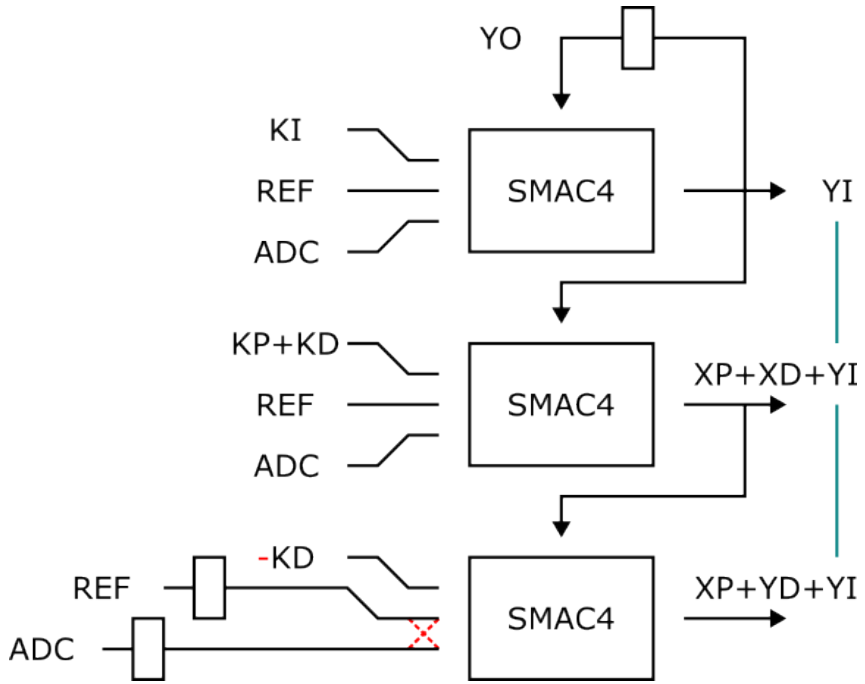
- config
  - DSP coefficients/bypass
  - ADC instants/openloop
  - DPWM ramp/range
- runtime
  - IRQ handler



SW/HW Controller



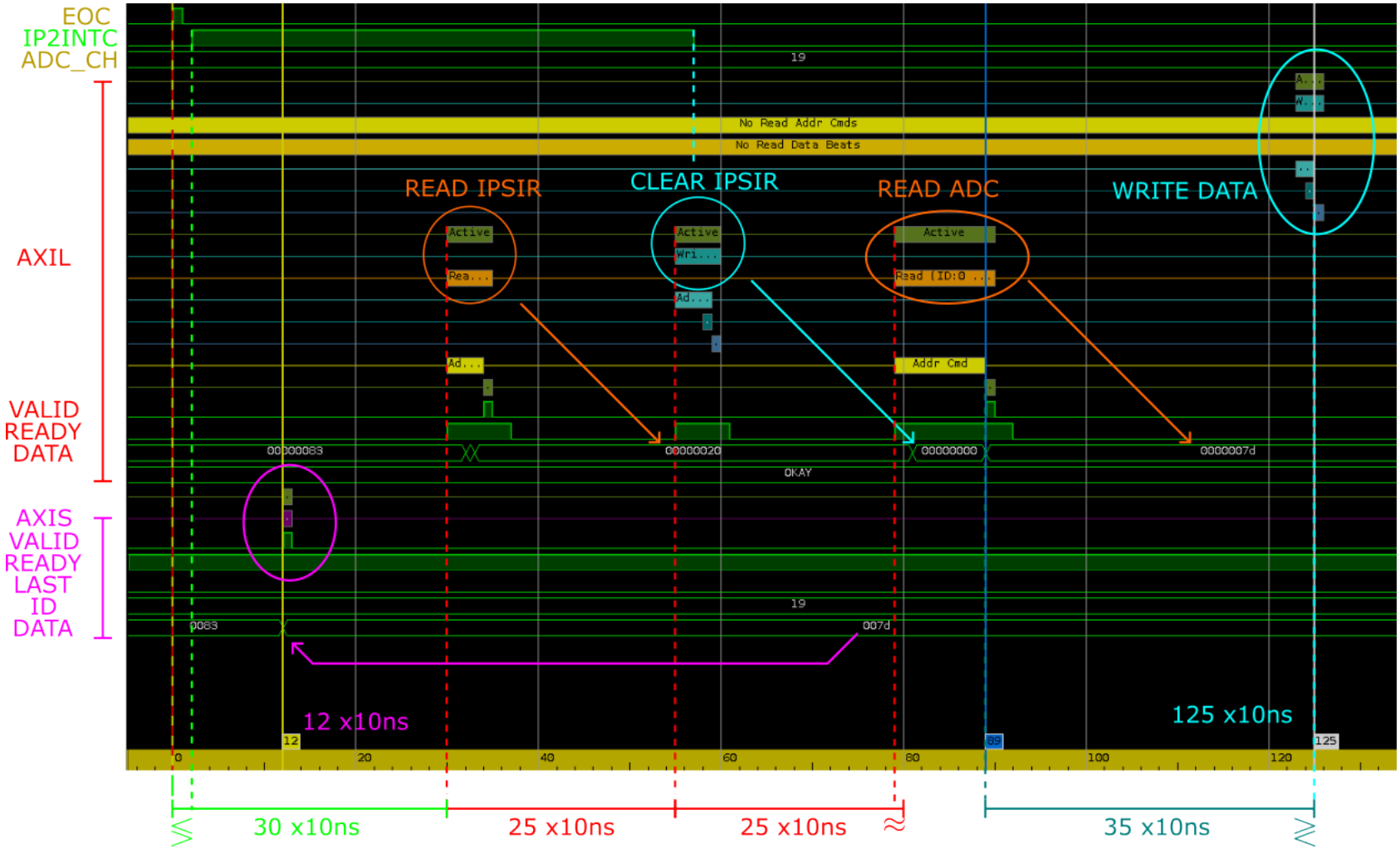

```
void IRQHandler(void *CallBackRef){
    // >>> AXI READ >>>
    reg = AXI_mRead(XADC, IPISR);
    adc = AXI_mRead(XADC, VAUX) >> 4;
    // >>> SOFTWARE PID >>>
    err = ref - adc;
    xi = kiT*err >> shift;
    xd = kdF*err >> shift;
    xp = kp*err >> shift;
    yi = yold + xi;
    yd = xd - xold;
    y = yi + xp + yd;
    // >>> STORE VARIABLES >>>
    yold = yi;
    xold =  xd;
    // >>> AXI WRITE >>>
    AXI_mWrite(DSP, CMP, y);
    AXI_mWrite(XADC, IPISR, reg);
```



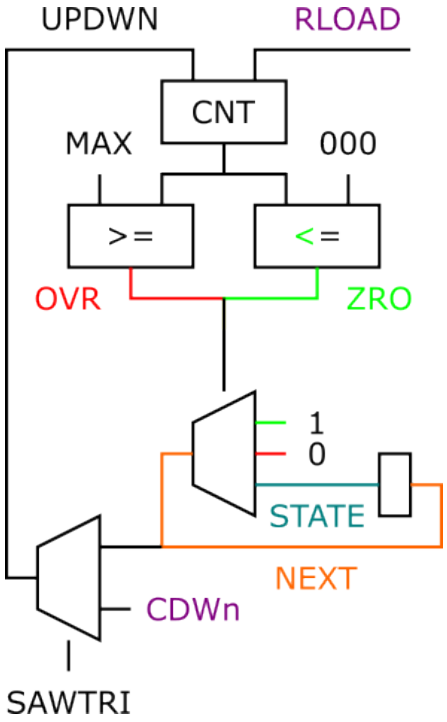
Timing $T_{CLK} = 10ns$

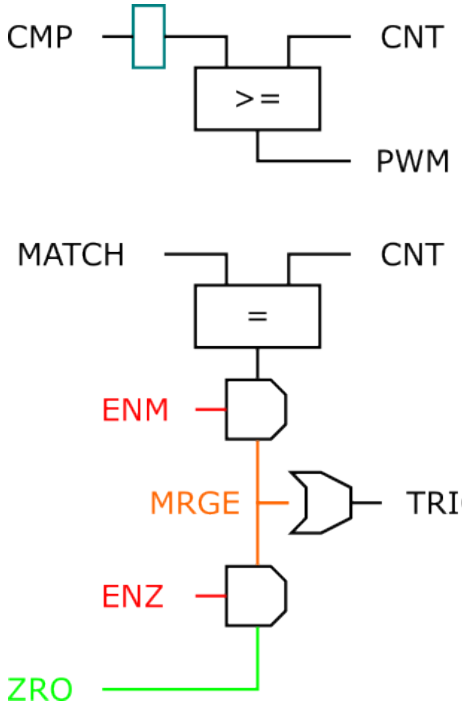
$$T_{ADC} = (105 \pm 1)T_{CLK} \approx 1us$$

$$T_{DSP} \approx [4 + 2(D - 1)]T_{CLK} = 80ns$$



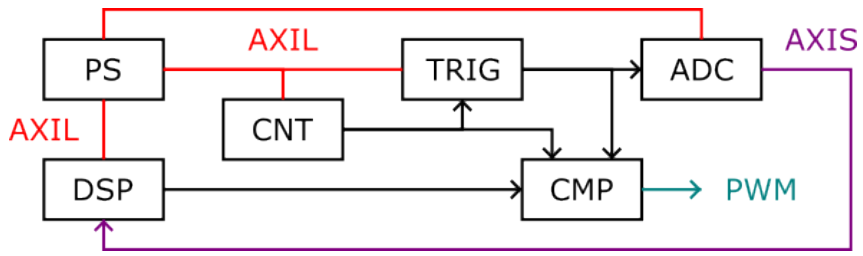
Digital PWM



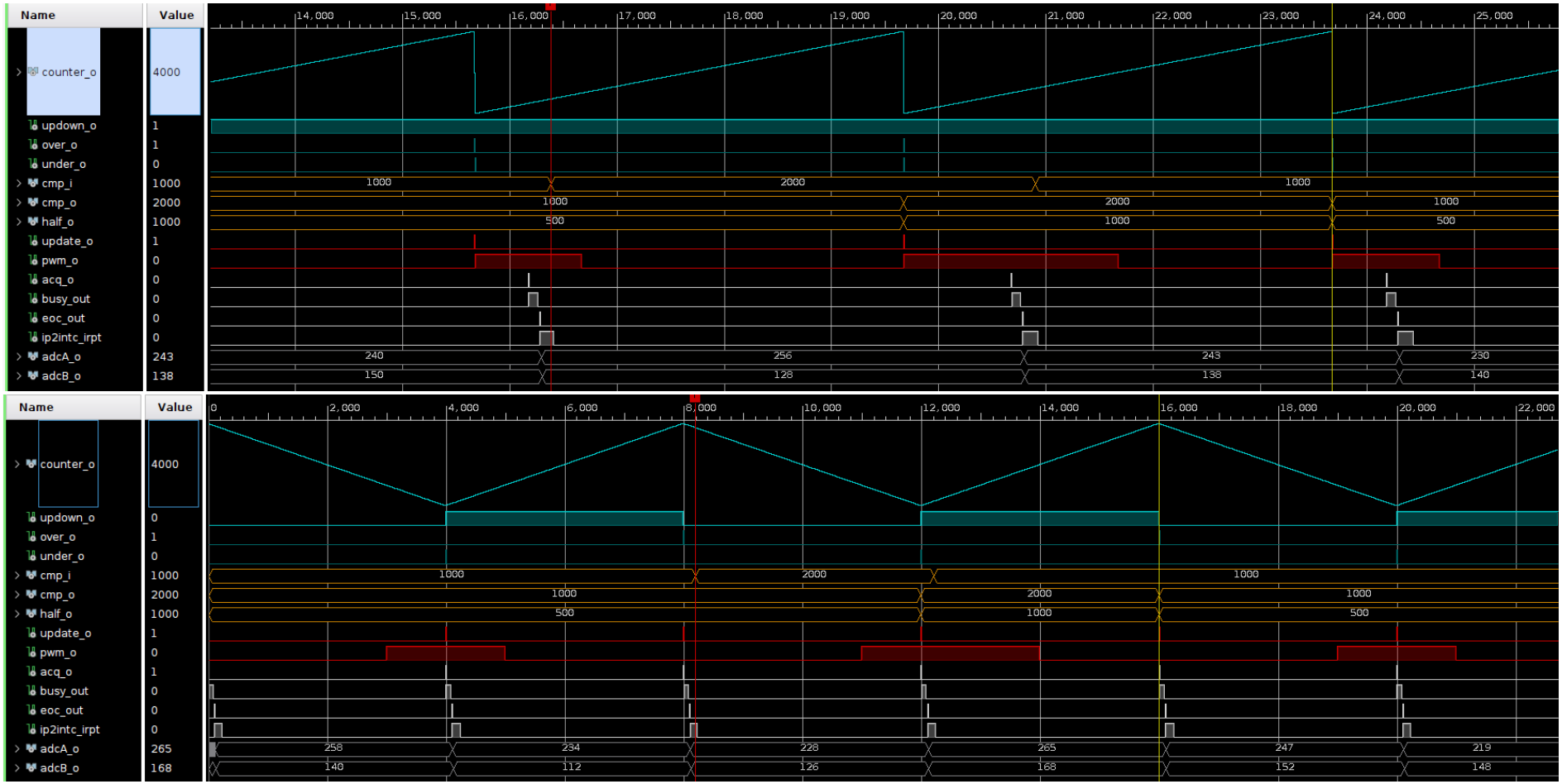


x 2^ = → CLK = 100MHz

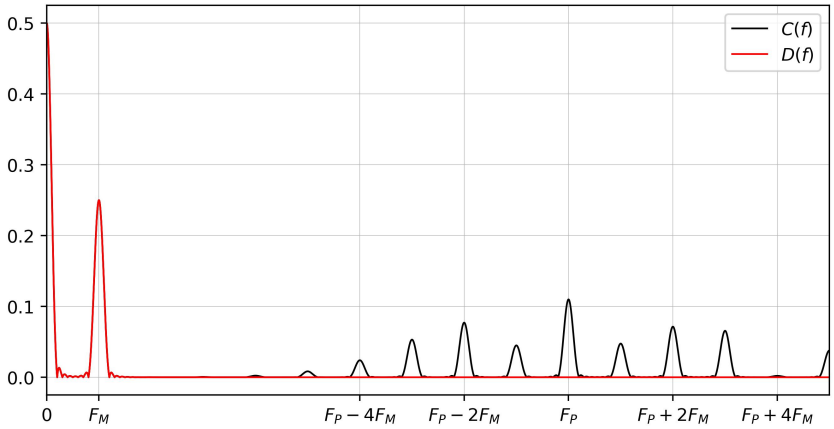
ENOB	8bit	12bit	16bit
MOD	390kHz	24kHz	1.5kHz

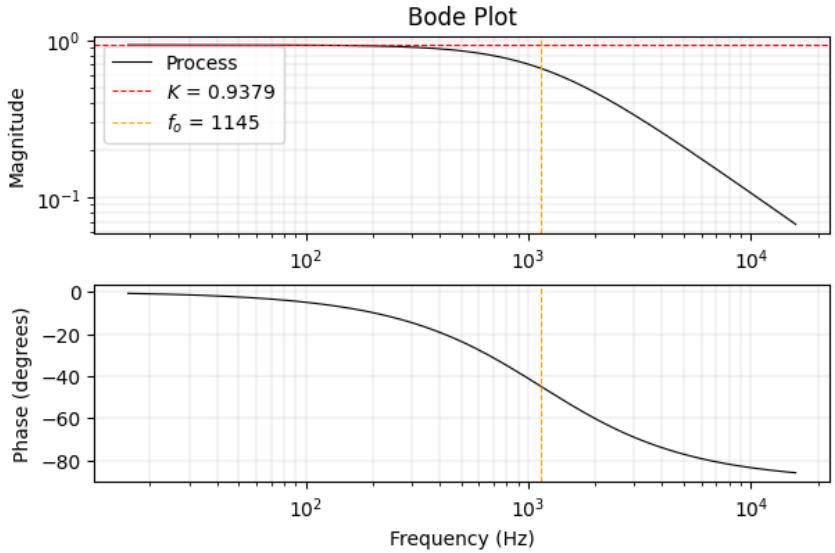


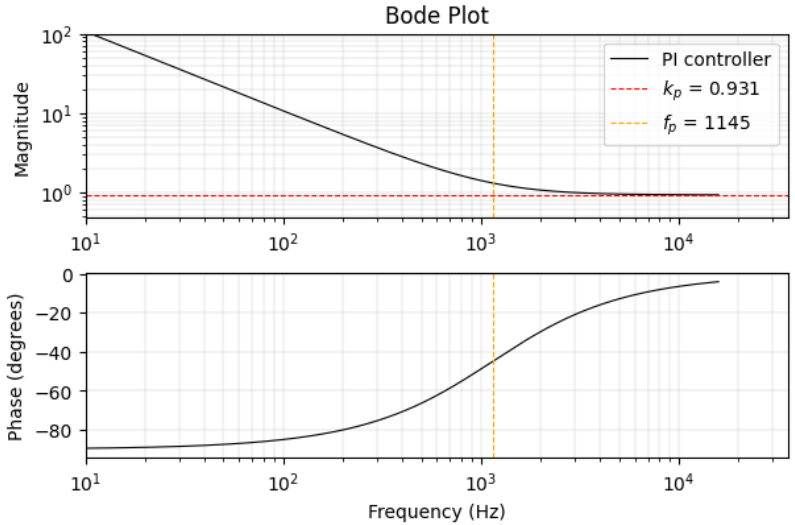
SAW TRI Timing

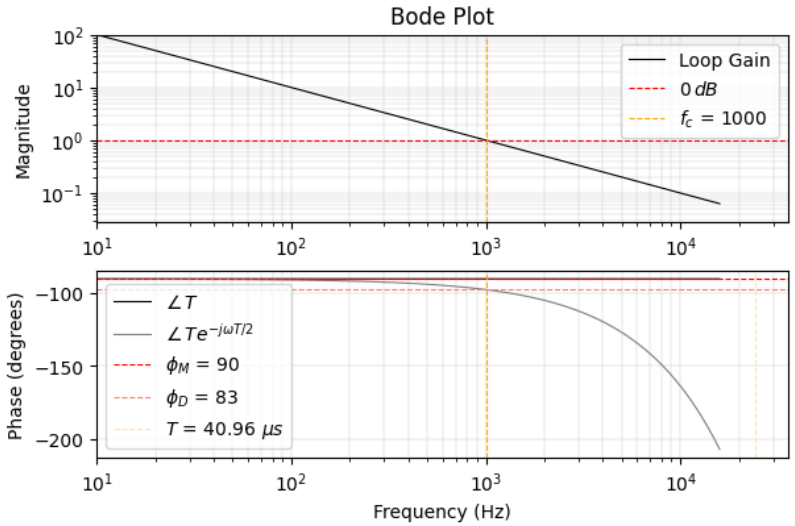


Test setup MOD = 24kHz

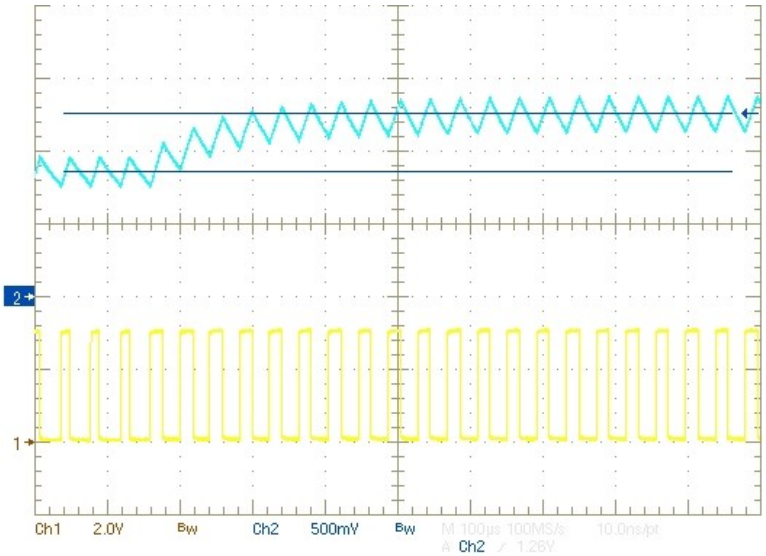


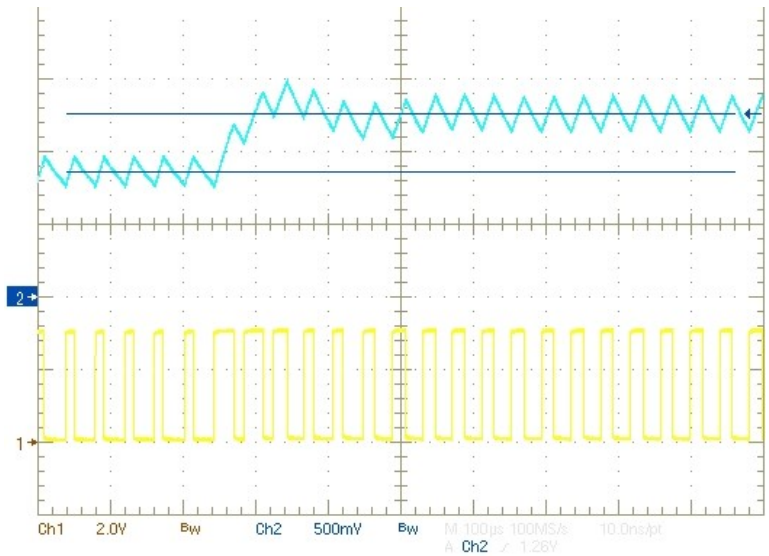


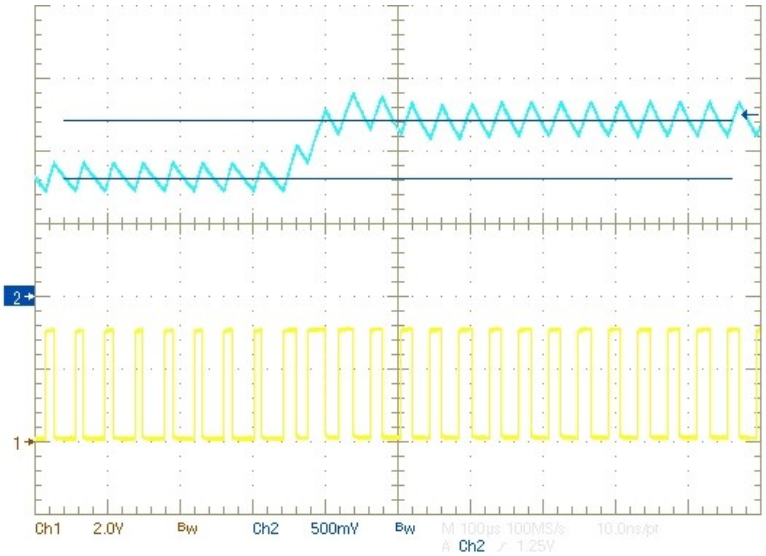


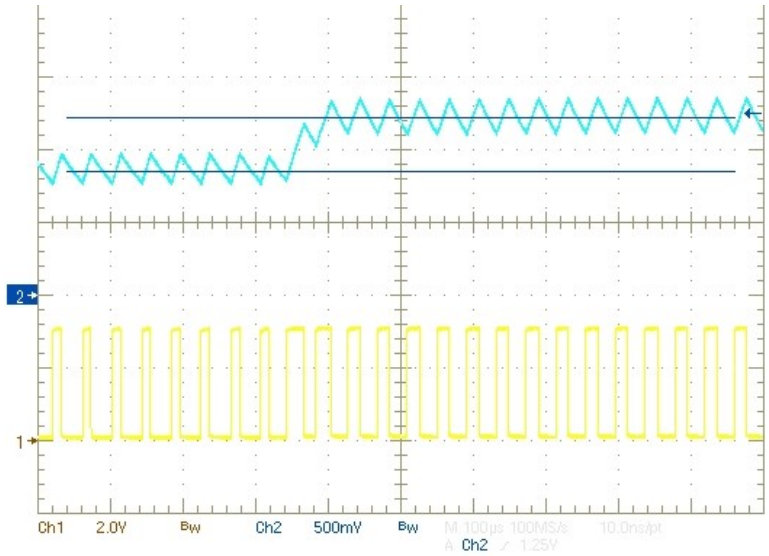


Step response SAW-TRI









Thank you!

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