Anton Melnychuk

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EDUCATION

Yale University, B.S. in Electrical Engineering & Computer Science *May 2026 (Senior)*

- **Relevant Coursework (GPA 3.65/4):** Computer Networks, Building Distributed Systems, Big Data Systems (Disaggregated Infra), Computer Architecture (EE)†, Introduction to VLSI System Design (EE), FPGA-Based Acceleration, Design and Implementation of Operating Systems†, Principles of Computer System Design.

Osaka Gakuin University, Study Abroad Japan, Intermediate-Advanced Japanese. *Jun 2023 - Aug 2023*

Programming:	Rust; C; C++; SystemVerilog (VHDL; Python; Go; Bash; x86-64 asm; Systemd)
Technologies:	AWS/GCP; K8s; Linux; eBPF/LKM; Xilinx (Vivado, Vitis); Yocto; Terraform; git
Language Skills:	English; Ukrainian (Native); Russian; Japanese (Advanced); Polish (Limited)

RELEVANT WORK EXPERIENCE

Thesis, Yale Computer Systems Lab (Prof. Bhattacharjee) *July 2025 −Present*

- Contributed to VLSI design restructuring for peripheral interfaces and data pipelines on the previously taped-out neural-processor ASIC (BCI) supporting Intan-based signal processing at 46 Mbps under an ultra-low-power budget.
- Developing ASIC-based FFT accelerators for implanted BCI applications, including Verilog implementation, physical synthesis in 12nm CMOS, and evaluation of area, power, and latency for an upcoming paper submission.

FPGA Research Intern, Yale Efficient Computing Lab (Prof. Lin Zhong) [View] *Jan 2024 - Present [1.5 year]*

- Set up and implemented a Vivado PS/PL design for a QEC decoding system that overcomes real-time resource constraints of 100 logical qubit decoding using a distributed GTX Aurora SFP+ network across 5 Xilinx VMK180 FPGAs.
- Partnered with Xilinx to co-develop a scalable SoC management tool for remote virtual file system based deployment of Versal/UltraScale+ FPGAs, enabling Linux runtime reconfiguration with A/B fallback.

Rust Operating System, System Programming Course [View] *Sep 2024 - Apr 2025 [8 month]*

- Developed rWeensyOS (5k+ LOC), a minimal POSIX-compatible teaching-purpose microkernel written in memory-safe Rust with FFI bindings to a C/x86_64 assembly bootloader; adopted by Yale's core systems course (Spring '24).
- Assisted on a prototype Rust-based network driver for Theseus, experimental Rust operating system, with support for high-throughput NICs (e.g. 10GbE), integrating eBPF hooks for dynamic packet filtering and runtime safety analysis.

Embedded Engineer, Iron Flight (Ukraine Humanitarian Drone R&D) *July 2024 - December 2024 [5 month]*

- Partitioned drone DNN workloads from STM32 MCU to a remote host with onboard FPV goggles.

OPEN SOURCE CONTRIBUTOR

Rust for Linux Initiative, Open-Source Contributor [View] *June 2024 −July 2024 [1 month]*

- Contributed to open-source Linux kernel (Ubuntu 22.04) to allow kernel cross-compile Rust loadable kernel modules.

Fast Raft: Hierarchical Consensus, Performance-Based Study [View] *Nov 2024 −Feb 2025 [3 month]*

- Developed the first gRPC-based implementation of the Fast Raft (vs Raft) hierarchical consensus algorithm in Go.

PROJECTS

FPGA-Based HFT Accelerator, Personal Project (modeled after MIT 6.111) *June 2025 −Present (Ongoing)*

- Custom open-source FPGA high-frequency trading accelerator, achieving sub-μs latency over NASDAQ ITCH.
- Pipelined architecture for real-time parsing, book-building, and MVP trading with scalable throughput.

Custom CPU with Speculative OoO Execution, Computer Architecture [View] *March 2025 −May 2025 [2 month]*

- Built a SystemVerilog CPU with speculative fetch, dynamic scheduling, reorder buffer, and in-order retirement.
- Achieved an average 33.2% speedup on SPEC-like benchmarks with robust handling of WAW hazards and data deps.