MITSUBISHI MICROCOMPUTERS

M5L8042-XXXP

SLAVE MICROCOMPUTER

T-49-19-05

DESCRIPTION

The M5L8042-XXXP is a general-purpose programmable interface device designed for use with a variety of 8-bit microcomputer systems. The device is fabricated using n-channel silicon-gate ED-MOS technology.

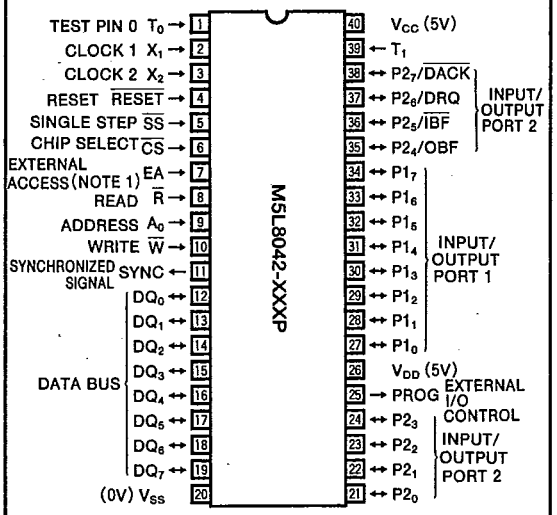
FEATURES

- Mask ROM ..... 2048-word by 8-bit
- Static RAM ..... 128-word by 8-bit
- 18 programmable I/O pins
- Asynchronous data register for interface to master processor
- 8-bit CPU, ROM, RAM, I/O, timer, clock and low-power stand-by mode
- Single 5V power supply
- Alternative to custom LSI
- Interchangeable with i8042

APPLICATION

Alternative to custom LSI for peripheral interfaces

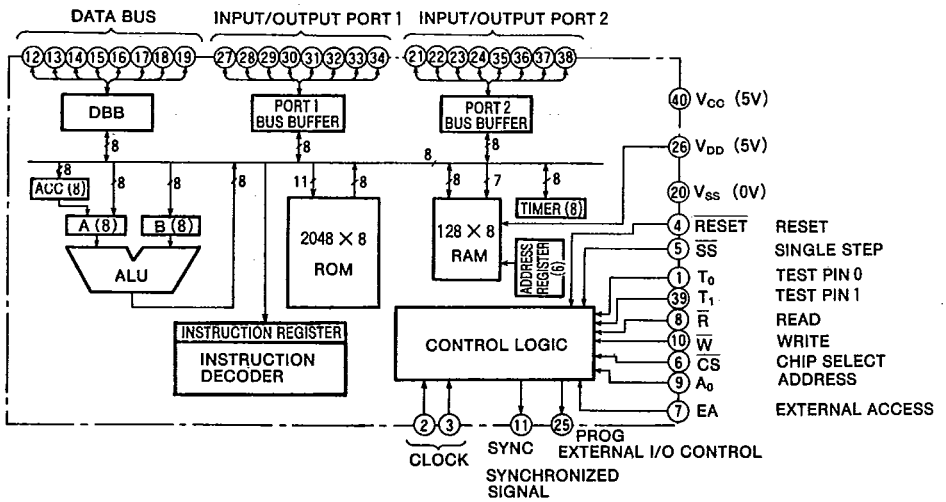
PIN CONFIGURATION (TOP VIEW)



Outline 40P4

Note 1 : Connect to V_{SS} in the operating condition.

BLOCK DIAGRAM



FUNCTION

The M5L8042-XXXP is designed as an ordinary 8-bit CPU peripheral LSI chip and it contains a small stand-alone microcomputer. Although this microcomputer functions independently, when it is used as a peripheral controller, it is called the slave microcomputer in contrast to the master computer. These two devices can transfer the data alternatively through the buffer register between them. The M5L8042-XXXP contains the buffer register to use this LSI as a slave microcomputer and it can be accessed in the same way as other standard peripheral devices. Since the M5L8042-XXXP is a complete microcomputer, it is easy to develop a user-oriented mask-programmed peripheral LSI only by changing the control software.

PIN DESCRIPTION

Pin	Name	Input or output	Function
V_{SS}	Ground	—	Connected to a 0V supply (ground).
V_{CC}	Main power supply	—	Connected to a 5V supply.
V_{DD}	Power supply	—	Connected to a 5V supply. Used as a memory hold when V_{CC} is cut off.
T_0	Test pin 0	Input	Provides external control of conditional program jumps (JTO/JNTO instructions).
X_1, X_2	Crystal inputs	Input	An internal clock circuit is provided so that by connecting an RC circuit or crystal to these input pins, the clock frequency can be determined. X_1 and X_2 can also be used to input an external clock signal.
$\overline{RESET}$	Reset	Input	CPU initialization input.
$\overline{SS}$	Single step	Input	Used to halt the execution of a command by the CPU. When used in combination with the SYNC signal, the command execution of the CPU can be halted every instruction to enable single step operation.
$\overline{CS}$	Chip select input	Input	Chip select input for data bus control.
EA	External access	Input	Normally maintained at 0V.
$\overline{R}$	Read enable signal	Input	Serves as the read signal when the master CPU is accepting data on the data bus from the M5L8042-XXXP.
A_0	Address input	Input	An address input used to indicate whether the signal on the data bus is data or a command.
$\overline{W}$	Write enable signal	Input	Serves as the write signal when the master CPU is outputting data from the bus to the M5L8042-XXXP.
SYNC	Sync signal output	Output	Output 1 time for each machine cycle.
DQ_0~DQ_7	Data bus	Input/output	Three-state, bidirectional data bus. Data bus is used to interface the M5L8042-XXXP to a master system data bus.
$P2_0$~$P2_7$	Port 2	Input/output	Quasi-bidirectional port. When used as an input port, FF_{16} must first be output to this port. After resetting, however, when not used afterwards as an output port, this is not necessary. $P2_0$~$P2_3$ are used when the M5L8243P I/O expander is used.
PROG	Program	Output	Serves as the strobe signal when the M5L8243P I/O expander is used.
$P1_0$~$P1_7$	Port 1	Input/output	Quasi-bidirectional port. When used as an input port, FF_{16} must first be output to this port. After resetting, however, when not used afterwards as an output port, this is not necessary.
T_1	Test pin 1	Input	Provides external control of conditional program jumps (JT1/JNT1 instructions). Can serve as the input pin for the event counter (STRT CNT instruction).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~7	V
V_{DD}	Supply voltage		−0.5~7	V
V_I	Input voltage		−0.5~7	V
V_O	Output voltage		−0.5~7	V
P_d	Power dissipation	T_a = 25℃	1500	mW
T_{opr}	Operating temperature range		0~70	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.2			V
V_{IL}	Low-level input voltage			0.8	V
$f_{(\phi)}$	Operating frequency	1		12	MHz

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5 V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{IH1}	High-level input voltage (all except X_1, X_2, $\overline{RESET}$)		2.2		V_{CC}	V
V_{IH2}	High-level input voltage (X_1, X_2, $\overline{RESET}$)		3.8		V_{CC}	V
V_{OL1}	Low-level output voltage (DQ_0~DQ_7)	I_{OL} = 2mA			0.45	V
V_{OL2}	Low-level output voltage ($P1_0$~$P1_7$, $P2_0$~$P2_7$, SYNC)	I_{OL} = 1.6 mA			0.45	V
V_{OL3}	Low-level output voltage (PROG)	I_{OL} = 1mA			0.45	V
V_{OH1}	High-level output voltage (DQ_0~DQ_7)	I_{OH} = −400μA	2.4			V
V_{OH2}	High-level output voltage (all other outputs)	I_{OH} = −50μA	2.4			V
I_I	Input leakage current (T_0, T_1, $\overline{R}$, $\overline{W}$, $\overline{CS}$, A_0, EA)	$V_{SS} \leq V_I \leq V_{CC}$	−10		10	μA
I_{OZL}	High-impedance state output leakage current (DQ_0~DQ_7)	V_{SS} + 0.45 ≤ $V_O \leq V_{CC}$	−10		10	μA
I_{IL1}	Low-level input load current ($P1_0$~$P1_7$, $P2_0$~$P2_7$)	V_{IL} = 0.8V	−0.5			mA
I_{IL2}	Low-level input load current ($\overline{RESET}$, $\overline{SS}$)	V_{IL} = 0.8V	−0.2			mA
I_{DD}	Supply current from V_{DD}				10	mA
$I_{CC} + I_{DD}$	Total supply current				145	mA

TIMING REQUIREMENTS (T_a = 0~70℃, V_{CC} = 5V±10%, unless otherwise noted)

DBB Read

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{C(\phi)}$	Cycle time	t_{CY}		1.25		15	μs
$t_{W(R)}$	Read pulse width	t_{RR}	$t_{C(\phi)}$ = 1.25 μs	160			ns
$t_{SU(CS-R)}$	Chip select setup time before read	t_{AR}		0			ns
$t_{h(R-CS)}$	Chip select hold time after read	t_{RA}		0			ns

DBB Write

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{W(W)}$	Write pulse width	t_{WW}		160			ns
$t_{SU(CS-W)}$ $t_{SU(A0-W)}$	$\overline{CS}$, A_0, setup time before write	t_{AW}		0			ns
$t_{h(W-CS)}$ $t_{h(W-A0)}$	$\overline{CS}$, A_0, hold time after write	t_{WA}		0			ns
$t_{SU(DQ-W)}$	Data setup time before write	t_{DW}		130			ns
$t_{h(W-DQ)}$	Data hold time after write	t_{WD}		0			ns

Port 2

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{W(PR)}$	PROG pulse width	t_{PP}		700			ns
$t_{SU(PC-PR)}$	Port control setup time before PROG	t_{CP}	C_L = 80pF	80			ns
$t_{h(PR-PC)}$	Port control hold time after PROG	t_{PC}	C_L = 20pF	60			ns
$t_{SU(Q-PR)}$	Output data setup time before PROG	t_{DP}	C_L = 80pF	200			ns
$t_{SU(D-PR)}$	Input data hold time before PROG	t_{PR}	C_L = 80pF			650	ns
$t_{h(PR-D)}$	Input data hold time after PROG	t_{PF}	C_L = 20pF	0		150	ns

DMA

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{SU(DACK-R)}$	$\overline{DACK}$ setup time before read	t_{ACC}		0			ns
$t_{h(R-DACK)}$	$\overline{DACK}$ hold time after read	t_{CAC}		0			ns
$t_{SU(DACK-W)}$	$\overline{DACK}$ setup time before write	t_{ACC}		0			ns
$t_{h(W-DACK)}$	$\overline{DACK}$ hold time after write	t_{CAC}		0			ns

Note 1 : Input voltage level V_{IL} = 0.45V, V_{IH} = 2.4V.

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V±10%, unless otherwise noted)

DBB Read

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PZX(CS-DQ)}$	Data enable time after $\overline{CS}$	t_{AD}	C_L = 100 pF			130	ns
$t_{PZX(A0-DQ)}$	Data enable time after address	t_{AD}	C_L = 100 pF			130	ns
$t_{PZX(R-DQ)}$	Data enable time after read	t_{RD}	C_L = 100 pF			130	ns
$t_{PXZ(R-DQ)}$	Data disable time after read	t_{DF}				85	ns

DMA

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PZX(DACK-DQ)}$	Data enable time after $\overline{DACK}$	t_{ACD}	C_L = 150 pF			130	ns
$t_{PHL(R-DRQ)}$	DRQ disable time after read	t_{CRQ}				90	ns
$t_{PHL(W-DRQ)}$	DRQ disable time after write	t_{CRQ}				90	ns

Note 2 : Output voltage discriminating levels, low and high, are 0.8V and 2.0V respectively.

TIMING DIAGRAMS

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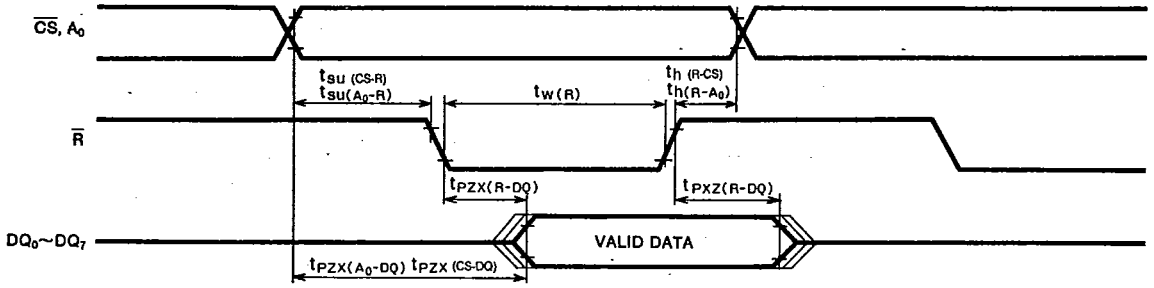
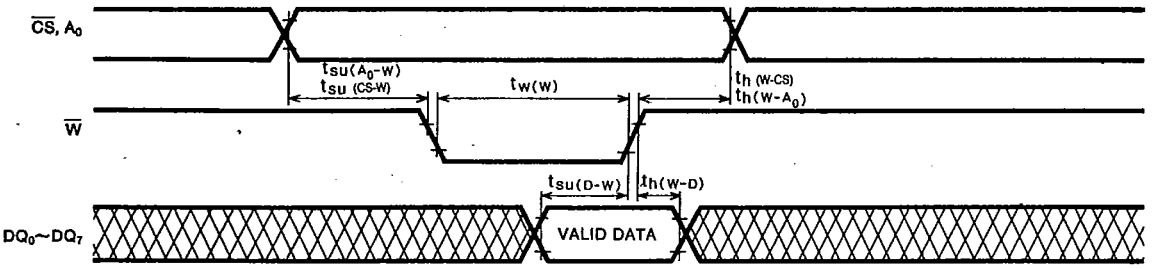
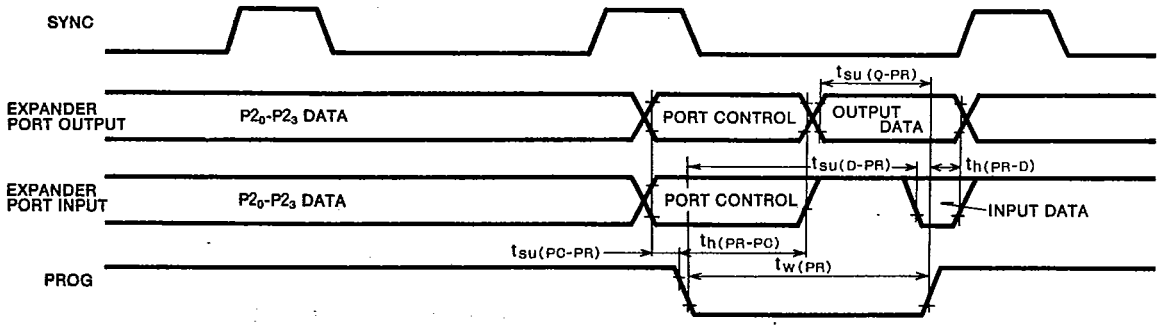
Read



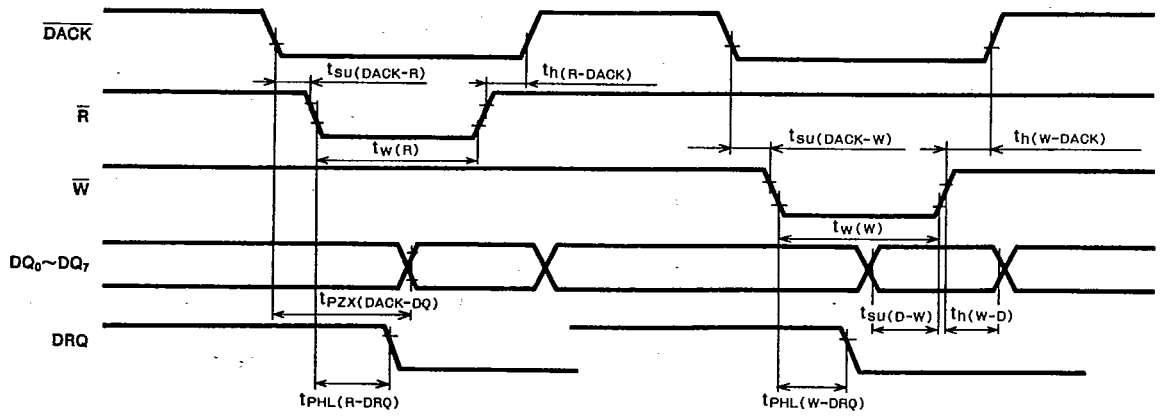
Write



Port 2



DMA



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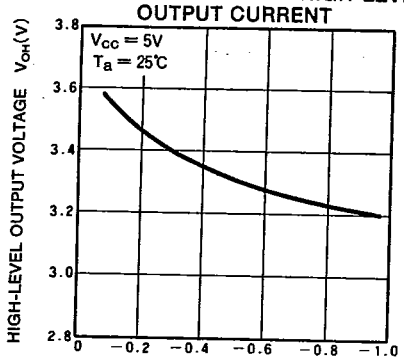
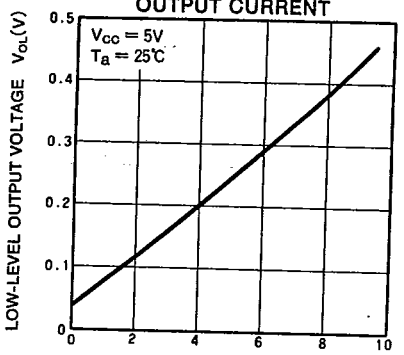
TYPICAL CHARACTERISTICS

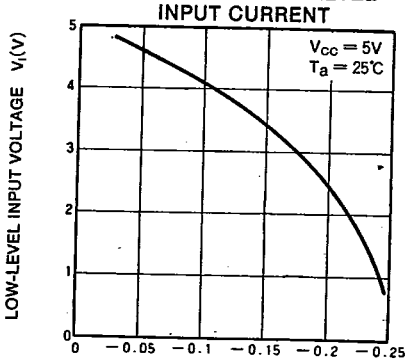
DATA BUS HIGH-LEVEL OUTPUT VOLTAGE VS. HIGH-LEVEL OUTPUT CURRENT



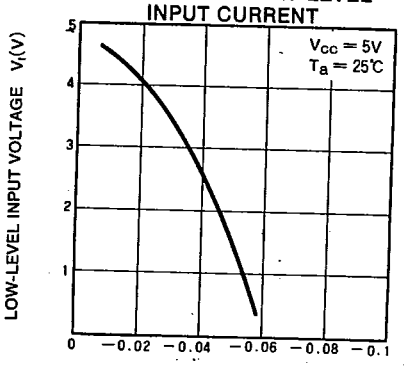
DATA BUS LOW-LEVEL OUTPUT VOLTAGE VS. LOW-LEVEL OUTPUT CURRENT



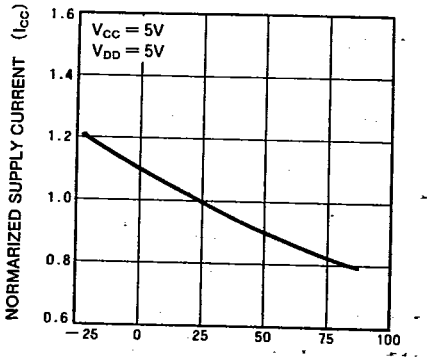
P_1, P_2 LOW-LEVEL INPUT VOLTAGE VS. LOW-LEVEL INPUT CURRENT



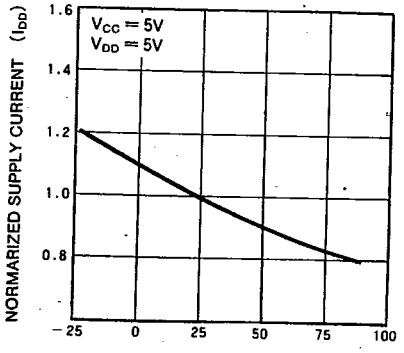
RESET LOW-LEVEL INPUT VOLTAGE VS. LOW-LEVEL INPUT CURRENT



NORMARIZED SUPPLY CURRENT (I_{CC}) VS. AMBIENT TEMPERATURE

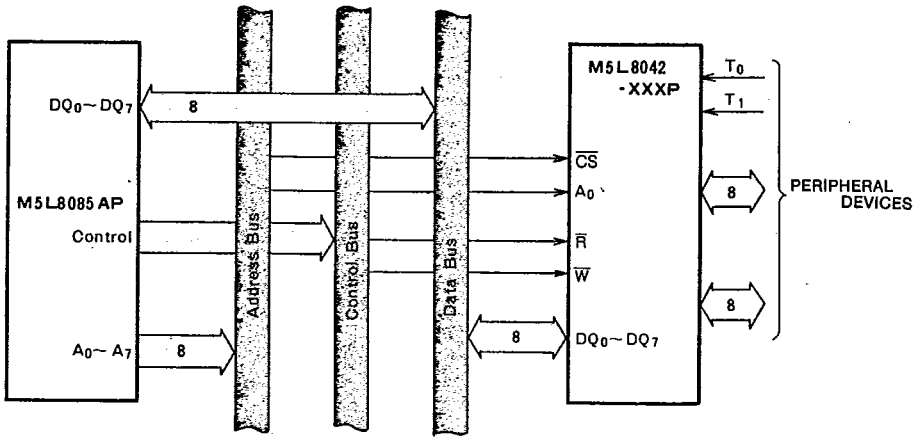


NORMARIZED SUPPLY CURRENT (I_{DD}) VS. AMBIENT TEMPERATURE



APPLICATION EXAMPLES

(1) Interface with M5L8085AP



(2) Interface with Series MELPS 8-48 Microcomputer and M5L8243P