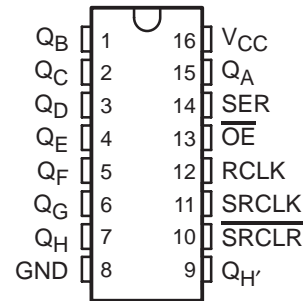


- 8-Bit Serial-In, Parallel-Out Shift
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 14$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Shift Register Has Direct Clear

DW, E, M, NS, OR SM PACKAGE
 (TOP VIEW)



description/ordering information

The CD74HC595 device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers. The shift register has a direct overriding clear (\overline{SRCLR}) input, serial (SER) input, and serial output for cascading. When the output-enable (\overline{OE}) input is high, the outputs are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|--------------|-----------------------|------------------|
| –55°C to 125°C | PDIP – E | Tube of 25 | CD74HC595E | CD74HC595E |
| | SOIC – DW | Tube of 40 | CD74HC595DW | HC595M |
| | | Reel of 2000 | CD74HC595DWR | |
| | SOIC – M | Tube of 40 | CD74HC595M | HC595M |
| | | Reel of 2500 | CD74HC595M96 | |
| | | Reel of 250 | CD74HC595MT | |
| | SOP – NS | Reel of 2000 | CD74HC595NSR | HC595M |
| | SSOP – SM | Tube of 80 | CD74HC595SM | HJ595 |
| | | Reel of 2000 | CD74HC595SM96 | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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CD74HC595

8-BIT SHIFT REGISTERS

WITH 3-STATE OUTPUT REGISTERS

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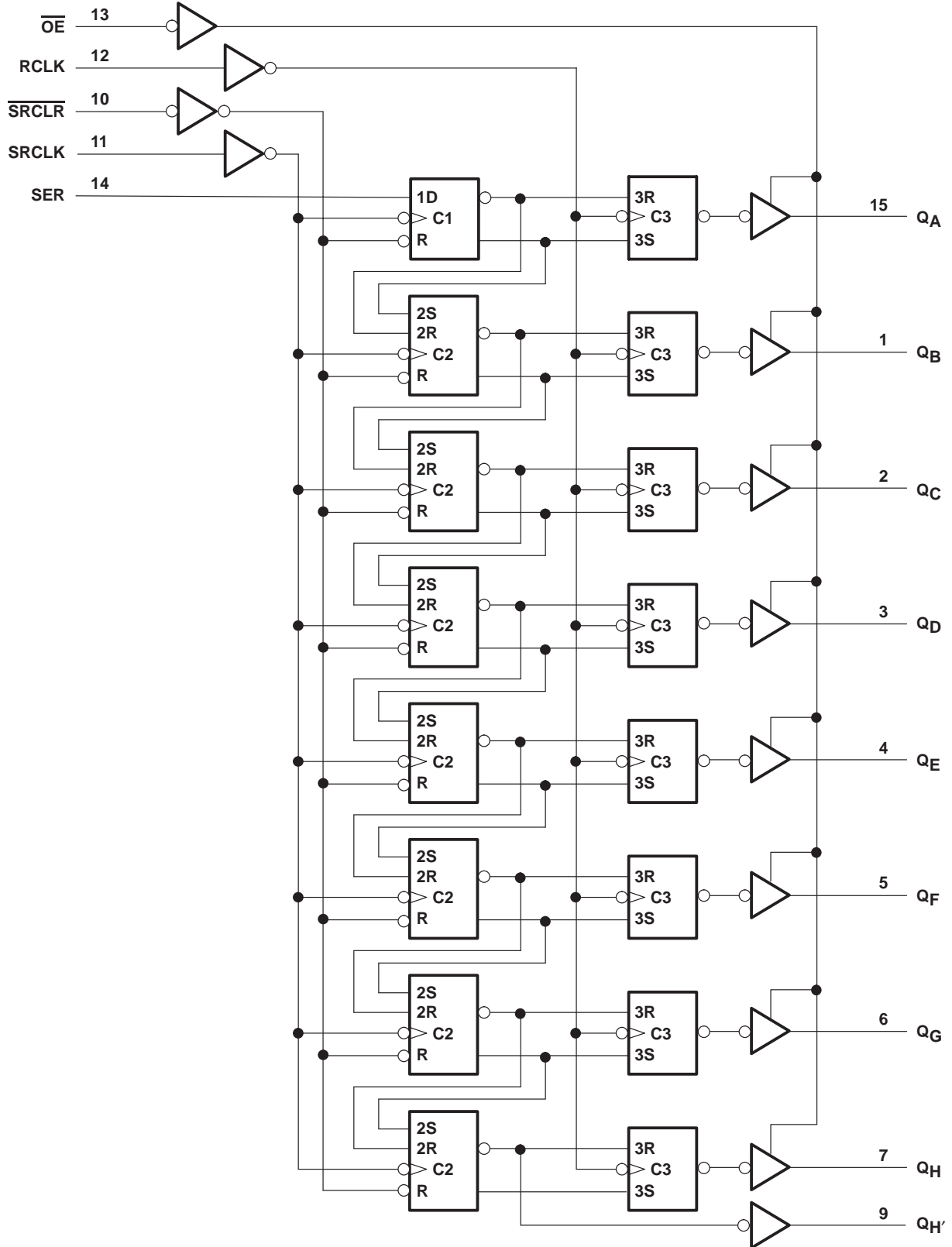
FUNCTION TABLE

| INPUTS | | | | | FUNCTION |
|--------|-------|---------------------------|------|------------------------|--|
| SER | SRCLK | $\overline{\text{SRCLR}}$ | RCLK | $\overline{\text{OE}}$ | |
| X | X | X | X | H | Outputs Q_A – Q_H are disabled. |
| X | X | X | X | L | Outputs Q_A – Q_H are enabled. |
| X | X | L | X | X | Shift register is cleared. |
| L | ↑ | H | X | X | First stage of the shift register goes low. Other stages store the data of previous stage, respectively. |
| H | ↑ | H | X | X | First stage of the shift register goes high. Other stages store the data of previous stage, respectively. |
| X | X | X | ↑ | X | Shift-register data is stored in the storage register. |



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logic diagram (positive logic)



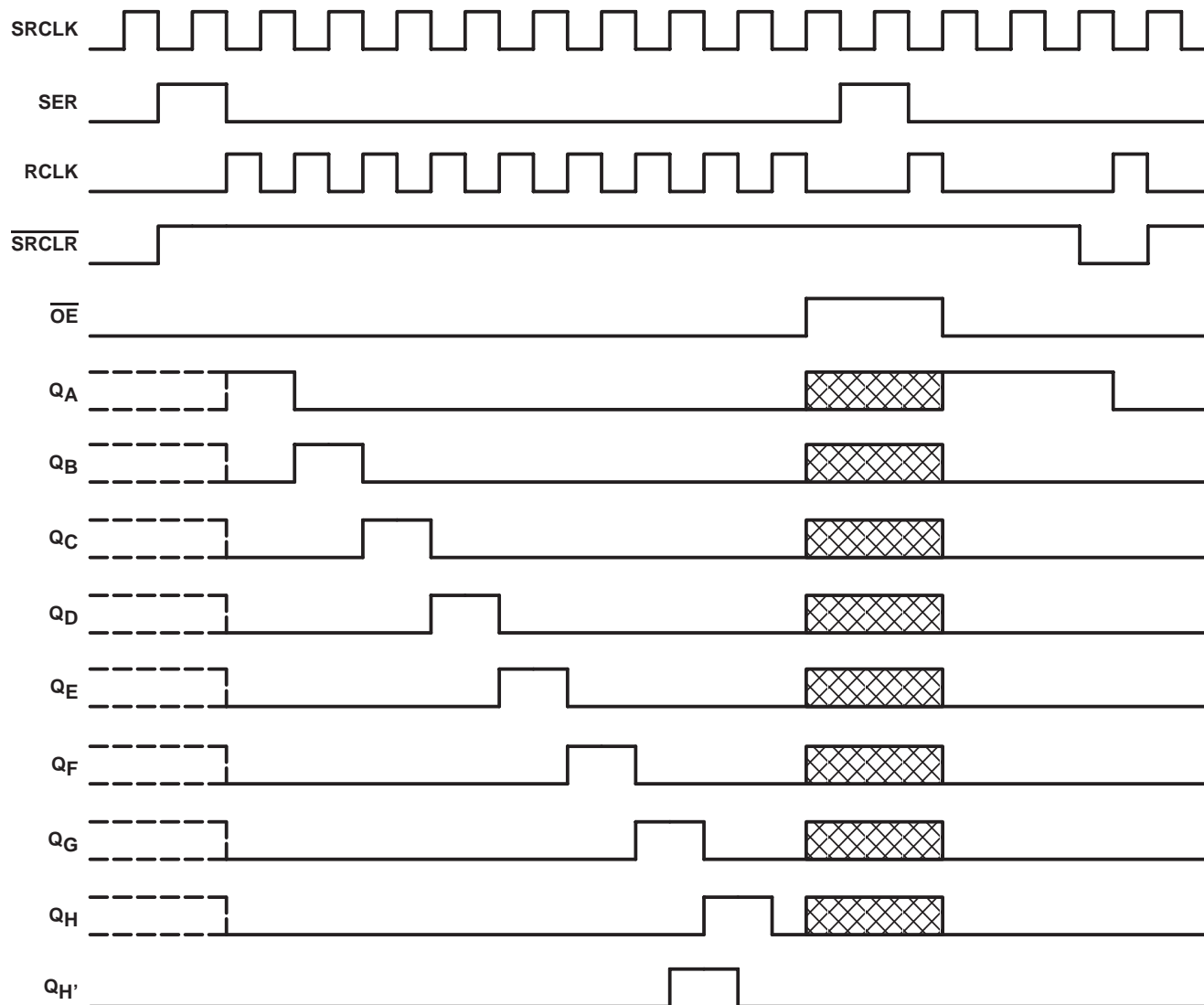
CD74HC595


8-BIT SHIFT REGISTERS

WITH 3-STATE OUTPUT REGISTERS

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timing diagram



NOTE:  implies that the output is in 3-State mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|----------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±35 mA |
| Continuous current through V_{CC} or GND | ±70 mA |
| Package thermal impedance, θ_{JA} (see Note 2): E package | 67°C/W |
| DW package | 57°C/W |
| M package | 73°C/W |
| NS package | 64°C/W |
| SM package | 82°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | MIN | NOM | MAX | UNIT |
|--------------------------------|---------------------------------|------------------|------|----------|------|
| V_{CC} | Supply voltage | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | 1.5 | | V |
| | | $V_{CC} = 4.5$ V | 3.15 | | |
| | | $V_{CC} = 6$ V | 4.2 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | 0.5 | V |
| | | $V_{CC} = 4.5$ V | | 1.35 | |
| | | $V_{CC} = 6$ V | | 1.8 | |
| V_I | Input voltage | 0 | | V_{CC} | V |
| V_O | Output voltage | 0 | | V_{CC} | V |
| $\Delta t/\Delta v^{\ddagger}$ | Input transition rise/fall time | $V_{CC} = 2$ V | | 1000 | ns |
| | | $V_{CC} = 4.5$ V | | 500 | |
| | | $V_{CC} = 6$ V | | 400 | |
| T_A | Operating free-air temperature | –55 | | 125 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

[‡] If this device is used in the threshold region (from $V_{ILmax} = 0.5$ V to $V_{IHmin} = 1.5$ V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_f = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

CD74HC595
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | T _A = -55°C TO 125°C | | T _A = -40°C TO 85°C | | UNIT |
|-----------------|---|--|-----------------|-----------------------|-------|------|---------------------------------|-------|--------------------------------|-------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 µA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | | V |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | Q _{H'} , I _{OH} = -4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | Q _A -Q _H , I _{OH} = -6 mA | | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | Q _{H'} , I _{OH} = -5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| | | Q _A -Q _H , I _{OH} = -7.8 mA | | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| | | | | | | | | | | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 µA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | Q _{H'} , I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | Q _A -Q _H , I _{OL} = 6 mA | | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | Q _{H'} , I _{OL} = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| | | Q _A -Q _H , I _{OL} = 7.8 mA | | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| | | | | | | | | | | | |
| I _I | V _I = V _{CC} or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| I _{OZ} | V _O = V _{CC} or 0, Q _A -Q _H | | 6 V | | ±0.01 | ±0.5 | | ±10 | | ±5 | µA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 6 V | | | 8 | | 160 | | 80 | µA |
| C _i | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | T _A = -55°C TO 125°C | | T _A = -40°C TO 85°C | | UNIT |
|--------------------|---|-----------------|-----------------------|-----|---------------------------------|-----|--------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 2 V | | 6 | | 4.2 | | 5 | MHz |
| | | 4.5 V | | 31 | | 21 | | 25 | |
| | | 6 V | | 36 | | 25 | | 29 | |
| t _w | SRCLK or RCLK high or low | 2 V | 80 | | 120 | | 100 | | ns |
| | | 4.5 V | 16 | | 24 | | 20 | | |
| | | 6 V | 14 | | 20 | | 17 | | |
| | $\overline{\text{SRCLR}}$ low | 2 V | 80 | | 120 | | 100 | | |
| | | 4.5 V | 16 | | 24 | | 20 | | |
| | | 6 V | 14 | | 20 | | 17 | | |
| t _{su} | SER before SRCLK↑ | 2 V | 100 | | 150 | | 125 | | ns |
| | | 4.5 V | 20 | | 30 | | 25 | | |
| | | 6 V | 17 | | 25 | | 21 | | |
| | SRCLK↑ before RCLK↑† | 2 V | 75 | | 113 | | 94 | | |
| | | 4.5 V | 15 | | 23 | | 19 | | |
| | | 6 V | 13 | | 19 | | 16 | | |
| | $\overline{\text{SRCLR}}$ low before RCLK↑ | 2 V | 50 | | 75 | | 65 | | |
| | | 4.5 V | 10 | | 15 | | 13 | | |
| | | 6 V | 9 | | 13 | | 11 | | |
| | $\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑ | 2 V | 50 | | 75 | | 60 | | |
| | | 4.5 V | 10 | | 15 | | 12 | | |
| | | 6 V | 9 | | 13 | | 11 | | |
| t _h | Hold time, SER after SRCLK↑ | 2 V | 0 | | 0 | | 0 | | ns |
| | | 4.5 V | 0 | | 0 | | 0 | | |
| | | 6 V | 0 | | 0 | | 0 | | |

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

CD74HC595
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF
(unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | $T_A = -55^\circ\text{C TO } 125^\circ\text{C}$ | | $T_A = -40^\circ\text{C TO } 85^\circ\text{C}$ | | UNIT |
|------------|---------------------------|----------------|----------|--------------------------|-----|-----|---|-----|--|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{\max} | | | 2 V | 6 | 26 | | 4.2 | | 5 | | MHz |
| | | | 4.5 V | 31 | 38 | | 21 | | 25 | | |
| | | | 6 V | 36 | 42 | | 25 | | 29 | | |
| t_{pd} | SRCLK | Q_H' | 2 V | | 50 | 160 | | 240 | | 200 | ns |
| | | | 4.5 V | | 17 | 32 | | 48 | | 40 | |
| | | | 6 V | | 14 | 27 | | 41 | | 34 | |
| | RCLK | Q_A-Q_H | 2 V | | 50 | 150 | | 225 | | 187 | |
| | | | 4.5 V | | 17 | 30 | | 45 | | 37 | |
| | | | 6 V | | 14 | 26 | | 38 | | 32 | |
| t_{PHL} | $\overline{\text{SRCLR}}$ | Q_H' | 2 V | | 51 | 175 | | 261 | | 219 | ns |
| | | | 4.5 V | | 18 | 35 | | 52 | | 44 | |
| | | | 6 V | | 15 | 30 | | 44 | | 37 | |
| t_{en} | $\overline{\text{OE}}$ | Q_A-Q_H | 2 V | | 40 | 150 | | 225 | | 187 | ns |
| | | | 4.5 V | | 15 | 30 | | 45 | | 37 | |
| | | | 6 V | | 13 | 26 | | 38 | | 32 | |
| t_{dis} | $\overline{\text{OE}}$ | Q_A-Q_H | 2 V | | 42 | 200 | | 300 | | 250 | ns |
| | | | 4.5 V | | 23 | 40 | | 60 | | 50 | |
| | | | 6 V | | 20 | 34 | | 51 | | 43 | |
| t_t | | Q_A-Q_H | 2 V | | 28 | 60 | | 90 | | 75 | ns |
| | | | 4.5 V | | 8 | 12 | | 18 | | 15 | |
| | | | 6 V | | 6 | 10 | | 15 | | 13 | |
| | | Q_H' | 2 V | | 28 | 75 | | 110 | | 95 | |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF
(unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | $T_A = -55^\circ\text{C TO } 125^\circ\text{C}$ | | $T_A = -40^\circ\text{C TO } 85^\circ\text{C}$ | | UNIT |
|-----------|------------------------|----------------|----------|--------------------------|-----|-----|---|-----|--|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | RCLK | Q_A-Q_H | 2 V | | 60 | 200 | | 300 | | 250 | ns |
| | | | 4.5 V | | 22 | 40 | | 60 | | 50 | |
| | | | 6 V | | 19 | 34 | | 51 | | 43 | |
| t_{en} | $\overline{\text{OE}}$ | Q_A-Q_H | 2 V | | 70 | 200 | | 298 | | 250 | ns |
| | | | 4.5 V | | 23 | 40 | | 60 | | 50 | |
| | | | 6 V | | 19 | 34 | | 51 | | 43 | |
| t_t | | Q_A-Q_H | 2 V | | 45 | 210 | | 315 | | 265 | ns |
| | | | 4.5 V | | 17 | 42 | | 63 | | 53 | |
| | | | 6 V | | 13 | 36 | | 53 | | 45 | |

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C_{pd} Power dissipation capacitance | No load | 400 | pF |

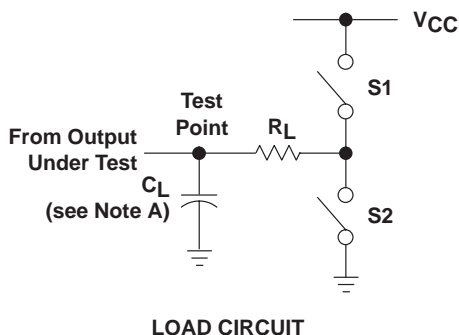
CD74HC595

8-BIT SHIFT REGISTERS

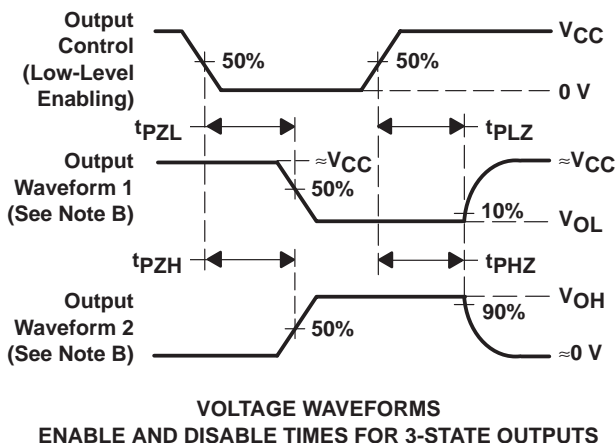
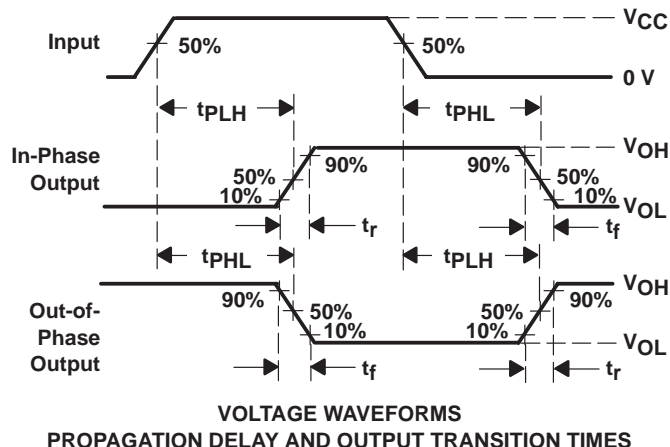
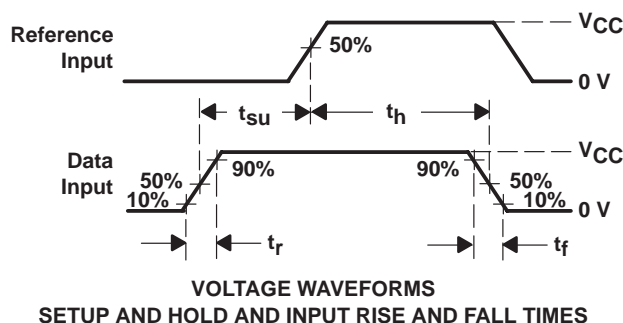
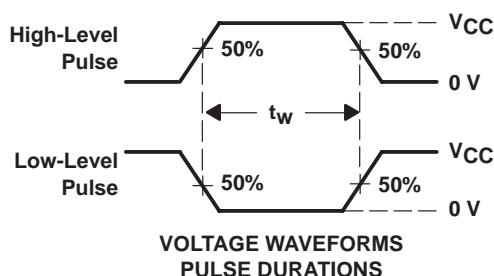
WITH 3-STATE OUTPUT REGISTERS

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PARAMETER MEASUREMENT INFORMATION



| PARAMETER | R_L | C_L | S1 | S2 |
|-------------------|--------------|-----------------|--------|--------|
| t_{en} | 1 k Ω | 50 pF or 150 pF | Open | Closed |
| | | | Closed | Open |
| t_{dis} | 1 k Ω | 50 pF | Open | Closed |
| | | | Closed | Open |
| t_{pd} or t_t | --- | 50 pF or 150 pF | Open | Open |



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - The outputs are measured one at a time, with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD74HC595DW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC595M | Samples |
| CD74HC595DWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC595M | Samples |
| CD74HC595E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC595E | Samples |
| CD74HC595EE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC595E | Samples |
| CD74HC595M | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC595M | Samples |
| CD74HC595M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC595M | Samples |
| CD74HC595MG4 | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC595M | Samples |
| CD74HC595MT | ACTIVE | SOIC | D | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC595M | Samples |
| CD74HC595NSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC595M | Samples |
| CD74HC595SM96 | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ595 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

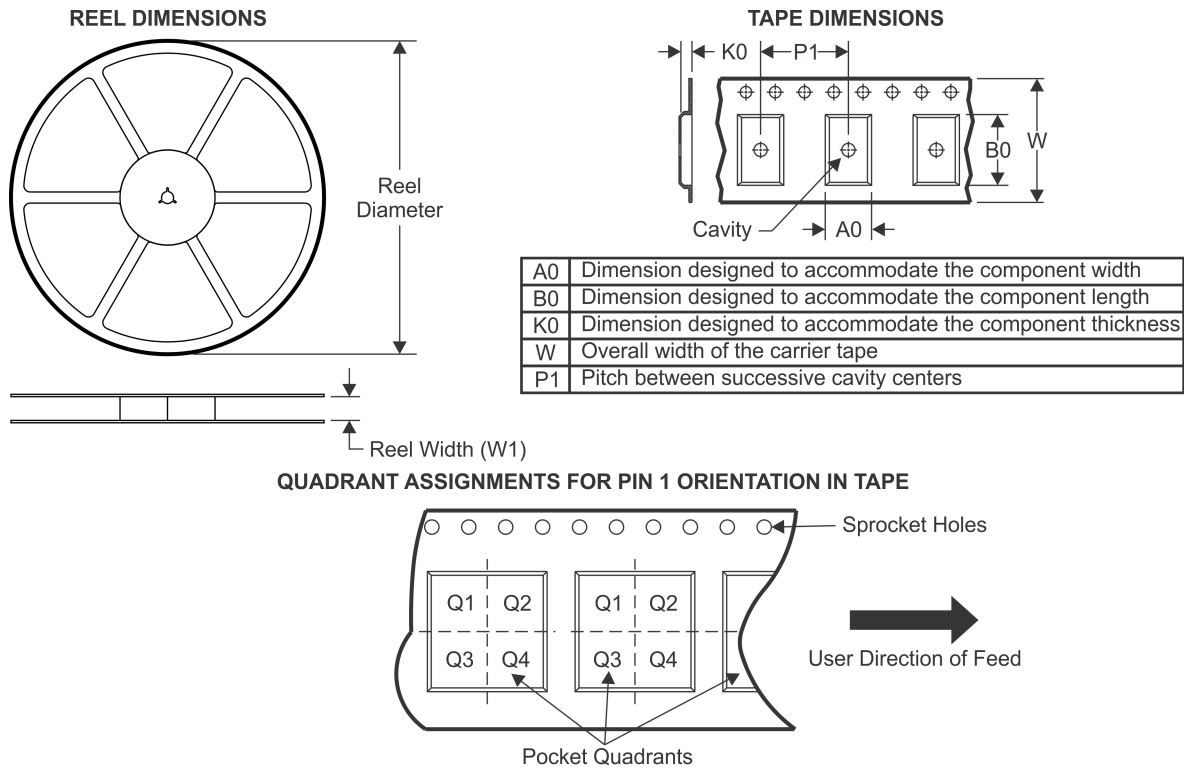
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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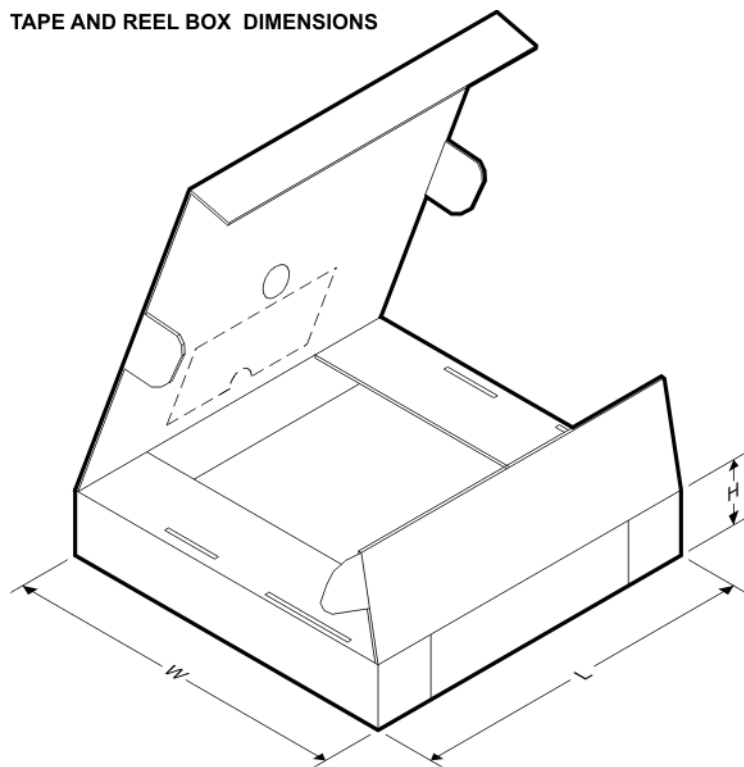
TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC595DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| CD74HC595M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC595NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74HC595SM96 | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC595DWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| CD74HC595M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HC595NSR | SO | NS | 16 | 2000 | 853.0 | 449.0 | 35.0 |
| CD74HC595SM96 | SSOP | DB | 16 | 2000 | 853.0 | 449.0 | 35.0 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---------------|-------|-------|-------|-------|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

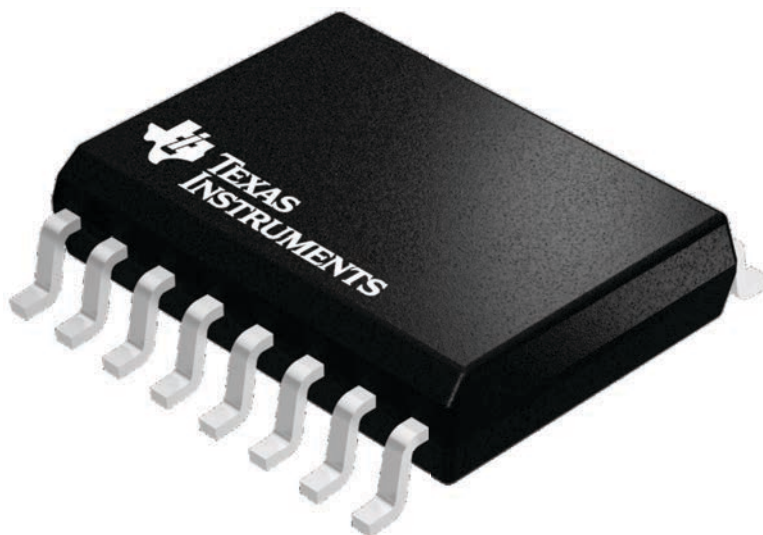
DW 16

SOIC - 2.65 mm max height

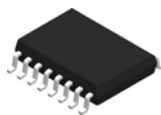
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

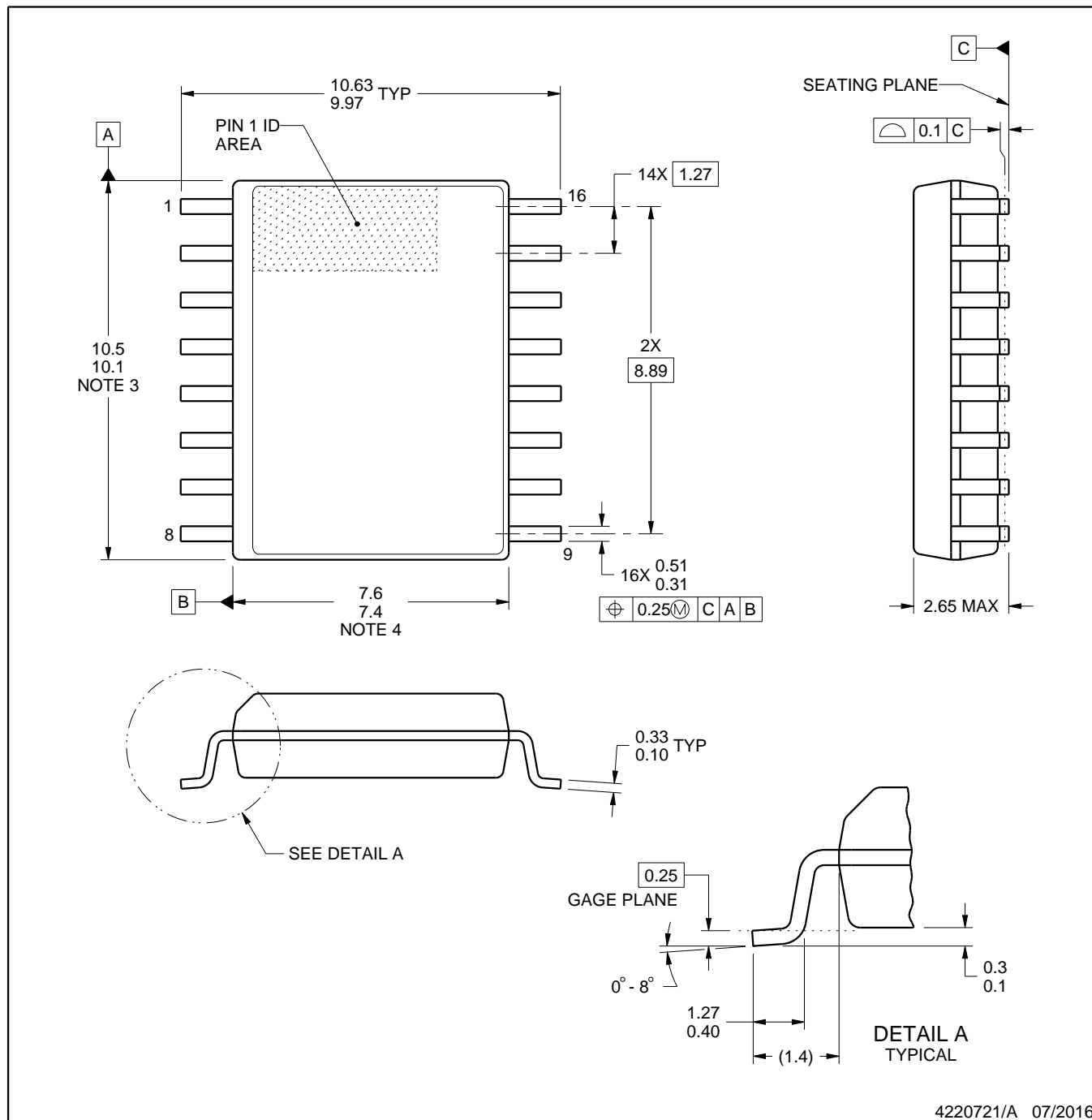


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

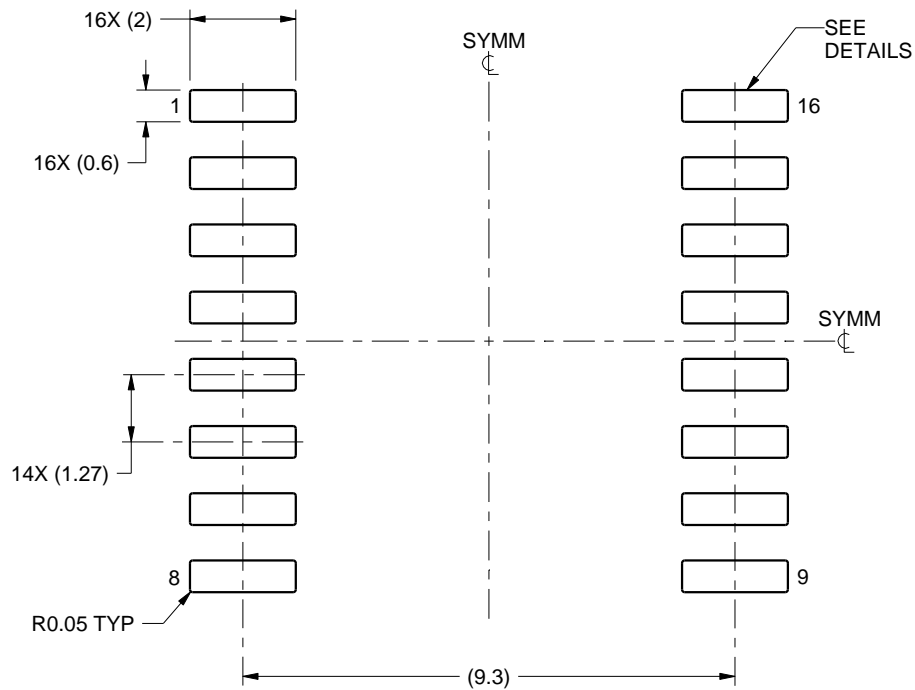
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

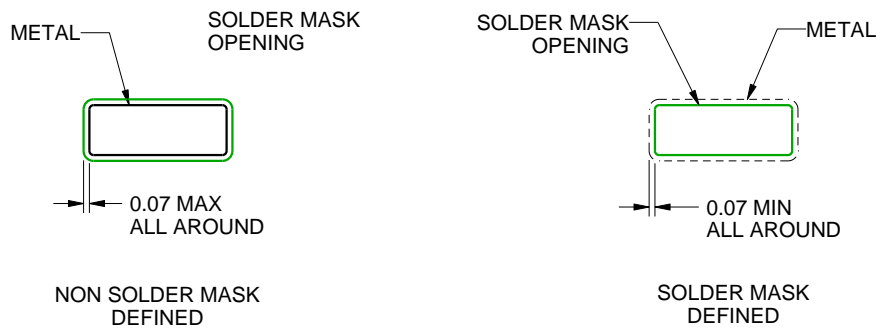
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

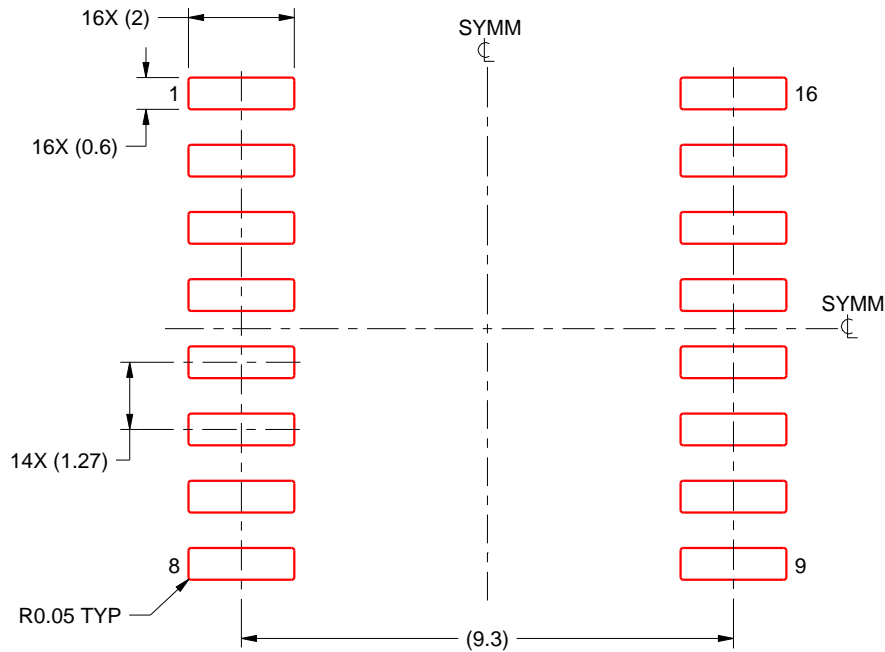
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

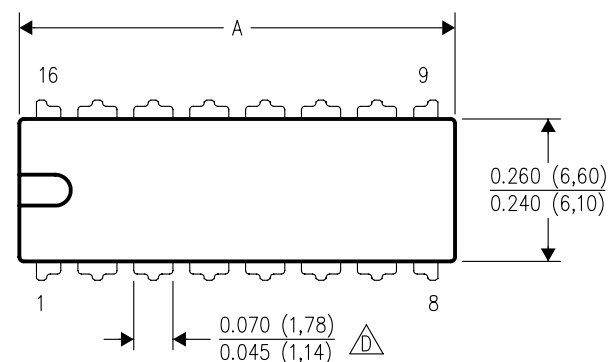


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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