Embedded system, from software to hardware

(EDAN15 VT15 Final Report)

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Abstract

Brief description of the report. Context, hypothesis, experiments, results, conclusion. The abstract should contain enough information about the rest of the document, but not too many details. Between 5–10 lines in this format.

1 Introduction

This is the lab report on the laboratory work in the Embedded Systems Design(EDAN15) course at LTH. The purpose of the laboratory is too use and implement an embedded system hands-on. Too see how different software and hardware solutions differ in relation to effiency, power and utilization. Starting off with pure software solution and slowly descend into hardware solutions. In addtion the purpose is to explore the framework and tool chains related to developing embedded systems. The embedded system used in the laboratory is an FPGA platform.

This part of the course is the practical part where the rest the course is more theorethical.

This document contain our experiments and results from 5 laboratory sessions.

2 Experiments

The experiment was divided into 5 lab sessions. The goal was to evaluate software and harware solutions running on a Xilinix FPGA platform. The board used for testing was a Digilent Nexys-3. All software was developed using C.

First laboratory was to implement and compare two pure soft-ware solution of a Greatest Common Divisor (GCD) algorithm for N numbers. Furthermore, the software has to run on a single processor system.

Second laboratory session was to implement and evaluate again a pure software solution of a gcd algorithm for N numbers. This time the architecture should use a multi-processor system. The system uses two MicroBlaze processors, working on the same data set.

Third and fourth laboratory session was to choose a part of the gcd algorithm for N number and implement it in hardware. The hardware part was writen and simulated in VHDL using Xilinx ISE. The hardware should input/output data following a protocol specifed in the laboratory manual.

Last laboratory session was to integrate the hardware developed in the previous session into a larger system. The system should contain software to write the necessary communication and computations, to obtain a functioning hardware/software solution for the gcd of N-numbers problem.

2.1 Software algorithms

The software algorithm choosen was the Euclidean subtraction algorithm. This was choosen to avoid the need of calculations using division, modulo and recursion. The algorithm is very simple and well defined.

```
function gcd(a,b)
        while(a != b) {
                if a>b
                        a = a-b
                else
                        b = b-a
        }
        return a;
}
```

Listing 1: Euclidean subtracion algorithm

2.2 Single processor

The single processor system was implemented using a single MicroBlaze core. Software handled reading data from the serial port, calculate gcd and output it too the user. The gcd used is the one described above.

2.3 Dual processor

The dual processor system was implemented using two separate MicroBlaze cores. The communicated using two FSL-connections connected to each core. This was choosen over sharing memory between the two cores. Relation between the cores was divided into master/slave where one core acted as the master. The software was divided onto the two cores accordingly with the master/slave principle. Software on the master core was responsible for fetching the input data, split it and send half of it to the slave core. The slave core contained only the code for communcating through FSL and calculating gcd. Both cores calculated gcd for their half the data set. Final caluclation was done on the master core after the slave had returned the gcd for the data set on the slave core.

2.4 Hardware accelerated

The part choosen for hardware acceleration was the gcd algorithm. More specific gcd for two numbers and not N numbers. The hardware runs on a custom IP-core on the same board as the MicroBlaze core running the software. The software reads input and output each element in the data set through FSL-communication to the hardware core.

Use pictures and timing diagrams, such as the one in Figure 1. Do explain every picture and diagram.

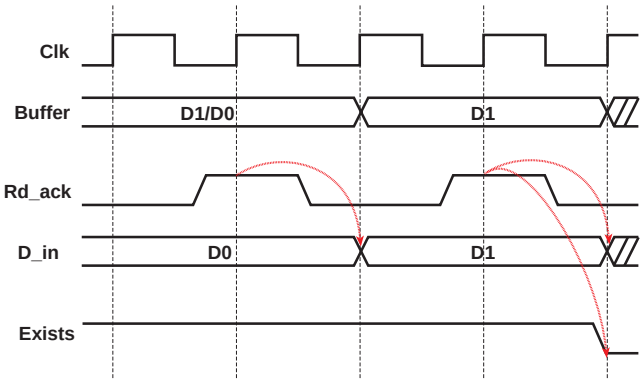

Figure 1: A figure example

3 Measurements and Discussion

This is probably the most important part of the report. In here you must describe the what and how you measure. Describe any specific parts in the hardware architecture or the software that help you conduct measurements. You should use graphs or tables to present your results, such as Table 1 or 2, but do not forget to describe the measures and units in the columns or graph axis.

Item		
GCD	Single Processor	Dual processor
Hardware accelerated ($)		
10	2433868	13.65
30	1846630	0.01
50	13142315	92.50
70	1479966	33.33
100	3152887	8.99

Table 1: Clockcycles using the different solutions.

		Primes				
		2	3	5	7	
Powers	504	3	2	0	1	
	540	2	3	1	0	
Powers	gcd	2	2	0	0	min
	lcm	3	3	1	1	max

Table 2: Uses *multirow* LaTeXpackage

Say a few words about the complexity of the different solutions and how long did it take to reach a working design.

3.1 Performance

Give the performance figures for your solutions. Note that both the number of clock cycles AND the clock frequency is important for performance!

Discuss how and why the figures are different in between solutions. Discuss how these figures are different from your expectation. For example, should a dual processor system be twice faster than a single processor system? Is it? Why? How about compiler optimizations?

Explain whether and how the data sets your algorithm operates on influence the results. For example, why computing the something for 10 numbers is slower than computing the same thing for 30 numbers?

3.2 Device Utilization

Give the FPGA resources consumed by each of your solutions. Explain how these relate to each other – e.g. whether a dual processor system has double the area of a single processor system and how do these relate to the hardware accelerated solution. Explain why or how using different algorithms influences or not the device utilization.

3.3 Power and Energy

The power and energy consumption are also important for a design. The XPower Analyser that comes with the Xilinx ISE helps you determine the power consumption for your designs. Have a look at the hierarchical breakdown of power consumption and identify the parts of your design that consume a lot of power. Also, as you know energy is the time integral of power:

$$E = \int_{t_1}^{t_2} P dt \approx P \Delta t \tag{1}$$

How do your different solutions compare from the power and energy consumption point of view?

4 Summary

In this part you briefly summarize your report. Continue with conclusions, lessons learned, unexpected results, unsolved problems or other issues that remain open. Relate back to the content of the course and explain whether or how the laboratory work helped you or not with understanding certain issues from the theoretical part.

References