cadence®

Reference Manual

Generic 45nm Salicide 1.0V/1.8V 1P 11M

Process Design Kit

and Rule Decks (PRD)

Revision 6.0

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Table of Contents

1 Overview

The purpose of this Reference Manual is to describe the technical details of the 45nm Generic Process Design Kit (“GPDK045”) provided by Cadence Design Systems, Inc. (“Cadence”).

1.1 Software Environment

The GPDK045 has been designed for use within a Cadence software environment that consists of the following tools –

GPDK045 Cadence IC618 Database

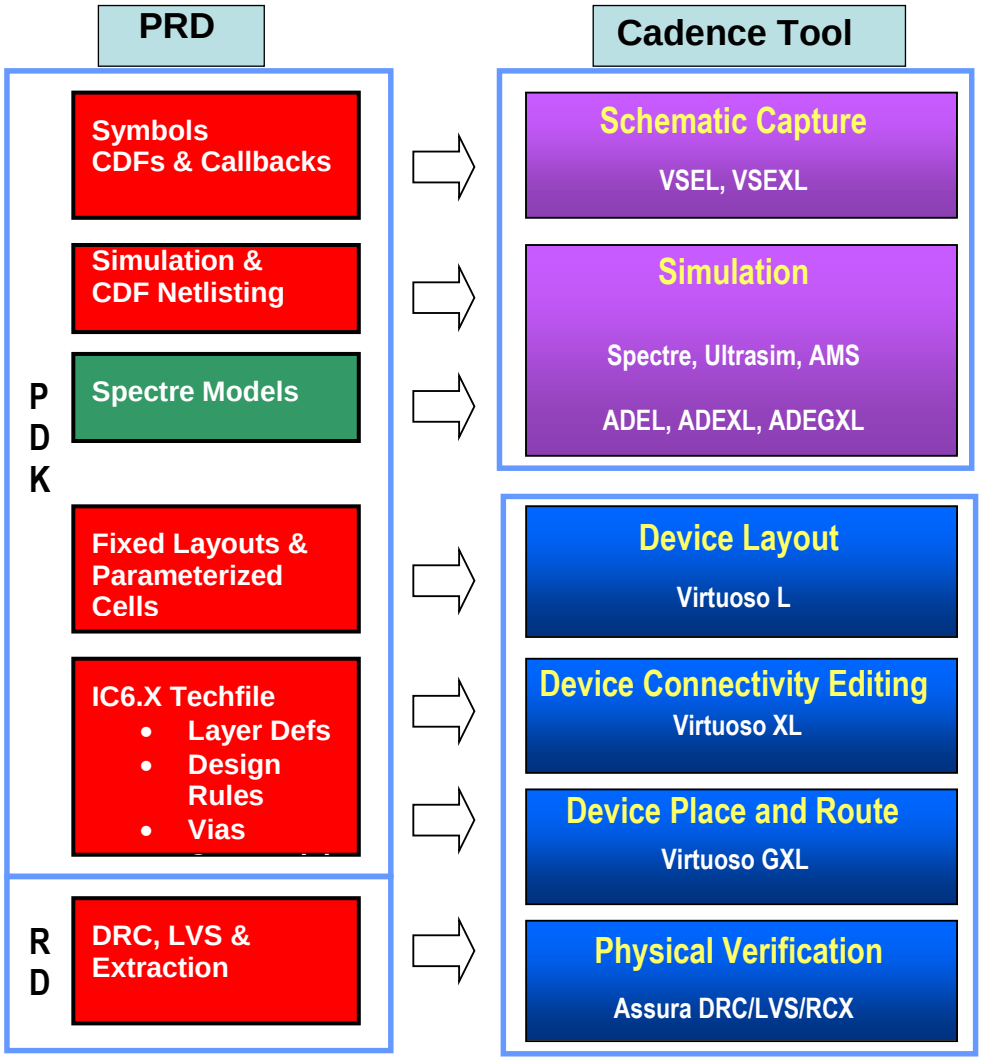
Software Release Stream	Key Products
IC618	Cadence Virtuoso Design Environment, Analog Design and Simulation, Physical Design
IUS81	Cadence AMS Designer, AMS/Ultra
SPECTRE18.1	Cadence Spectre (18.10.072)
ASSURA41	Cadence DRC, LVS
PVS16.12	Cadence DRC, LVS
EXT19.1	Cadence QRC Extraction (L, XL, GXL)
Innovus 16.1	Cadence Innovus

2 Documents

	Documents Used	Revision
Design Rule Document	gpdk045_drc.pdf	5.0
Design Rule Document	gpdk045_drc.pdf	4.0
Design Rule Document	gpdk045_drc.pdf	3.5
Design Rule Document	gpdk045_drc.pdf	3.0
Design Rule Document	gpdk045_drc.pdf	2.0
Design Rule Document	gpdk045_drc.pdf	1.0

3 What makes up a PRD?

A PRD contains the process technology and needed information to do chip-level design in the Cadence IC6.X environment. The diagram shows the relationship between the PRD and the Cadence IC6.X tool suite that it enables.



Process Design Kits (PDK) contains the following:

- Symbols & CDFs & Callbacks
- Simulation & CDFs
- Spectre Models
- Fixed Layouts & Parameterized Cells
- IC6.X Technology File

Rule Decks (RD) contain the following

- DRC Rule Decks
- LVS Rule Decks
- Extraction Files

4 Installation of the PRD

The user who will own and maintain the PRD should logon to the computer.

Choose a disk and directory under which the PRD will be installed. This disk should be exported to all client machines and must be mounted consistently across all client machines.

Connect to the directory where the PRD will be installed:

cd <**PRD_install_directory**>

Extract the PRD from the archive using the following commands:

gzip -dc <path_to_PRD_tar_file>/gpdk045_<version>.tar.gz | tar xf -

The default permissions on the PRD have already been set to allow only the owner to have write, read and execute access. Other users will have only read and execute access.

This PRD requires the following UNIX environmental variables:

"CDS_Netlisting_Mode" to be set to "Analog"

"CDSHOME" to be set to the Cadence DFII installation path

5 PRD Install Directory Structure/Contents

Within the <**PRD_install_directory>** directory there are several directories to organize the information associated with the PRD.

assura_tech.lib - File containing the Cadence Assura PV initialization path

pvtech.lib – File containing the Cadence PVS initialization path

cds.lib - File containing the Cadence library definition file.

docs - Directory containing the Cadence PRD documentation and the Process

gpdk045 – The IC618 version of the PDK library

assura - Directory containing the Physical Verification Rule Decks for Assura

lib.defs - File containing the Cadence library definition file.

models - Directory containing the device spectre models

pvs - containing the Physical Verification Rule Decks for PVS

qrc – contains rcx/qrc data (best, worst and typical) for assura-QRC or PVS-QRC flow

ead – ead related files for EAD set-up.

EAD technology files generated in IC618 ISR5 is in separate package in “gpdk045_ead_v_6_0.tar.gz”. It can be downloaded from support.cadence.com. Please read “README.txt” in “ead” directory for more details.

ict – Inter Connect Files related to each corner (best, worst and typical)

6 Creation of a Design Project

A unique directory should be created for each circuit design project. The following command can be executed in UNIX:

mkdir ~/circuit_design

cd ~/circuit_design

All work by the user should be performed in this circuit design directory.

The user should create a "cds.lib" file. Using any text editor the following entry should be put in the cds.lib file:

INCLUDE <**PRD_install_directory**>/cds.lib

Where "**PRD_install_directory**" is the path to where the GPDK045 PRD was installed.

The following UNIX links are optional but may aid the user in entering certain forms with the Cadence environment. In UNIX the following command can be used:

ln -s <**PRD_install_directory**>/models

Where, again, "**PRD_install_directory**" is the path to where the GPDK045 PRD was installed.

7 Technology File Methodology

The GPDK045 Library techfile will be designated as the **master** techfile. This techfile will contain all required techfile information. An ASCII version of this techfile is shipped with the PRD. This ASCII version represents the techfile currently compiled into the gpdk045 library

The **attach** method should be used for any design library that is created. This allows the design database techfile to be kept in sync with the techfile in the process PRD. To create a new library that uses an attached techfile, use the command *File->New->Library* from either the CIW or library manager and select the *Attach to an existing techfile* option. Select the gpdk045 library when asked for the name of the *Attach To Technology Library*.

Note: This PRD is using 2000uu/dbu for all layout views.

8 Customizing Layer Display Properties

The display.drf file is automatically loaded by the libInit.il file whenever the gpdk045 library is opened.

To auto-loaded your own display.drf file at Cadence start-up time put the display.drf file in the Cadence start-up directory. To manually load the display.drf file (or load a new version), choose *Tools->Display Resources->Merge Files...* from the CIW and enter the location of the display.drf file that you want to use. If the display.drf file is not auto-loaded and you do not manually load it, you will get error messages about missing packets when you try to open a schematic or layout view and you will not be able to see any process specific layers.

A display.drf file for the GPDK045 can be found in the PRD install directory under techFiles directory.

Listed below are the packet, color, lineStyle, and stipplePattern definitions for a metal3 drawing layer. The packet info references predefined color, lineStyle, and stipplePattern definitions. Any of these can be changed to suit an individual user's preferences in the project copy of the display.drf file.

```
drDefinePacket(
;( DisplayName      PacketName          Stipple              LineStyle
       Fill     Outline )
 ( display      m3              dots          solid          green  green )
)

drDefineColor(
;( DisplayName      ColorName          Red          Green          Blue    Blink )
 ( display      green          0          204          102     nil )
)

drDefineLineStyle(
;( DisplayName      LineStyle          Size          Pattern )
 ( display      solid          1          (1 1 1) )
)

drDefineStipple(
;( DisplayName      StippleName          Bitmap )
 ( display      dots                    (
```

(0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0)
(0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
(0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1)
(0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
(0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0)
(0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
(0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1)
(0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
(0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0)
(0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
(0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1)
(0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
(0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0)
(0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)
(0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1)
(0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0)

)

9 Schematic Design

The user should follow the guidelines listed below while building schematics using Composer:

Project libraries should list the primitive PRD library as a reference library in the library properties form.

Users can add instances from the PRD library to designs stored in the project libraries.

When performing hierarchical copy of schematic designs, care should be taken to preserve the references to the PRD libraries. These references should not be copied locally to the project directories and the references set to the local copy of PRD cells. This would prevent your designs from inheriting any fixes done to the PRD library from an upgrade.

Users should exercise caution when querying an instance and changing the name of the cell and replacing it with a reference to another cell. While similar parameters will inherit values, callbacks are not necessarily executed. This would cause dependent parameters to have incorrect values.

Schematics should be designed with schematic driven layout methodology in mind. Partitioning of schematics, hierarchical design, input and output ports, should be done in a clean and consistent fashion.

10 Library Device Setup

10.1 Resistors

The resistors in the library consist of three types; *diffused*, *insulated*, and *metal*. The diffused types include p+ and n+ and come in three-terminal varieties. The insulated resistors are those that are isolated from silicon by an insulator (oxide) such as poly resistors. These resistors are also three-terminal devices. The metal resistors are those resistors that are used as interconnect and feed-throughs; they are 2-terminal devices. Serpentine resistor layouts are not allowed.

Units:

The length and width are specified in meters for schematic simulation. Design variables are supported for both the length and width parameters.

Calculation:

The user has two choices in determining how the final resistor configuration is calculated. The user may request the calculation of either the resistor length or the resistor value. In both cases, the calculated values are determined based upon a combination of the length, width, resistance value, number of resistor segments (series or parallel), and contact resistance.

The width and length are snapped to grid, and the resistances are recalculated and updated on the component form based on actual dimensions.

Simulation:

Subcircuit definitions are used to model the resistors

10.2 Mosfets

All mosfets in the PRD library are 4 terminals.

Units:

Length and width are in meters, with areas and perimeters in meters squared and meters, respectively. Design variables are allowed for specifying parameter values on mosfet devices.

Calculation:

The area and perimeter parameters for the sources and drains are calculated from the width and the number of fingers used. This calculation assumes that the drain will always have the less capacitance (area) when there are an even number of fingers (odd number of diffusion areas). The finger width is calculated by dividing the total width by the number of fingers. Depending upon which value is entered into the form by the user, either the total width or the finger width will be calculated using the aforementioned calculation.

Simulation:

These mosfets are netlisted as their predefined device names for simulation purposes.

10.3 Bipolar Transistors

All BJT's in the PRD library are 3 terminal.

Units:
Only fixed size devices are allowed. Emitter sizes of 2, 5, and 10 are available.

Calculation:

The area is calculated from the emitter size of the device.

Simulation:

These BJTs are netlisted as their predefined device names for simulation purposes.

10.4 Diodes

All diodes in the PRD library are two-terminal.

Units:
Length and width are in meters. Design variables are allowed for Length and Width entries.

Calculation:

The area is calculated from the width and length entered.

Simulation:

These diodes are netlisted as their predefined device names for simulation purposes.

10.5 Capacitor

The metal capacitor is three-terminal. The MOS capacitors are captured as two-terminal devices in schematics, four-terminal MOS in layout.

Units:
Length and width are in meters. Design variables are allowed for Length and Width entries.

Calculation:

The capacitance is calculated from the width and length entered.

Simulation:

These capacitors are netlisted as their predefined device names for simulation purposes.

10.6 Inductor

The inductor is three-terminal. It has symmetric and asymmetric inductors.

Units:

Radius and width are in meters.

Calculation:

The inductance value is computed using radius, width, space (not a variable) and number of turns.

Simulation:

These inductors are netlisted as their predefined device names for simulation purposes.

11 Supported Devices

11.1 Mosfets

- nmos1v - 1.1 volt nominal Vt NMOS transistor
- nmos1v_3 - 1.1 volt nominal Vt NMOS transistor with inherited BULK
- nmos1v_hvt - 1.1 volt high Vt NMOS transistor
- nmos1v_hvt-3 - 1.1 volt high Vt NMOS transistor with inherited BULK
- nmos1v_lvt – 1.1 volt low Vt NMOS transistor
- nmos1v_lvt_3 – 1.1 volt low Vt NMOS transistor with inherited BULK
- nmos1v_nat – 1.1 volt native Vt NMOS transistor
- nmos1v_nat_3 – 1.1 volt native Vt NMOS transistor with inherited BULK
- nmos2v – 1.8 volt nominal Vt NMOS transistor
- nmos2v_3 – 1.8 volt nominal Vt NMOS transistor with inherited BULK
- nmos2v_nat – 1.8 volt native Vt NMOS transistor
- nmos2v_nat_3 – 1.8 volt native Vt NMOS transistor with inherited BULK
- pmos1v – 1.1 volt nominal Vt PMOS transistor
- pmos1v_3 – 1.1 volt nominal Vt PMOS transistor with inherited BULK
- pmos1v_hvt – 1.1 volt high Vt PMOS transistor
- pmos1v_hvt_3 – 1.1 volt high Vt PMOS transistor with inherited BULK
- pmos1v_lvt – 1.1 volt low Vt PMOS transistor
- pmos1v_lvt_3 – 1.1 volt low Vt PMOS transistor with inherited BULK
- pmos2v - 1.8 volt nominal Vt PMOS transistor
- pmos2v_3 - 1.8 volt nominal Vt PMOS transistor with inherited BULK

11.2 Resistors

- resnsndiff - N+ diffused resistor w/o salicide
- resnsndiff_2 - N+ diffused resistor w/o salicide with inherited BULK
- resnspdiff - P+ diffused resistor w/o salicide
- resnspdiff_2 - P+ diffused resistor w/o salicide with inherited BULK
- ressndiff - N+ diffused resistor w/i salicide
- ressndiff_2 - N+ diffused resistor w/i salicide with inherited BULK

- resspdiff - P+ diffused resistor w/i salicide
- resspdiff_2 - P+ diffused resistor w/i salicide with inherited BULK
- resnwsti - N-Well resistor under STI
- resnwsti_2 - N-Well resistor under STI with inherited BULK
- resnwoxide - N-Well resistor under OD
- resnwoxide_2 - N-Well resistor under OD with inherited BULK
- resnsnpoly - N+ Poly resistor w/salicide
- resnsnpoly_2 - N+ Poly resistor w/salicide with inherited BULK
- resnsppoly - P+ Poly resistor w/salicide
- resnsppoly_2 - P+ Poly resistor w/salicide with inherited BULK
- ressnpoly - N+ Poly resistor w/o salicide
- ressnpoly_2 - N+ Poly resistor w/o salicide with inherited BULK
- ressppoly - P+ Poly resistor w/o salicide
- ressppoly_2 - P+ Poly resistor w/o salicide with inherited BULK
- resm<k> - Metal <k> resistor (k=1..11)

11.3 Capacitor

- mimcap – CapMetal (Intermediate Metal 11) to Metal 10 cap
- nmoscap1v – 1.1 volt Nmos cap
- pmoscap1v – 1.1 volt Pmos cap
- nmoscap2v – 1.8 volt Nmos cap
- pmoscap2v – 1.8 volt Pmos cap

11.4 Bipolars

- vpnp2 - Vertical substrate PNP 2x2 Emitter
- vpnp5 - Vertical substrate PNP 5x5 Emitter
- vpnp10 - Vertical substrate PNP 10x10 Emitter
- npn2 - Vertical substrate NPN 2x2 Emitter
- npn5 - Vertical substrate NPN 5x5 Emitter
- npn10 - Vertical substrate NPN 10x10 Emitter

11.5 Diodes

- pdio – 1.1 volt P+/nwell diode
- pdio_hvt – 1.1 volt high Vt P+/nwell diode
- pdio_lvt – 1.1 volt low Vt P+/nwell diode
- pdio_2v – 1.8 volt P+/nwell diode
- ndio – 1.1 volt N+/psub diode
- ndio_hvt – 1.1 volt high Vt N+/psub diode
- ndio_lvt – 1.1 volt low Vt N+/psub diode
- ndio_nvt – 1.1 volt native Vt N+/psub diode
- ndio_2v – 1.8 volt N+/psub diode
- ndio_2v_nvt – 1.8 volt native Vt N+/psub diode

11.6 Inductors

- ind_a – Asymmetric Inductor
- ind_s – Symmetric Inductor

12 Views provided

The following table explains the use of the cellviews provided as part of this PRD:

symbol	Used in Composer schematics
spectre	Simulation / netlisting view for the Spectre & UltraSim simulator
hspiceD	Simulation / netlisting view for the hspiceD simulator
schematic	Simulation / netlisting view for all simulators; Mixed-mode and logic resistors use schematic to call other simulator resistor views. It is used to implement series and parallel features in those resistors.
auLvs	Netlisting view for DIVA and Assura
auCdl	Circuit Descriptive Language netlisting view typically used to generate a netlist for Dracula or third party simulators.
ivpcell	Device recognition symbol used in the extracted layout for netlisting purposes with DIVA and Assura
layout	Fixed cell or pcell used in Virtuoso Layout Editor.

12.1 Mosfets

- Four terminals (D, G, S, B)
- symbol, spectre, hspiceD, auLvs, auCdl, ivpcell, layout (Pcells)

12.2 Resistors

- Three terminals (PLUS, MINUS, B) for diffused and poly resistors
- Two terminals (PLUS, MINUS) for metal resistors
- symbol, schematic, auLvs, auCdl, ivpcell, layout (Pcells)
- Resistors called in schematic views include views for all simulators, symbol, spectre, hspiceD, auLvs, auCdl, ivpcell

12.3 Capacitor

- Two terminals (really four -- S/D/B overlapped) (G, D/S/B) for mos caps
- Three terminals (PLUS, MINUS, B) for metal mimcap capacitor
- symbol, spectre, hspiceD, auLvs, auCdl, ivpcell, layout (Pcells)

12.4 Diodes

- Two terminals (PLUS, MINUS)
- symbol, spectre, hspiceD, auLvs, auCdl, ivpcell, layout (Pcells)

12.5 Bipolars

- Three terminals (C, B, E)
- symbol, spectre, hspiceD, auLvs, auCdl, ivpcell, layout (Pcells)

12.6 Inductors

- Three terminals (PLUS, MINUS, B)
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)

13 CDF parameters

13.1 Mosfets

Model Name - spectre model name (non-editable)

Multiplier - number of Parallel MOS devices

Length (M) - gate length in meters

Total Width (M) - gate width in meters (sum of all fingers)

Finger Width - width of each gate finger/stripe

Fingers - number of poly gate fingers/stripes used in layout

Threshold – finger width at which to apply device folding of the layout

Apply Threshold – button to apply threshold or not

Gate Connection – allow shorting of multi-fingered devices and addition of contact heads to gate ends

S/D Connection – allow shorting of sources and/or drains on multi-finger devices

S/D Metal Width – width of metal used to short sources/drains

Switch S/D – source is defined as left-most diffusion region and alternating regions to the right. Pins are not automatically permuted and can be switched using this parameter

Diff Cont – To switch on/off diffusion contact

Bodytie Type – None, Detached, or Integrated (butting source)

- For Detached, user may select Left, Right, Top, and/or Bottom to specify the located of bodyties. Selection of all four creates a guardring
- For Detached, the user may specify Tap Extension (in microns) which sets the distance from the bodytie to the device. Maximum distance is 100 microns
- For Integrated, the user may select Left or Right for a device with an odd number of fingers (1, 3, 5, …). The user may select Left and Right for an even fingered device

Edit Area & Perim – allow Drain/Soure area and periphery be entered manually for simulation

Drain diffusion area, etc. – several simulation parameters are presented. The area and perimeter parameters are calculated and netlisted in accordance with the layouts or can be entered manually if “Edit Area & Perim” is checked

13.2 Resistors

Model Name – Spectre model name (non-editable)

Segments – number of series or parallel segments for a resistor

Segment Connection – cyclic field used for series or parallel segments

Calculated Parameter – radio button that determines whether resistance or Length is the calculated value when instantiating a new resistor device

Resistance – total resistance value equal to the sum of body resistance, contact resistance, end resistance, and grain resistance

Segment Width – resistor segment width in meters

Segment Length – resistor segment length in meters

Effective Width – effective resistor segment width in meters

Effective Length – effective resistor segment length in meters

Left Dummy – boolean value used to place a dummy resistor strip on the left side of the main resistor

Right Dummy – boolean value used to place a dummy resistor strip on the right side of the main resistor

Contact Rows – integer number of contact rows

Contact Columns – integer number of contact columns

Show Tap Params – boolean value allowing the user to set the visibility of the resistor tap properties

Left Tap – boolean value used to place a resistor tap on the left side of a device

Right Tap – boolean value used to place a resistor tap on the right side of a device

Top Tap – boolean value used to place a resistor tap on the top side of a device

Bottom Tap – boolean value used to place a resistor tap on the bottom side of a device

Tap Extension – float values to set where the left, right, top, and bottom taps would be to its original placements. This parameter is related to the stretch handle on the taps. The input format should be “left 1.3 right 1.0 top 0.0 bottom 2.0” without the quotes. If neither pair is not present, a zero is assumed

Sheet Resistivity – sheet rho value for body of resistor (non-editable)

End Resistance – resistance value for any salicided area near the contact heads in a non-salicided resistor (non-editable)

Contact Resistance – resistance value for the contact heads of a particular resistor (non-editable)

Grain Resistance – constant resistance value for any salicided area near the contact heads in a non-salicided resistor (non-editable)

Delta Width – resistor width process variation value in meters (non-editable)

Delta Length – resistor length process variation value in meters (non-editable)

Temperature Coefficient 1 – temperature coefficient #1 for resistor (non-editable)

Temperature Coefficient 2 – temperature coefficient #2 for resistor (non-editable)

Differential Temperature – Temperature rise

13.3 MOScaps

Model Name - spectre model name (non-editable)

Multiplier - number of Parallel MOS devices

Calculated Parameter - Calculated parameter cyclic (Capacitance, Length, Width, Length&Width)

Capacitance – total capacitance

Length (M) - gate length in meters

Total Width (M) - gate width in meters (sum of all fingers)

Finger Width - width of each gate finger/stripe

Fingers - number of poly gate fingers/stripes used in layout

Gate Connection – allow shorting of multi-fingered devices and addition of contact heads to gate ends

S/D Connection – allow shorting of sources and/or drains on multi-finger devices

S/D Metal Width – width of metal used to short sources/drains

Switch S/D – source is defined as left-most diffusion region and alternating regions to the right. Pins are not automatically permuted and can be switched using this parameter

Bodytie Type – None, Detached, or Integrated (butting source)

- For Detached, user may select Left, Right, Top, and/or Bottom to specify the located of bodyties. Selection of all four creates a guardring
- For Detached, the user may specify Tap Extension (in microns) which sets the distance from the bodytie to the device. Maximum distance is 100 microns
- For Integrated, the user may select Left or Right for a device with an odd number of fingers (1, 3, 5, …). The user may select Left and Right for an even fingered device

Area capacitance – Capacitance per unit area used in parameter calculations (non-editable)

Fringe capacitance – Fringe Capacitance of perimeter used in parameter calculations (non-editable)

Temp rise from ambient, etc. – several simulation parameters are presented.

13.4 Bipolars

Model name	Model name used in simulation
Device Area	Emitter area in microns squared (non-editable
Emitter width	Emitter width microns (non-editable)
Multiplier	Number of Parallel Bipolar devices
Estimated operating region	Simulation operating region

Diodes

Model name	Model used for simulation name
Calculate Parameter	Choices are 'area' , 'width' or 'length'
Device Area	Calculated junction area in meters squared (non-editable)
Length (M)	Diode length in meters
Width (M)	Diode width in meters
Multiplier	Number of Parallel Diode devices
Periphery of junction	Calculated junction periphery in meters (non-editable)

13.5 Inductors

Model	Model used for simulation name
Inductance (H)	Inductance value in Henry
Inner Radius	Inner Radius of Inductor in meters
Inductor Width	Width of each metal turns in meters.
Inductor Space	Space between each metal turns in meters (non-editable)
Multiplier	Number of Parallel Inductor devices
Number of Turns	Number of metal turns of Inductor in cyclic field.

14 Model Setup

This PRD supports the Cadence Spectre, Ultrasim, and AMS circuit simulators.

The following model sections are defined in the <**PRD_install_directory**>/models/spectre/gpdk045.scs file.

Section
tt
ff
ss
fs
sf
mc

tt – Typical N and P model parameters

ff – Fast N and P model parameters

ss – Slow N and P model parameters

fs – Fast N and slow P model parameters

sf – Slow N and Fast P model parameters

mc – Monte Carlo model parameters

15 Techfile Layers

Cadence will provide a standard display setup, and will not support desired changes to the display. The customer is free to modify the display.drf file used on-site to achieve any desired display.

CDS #	GDS #	GDS type	CDS name	CDS purpose	Description
2	1	0	Oxide	drawing	Oxide
4	24	0	Oxide_thk	drawing	Thick Oxide
6	2	0	Nwell	drawing	Nwell
10	3	0	Poly	drawing	Poly
11	18	0	Nhvt	drawing	N+ high Vt implant
12	4	0	Nimp	drawing	N+ implant
13	23	0	Phvt	drawing	P+ high Vt implant
14	5	0	Pimp	drawing	P+ implant
15	52	0	Nzvt	drawing	Native Nmos
16	72	0	SiProt	drawing	Salicide Blocking
18	19	0	Nburied	drawing	N buried
20	6	0	Cont	drawing	Contact
26	26	0	Nlvt	drawing	N+ low Vt implant
27	27	0	Plvt	drawing	P+ low Vt implant
30	7	0	Metal1	drawing	Metal1
32	8	0	Via1	drawing	Via1
34	9	0	Metal2	drawing	Metal2
36	10	0	Via2	drawing	Via2
38	11	0	Metal3	drawing	Metal3
40	30	0	Via3	drawing	Via3
42	31	0	Metal4	drawing	Metal4
44	32	0	Via4	drawing	Via4
46	33	0	Metal5	drawing	Metal5
48	34	0	Via5	drawing	Via5
50	35	0	Metal6	drawing	Metal6
52	37	0	Via6	drawing	Via6
54	38	0	Metal7	drawing	Metal7
56	39	0	Via7	drawing	Via7
58	40	0	Metal8	drawing	Metal8
60	41	0	Via8	drawing	Via8
62	42	0	Metal9	drawing	Metal9
64	151	0	Via9	drawing	Via9
66	152	0	Metal10	drawing	Metal10
68	161	0	Via10	drawing	Via10
70	162	0	Metal11	drawing	Metal11
30	7	1	Metal1	pin	Pin purpose

34	9	1	Metal2	pin	Pin purpose
38	11	1	Metal3	pin	Pin purpose
42	31	1	Metal4	pin	Pin purpose
46	33	1	Metal5	pin	Pin purpose
50	35	1	Metal6	pin	Pin purpose
54	38	1	Metal7	pin	Pin purpose
58	40	1	Metal8	pin	Pin purpose
62	42	1	Metal9	pin	Pin purpose
66	152	1	Metal10	pin	Pin purpose
70	162	1	Metal11	pin	Pin purpose
30	7	3	Metal1	label	Label purpose
34	9	3	Metal2	label	Label purpose
38	11	3	Metal3	label	Label purpose
42	31	3	Metal4	label	Label purpose
46	33	3	Metal5	label	Label purpose
50	35	3	Metal6	label	Label purpose
54	38	3	Metal7	label	Label purpose
58	40	3	Metal8	label	Label purpose
62	42	3	Metal9	label	Label purpose
66	152	3	Metal10	label	Label purpose
70	162	3	Metal11	label	Label purpose
30	7	5	Metal1	fill	Fill purpose
34	9	5	Metal2	fill	Fill purpose
38	11	5	Metal3	fill	Fill purpose
42	31	5	Metal4	fill	Fill purpose
46	33	5	Metal5	fill	Fill purpose
50	35	5	Metal6	fill	Fill purpose
54	38	5	Metal7	fill	Fill purpose
58	40	5	Metal8	fill	Fill purpose
62	42	5	Metal9	fill	Fill purpose
66	152	5	Metal10	fill	Fill purpose
70	162	5	Metal11	fill	Fill purpose
71	7	2	Metal1	slot	Slot purpose
72	9	2	Metal2	slot	Slot purpose
73	11	2	Metal3	slot	Slot purpose
74	31	2	Metal4	slot	Slot purpose
75	33	2	Metal5	slot	Slot purpose
76	35	2	Metal6	slot	Slot purpose
77	38	2	Metal7	slot	Slot purpose
78	40	2	Metal8	slot	Slot purpose
79	42	2	Metal9	slot	Slot purpose
66	152	2	Metal10	slot	Slot purpose
70	162	2	Metal11	slot	Slot purpose
80	25	0	Psub	drawing	P substrate
82	22	0	DIOdummy	drawing	Recognition layer for diodes
84	21	0	PNPdummy	drawing	Recognition layer for pnp

85	85	0	PWdummy	drawing	Recognition layer for substrate
86	20	0	NPNdummy	drawing	Recognition layer for npn
87	60	0	VPNP2dum	drawing	Recognition layer for vpnp2x2
88	17	0	IND2dummy	drawing	Recognition layer for inductor
89	61	0	VPNP5dum	drawing	Recognition layer for vpnp5x5
90	16	0	INDdummy	drawing	Recognition layer for inductor
91	62	0	VPNP10dum	drawing	Recognition layer for vpnp10x10
92	15	0	BJTdum	drawing	Recognition layer for vpnp's
93	84	0	Cap3dum	drawing	Recognition layer for moscap
94	13	0	Resdum	drawing	Recognition layer for resistor
95	36	0	Bondpad	drawing	Recognition layer for bondpad
96	12	0	Capdum	drawing	Recognition layer for moscap
97	14	0	CapMetal	drawing	Recognition layer for moscap
98	71	0	ResWdum	drawing	Recognition layer for resistor
99	75	0	M1Resdum	drawing	Recognition layer for metal res1
100	76	0	M2Resdum	drawing	Recognition layer for metal res2
101	77	0	M3Resdum	drawing	Recognition layer for metal res3
102	78	0	M4Resdum	drawing	Recognition layer for metal res4
103	79	0	M5Resdum	drawing	Recognition layer for metal res5
104	80	0	M6Resdum	drawing	Recognition layer for metal res6
105	81	0	M7Resdum	drawing	Recognition layer for metal res7
106	82	0	M8Resdum	drawing	Recognition layer for metal res8
107	83	0	M9Resdum	drawing	Recognition layer for metal res9
108	93	0	M10Resdum	drawing	Recognition layer for metal res10
109	103	0	M11Resdum	drawing	Recognition layer for metal res11
114	70	0	IND3dummy	drawing	Recognition layer for inductor
115	74	0	ESDdummy	drawing	Recognition layer for esd

16 Virtuoso L,XL,GXL

The standard Cadence Virtuoso Layout design flow will be implemented. This includes basic connectivity of connection layers, wells, and substrate, and symbolic contacts. The M factor will be used for device instance multiplier - there will be no conflict with the parameter used in cell operation. Names will be displayed on the layout views to aid in schematic-layout instance correlation. Auto-abutment of MOSFET devices is supported. Pin permuting of MOSFET and Resistor device is also supported. The skill pcell layouts are compiled into the PRD.

The users should follow the guidelines listed below for layout design:

The Virtuoso Layout tool requires a separate license for operation.

Users obtain maximum leverage from the PRD by doing schematic driven layout in the Virtuoso Layout environment. This flow will produce a correct by design layout. The Virtuoso Custom Router (VCR) and Virtuoso Shape Based Router (VSR) can be used to finish the unconnected interconnect in the layout.

The Router rules file for the target process is provided with the PRD.

Abutment is currently supported only for MOS transistors.
Note, abutment will work only on schematic driven layouts.

Schematic Driven Layout is recommended over Netlist Driven Layout.

NOTE: Skill pcell source code is not included in the PRD kit.

17 Diva Decks

These decks can be found in the extracted PRD directory tree located under the ‘gpdk045’ directory.

17.1 Diva Extract

Diva Extract file is for extraction of all devices in PDK.

The file is:

- divaEXT.rul

17.2 Diva LVS

Diva LVS ruldeck is for compare and parameter check.

The file is:

- divaLVS.rul

18 Assura Decks

Cadence has developed the Assura DRC, EXT, and LVS rule files from the documentation provided.

These decks can be found in the extracted PRD directory tree in the directory:

- assura

18.1 Assura DRC

The Assura DRC file includes DRC check as well as antenna and density checks

- assuraDRC.rul

18.2 Assura LVS

The Assura LVS files provided are named

- extract.rul
- compare.rul

19 PVS Decks

Cadence has developed the PVS DRC, Antenna, and LVS rule files from the documentation provided.

These decks can be found in the extracted PRD directory tree in the directory:

- pvs

19.1 pvl DRC

The PVS DRC file includes DRC check as well as density checks

- pvlDRC.rul

19.2 pvlLVS

The PVS LVS files provided is named as

- pvlLVS.rul

19.3 pvlAnt

The PVS antenna files are also located inside pvs directory.

- pvlAnt.rul

19.4 pvl Extraction

The PVS extraction based files are also located inside pvs directory.

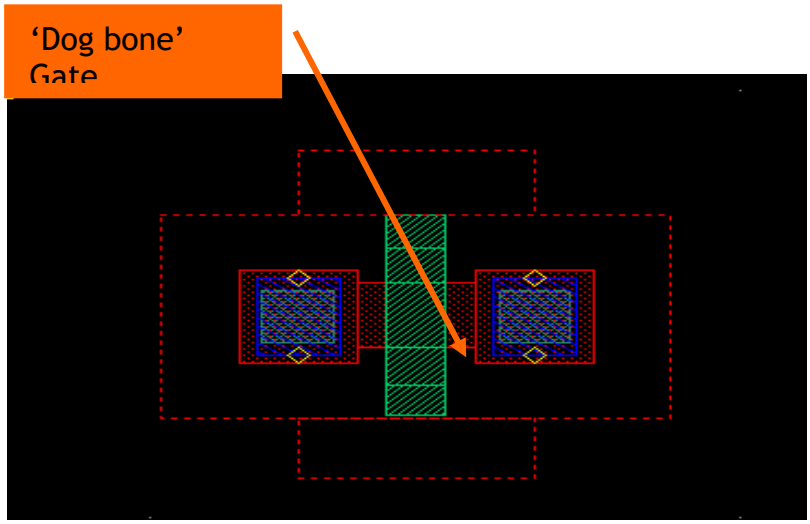
- extview.rul

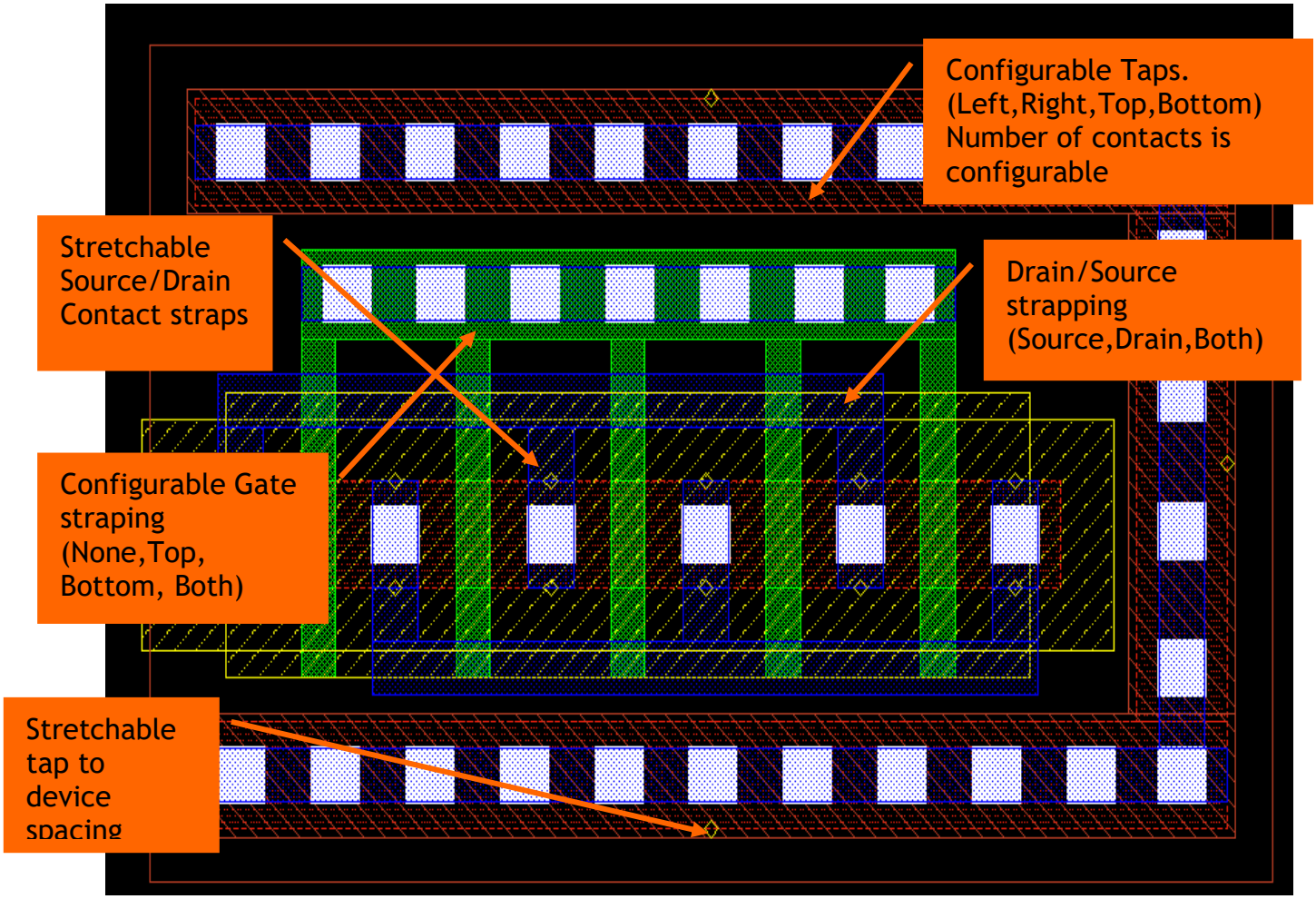
pvtech.lib is available in extracted PRD directory and pvs_control_file is a control file inside “pvs” directory.

20 GPDK045 Pcell Layouts

20.1 Mos Pcell

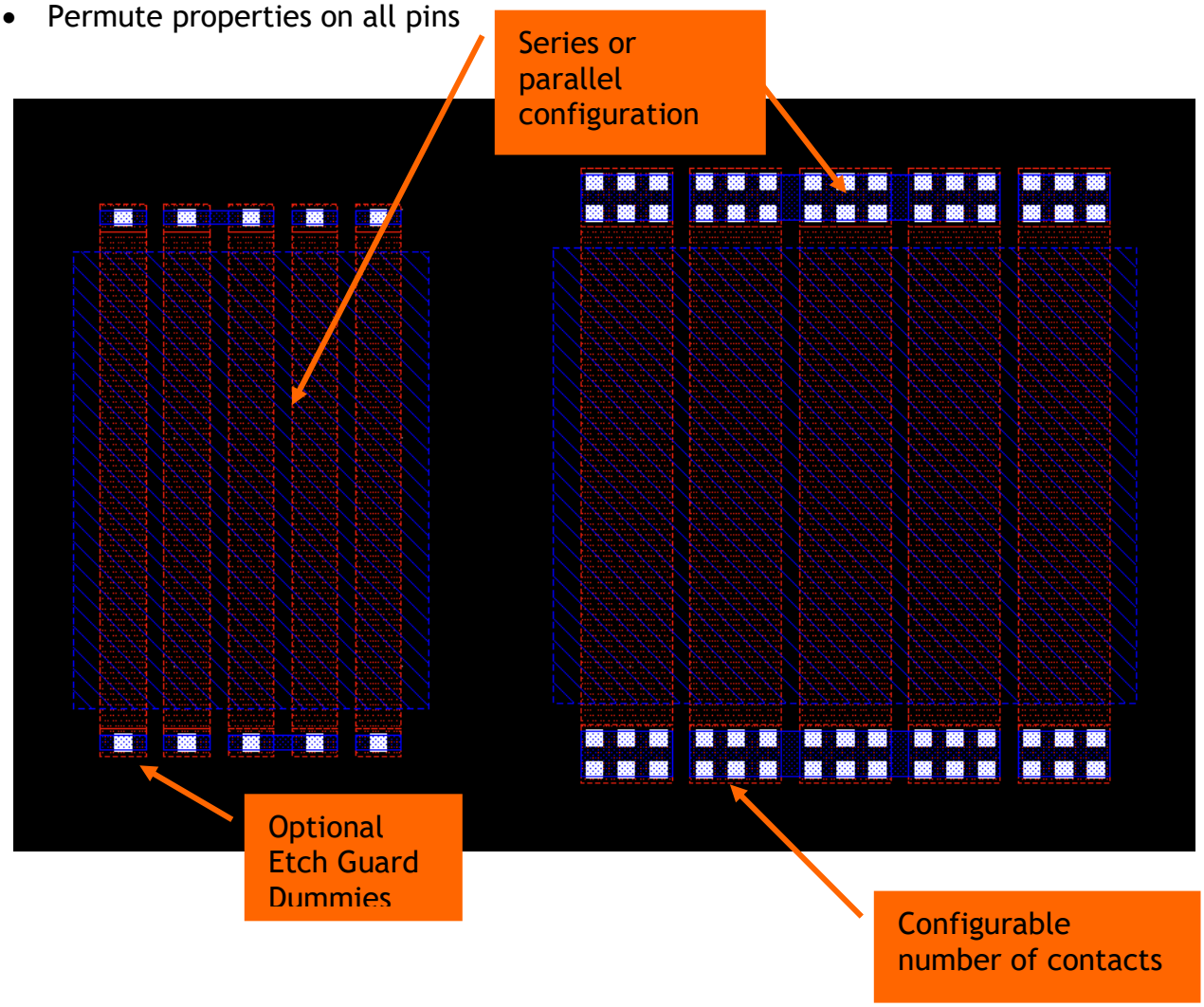
- Multi-fingered gates.
- Dog bone gate
- Configurable source-drain connection for multi fingered devices.(gate,source,both)
- Configurable gate straps for multi fingered devices (top, bottom, both, alternate)
- Variable source/drain contact coverage with stretch handles on each contact strap.
- Optional tap placement for four terminal device. Tab can be configured. (top,bottom,left,right) Spacing between device and tab can be controlled by stretch handle.
- Auto abutment enabled.
- VXL ready connectivity. Pins access direction needs to allow routing with CCAR.
- Permute properties on all pins.




Configurable Taps.
(Left,Right,Top,Bottom)
Number of contacts is
configurable
Stretchable
Source/Drain
Contact straps
Drain/Source
strapping
(Source,Drain,Both)
Configurable Gate
straping
(None,Top,
Bottom, Both)
Stretchable
tap to
device
spacing

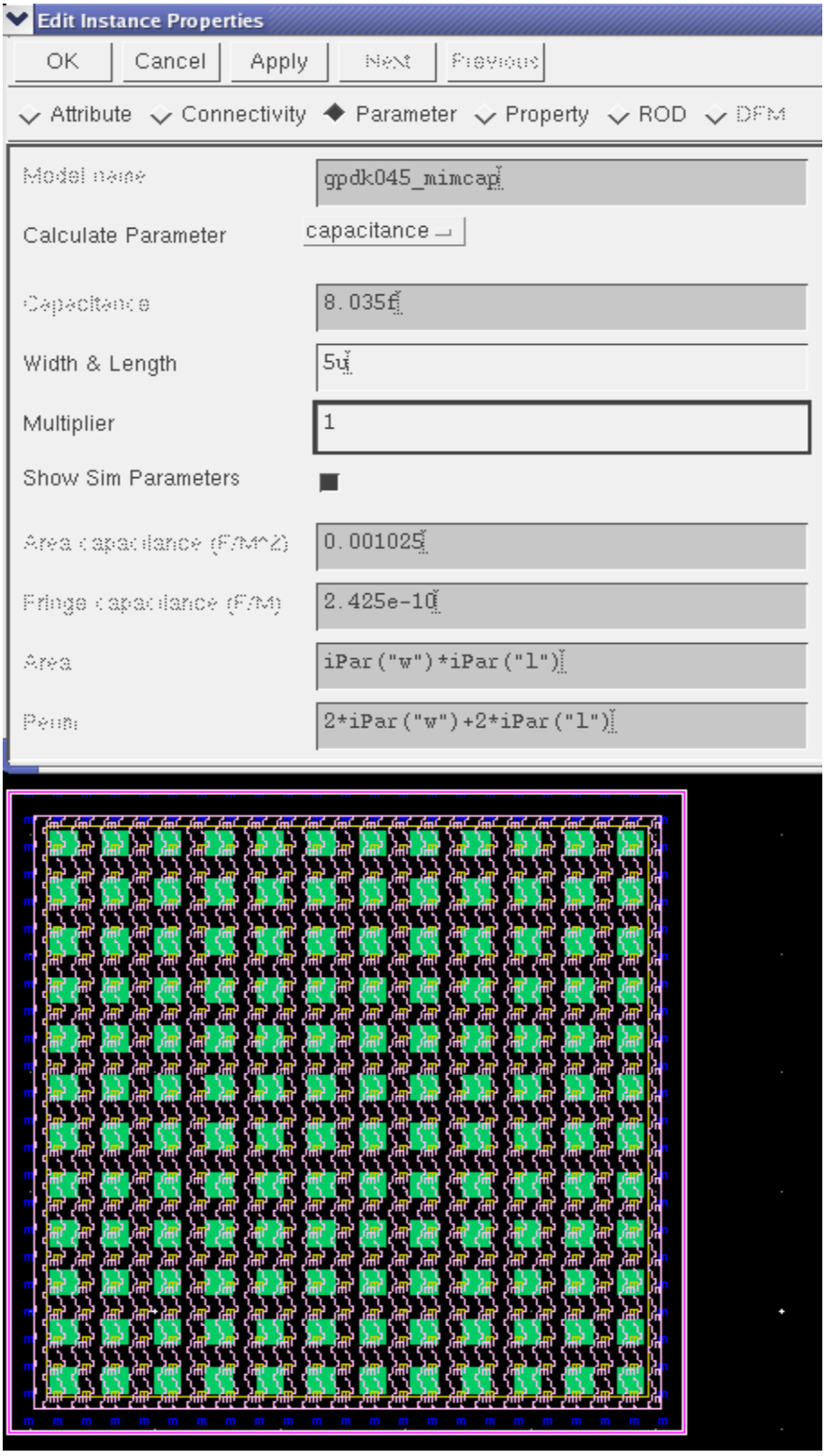
20.2 Resistor Pcell

- Parallel/Series configuration with metal straps.
- Dog bone
- VXL ready connectivity
- Optional etch guard resistors
- Permute properties on all pins



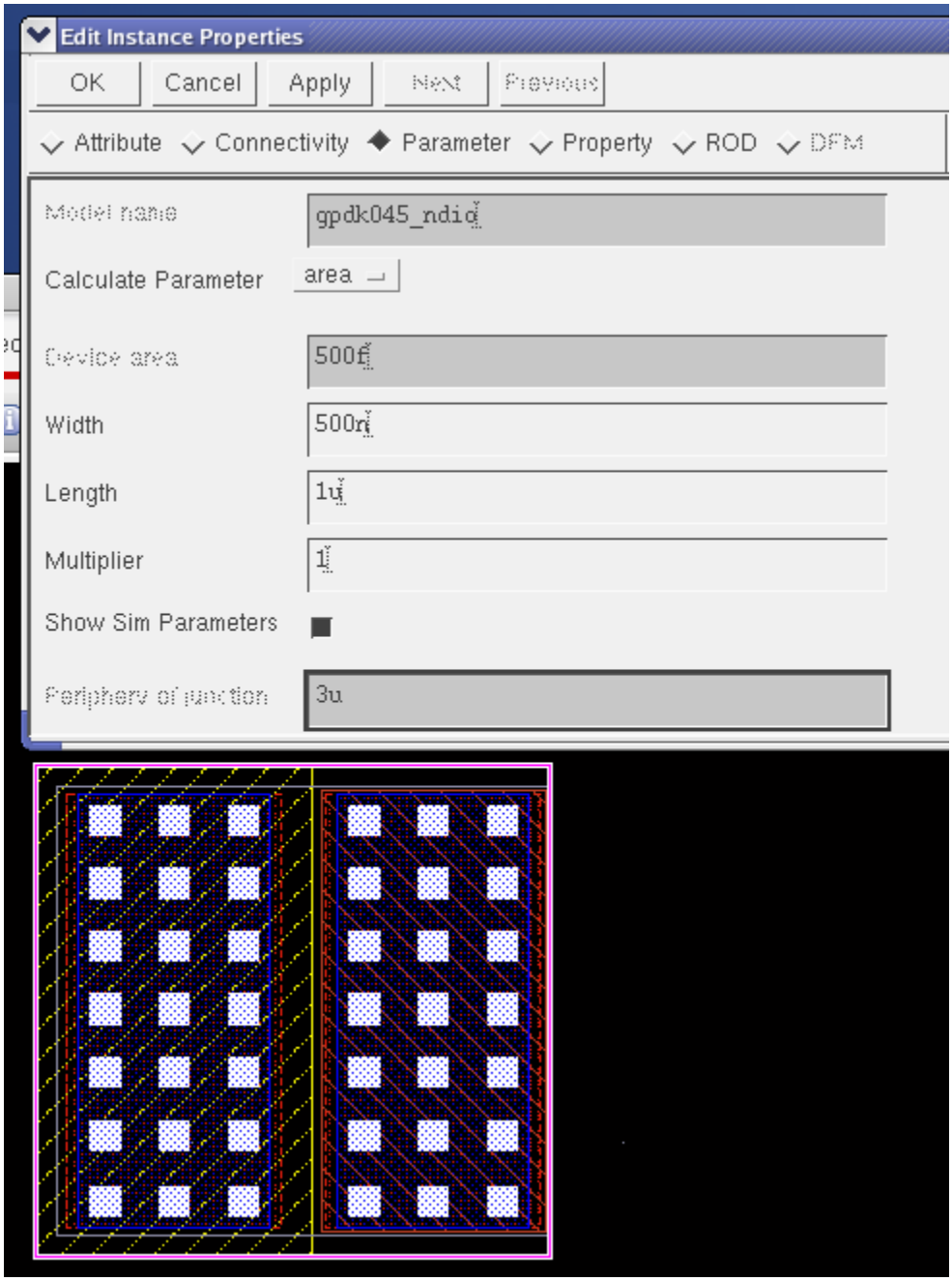
20.3 Capacitor Pcell

- Configurable width, length or capacitance



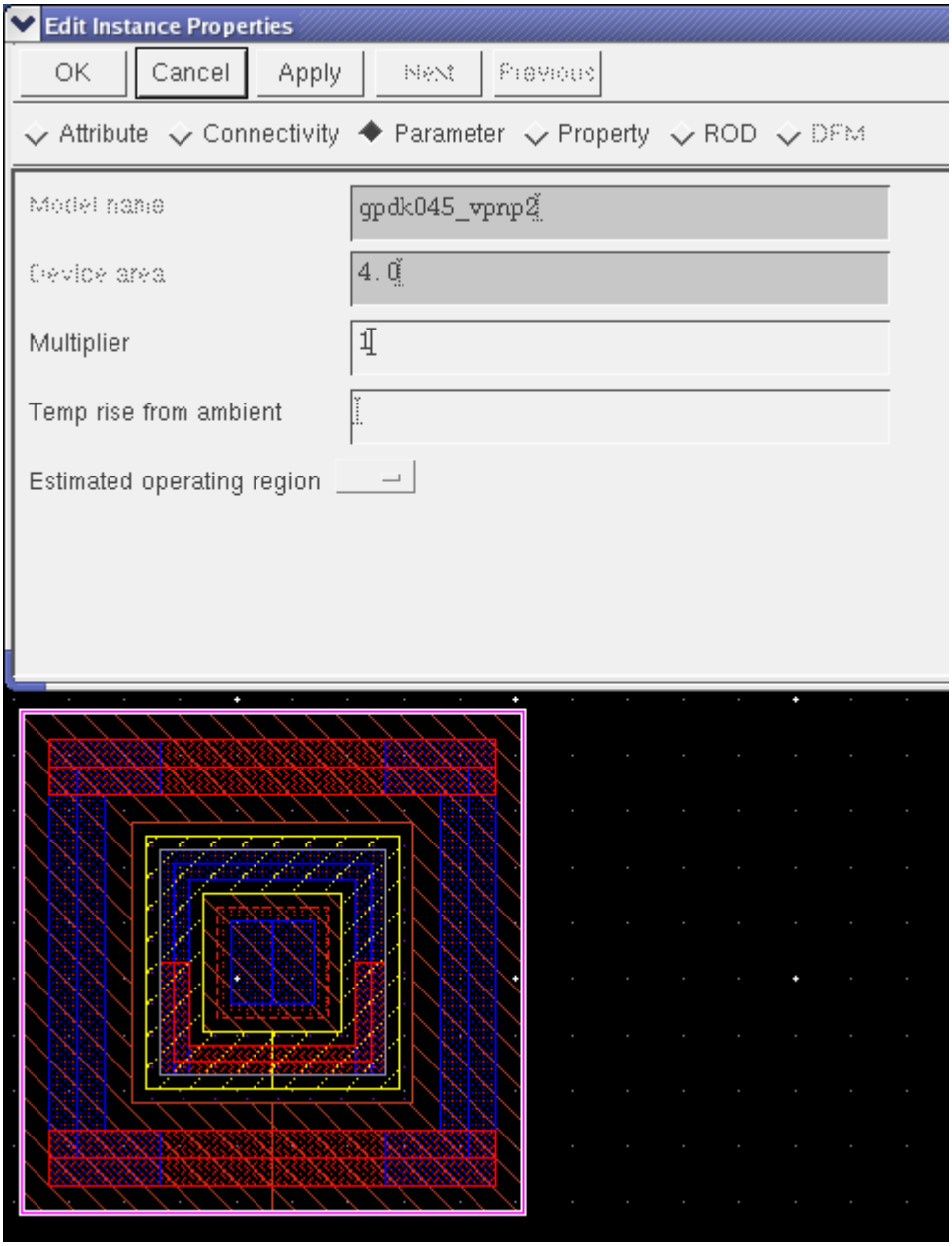
20.4 Diode Pcell

- Configurable width, length or area



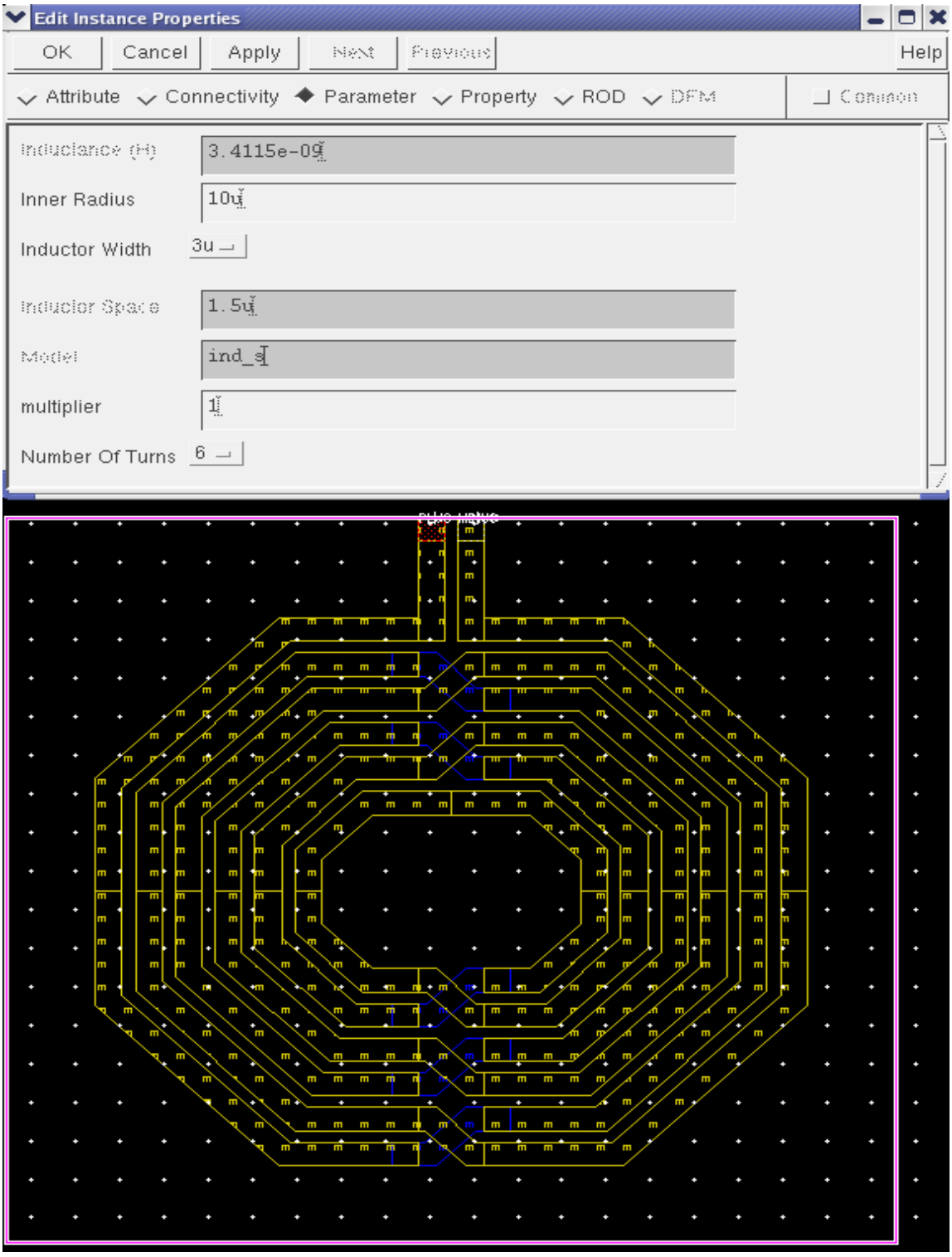
20.5 Bipolar Pcell

- BJT is a fixed layout



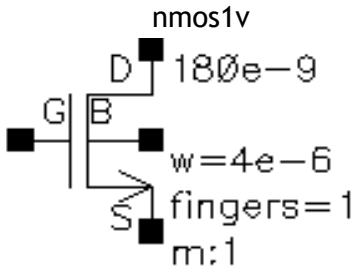
20.6 Inductor Pcell

- Configurable width, turns and radius



21 GPDK045 Device Datasheets

21.1 nmos1v datasheet



Spectre Netlist
Spectre Model Name = "g45n1svt"

```
NM1 (D G S B) g45n1svt w=4u l=180.0n nf=1 as=5.6e-12 ad=5.6e-12  \
              ps=8.28u pd=8.28u m=1 nrs=35m nrd=35m sa=0.14e-9 sb=0.14e-9 sd=0.16e-9
              sca=76.0613 scb=0.0758094 scc=0.00958187
```

DIVA LVS Netlist
DIVA Device Name = "g45n1svt"

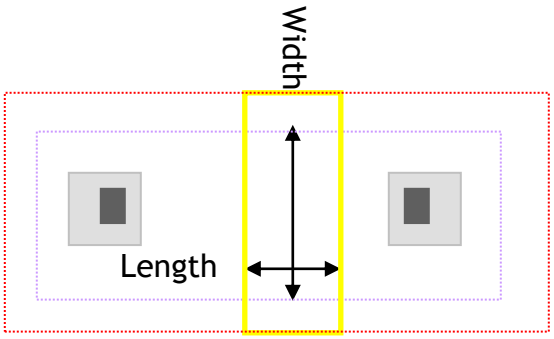
```
; g45n1svt Instance /NM1 = auLvs device M1
d g45n1svt D G S B (p D S)
i 1 g45n1svt D G S B " m 1.0 l 180e-9 w 4e-6 "
```

CDL Netlist
CDL Device Name = "g45n1svt"

```
MNM1 D G S B g45n1svt W=4u L=180.0n M=1.0
```

Assura Netlist
Assura auLvs Device Name = "g45n1svt"

```
c g45n1svt MOS  D B       G B       S B       B B   ;;
* 4 pins
* 4 nets
S (p D S);
i NM1  g45n1svt  D G S B  ;  m 1       l 1.8e-07  w 4e-06  ;
```



nmos1v – 1.2 volt nominal VT NMOS transistor

Device Layers	
Layer	**Color and Fill**
Oxide	
Nimp	
Poly	
Cont	
Metal1	

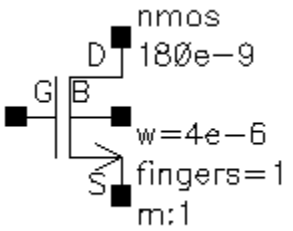
Device Derivation	
Device	**Layer Derivation**
Recognition	**OXIDE AND NIMP CONTAINS POLY**
G	Poly
D	Oxide AND Nimp NOT Poly
S	Oxide AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

- S and D are PERMUTABLE

21.2 nmos1v_hvt datasheet

nmos1v_hvt



Spectre Netlist
Spectre Model Name = "g45n1hvt"

```
NM1 (D G S B) g45n1hvt w=4u l=180.0n nf=1 as=5.6e-12 ad=5.6e-12  \
        ps=8.28u pd=8.28u m=1 nrs=35m nrd=35m sa=0.14e-9 sb=0.14e-9 sd=0.16e-9
        sca=76.0613 scb=0.0758094 scc=0.00958187
```

DIVA LVS Netlist
DIVA Device Name = "g45n1hvt"

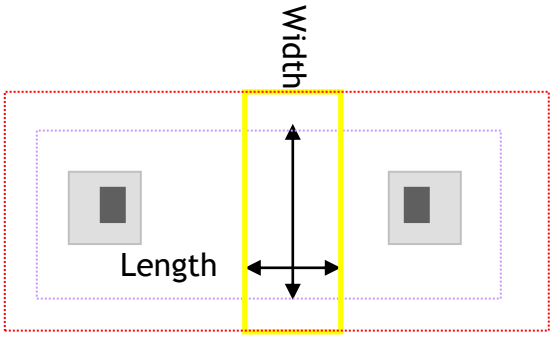
```
; g45n1hvt Instance /NM1 = auLvs device M1
d g45n1hvt D G S B (p D S)
i 1 g45n1hvt D G S B " m 1.0 l 180e-9 w 4e-6 "
```

CDL Netlist
CDL Device Name = "g45n1hvt"

```
MNM1 D G S B g45n1hvt W=4u L=180.0n M=1.0
```

Assura Netlist
Assura auLvs Device Name = "g45n1hvt"

```
c g45n1hvt MOS  D B       G B       S B       B B   ;;
* 4 pins
* 4 nets
S (p D S);
i NM1  g45n1hvt  D G S B  ;  m 1       l 1.8e-07  w 4e-06  ;
```



nmos1v_hvt - 1.2 volt high VT NMOS transistor

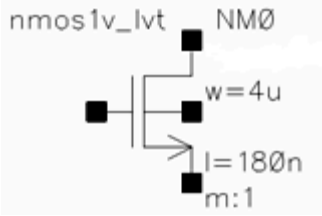
Device Layers	
Layer	**Color and Fill**
Oxide	
Nimp & Nhvt	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**OXIDE AND NIMP AND NHVT CONTAINS POLY**
G	Poly
D	Oxide AND Nimp AND Nhvt NOT Poly
S	Oxide AND Nimp AND Nhvt NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

21.3 nmos1v_lvt datasheet



Spectre Netlist
Spectre Model Name = "g45n1lvt"

```
NM1 (D G S B) g45n1lvt w=4u l=180.0n nf=1 as=5.6e-12 ad=5.6e-12  \
              ps=8.28u pd=8.28u m=1 nrs=35m nrd=35m sa=0.14e-9 sb=0.14e-9 sd=0.16e-9
              sca=76.0613 scb=0.0758094 scc=0.00958187
```

DIVA LVS Netlist
DIVA Device Name = "g45n1lvt"

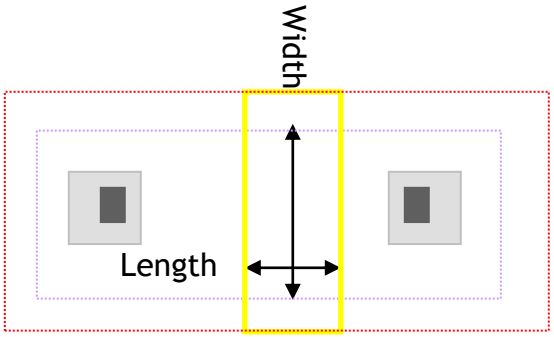
```
; g45n1lvt Instance /NM1 = auLvs device M1
d g45n1lvt D G S B (p D S)
i 1 g45n1lvt D G S B " m 1.0 l 180e-9 w 4e-6 "
```

CDL Netlist
CDL Device Name = "g45n1lvt"

```
MNM1 D G S B g45n1lvt W=4u L=180.0n M=1.0
```

Assura Netlist
Assura auLvs Device Name = "g45n1lvt"

```
c g45n1lvt MOS  D B       G B       S B       B B  ;;
* 4 pins
* 4 nets
S (p D S);
i NM1  g45n1lvt  D G S B  ;  m 1       l 1.8e-07  w 4e-06  ;
```



nmos1v_lvt – 1.2 volt low VT NMOS transistor

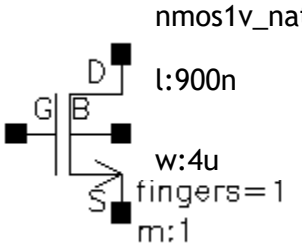
Device Layers	
Layer	**Color and Fill**
Oxide	
Nimp & Nlvt	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**OXIDE AND NIMP AND NHVT CONTAINS POLY**
G	Poly
D	Oxide AND Nimp AND Nlvt NOT Poly
S	Oxide AND Nimp AND Nlvt NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

21.4 nmos1v_nat datasheet



Spectre Netlist
Spectre Model Name = "g45n1nvt"

```
NM1 (D G S B) g45n1nvt w=4u l=180.0n nf=1 as=5.6e-12 ad=5.6e-12  \
        ps=8.28u pd=8.28u m=1 nrs=35m nrd=35m sa=0.14e-9 sb=0.14e-9 sd=0.16e-9
        sca=76.0613 scb=0.0758094 scc=0.00958187
```

DIVA LVS Netlist
DIVA Device Name = "g45n1nvt"

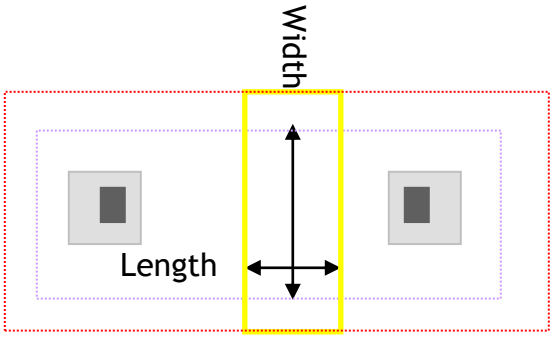
```
; g45n1nvt Instance /NM1 = auLvs device M1
d g45n1nvt D G S B (p D S)
i 1 g45n1nvt D G S B " m 1.0 l 900e-9 w 4e-6 "
```

CDL Netlist
CDL Device Name = "g45n1nvt"

```
MNM1 D G S B g45n1nvt W=4u L=900.0n M=1.0
```

Assura Netlist
Assura auLvs Device Name = "g45n1nvt"

```
c g45n1nvt MOS  D B       G B       S B       B B   ;;
* 4 pins
* 4 nets
S (p D S);
i NM1  g45n1nvt  D G S B  ;  m 1       l 9.0e-07  w 4e-06  ;
```



nmos1v_nat – 1.2 volt native VT MOS transistor

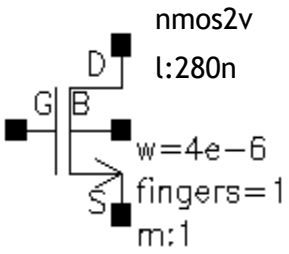
Device Layers	
Layer	**Color and Fill**
Oxide	
Nimp & Nzvt	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**OXIDE AND NIMP AND NZVT CONTAINS POLY**
G	Poly
D	Oxide AND Nimp AND Nzvt NOT Poly
S	Oxide AND Nimp AND NzvtT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

21.5 nmos2v datasheet



Spectre Netlist

Spectre Model Name = “g45n2svt”

```
NM1 (D G S B) g45n2svt w=4u l=280.0n nf=1 as=5.6e-12 ad=5.6e-12  \
              ps=8.28u pd=8.28u m=1 nrs=35m nrd=35m sa=0.14e-9 sb=0.14e-9 sd=0.16e-9
              sca=76.0613 scb=0.0758094 scc=0.00958187
```

DIVA LVS Netlist

DIVA Device Name = “g45n2svt”

```
; g45n2svt Instance /NM1 = auLvs device M1
d g45n2svt D G S B (p D S)
i 1 g45n2svt D G S B " m 1.0 l 280e-9 w 4e-6 "
```

CDL Netlist

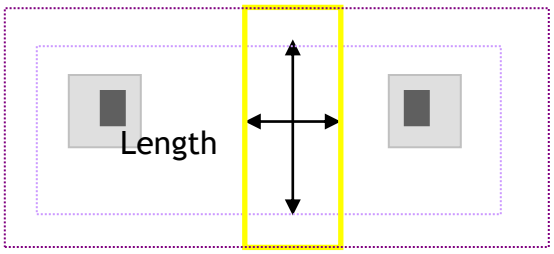
CDL Device Name = “g45n2svt”

```
MNM1 D G S B g45n2svt W=4u L=280.0n M=1.0
```

Assura Netlist

Assura auLvs Device Name = “g45n2svt”

```
c g45n2svt MOS  D B       G B       S B       B B   ;;
* 4 pins
* 4 nets
S (p D S);
i NM1  g45n2svt  D G S B  ;  m 1       l 2.8e-07  w 4e-06  ;
```



nmos2v – 1.8 volt nominal VT NMOS transistor

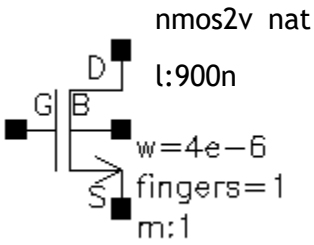
Device Layers	
Layer	**Color and Fill**
Oxide_thk	
Oxide	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**OXIDE_THK AND OXIDE AND NIMP CONTAINS POLY**
G	Poly
D	Oxide_thk AND Oxide AND Nimp NOT Poly
S	Oxide_thk AND Oxide AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

- S and D are PERMUTABLE

21.6 nmos2v_nat datasheet



Spectre Netlist
Spectre Model Name = "g45n2nvt"

```
NM1 (D G S B) g45n2nvt w=4u l=900.0n nf=1 as=6e-12 ad=6e-12  \
        ps=8.3u pd=8.3u m=1 nrs=37.5m nrd=37.5m sa=0.15e-9 sb=0.15e-9 sd=0.18e-9
        sca=76.0613 scb=0.0758094 scc=0.00958187
```

DIVA LVS Netlist
DIVA Device Name = "g45n2nvt"

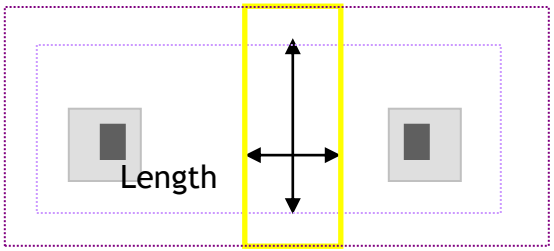
```
; g45n2nvt Instance /NM1 = auLvs device M1
d g45n2nvt D G S B (p D S)
i 1 g45n2nvt D G S B " m 1.0 l 900e-9 w 4e-6 "
```

CDL Netlist
CDL Device Name = "g45n2nvt"

```
MNM1 D G S B g45n2nvt W=4u L=900.0n M=1.0
```

Assura Netlist
Assura auLvs Device Name = "g45n2nvt"

```
c g45n2nvt MOS  D B       G B       S B       B B   ;;
* 4 pins
* 4 nets
S (p D S);
i NM1  g45n2nvt  D G S B  ;  m 1       l 9.0e-07  w 4e-06  ;
```



nmos2v_nat – 1.8 volt Native VT NMOS transistor

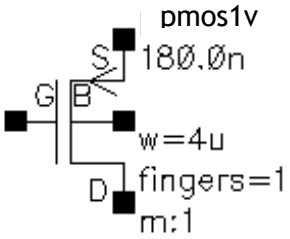
Device Layers	
Layer	**Color and Fill**
Oxide_thk	
Oxide	
Nimp & Nzvt	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**OXIDE_THK AND OXIDE AND NIMP AND NZVT CONTAINS POLY**
G	Poly
D	Oxide_thk AND Oxide AND Nimp AND Nzvt NOT Poly
S	Oxide_thk AND Oxide AND Nimp AND Nzvt NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

- S and D are PERMUTABLE

21.7 pmos1v datasheet



Spectre Netlist
Spectre Model Name = "g45p1svt"

```
PM1 (D G S B) g45p1svt w=4u l=180.0n nf=1 as=5.6e-12 ad=5.6e-12   \
              ps=8.28u pd=8.28u m=1 nrs=35m nrd=35m sa=0.14e-9 sb=0.14e-9 sd=0.16e-9
              sca=152.662 scb=0.0885908 scc=0.0183819
```

DIVA LVS Netlist
DIVA Device Name = "g45p1svt"

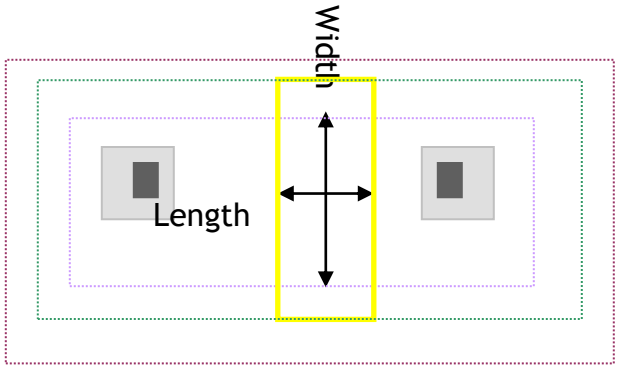
```
; g45p1svt Instance /PM1 = auLvs device M1
d g45p1svt D G S B (p D S)
i 1 g45p1svt D G S B " m 1.0 l 100e-9 w 4e-6 "
```

CDL Netlist
CDL Device Name = "g45p1svt"

```
MPM1 D G S B  g45p1svt  W=4u L=100.0n M=1.0
```

Assura Netlist
Assura auLvs Device Name = "g45p1svt"

```
c g45p1svt MOS  D B       G B       S B       B B   ;;
* 4 pins
* 4 nets
S (p D S);
i MP1  g45p1svt  D G S B  ;  m 1       l 1.0e-07  w 4e-06  ;
```



pmos1v – 1.2 volt nominal VT PMOS transistor

Device Layers	
Layer	**Color and Fill**
Nwell	
Oxide	
Pimp	
Poly	
Cont	
Metal1	

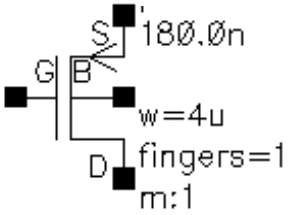
Device Derivation	
Device	**Layer Derivation**
Recognition	**NWELL AND OXIDE AND PIMP CONTAINS POLY**
G	Poly
D	Nwell AND Oxide AND Pimp NOT Poly
S	Nwell AND Oxide AND Pimp NOT Poly
B	Nwell

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

21.8 pmos1v_hvt datasheet

pmos1v_hvt



Spectre Netlist
Spectre Model Name = "g45p1hvt"

```
PM1 (D G S B) g45p1hvt w=4u l=180.0n nf=1 as=5.6e-12 ad=5.6e-12  \
              ps=8.28u pd=8.28u m=1 nrs=35m nrd=35m sa=0.14e-9 sb=0.14e-9 sd=0.16e-9
              sca=152.662 scb=0.0885908 scc=0.0183819
```

DIVA LVS Netlist
DIVA Device Name = "g45p1hvt"

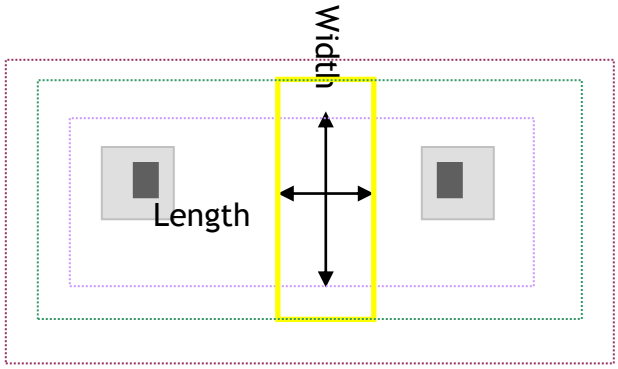
```
; g45p1hvt Instance /PM1 = auLvs device M1
d g45p1hvt D G S B (p D S)
i 1 g45p1hvt D G S B " m 1.0 l 100e-9 w 4e-6 "
```

CDL Netlist
CDL Device Name = "g45p1hvt"

```
MPM1 D G S B  g45p1hvt  W=4u L=100.0n M=1.0
```

Assura Netlist
Assura auLvs Device Name = "g45p1hvt"

```
c g45p1hvt MOS  D B       G B       S B       B B   ;;
* 4 pins
* 4 nets
S (p D S);
i MP1  g45p1hvt  D G S B  ;  m 1       l 1.0e-07  w 4e-06  ;
```



pmos1v_hvt - 1.2 volt high VT PMOS transistor

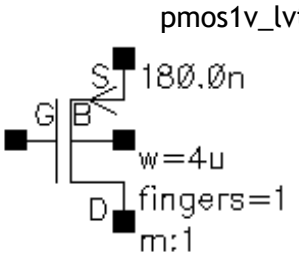
Device Layers	
Layer	**Color and Fill**
Nwell	
Oxide	
Pimp & Phvt	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**NWELL AND OXIDE AND PIMP AND PHVT CONTAINS POLY**
G	Poly
D	Nwell AND Oxide AND Pimp AND Phvt NOT Poly
S	Nwell AND Oxide AND Pimp AND Phvt NOT Poly
B	Nwell

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

- S and D are PERMUTABLE

21.9 pmos1v_lvt datasheet



Spectre Netlist
Spectre Model Name = "g45p1lvt"

```
PM1 (D G S B) g45p1lvt w=4u l=180.0n nf=1 as=5.6e-12 ad=5.6e-12   \
              ps=8.28u pd=8.28u m=1 nrs=35m nrd=35m sa=0.14e-9 sb=0.14e-9 sd=0.16e-9
              sca=152.662 scb=0.0885908 scc=0.0183819
```

DIVA LVS Netlist
DIVA Device Name = "g45p1lvt"

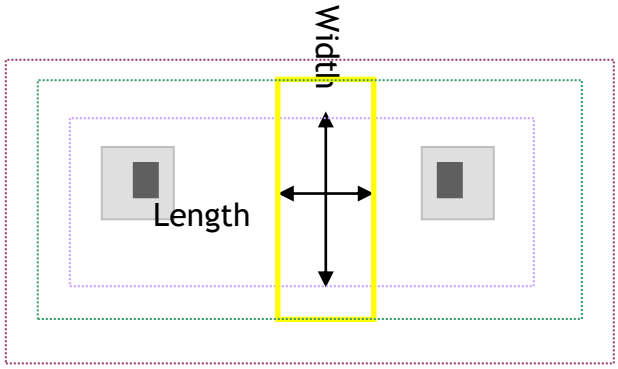
```
; g45p1lvt Instance /PM1 = auLvs device M1
d g45p1lvt D G S B (p D S)
i 1 g45p1lvt D G S B " m 1.0 l 100e-9 w 4e-6 "
```

CDL Netlist
CDL Device Name = "g45p1lvt"

```
MPM1 D G S B  g45p1lvt  W=4u L=100.0n M=1.0
```

Assura Netlist
Assura auLvs Device Name = "g45p1lvt"

```
c g45p1lvt MOS  D B        G B        S B        B B   ;;
* 4 pins
* 4 nets
S (p D S);
i MP1  g45p1lvt  D G S B  ;  m 1        l 1.0e-07  w 4e-06  ;
```



pmos1v_lvt - 1.2 volt low VT PMOS transistor

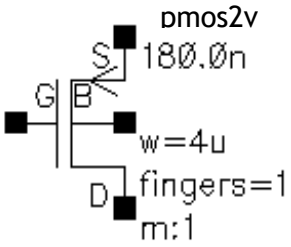
Device Layers	
Layer	**Color and Fill**
Nwell	
Oxide	
Pimp & Plvt	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**NWELL AND OXIDE AND PIMP AND PHVT CONTAINS POLY**
G	Poly
D	Nwell AND Oxide AND Pimp AND Plvt NOT Poly
S	Nwell AND Oxide AND Pimp AND Plvt NOT Poly
B	Nwell

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

- S and D are PERMUTABLE

21.10 pmos2v datasheet



Spectre Netlist
Spectre Model Name = "g45p2svt"

```
PM1 (D G S B) g45p2svt w=4u l=180.0n nf=1 as=5.6e-12 ad=5.6e-12  \
              ps=8.28u pd=8.28u m=1 nrs=35m nrd=35m sa=0.14e-9 sb=0.14e-9 sd=0.16e-9
              sca=152.662 scb=0.0885908 scc=0.0183819
```

DIVA LVS Netlist
DIVA Device Name = "g45p2svt"

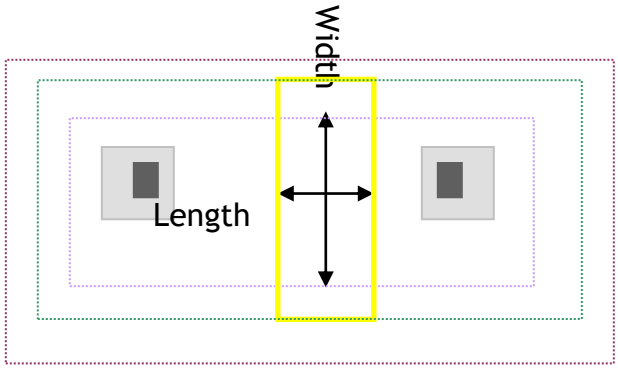
```
; g45p2svt Instance /PM1 = auLvs device M1
d g45p2svt D G S B (p D S)
i 1 g45p2svt D G S B " m 1.0 l 150e-9 w 4e-6 "
```

CDL Netlist
CDL Device Name = "g45p2svt"

```
MPM1 D G S B  g45p2svt  W=4u L=150.0n M=1.0
```

Assura Netlist
Assura auLvs Device Name = "g45p2svt"

```
c g45p2svt MOS  D B       G B       S B       B B   ;;
* 4 pins
* 4 nets
S (p D S);
i MP1  g45p2svt  D G S B  ;  m 1       l 1.5e-07  w 4e-06  ;
```



pmos2v – 1.8 volt nominal VT PMOS transistor

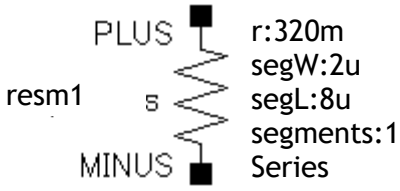
Device Layers	
Layer	**Color and Fill**
Nwell	
Oxide & Oxide_thk	
Pimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**NWELL AND OXIDE AND OXIDE_THK AND PIMP CONTAINS POLY**
G	Poly
D	Nwell AND Oxide AND Oxide_thk AND Pimp NOT Poly
S	Nwell AND Oxide AND Oxide_thk AND Pimp NOT Poly
B	Nwell

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

- S and D are PERMUTABLE

21.11 resm1-resm11 datasheet



Spectre Netlist
Spectre Model Name = "g45rm1"

```
R1 (MINUS PLUS) resm1_pcell1 segL=8u segW=2u dtemp=0
subckt resm1_pcell1 MINUS PLUS
parameters segL=8u segW=2u dtemp=0
  R0 (PLUS MINUS) g45rm1 l=segL w=segW trise=dtemp
ends resm1_pcell1
```

DIVA LVS Netlist
DIVA Device Name = "g45rm1"

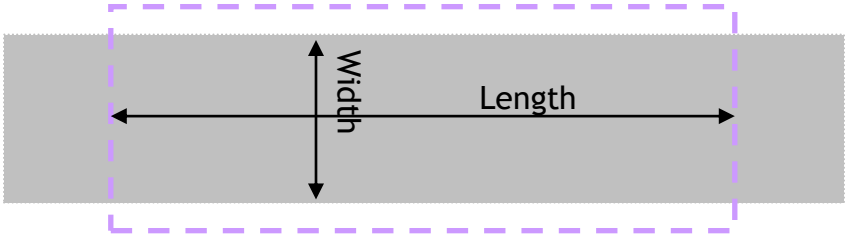
```
; g45rm1 Instance /R1 = auLvs device R1
d g45rm1 PLUS MINUS (p PLUS MINUS)
i 1 g45rm1 PLUS MINUS " r 320e-3 w 2e-6 l 8e-6"
```

CDL Netlist
CDL Device Name = "g45rm1"

```
RR1 PLUS MINUS $[g45rm1] w=2u l=8u
```

Assura Netlist
Assura auLvs Device Name = " g45rm1 "

```
c g45rm1 RES  PLUS B      MINUS B     ;;
* 2 pins
* 2 nets
S (p PLUS MINUS) ;
i R1 g45rm1 PLUS MINUS ;  r 0.32  w 2e-06  l=8e-06;
```



resm1 – Metal resistor

Device Layers	
Layer	**Color and Fill**
M1Resdum (Marker Layer)	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**METAL1 AND M1RESDUM**
PLUS	Metal1 TOUCHING M1Resdum
MINUS	Metal1 TOUCHING M1Resdum

LVS Comparison	
Parameter	**Calculation**
Length	**METAL1 AND M1RESDUM LENGTH (ILLUSTRATED ABOVE)**
Width	Metal1 AND M1Resdum Width (illustrated above)
Resistance	sheet resistance * Length / Width

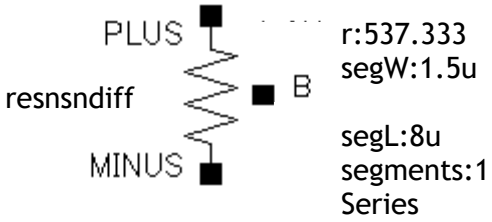
* PLUS and MINUS are PERMUTABLE

* The same format is used for resm2-resm11 as is used with resm1

* Only the metal sheet rho and device name changes

* Only the metal layer and recognition layer changes

21.12 resnsndiff datasheet



Spectre Netlist
Spectre Model Name = "g45rnsnd"

```
R1 (B MINUS PLUS) resnsndiff_pcell1 segL=8u segW=1.5u dtemp=0
subckt resnsndiff_pcell1 B MINUS PLUS
parameters segL=8u segW=1.5u dtemp=0
  R0 (PLUS MINUS B) g45rnsnd l=segL w=segW trise=dtemp
ends resnsndiff_pcell1
```

DIVA LVS Netlist
DIVA Device Name = "g45rnsnd"

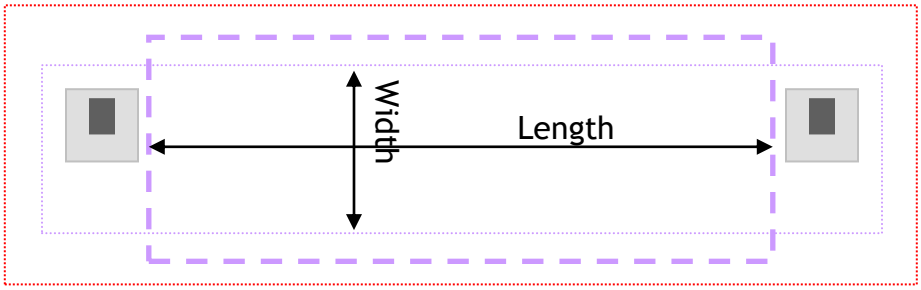
```
; g45rnsnd Instance /R1 = auLvs device R1
d g45rnsnd PLUS MINUS B (p PLUS MINUS)
i 1 g45rnsnd PLUS MINUS B " r 537.333 w 1.5e-6 l 8e-6"
```

CDL Netlist
CDL Device Name = "g45rnsnd"

```
RR1 PLUS MINUS $SUB=B $[g45rnsnd] w=1.5u l=8u
```

Assura Netlist
Assura auLvs Device Name = " g45rnsnd "

```
c g45rnsnd RES  PLUS B      MINUS B    B I  ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 g45rnsnd PLUS MINUS B ;  r 537.333  w 1.5e-06  l=8e-06;
```



resnsndiff - N+ diffused resistor without salicide

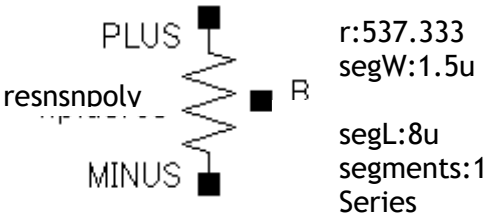
Device Layers	
Layer	**Color and Fill**
Oxide	
Nimp	
SiProt & Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**OXIDE AND NIMP AND SIPROT AND RESDUM**
PLUS	Oxide AND Nimp NOT Resdum
MINUS	Oxide AND Nimp NOT Resdum
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**SIPROT LENGTH (ILLUSTRATED ABOVE)**
Width	Oxide Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

21.13 resnsnpoly datasheet



Spectre Netlist
Spectre Model Name = "g45rnsnp"

R1 (B MINUS PLUS) resnsnpoly_pcell1 segL=8u segW=1.5u dtemp=0

subckt resnsnpoly_pcell1 B MINUS PLUS

parameters segL=8u segW=1.5u dtemp=0

R0 (PLUS MINUS B) g45rnsnp l=segL w=segW trise=dtemp

ends resnsnpoly_pcell1

DIVA LVS Netlist
DIVA Device Name = "g45rnsnp"

; g45rnsnp Instance /R1 = auLvs device R1

d g45rnsnp PLUS MINUS B (p PLUS MINUS)

i 1 g45rnsnp PLUS MINUS B " r 537.333 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = "g45rnsnp"

RR1 PLUS MINUS $SUB=B $[g45rnsnp] w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = " g45rnsnp "

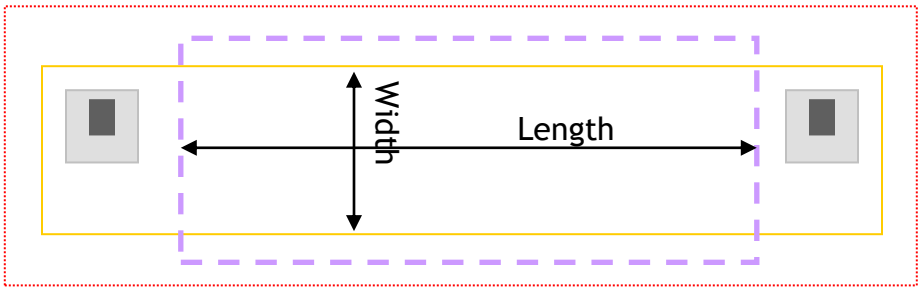
c g45rnsnp RES PLUS B MINUS B B I ;;

* 3 pins

* 3 nets

S (p PLUS MINUS) ;

i R1 g45rnsnp PLUS MINUS B ; r 537.333 w 1.5e-06 l=8e-06;



resnsnpoly - N+ poly resistor without salicide

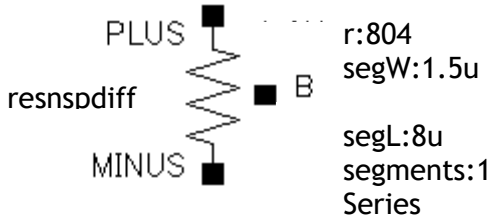
Device Layers	
Layer	**Color and Fill**
Poly	
Nimp	
SiProt & Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**POLY AND NIMP AND SIPROT AND RESDUM**
PLUS	Poly AND Nimp NOT Resdum
MINUS	Poly AND Nimp NOT Resdum

LVS Comparison	
Parameter	**Calculation**
Length	**SIPROT LENGTH (ILLUSTRATED ABOVE)**
Width	Poly Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

21.14 resnspdiff datasheet



Spectre Netlist
Spectre Model Name = "g45rnspd"

```
R1 (B MINUS PLUS) resnspdiff_pcell1 segL=8u segW=1.5u dtemp=0
subckt resnspdiff_pcell1 B MINUS PLUS
parameters segL=8u segW=1.5u dtemp=0
  R0 (PLUS MINUS B) g45rnspd l=segL w=segW trise=dtemp
ends resnspdiff_pcell1
```

DIVA LVS Netlist
DIVA Device Name = "g45rnspd"

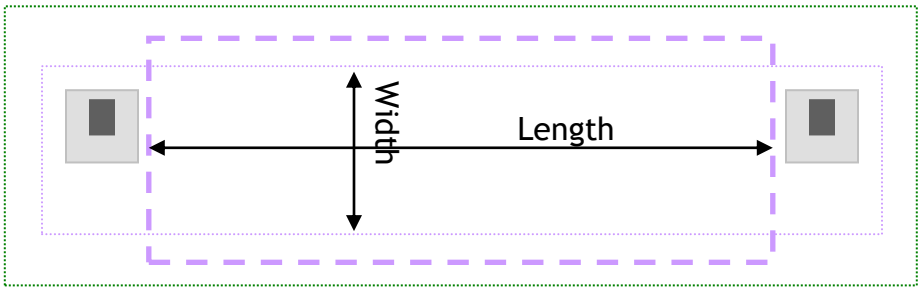
```
; g45rnspd Instance /R1 = auLvs device R1
d g45rnspd PLUS MINUS B (p PLUS MINUS)
i 1 g45rnspd PLUS MINUS B " r 804 w 1.5e-6 l 8e-6"
```

CDL Netlist
CDL Device Name = "g45rnspd"

```
RR1 PLUS MINUS $SUB=B $[g45rnspd] w=1.5u l=8u
```

Assura Netlist
Assura auLvs Device Name = " g45rnspd "

```
c g45rnspd RES  PLUS B      MINUS B    B I  ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 g45rnspd PLUS MINUS B ;  r 804  w 1.5e-06  l=8e-06;
```



resnspdiff - P+ diffused resistor without salicide

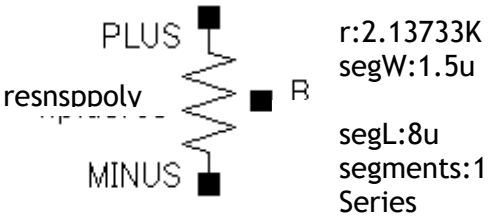
Device Layers	
Layer	**Color and Fill**
Oxide	
Pimp	
SiProt & Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**OXIDE AND PIMP AND SIPROT AND RESDUM**
PLUS	Oxide AND Pimp NOT Resdum
MINUS	Oxide AND Pimp NOT Resdum
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**SIPROT LENGTH (ILLUSTRATED ABOVE)**
Width	Oxide Width (illustrated above)
Resistance	sheet resistance * Length / Width

- PLUS and MINUS are PERMUTABLE

21.15 resnsppoly datasheet



Spectre Netlist
Spectre Model Name = "g45rnspp"

R1 (B MINUS PLUS) resnsppoly_pcell1 segL=8u segW=1.5u dtemp=0

subckt resnsppoly_pcell1 B MINUS PLUS

parameters segL=8u segW=1.5u dtemp=0

R0 (PLUS MINUS B) g45rnspp l=segL w=segW trise=dtemp

ends resnsppoly_pcell1

DIVA LVS Netlist
DIVA Device Name = "g45rnspp"

; g45rnspp Instance /R1 = auLvs device R1

d g45rnspp PLUS MINUS B (p PLUS MINUS)

i 1 g45rnspp PLUS MINUS B " r 2137.33 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = "g45rnspp"

RR1 PLUS MINUS $SUB=B $[g45rnspp] w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = " g45rnspp "

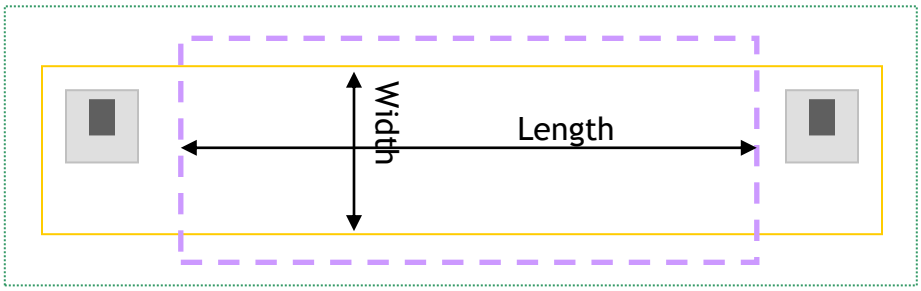
c g45rnspp RES PLUS B MINUS B B I ;;

* 3 pins

* 3 nets

S (p PLUS MINUS) ;

i R1 g45rnspp PLUS MINUS B ; r 2137.33 w 1.5e-06 l=8e-06;



resnsppoly - P+ poly resistor without salicide

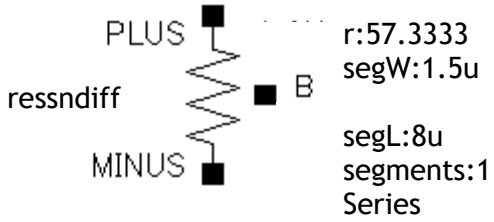
Device Layers	
Layer	**Color and Fill**
Poly	
Pimp	
SiProt & Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**POLY AND PIMP AND SIPROT AND RESDUM**
PLUS	Poly AND Pimp NOT Resdum
MINUS	Poly AND Pimp NOT Resdum

LVS Comparison	
Parameter	**Calculation**
Length	**SIPROT LENGTH (ILLUSTRATED ABOVE)**
Width	Poly Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

21.16 ressndiff datasheet



Spectre Netlist
Spectre Model Name = "g45rsnd"

```
R1 (B MINUS PLUS) ressndiff_pcell1 segL=8u segW=1.5u dtemp=0
subckt ressndiff_pcell1 B MINUS PLUS
parameters segL=8u segW=1.5u dtemp=0
  R0 (PLUS MINUS B) g45rsnd l=segL w=segW trise=dtemp
ends ressndiff_pcell1
```

DIVA LVS Netlist
DIVA Device Name = "g45rsnd"

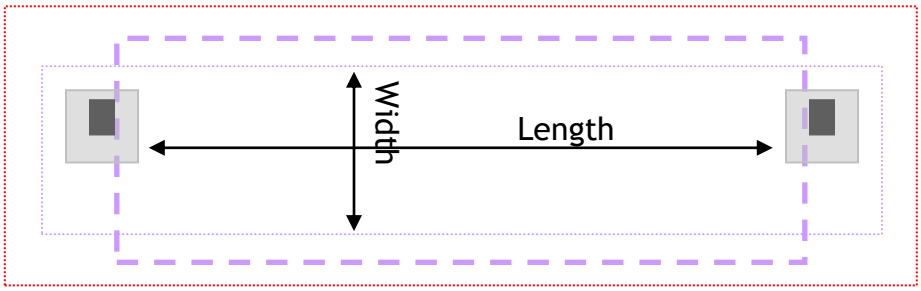
```
; g45rsnd Instance /R1 = auLvs device R1
d g45rsnd PLUS MINUS B (p PLUS MINUS)
i 1 g45rsnd PLUS MINUS B " r 57.3333 w 1.5e-6 l 8e-6"
```

CDL Netlist
CDL Device Name = "g45rsnd"

```
RR1 PLUS MINUS $SUB=B $[g45rsnd] w=1.5u l=8u
```

Assura Netlist
Assura auLvs Device Name = " g45rsnd "

```
c g45rsnd RES  PLUS B      MINUS B    B I  ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 g45rsnd PLUS MINUS B ;  r 57.3333  w 1.5e-06  l=8e-06;
```



ressndiff - N+ diffused resistor with salicide

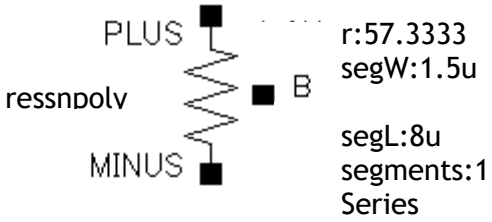
Device Layers	
Layer	**Color and Fill**
Oxide	
Nimp	
Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**OXIDE AND NIMP AND RESDUM NOT SIPROT**
PLUS	Oxide AND Nimp NOT Resdum
MINUS	Oxide AND Nimp NOT Resdum
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**RESDUM LENGTH (ILLUSTRATED ABOVE)**
Width	Oxide Width (illustrated above)
Resistance	sheet resistance * Length / Width

- PLUS and MINUS are PERMUTABLE

21.17 ressnpoly datasheet



Spectre Netlist
Spectre Model Name = "g45rsnp"

```
R1 (B MINUS PLUS) ressnpoly_pcell1 segL=8u segW=1.5u dtemp=0
subckt ressnpoly_pcell1 B MINUS PLUS
parameters segL=8u segW=1.5u dtemp=0
  R0 (PLUS MINUS B) g45rsnp l=segL w=segW trise=dtemp
ends ressnpoly_pcell1
```

DIVA LVS Netlist
DIVA Device Name = "g45rsnp"

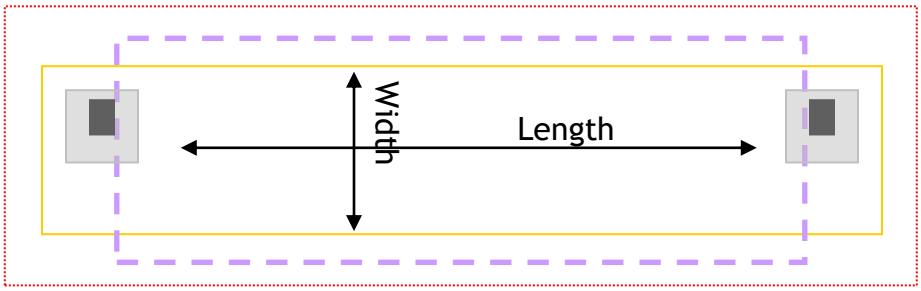
```
; g45rsnp Instance /R1 = auLvs device R1
d g45rsnp PLUS MINUS B (p PLUS MINUS)
i 1 g45rsnp PLUS MINUS B " r 57.3333 w 1.5e-6 l 8e-6"
```

CDL Netlist
CDL Device Name = "g45rsnp"

```
RR1 PLUS MINUS $SUB=B $[g45rsnp] w=1.5u l=8u
```

Assura Netlist
Assura auLvs Device Name = " g45rsnp "

```
c g45rsnp RES  PLUS B      MINUS B    B I  ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 g45rsnp PLUS MINUS B ;  r 57.3333  w 1.5e-06  l=8e-06;
```



ressnpoly – N+ poly resistor with salicide

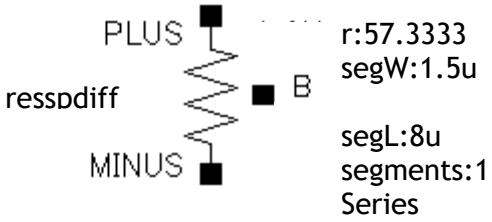
Device Layers	
Layer	**Color and Fill**
Poly	
Nimp	
Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**POLY AND NIMP AND RESDUM NOT SIPROT**
PLUS	Poly AND Nimp NOT Resdum
MINUS	Poly AND Nimp NOT Resdum

LVS Comparison	
Parameter	**Calculation**
Length	**RESDUM LENGTH (ILLUSTRATED ABOVE)**
Width	Poly Width (illustrated above)
Resistance	sheet resistance * Length / Width

- PLUS and MINUS are PERMUTABLE

21.18 resspdiff datasheet



Spectre Netlist
Spectre Model Name = "g45rspd"

R1 (B MINUS PLUS) resspdiff_pcell1 segL=8u segW=1.5u dtemp=0

subckt resspdiff_pcell1 B MINUS PLUS

parameters segL=8u segW=1.5u dtemp=0

R0 (PLUS MINUS B) g45rspd l=segL w=segW trise=dtemp

ends resspdiff_pcell1

DIVA LVS Netlist
DIVA Device Name = "g45rspd"

; g45rspd Instance /R1 = auLvs device R1

d g45rspd PLUS MINUS B (p PLUS MINUS)

i 1 g45rspd PLUS MINUS B " r 57.3333 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = "g45rspd"

RR1 PLUS MINUS $SUB=B $[g45rspd] w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = " g45rspd "

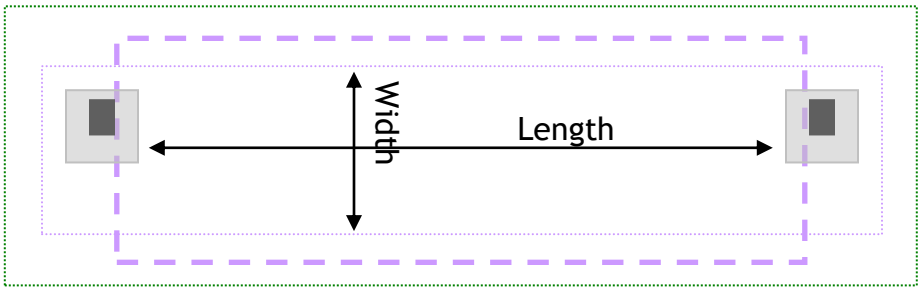
c g45rspd RES PLUS B MINUS B B I ;;

* 3 pins

* 3 nets

S (p PLUS MINUS) ;

i R1 g45rspd PLUS MINUS B ; r 57.3333 w 1.5e-06 l=8e-06;



resspdiff - P+ diffused resistor with salicide

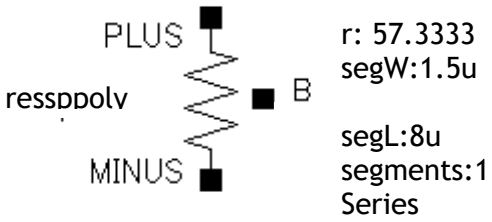
Device Layers	
Layer	**Color and Fill**
Oxide	
Pimp	
Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**OXIDE AND PIMP AND RESDUM NOT SIPROT**
PLUS	Oxide AND Pimp NOT Resdum
MINUS	Oxide AND Pimp NOT Resdum
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**RESDUM LENGTH (ILLUSTRATED ABOVE)**
Width	Oxide Width (illustrated above)
Resistance	sheet resistance * Length / Width

- PLUS and MINUS are PERMUTABLE

21.19 ressppoly datasheet



Spectre Netlist
Spectre Model Name = "g45rspp"

```
R1 (B MINUS PLUS) ressppoly_pcell1 segL=8u segW=1.5u dtemp=0
subckt ressppoly_pcell1 B MINUS PLUS
parameters segL=8u segW=1.5u dtemp=0
  R0 (PLUS MINUS B) g45rspp l=segL w=segW trise=dtemp
ends ressppoly_pcell1
```

DIVA LVS Netlist
DIVA Device Name = "g45rspp"

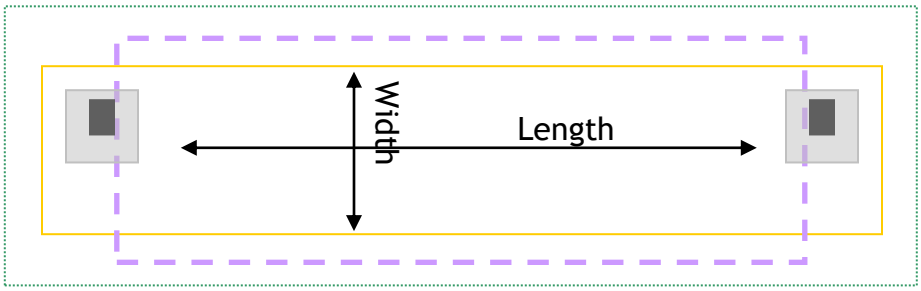
```
; g45rspp Instance /R1 = auLvs device R1
d g45rspp PLUS MINUS B (p PLUS MINUS)
i 1 g45rspp PLUS MINUS B " r 57.3333 w 1.5e-6 l 8e-6"
```

CDL Netlist
CDL Device Name = "g45rspp"

```
RR1 PLUS MINUS $SUB=B $[g45rspp] w=1.5u l=8u
```

Assura Netlist
Assura auLvs Device Name = " g45rspp "

```
c g45rspp RES  PLUS B      MINUS B    B I  ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 g45rspp PLUS MINUS B ;  r 57.3333 w 1.5e-06  l=8e-06;
```



ressppoly – P+ poly resistor with salicide

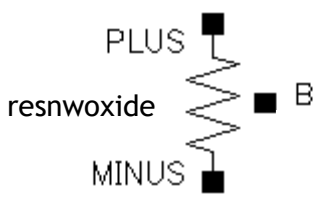
Device Layers	
Layer	**Color and Fill**
Poly	
Pimp	
Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**POLY AND PIMP AND RESDUM NOT SIPROT**
PLUS	Poly AND Pimp NOT Resdum
MINUS	Poly AND Pimp NOT Resdum

LVS Comparison	
Parameter	**Calculation**
Length	**RESDUM LENGTH (ILLUSTRATED ABOVE)**
Width	Poly Width (illustrated above)
Resistance	sheet resistance * Length / Width

- PLUS and MINUS are PERMUTABLE

21.20 resnwoxide datasheet



r:2.14K
segW:1.5u

segL:8u
segments:1
Series

Spectre Netlist
Spectre Model Name = "g45rnwo"

```
R1 (B MINUS PLUS) resnwoxide_pcell1 segL=8u segW=1.5u dtemp=0
subckt resnwoxide_pcell1 B MINUS PLUS
parameters segL=8u segW=1.5u dtemp=0
  R0 (PLUS MINUS B) g45rnwo l=segL w=segW trise=dtemp
ends resnwoxide_pcell1
```

DIVA LVS Netlist
DIVA Device Name = "g45rnwo"

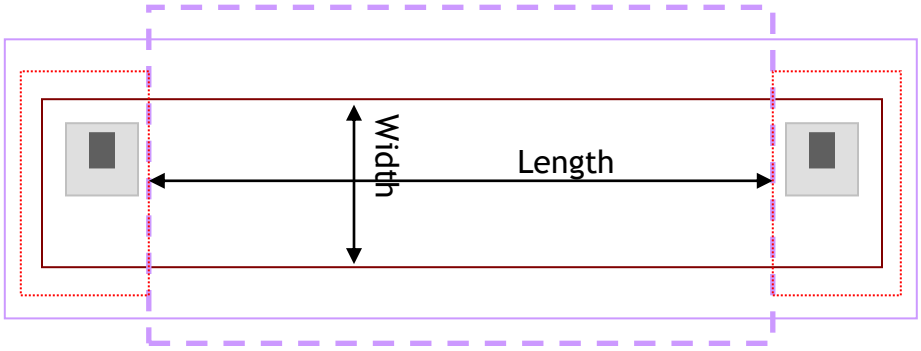
```
; g45rnwo Instance /R1 = auLvs device R1
d g45rnwo PLUS MINUS B (p PLUS MINUS)
i 1 g45rnwo PLUS MINUS B " r 2140 w 1.5e-6 l 8e-6"
```

CDL Netlist
CDL Device Name = "g45rnwo"

```
RR1 PLUS MINUS $SUB=B $[g45rnwo] w=1.5u l=8u
```

Assura Netlist
Assura auLvs Device Name = " g45rnwo "

```
c g45rnwo RES  PLUS B      MINUS B    B I  ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 g45rnwo PLUS MINUS B ;  r 2140  w 1.5e-06  l=8e-06;
```



resnwoxide - Nwell Resistor within diffusion

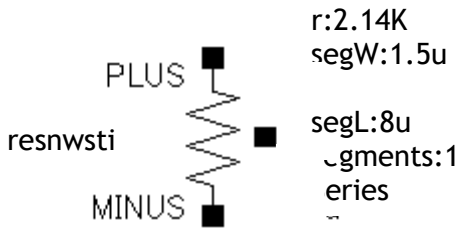
Device Layers	
Layer	**Color and Fill**
Oxide	
Nwell	
Nimp	
ResWdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**OXIDE AND NWELL AND SIPROT AND RESWDUM**
PLUS	Oxide AND Nwell NOT ResWdum
MINUS	Oxide AND Nwell NOT ResWdum
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**RESWDUM LENGTH (ILLUSTRATED ABOVE)**
Width	Nwell Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

21.21 resnwsti datasheet



Spectre Netlist
Spectre Model Name = "g45rnwi"

```
R1 (B MINUS PLUS) resnwsti_pcell1 segL=8u segW=1.5u dtemp=0
subckt resnwsti_pcell1 B MINUS PLUS
parameters segL=8u segW=1.5u dtemp=0
  R0 (PLUS MINUS B) g45rnwi l=segL w=segW trise=dtemp
ends resnwsti_pcell1
```

DIVA LVS Netlist
DIVA Device Name = "g45rnwi"

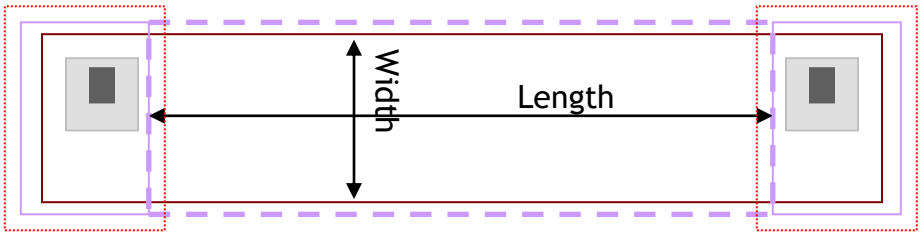
```
; g45rnwi Instance /R1 = auLvs device R1
d g45rnwi PLUS MINUS B (p PLUS MINUS)
i 1 g45rnwi PLUS MINUS B " r 2140 w 1.5e-6 l 8e-6"
```

CDL Netlist
CDL Device Name = "g45rnwi"

```
RR1 PLUS MINUS $SUB=B $[g45rnwi] w=1.5u l=8u
```

Assura Netlist
Assura auLvs Device Name = " g45rnwi "

```
c g45rnwi RES  PLUS B      MINUS B    B I  ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 g45rnwi PLUS MINUS B ;  r 2140  w 1.5e-06  l=8e-06;
```



resnwsti - Nwell Resistor Under STI

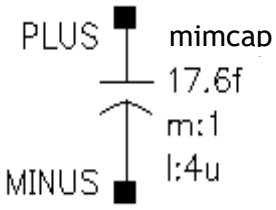
Device Layers	
Layer	**Color and Fill**
Oxide	
Nwell	
Nimp	
ResWdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	NWELL AND RESWDUM
PLUS	Nwell NOT ResWdum
MINUS	Nwell NOT ResWdum
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	RESWDUM LENGTH (ILLUSTRATED ABOVE)
Width	Nwell Width (illustrated above)
Resistance	sheet resistance * Length / Width

- PLUS and MINUS are PERMUTABLE

21.22 mimcap datasheet



Spectre Netlist
Spectre Model Name = “g45cmim”

C1 (PLUS MINUS) g45cmim area=16e-12 perim=16e-6 m=1 trise=0

DIVA LVS Netlist
DIVA Device Name = “g45cmim”

; g45cmim Instance /C1 = auLvs device C1

d g45cmim PLUS MINUS (p PLUS MINUS)

i 1 g45cmim PLUS MINUS " area 16e-12 m 1.0 "

CDL Netlist
CDL Device Name = “g45cmim”

CC1 PLUS MINUS 16e-12 $[g45cmim] m=1

Assura Netlist
Assura auLvs Device Name = “g45cmim”

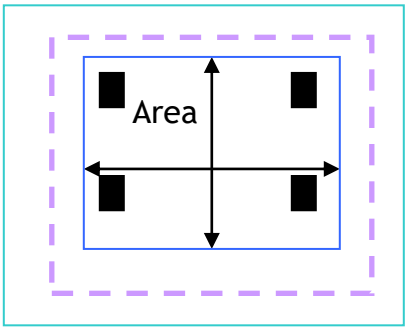
c g45cmim CAP PLUS B MINUS B ;;

* 2 pins

* 2 nets

S (p PLUS MINUS)

i C1 g45cmim PLUS MINUS ; area 16e-12 m 1 ;



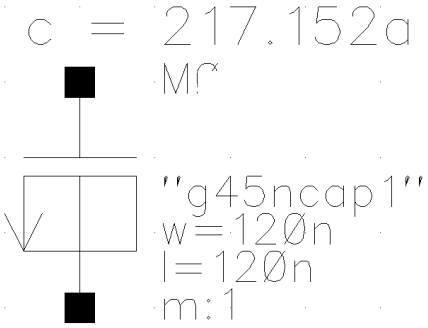
mimcap - Metal / Metal capacitor

Device Layers	
Layer	**Color and Fill**
Metal 2	
CapMetal	
Via2	
Metal3	

Device Derivation	
Device	**Layer Derivation**
Recognition	**CAPMETAL AND METAL2**
PLUS	CapMetal
MINUS	Metal2 UNDER CapMetal

LVS Comparison	
Parameter	**Calculation**
Area	**AREA OF CAPMETAL (ILLUSTRATED ABOVE)**
Perimeter	Perimeter of CapMetal

21.23 nmoscap1v datasheet

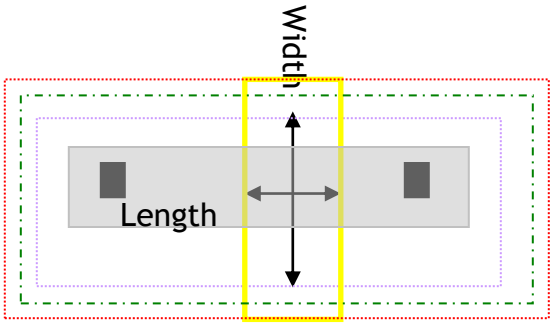


Spectre Netlist
Spectre Model Name = “g45ncap1”
M1 (D G S B) g45ncap1 w=10u l=10u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “g45ncap1”
; g45ncap1 Instance /M1 = auLvs device M1
d g45ncap1 D G S B (p D S)
i 1 g45ncap1 D G S B " m 1.0 l 10e-6 w 10e-6 "

CDL Netlist
CDL Device Name = “g45ncap1”
MM1 D G S B g45ncap1 W=10u L=10u M=1

Assura Netlist
Assura auLvs Device Name = “g45ncap1”
c g45ncap1 MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i M1 g45ncap1 D G S B ; m 1 l 1e-05 w 1e-05 ;



nmoscap1v – 1.2 volt NMOS capacitor

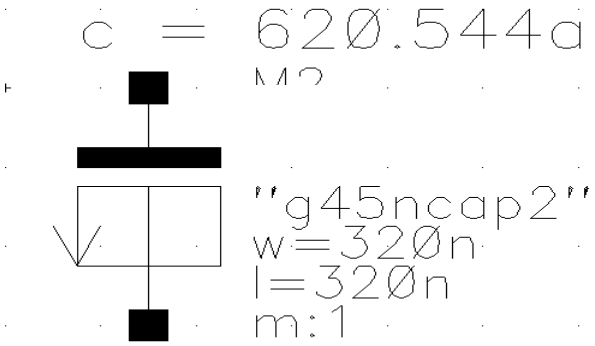
Device Layers	
Layer	**Color and Fill**
Capdum	
Oxide	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**CAPDUM AND OXIDE AND NIMP CONTAINS POLY**
TOP	Poly
BOT	Capdum AND Oxide AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

* Nmos Source, Drain, and Body are Shorted Together

21.24 nmoscap2v datasheet

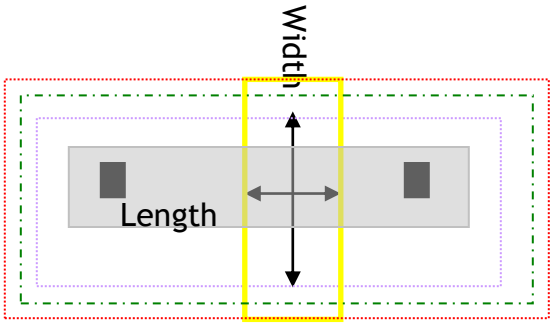


Spectre Netlist
Spectre Model Name = "g45ncap2"
M1 (D G S B) g45ncap2 w=10u l=10u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = "g45ncap2"
; g45ncap2 Instance /M1 = auLvs device M1
d g45ncap2 D G S B (p D S)
i 1 g45ncap2 D G S B " m 1.0 l 10e-6 w 10e-6 "

CDL Netlist
CDL Device Name = "g45ncap2"
MM1 D G S B g45ncap2 W=10u L=10u M=1

Assura Netlist
Assura auLvs Device Name = "g45ncap2"
c g45ncap2 MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i M1 g45ncap2 D G S B ; m 1 l 1e-05 w 1e-05 ;



nmoscap2v – 1.8 volt NMOS capacitor

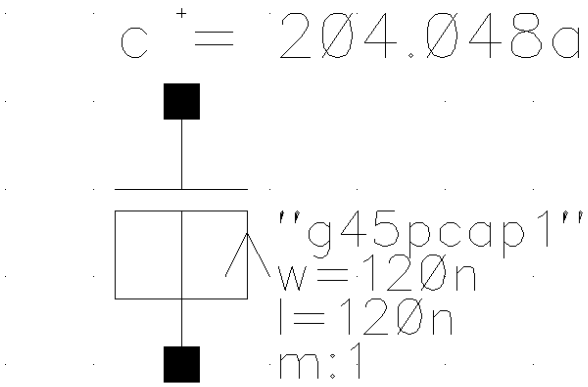
Device Layers	
Layer	**Color and Fill**
Capdum	
Oxide & Oxide_thk	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**CAPDUM AND OXIDE AND OXIDE_THK AND NIMP CONTAINS POLY**
TOP	Poly
BOT	Capdum AND Oxide AND Oxide_thk AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

* Nmos Source, Drain, and Body are Shorted Together

21.25 pmoscap1v datasheet

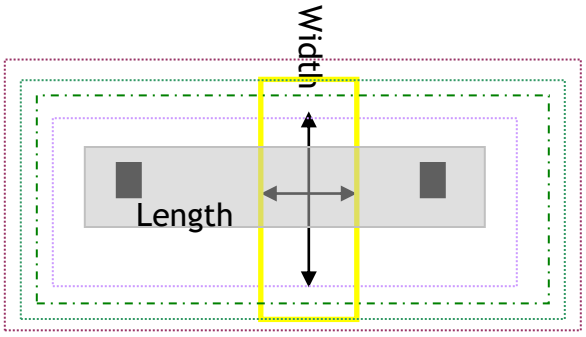


Spectre Netlist
Spectre Model Name = “g45pcap1”
M1 (D G S B) g45pcap1 w=10u l=10u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “g45pcap1”
; g45pcap1 Instance /M1 = auLvs device M1
d g45pcap1 D G S B (p D S)
i 1 g45pcap1 D G S B " m 1.0 l 10e-6 w 10e-6 "

CDL Netlist
CDL Device Name = “g45pcap1”
MM1 D G S B g45pcap1 W=10u L=10u M=1

Assura Netlist
Assura auLvs Device Name = “g45pcap1”
c g45pcap1 MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i M1 g45pcap1 D G S B ; m 1 l 1e-05 w 1e-05 ;



pmoscap1v – 1.2 volt PMOS capacitor

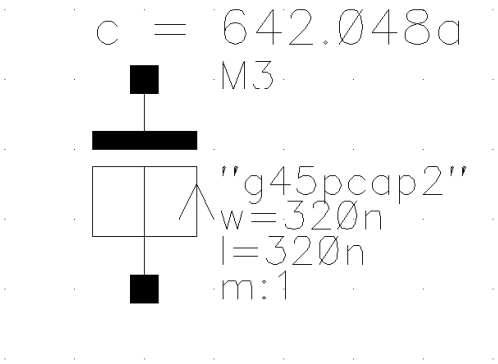
Device Layers	
Layer	**Color and Fill**
Nwell	
Capdum	
Oxide	
Pimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	CAPDUM AND OXIDE AND PIMP AND NWELL CONTAINS POLY
TOP	Poly
BOT	Capdum AND Oxide AND Pimp AND Nwell NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)
Width	Poly inside Oxide (illustrated above)

* Pmos Source, Drain, and Body are Shorted Together

21.26 pmoscap2v datasheet

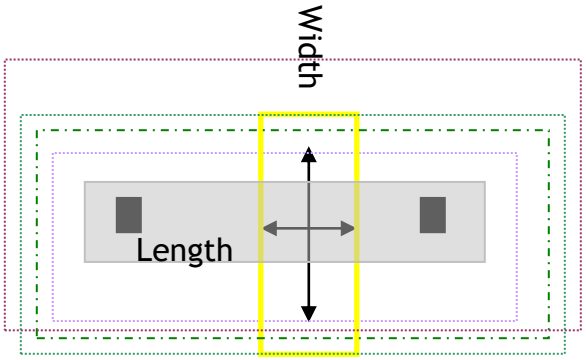


Spectre Netlist
Spectre Model Name = “g45pcap2”
M1 (D G S B) g45pcap2 w=10u l=10u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “g45pcap2”
; g45pcap2 Instance /M1 = auLvs device M1
d g45pcap2 D G S B (p D S)
i 1 g45pcap2 D G S B " m 1.0 l 10e-6 w 10e-6 "

CDL Netlist
CDL Device Name = “g45pcap2”
MM1 D G S B g45pcap2 W=10u L=10u M=1

Assura Netlist
Assura auLvs Device Name = “g45pcap2”
c g45pcap2 MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i M1 g45pcap2 D G S B ; m 1 l 1e-05 w 1e-05 ;



pmoscap2v – 1.8 volt PMOS capacitor

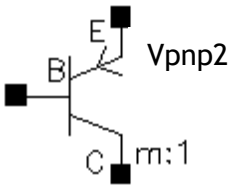
Device Layers	
Layer	**Color and Fill**
Nwell	
Capdum	
Oxide	
Pimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	**CAPDUM AND OXIDE AND PIMP AND NWELL CONTAINS POLY**
TOP	Poly
BOT	Capdum AND Oxide AND Pimp AND Nwell NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	**POLY INTERSECTING OXIDE (ILLUSTRATED ABOVE)**
Width	Poly inside Oxide (illustrated above)

* Pmos Source, Drain, and Body are Shorted Together

21.27 vpnp2 datasheet

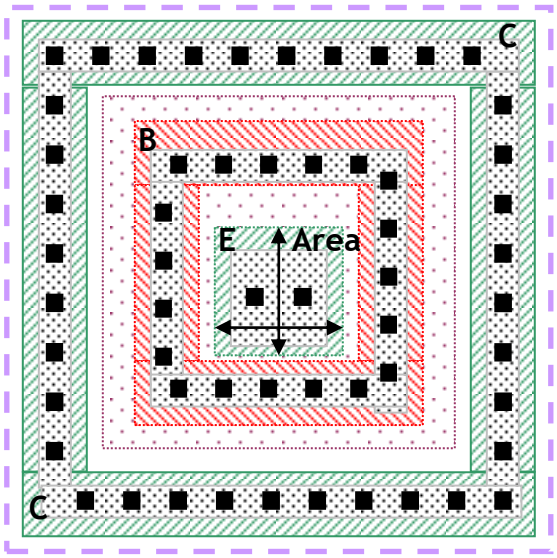


Spectre Netlist
Spectre Model Name = "g45vpnp2"
Q0 (C B E) g45vpnp2 area=4 m=1

DIVA LVS Netlist
DIVA Device Name = "g45vpnp2"
; g45vpnp2 Instance /Q0 = auLvs device Q0
d vpnp C B E
i 0 g45vpnp2 C B E " area 4.0 m 1.0 "

CDL Netlist
CDL Device Name = " g45vpnp2"
QQ0 C B E g45vpnp2 M=1 area=4.0

Assura Netlist
Assura auLvs Device Name = " g45vpnp2"
c g45vpnp2 BJT C B B B E B ;;
* 3 pins
* 3 nets
i Q0 g45vpnp2 C B E; area 4 m 1 ;



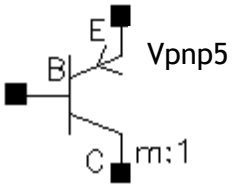
vpnp2 – 1.2 volt vertical substrate PNP with 2x2 fixed emitter

Device Layers	
Layer	**Color and Fill**
BJTdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal3	

Device Derivation	
Device	**Layer Derivation**
Recognition	**BJTDUMMY CONTAINS NIMP AND PIMP**
E	BJTDummy AND Pimp And Oxide AND Nwell
B	BJTDummy AND Nimp And Oxide AND Nwell
C	BJTDummy AND Pimp And Oxide ANDNOT Nwell

LVS Comparison	
Parameter	**Calculation**
Area	**AREA OF EMITTER (ILLUSTRATED ABOVE)**

21.28 vpnp5 datasheet

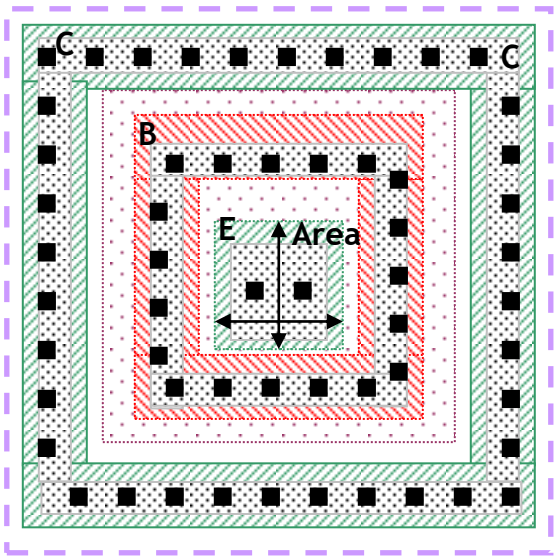


Spectre Netlist
Spectre Model Name = "g45vpnp5"
Q0 (C B E) g45vpnp5 area=25 m=1

DIVA LVS Netlist
DIVA Device Name = "g45vpnp5"
; g45vpnp5 Instance /Q0 = auLvs device Q0
d vpnp C B E
i 0 g45vpnp5 C B E " area 25.0 m 1.0 "

CDL Netlist
CDL Device Name = " g45vpnp5"
QQ0 C B E g45vpnp5 M=1 area=25.0

Assura Netlist
Assura auLvs Device Name = " g45vpnp5"
c g45vpnp5 BJT C B B B E B ;;
* 3 pins
* 3 nets
i Q0 g45vpnp5 C B E; area 25 m 1 ;



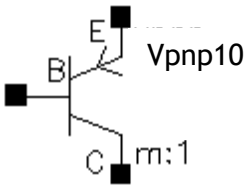
vpnp5 – 1.2 volt vertical substrate PNP with 5x5 fixed emitter

Device Layers	
Layer	**Color and Fill**
BJTdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal3	

Device Derivation	
Device	**Layer Derivation**
Recognition	**BJTDUMMY CONTAINS NIMP AND PIMP**
E	BJTDummy AND Pimp And Oxide AND Nwell
B	BJTDummy AND Nimp And Oxide AND Nwell
C	BJTDummy AND Pimp And Oxide ANDNOT Nwell

LVS Comparison	
Parameter	**Calculation**
Area	**AREA OF EMITTER (ILLUSTRATED ABOVE)**

21.29 vpnp10 datasheet

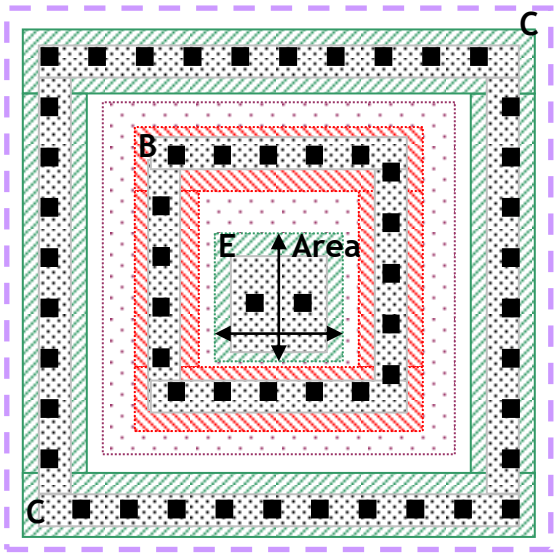


Spectre Netlist
Spectre Model Name = "g45vpnp10"
Q0 (C B E) g45vpnp10 area=100 m=1

DIVA LVS Netlist
DIVA Device Name = "g45vpnp10"
; g45vpnp10 Instance /Q0 = auLvs device Q0
d vpnp C B E
i 0 g45vpnp10 C B E " area 100.0 m 1.0 "

CDL Netlist
CDL Device Name = " g45vpnp10"
QQ0 C B E g45vpnp10 M=1 area=100.0

Assura Netlist
Assura auLvs Device Name = " g45vpnp10"
c g45vpnp10 BJT C B B B E B ;;
* 3 pins
* 3 nets
i Q0 g45vpnp10 C B E; area 100 m 1 ;



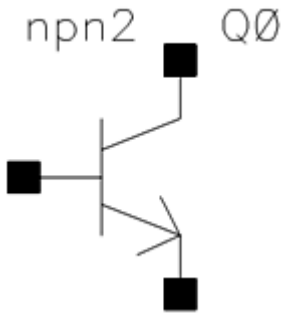
vpnp10 - 1.2 volt vertical substrate PNP with 10x10 fixed emitter

Device Layers	
Layer	**Color and Fill**
BJTdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal3	

Device Derivation	
Device	**Layer Derivation**
Recognition	**BJTDUMMY CONTAINS NIMP AND PIMP**
E	BJTDummy AND Pimp And Oxide AND Nwell
B	BJTDummy AND Nimp And Oxide AND Nwell
C	BJTDummy AND Pimp And Oxide ANDNOT Nwell

LVS Comparison	
Parameter	**Calculation**
Area	**AREA OF EMITTER (ILLUSTRATED ABOVE)**

21.30 npn2 datasheet

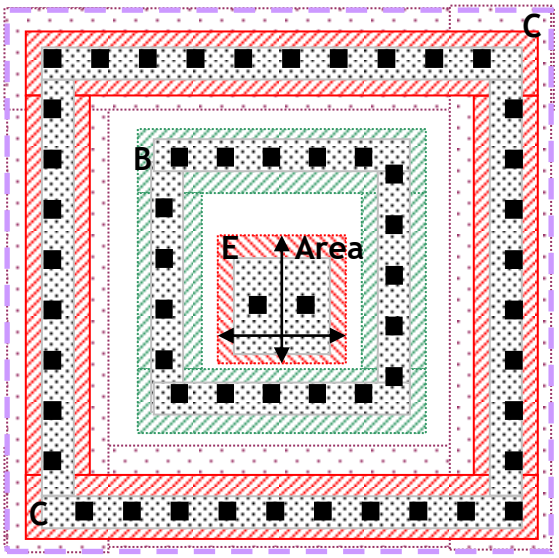


Spectre Netlist
Spectre Model Name = “g45vnpn2”
Q1 (C B E) g45vnpn2 area=4.0 m=1

DIVA LVS Netlist
DIVA Device Name = “g45vnpn2”
; g45vnpn2 Instance /Q1 = auLvs device Q1
d vnpn C B E
i 1 g45vnpn2 C B E " area 4.0 m 1.0 "

CDL Netlist
CDL Device Name = “g45vnpn2”
QQ1 C B E g45vnpn2 area=4.0 m=1

Assura Netlist
Assura auLvs Device Name = “g45vnpn2”
c g45vnpn2 BJT C B B B E B ;;
* 3 pins
* 3 nets
* 0 instances
i Q1 g45vnpn2 C B E ; area 4.0 m 1 ;



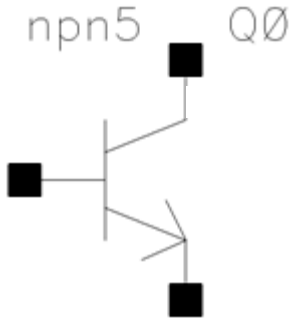
npn2 – 1.2 volt vertical substrate NPN with 2x2 fixed emitter

Device Layers	
Layer	**Color and Fill**
BJTdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal3	

Device Derivation	
Device	**Layer Derivation**
Recognition	**BJTDUMMY CONTAINS NIMP AND PIMP**
E	BJTDummy AND Pimp And Oxide AND Nwell
B	BJTDummy AND Nimp And Oxide AND Nwell
C	BJTDummy AND Pimp And Oxide ANDNOT Nwell

LVS Comparison	
Parameter	**Calculation**
Area	**AREA OF EMITTER (ILLUSTRATED ABOVE)**

21.31 npn5 datasheet

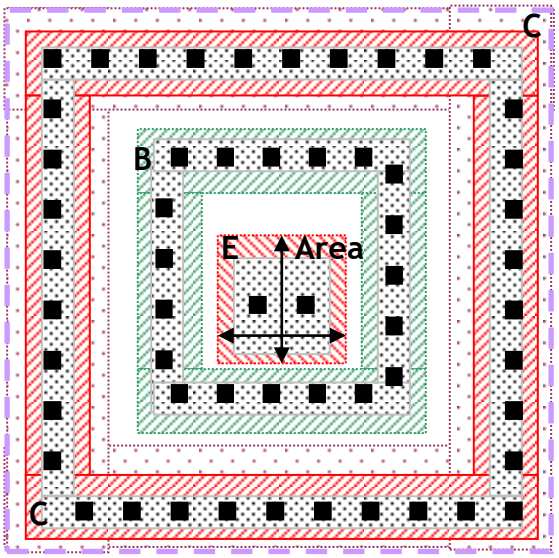


Spectre Netlist
Spectre Model Name = “g45vnpn5”
Q1 (C B E) g45vnpn5 area=25.0 m=1

DIVA LVS Netlist
DIVA Device Name = “g45vnpn5”
; g45vnpn5 Instance /Q1 = auLvs device Q1
d vnpn C B E
i 1 g45vnpn5 C B E " area 25.0 m 1.0 "

CDL Netlist
CDL Device Name = “g45vnpn5”
QQ1 C B E g45vnpn5 area=25.0 m=1

Assura Netlist
Assura auLvs Device Name = “g45vnpn5”
c g45vnpn5 BJT C B B B E B ;;
* 3 pins
* 3 nets
* 0 instances
i Q1 g45vnpn5 C B E ; area 25.0 m 1 ;



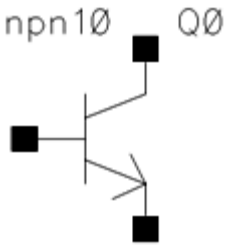
npn5 – 1.2 volt vertical substrate NPN with 5x5 fixed emitter

Device Layers	
Layer	**Color and Fill**
BJTdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal3	

Device Derivation	
Device	**Layer Derivation**
Recognition	**BJTDUMMY CONTAINS NIMP AND PIMP**
E	BJTDummy AND Pimp And Oxide AND Nwell
B	BJTDummy AND Nimp And Oxide AND Nwell
C	BJTDummy AND Pimp And Oxide ANDNOT Nwell

LVS Comparison	
Parameter	**Calculation**
Area	**AREA OF EMITTER (ILLUSTRATED ABOVE)**

21.32 npn10 datasheet

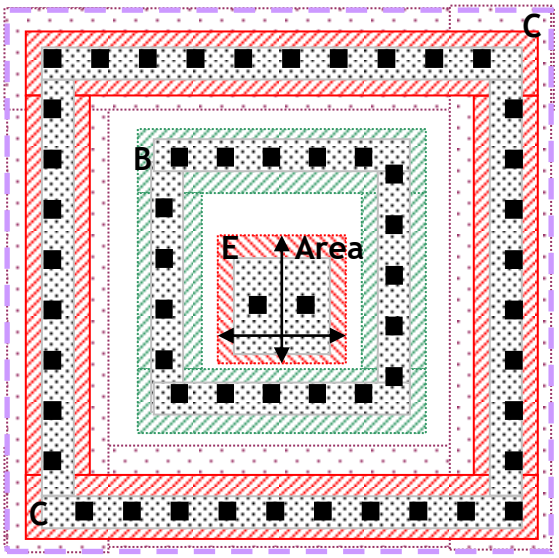


Spectre Netlist
Spectre Model Name = “g45vnpn10”
Q1 (C B E) g45vnpn10 area=100.0 m=1

DIVA LVS Netlist
DIVA Device Name = “g45vnpn10”
; g45vnpn10 Instance /Q1 = auLvs device Q1
d vnpn C B E
i 1 g45vnpn10 C B E " area 100.0 m 1.0 "

CDL Netlist
CDL Device Name = “g45vnpn10”
QQ1 C B E g45vnpn10 area=100.0 m=1

Assura Netlist
Assura auLvs Device Name = “g45vnpn10”
c g45vnpn10 BJT C B B B E B ;;
* 3 pins
* 3 nets
* 0 instances
i Q1 g45vnpn10 C B E ; area 100.0 m 1 ;



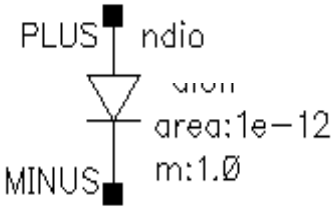
npn10 – 1.2 volt vertical substrate NPN with 10x10 fixed emitter

Device Layers	
Layer	**Color and Fill**
BJTdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal3	

Device Derivation	
Device	**Layer Derivation**
Recognition	**BJTDUMMY CONTAINS NIMP AND PIMP**
E	BJTDummy AND Pimp And Oxide AND Nwell
B	BJTDummy AND Nimp And Oxide AND Nwell
C	BJTDummy AND Pimp And Oxide ANDNOT Nwell

LVS Comparison	
Parameter	**Calculation**
Area	**AREA OF EMITTER (ILLUSTRATED ABOVE)**

21.33 ndio datasheet

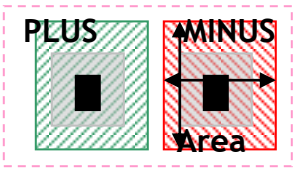


Spectre Netlist
Spectre Model Name = “g45nd1svt”
D0 (PLUS MINUS) g45nd1svt area=160f pj=1.6u m=1

DIVA LVS Netlist
DIVA Device Name = “g45nd1svt”
; g45nd1svt Instance /D0 = auLvs device D0
d g45nd1svt PLUS MINUS
i 0 g45nd1svt PLUS MINUS " area 1e-12 pj 1.6e-6 m 1.0 "

CDL Netlist
CDL Device Name = “g45nd1svt”
DD0 PLUS MINUS g45nd1svt 160f 1.6u m=1

Assura Netlist
Assura auLvs Device Name = “g45nd1svt”
c g45nd1svt DIO PLUS B MINUS B ;;
* 2 pins
* 2 nets
i D0 g45nd1svt PLUS MINUS ; area 1e-12 pj 1.6e-6 m 1 ;



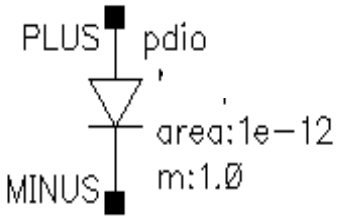
ndio - 1.2 volt N+/Psub diode

Device Layers	
Layer	**Color and Fill**
DIOdummy	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	DIODUMMY AND NIMP
PLUS	DIOdummy AND Pimp
MINUS	DIOdummy AND Nimp

LVS Comparison	
Parameter	**Calculation**
area	**Area of MINUS (illustrated above)**

21.34 pdio datasheet

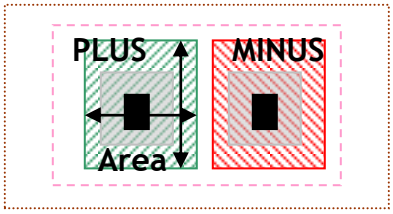


Spectre Netlist
Spectre Model Name = “g45pd1svt”
D0 (PLUS MINUS) g45pd1svt area=160f pj=1.6u m=1

DIVA LVS Netlist
DIVA Device Name = “g45pd1svt”
; g45pd1svt Instance /D0 = auLvs device D0
d g45pd1svt PLUS MINUS
i 0 g45pd1svt PLUS MINUS " area 160e-15 pj 1.6e-6 m 1.0 "

CDL Netlist
CDL Device Name = “g45pd1svt”
DD0 PLUS MINUS g45pd1svt 160f 1.6u m=1

Assura Netlist
Assura auLvs Device Name = “g45pd1svt”
c g45pd1svt DIO PLUS B MINUS B ;;
* 2 pins
* 2 nets
i D0 g45pd1svt PLUS MINUS ; area 1.6e-13 pj 1.6e-6 m 1 ;



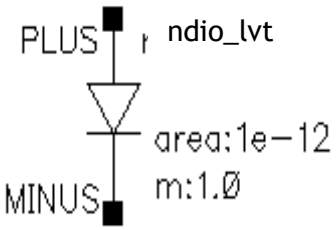
pdio - 1.2 volt P+/Nwell diode

Device Layers	
Layer	**Color and Fill**
DIOdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	DIODUMMY AND PIMP AND NWELL
PLUS	DIOdummy AND Pimp AND Nwell
MINUS	DIOdummy AND Nimp AND Nwell

LVS Comparison	
Parameter	**Calculation**
area	**Area of PLUS (illustrated above)**

21.35 ndio_lvt datasheet



Spectre Netlist
Spectre Model Name = "g45nd1lvt"

D0 (PLUS MINUS) g45nd1lvt area=160f pj=1.6u m=1

DIVA LVS Netlist
DIVA Device Name = "g45nd1lvt"

; g45nd1lvt Instance /D0 = auLvs device D0

d g45nd1lvt PLUS MINUS

i 0 g45nd1lvt PLUS MINUS " area 1e-12 pj 1.6e-6 m 1.0 "

CDL Netlist
CDL Device Name = "g45nd1lvt"

DD0 PLUS MINUS g45nd1lvt 160f 1.6u m=1

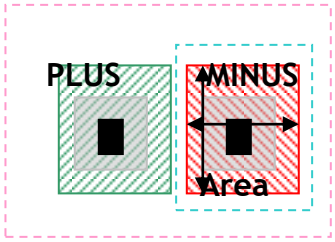
Assura Netlist
Assura auLvs Device Name = "g45nd1lvt"

c g45nd1lvt DIO PLUS B MINUS B ;;

* 2 pins

* 2 nets

i D0 g45nd1lvt PLUS MINUS ; area 1e-12 pj 1.6e-6 m 1 ;



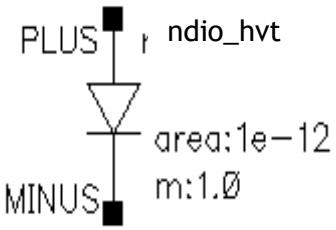
ndio_lvt - 1.2 volt low VT N+/Psub diode

Device Layers	
Layer	**Color and Fill**
DIOdummy	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	
Nlvt	

Device Derivation	
Device	**Layer Derivation**
Recognition	DIODUMMY AND NIMP
PLUS	DIOdummy AND Pimp
MINUS	DIOdummy AND Nimp

LVS Comparison	
Parameter	**Calculation**
area	**Area of MINUS (illustrated above)**

21.36 ndio_hvt datasheet

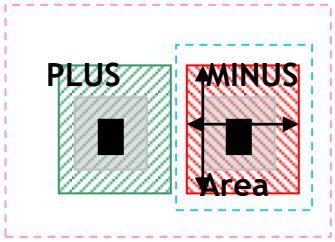


Spectre Netlist
Spectre Model Name = "g45nd1hvt"
D0 (PLUS MINUS) g45nd1hvt area=160f pj=1.6u m=1

DIVA LVS Netlist
DIVA Device Name = "g45nd1hvt"
; g45nd1hvt Instance /D0 = auLvs device D0
d g45nd1hvt PLUS MINUS
i 0 g45nd1hvt PLUS MINUS " area 1e-12 pj 1.6e-6 m 1.0 "

CDL Netlist
CDL Device Name = "g45nd1hvt"
DD0 PLUS MINUS g45nd1hvt 160f 1.6u m=1

Assura Netlist
Assura auLvs Device Name = "g45nd1hvt"
c g45nd1hvt DIO PLUS B MINUS B ;;
* 2 pins
* 2 nets
i D0 g45nd1hvt PLUS MINUS ; area 1e-12 pj 1.6e-6 m 1 ;



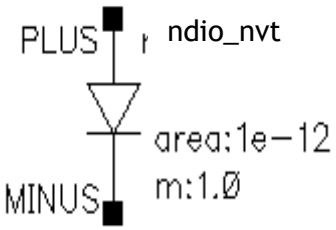
ndio_hvt – 1.2 volt high VT N+/Psub diode

Device Layers	
Layer	**Color and Fill**
DIOdummy	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	
Nhvt	

Device Derivation	
Device	**Layer Derivation**
Recognition	DIODUMMY AND NIMP
PLUS	DIOdummy AND Pimp
MINUS	DIOdummy AND Nimp

LVS Comparison	
Parameter	**Calculation**
area	**Area of MINUS (illustrated above)**

21.37 ndio_nvt datasheet



Spectre Netlist
Spectre Model Name = "g45nd1nvt"

D0 (PLUS MINUS) g45nd1nvt area=160f pj=1.6u m=1

DIVA LVS Netlist
DIVA Device Name = "g45nd1nvt"

; g45nd1nvt Instance /D0 = auLvs device D0

d g45nd1nvt PLUS MINUS

i 0 g45nd1nvt PLUS MINUS " area 1e-12 pj 1.6e-6 m 1.0 "

CDL Netlist
CDL Device Name = "g45nd1nvt"

DD0 PLUS MINUS g45nd1nvt 160f 1.6u m=1

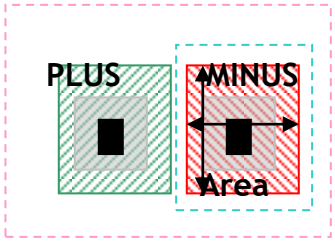
Assura Netlist
Assura auLvs Device Name = "g45nd1nvt"

c g45nd1nvt DIO PLUS B MINUS B ;;

* 2 pins

* 2 nets

i D0 g45nd1nvt PLUS MINUS ; area 1e-12 pj 1.6e-6 m 1 ;



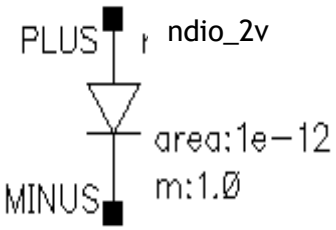
ndio_nvt – 1.2 volt native VT N+/Psub diode

Device Layers	
Layer	**Color and Fill**
DIOdummy	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	
Nhvt	

Device Derivation	
Device	**Layer Derivation**
Recognition	DIODUMMY AND NIMP
PLUS	DIOdummy AND Pimp
MINUS	DIOdummy AND Nimp

LVS Comparison	
Parameter	**Calculation**
area	**Area of MINUS (illustrated above)**

21.38 ndio_2v datasheet

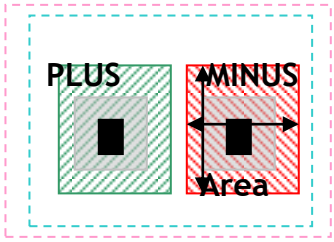


Spectre Netlist
Spectre Model Name = "g45nd2svt"
D0 (PLUS MINUS) g45nd2svt area=160f pj=1.6u m=1

DIVA LVS Netlist
DIVA Device Name = "g45nd2svt"
; g45nd2svt Instance /D0 = auLvs device D0
d g45nd2svt PLUS MINUS
i 0 g45nd2svt PLUS MINUS " area 1e-12 pj 1.6e-6 m 1.0 "

CDL Netlist
CDL Device Name = "g45nd2svt"
DD0 PLUS MINUS g45nd2svt 160f 1.6u m=1

Assura Netlist
Assura auLvs Device Name = "g45nd2svt"
c g45nd2svt DIO PLUS B MINUS B ;;
* 2 pins
* 2 nets
i D0 g45nd2svt PLUS MINUS ; area 1e-12 pj 1.6e-6 m 1 ;



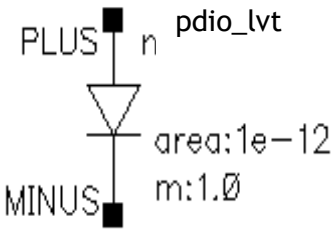
ndio_2v - 1.8 volt N+/Psub diode

Device Layers	
Layer	**Color and Fill**
DIOdummy	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	
Oxide_thk	

Device Derivation	
Device	**Layer Derivation**
Recognition	DIODUMMY AND NIMP
PLUS	DIOdummy AND Pimp
MINUS	DIOdummy AND Nimp

LVS Comparison	
Parameter	**Calculation**
area	**Area of MINUS (illustrated above)**

21.39 pdio_lvt datasheet

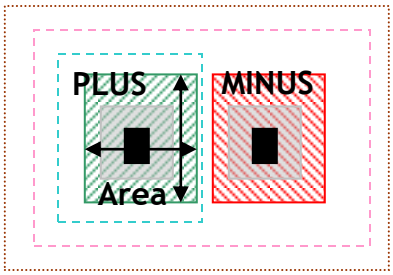


Spectre Netlist
Spectre Model Name = “g45pd1lvt”
D0 (PLUS MINUS) g45pd1lvt area=160f pj=1.6u m=1

DIVA LVS Netlist
DIVA Device Name = “g45pd1lvt”
; g45pd1lvt Instance /D0 = auLvs device D0
d g45pd1lvt PLUS MINUS
i 0 g45pd1lvt PLUS MINUS " area 1e-12 pj 1.6e-6 m 1.0 "

CDL Netlist
CDL Device Name = “g45pd1lvt”
DD0 PLUS MINUS g45pd1lvt 160f 1.6u m=1

Assura Netlist
Assura auLvs Device Name = “g45pd1lvt”
c g45pd1lvt DIO PLUS B MINUS B ;;
* 2 pins
* 2 nets
i D0 g45pd1lvt PLUS MINUS ; area 1e-12 pj 1.6e-6 m 1 ;



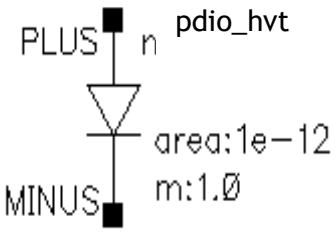
pdio_lvt - 1.2 volt low VT P+/Nwell diode

Device Layers	
Layer	**Color and Fill**
DIOdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	
Nlvt	

Device Derivation	
Device	**Layer Derivation**
Recognition	DIODUMMY AND NIMP
PLUS	DIOdummy AND Pimp
MINUS	DIOdummy AND Nimp

LVS Comparison	
Parameter	**Calculation**
area	**Area of PLUS (illustrated above)**

21.40 pdio_hvt datasheet

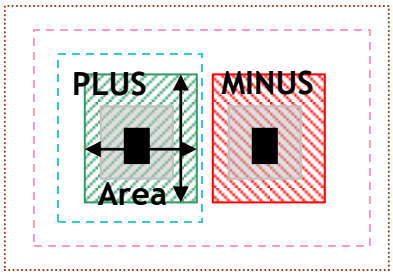


Spectre Netlist
Spectre Model Name = "g45pd1hvt"
D0 (PLUS MINUS) g45pd1hvt area=160f pj=1.6u m=1

DIVA LVS Netlist
DIVA Device Name = "g45pd1hvt"
; g45pd1hvt Instance /D0 = auLvs device D0
d g45pd1hvt PLUS MINUS
i 0 g45pd1hvt PLUS MINUS " area 1e-12 pj 1.6e-6 m 1.0 "

CDL Netlist
CDL Device Name = "g45pd1hvt"
DD0 PLUS MINUS g45pd1hvt 160f 1.6u m=1

Assura Netlist
Assura auLvs Device Name = "g45pd1hvt"
c g45pd1hvt DIO PLUS B MINUS B ;;
* 2 pins
* 2 nets
i D0 g45pd1hvt PLUS MINUS ; area 1e-12 pj 1.6e-6 m 1 ;



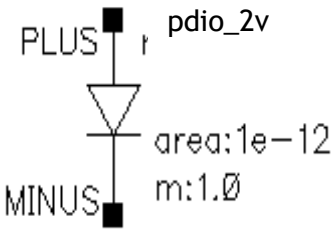
pdio_hvt – 1.2 volt high VT P+/Nwell diode

Device Layers	
Layer	**Color and Fill**
DIOdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	
Nhvt	

Device Derivation	
Device	**Layer Derivation**
Recognition	DIODUMMY AND NIMP
PLUS	DIOdummy AND Pimp
MINUS	DIOdummy AND Nimp

LVS Comparison	
Parameter	**Calculation**
area	**Area of PLUS (illustrated above)**

21.41 pdio_2v datasheet

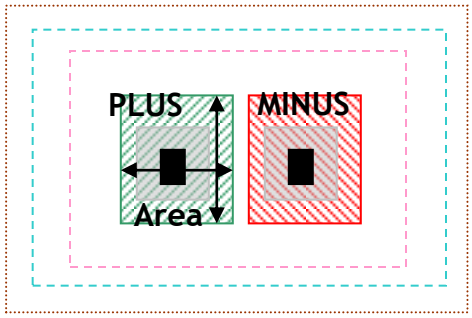


Spectre Netlist
Spectre Model Name = "g45pd2svt"
D0 (PLUS MINUS) g45pd2svt area=160f pj=1.6u m=1

DIVA LVS Netlist
DIVA Device Name = "g45pd2svt"
; g45pd2svt Instance /D0 = auLvs device D0
d g45pd2svt PLUS MINUS
i 0 g45pd2svt PLUS MINUS " area 1e-12 pj 1.6e-6 m 1.0 "

CDL Netlist
CDL Device Name = "g45pd2svt"
DD0 PLUS MINUS g45pd2svt 160f 1.6u m=1

Assura Netlist
Assura auLvs Device Name = "g45pd2svt"
c g45pd2svt DIO PLUS B MINUS B ;;
* 2 pins
* 2 nets
i D0 g45pd2svt PLUS MINUS ; area 1e-12 pj 1.6e-6 m 1 ;



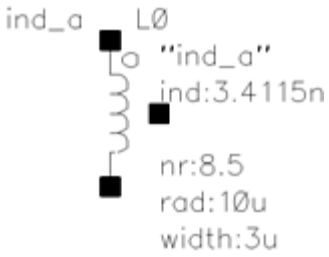
pdio_2v - 1.8 volt P+/Nwell diode

Device Layers	
Layer	**Color and Fill**
DIOdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	
Oxide_thk	

Device Derivation	
Device	**Layer Derivation**
Recognition	DIODUMMY AND NIMP
PLUS	DIOdummy AND Pimp
MINUS	DIOdummy AND Nimp

LVS Comparison	
Parameter	**Calculation**
area	**Area of PLUS (illustrated above)**

21.42 ind_a datasheet



Spectre Netlist
Spectre Model Name = "g45inda"

L0 (PLUS MINUS B) g45inda w=3u s=1.5u r=10u nr=8.5 m=1

DIVA LVS Netlist
DIVA Device Name = "g45inda"

; g45inda Instance /L1 = auLvs device L0

d g45inda PLUS MINUS B

i 0 g45inda PLUS MINUS B "width 3u space 1.5e-6 rad 10e-6 nr 8.5 m 1.0 "

CDL Netlist
CDL Device Name = "g45inda"

L0 PLUS MINUS B g45inda width 3u space 1.5e-6 rad 10e-6 nr 8.5 m 1

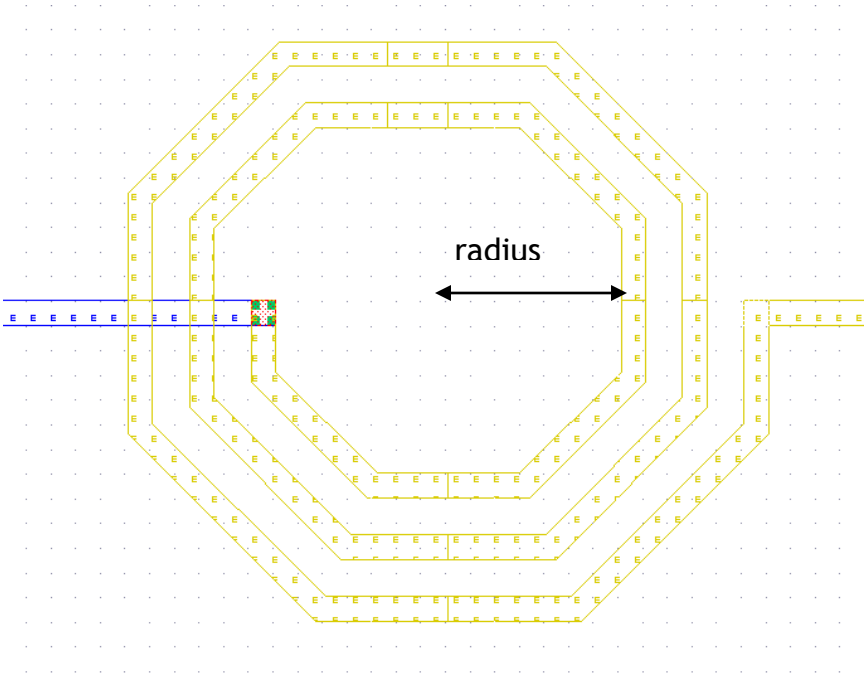
Assura Netlist
Assura auLvs Device Name = "g45inda"

c g45inda IND PLUS B MINUS B B B ;;

* 3 pins

* 3 nets

i L0 g45inda PLUS MINUS B m 1 nr 8.5 width 3e-06 space 1.5e-06 rad 10e-06 ;



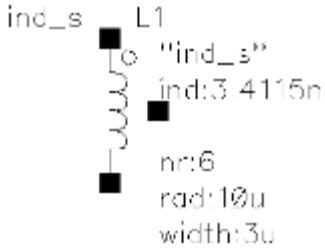
ind_a - Asymmetric Inductor

Device Layers	
Layer	**Color and Fill**
INDdummy	
Metal11	
Metal10	
IND2dummy	
Cont	

Device Derivation	
Device	**Layer Derivation**
Recognition	**INDDUMMY AND METAL11**
PLUS	INDdummy AND Metal11
MINUS	INDdummy AND Metal10

LVS Comparison	
Parameter	**Calculation**
radius	**Inner radius of Metal11 turn (illustrated above)**
width	**Width of Metal11**

21.43 ind_s datasheet

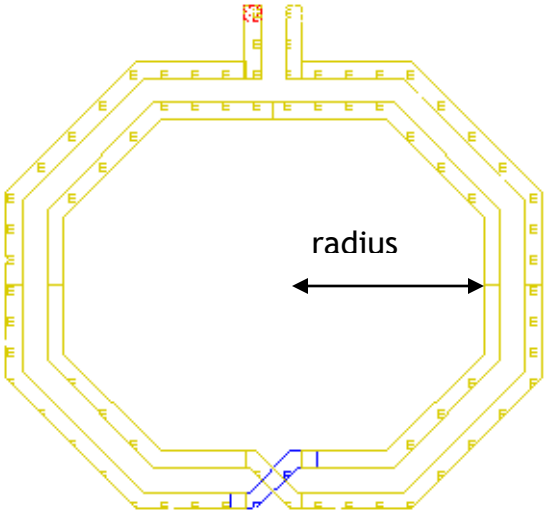


Spectre Netlist
Spectre Model Name = “g45inds”
L1 (PLUS MINUS B) g45inds w=3u s=1.5u r=10u nr=6 m=1

DIVA LVS Netlist
DIVA Device Name = “g45inds”
; g45inds Instance /L2 = auLvs device L1 d g45inds PLUS MINUS B i 1 g45inds PLUS MINUS B "width 3u space 1.5e-6 rad 10e-6 nr 6 m 1.0 "

CDL Netlist
CDL Device Name = “g45inds”
L1 PLUS MINUS B g45inds width 3u space 1.5e-6 rad 10e-6 nr 6 m 1

Assura Netlist
Assura auLvs Device Name = “g45inds”
c g45inds IND PLUS B MINUS B B B ;; * 3 pins * 3 nets i L1 g45inds PLUS MINUS B m 1 nr 6 width 3e-06 space 1.5e-06 rad 10e-06 ;



ind_s - Symmetric Inductor

Device Layers	
Layer	**Color and Fill**
INDdummy	
Metal11	
Metal10	
IND2dummy	
Cont	

Device Derivation	
Device	**Layer Derivation**
Recognition	**INDDUMMY AND METAL11**
PLUS	IND2dummy AND Metal11
MINUS	IND3dummy AND Metal11

LVS Comparison	
Parameter	**Calculation**
radius	**Inner radius of Metal11 turn (illustrated above)**
width	**Width of Metal11**