1   Introduction

This report describes the predictive SPICE models developed by Accelicon Technologies, Inc. for a generic 45nm technology based on semiconductor research. The extracted model list is attached in the later sections followed by the predicted simulation PCM targets (Idsat, Vth) of all corners. The delivered models are in the format of SPECTRE.

2   MOSFET Models

This section lists the details of the MOSFET models developed for this project. The target definition for Vth and Idat is listed below:

Vth is obtained using constant current method, the intercept current=Icon*W/L (Icon=1e-8A for 1.1V device and Icon=1e-7A for 1.8V device), Vth unit is V.

Idsat is obtained from the drain current at Vds=Vdd, Vgs=Vdd and Vbs=0, Idsat unit is A. Idsat/W is the normalized Idsat value, Unit is A/m.

2.1: MOSFET Intrinsic Models

There are total of 10 MOSFET models developed for this project. The binning model approach is adopted according to customer request. The model naming, valid geometry range, temperature range and Vdd are listed in table 2-1.

Device	Model Name	Vdd (V)	Bins	Temp scale (℃)	Wmin(um)	Wmax (um)	Lmin (um)	Lmax (um)
1.1V Standard-Vt	nch	1.1	30	-40 to 125	0.12	10	0.04	10
	pch	1.1	30	-40 to 125	0.12	10	0.04	10
1.1V High-Vt	nch_hvt	1.1	30	-40 to 125	0.12	10	0.04	10
	pch_hvt	1.1	30	-40 to 125	0.12	10	0.04	10
1.1V low-Vt	nch_lvt	1.1	30	-40 to 125	0.12	10	0.04	10
	pch_lvt	1.1	30	-40 to 125	0.12	10	0.04	10
1.1V native	nch_na	1.1	9	-40 to 125	0.5	10	0.3	10
1.8V	nch_18	1.8	12	-40 to 125	0.32	10	0.15	10
	pch_18	1.8	12	-40 to 125	0.32	10	0.15	10
1.8V native	nch18_na	1.8	9	-40 to 125	0.5	10	0.8	10

Table2.1 List of MOSFET Models

Device	Model Name	Vdd (V)	Bins	Temp scale (℃)	Wmin (um)	Wmax (um)	Lmin (um)	Lmax (um)
1.1V Standard-Vt	nch _mis	1.1	30	-40 to 125	0.12	10	0.04	10
	nch _mis	1.1	30	-40 to 125	0.12	10	0.04	10
1.1V High-Vt	nch_hvt _mis	1.1	30	-40 to 125	0.12	10	0.04	10
	pch_hvt _mis	1.1	30	-40 to 125	0.12	10	0.04	10
1.1V low-Vt	nch_lvt _mis	1.1	30	-40 to 125	0.12	10	0.04	10
	pch_lvt _mis	1.1	30	-40 to 125	0.12	10	0.04	10
1.1V native	nch_na_mis	1.1	9	-40 to 125	0.5	10	0.3	10
1.8V	nch_18 _mis	1.8	12	-40 to 125	0.32	10	0.15	10
	pch_18 _mis	1.8	12	-40 to 125	0.32	10	0.15	10
1.8V native	nch18_na _mis	1.8	9	-40 to 125	0.5	10	0.8	10

Table2.2 List of MOSFET Statistical Models and Mismatch Models.

2.2: MOSFET Corner and Statistical Models

Corner Models and Statistical Models (with Mismatch) are also developed, the model list is shown in Table 2-3.

Device	Typical Nmos & PMOS	Fast Nmos & PMOS	Slow Nmos& PMOS	Fast Nmos & Slow mos	Slow mos & Fast Pmos
1.1V Standard Vt	tt	ff	ss	fs	sf
1.1V High Vt	tt_hvt	ff _hvt	ss _hvt	fs _hvt	sf _hvt
1.1V Low Vt	tt_lvt	ff _lvt	ss _lvt	fs _lvt	sf _lvt
1.1v native	tt_na	ff _na	ss _na	fs _na	sf _na
1.8 v	tt_18	ff _18	ss _18	fs _18	sf _18
1.8v Native	tt_na18	ff _na18	ss _na18	fs _na18	sf _na18

Table2.3 List of MOSFET Corner Models

2.3: MOSFET Model Characteristics

2.3.1: 1.1V Standard Vt NMOS

Binning Scheme:
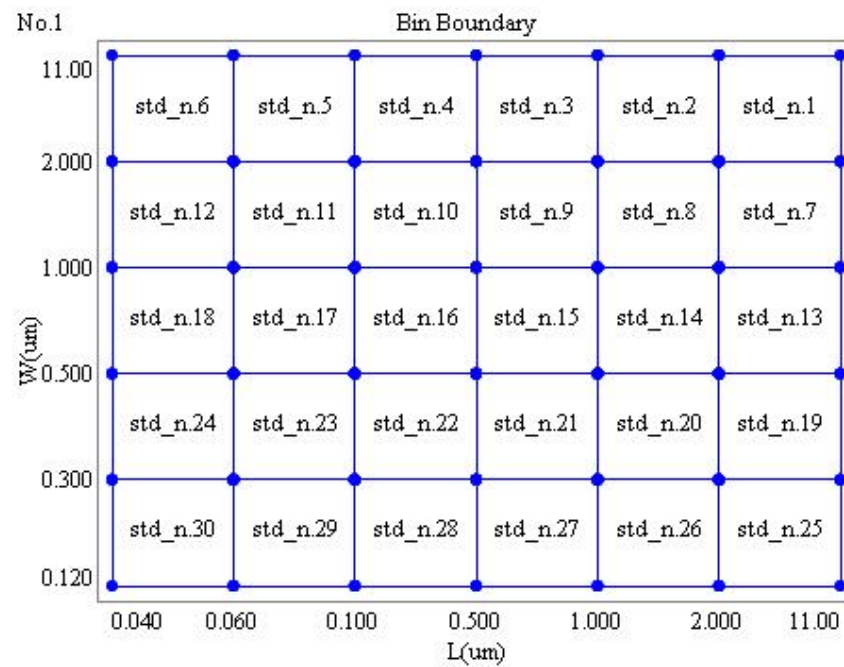
Model Spec:

W(um)	L(um)	Vth	Idsat
10	10	0.36	9.01E-05
0.12	0.04	0.36	7.40E-05
10	0.04	0.38	5.96E-03
0.12	10	0.14	1.21E-06

Table 2.4 1.1v Standard Vt NMOS Model Spec

Corner Model Spec

Target	W(um)	L (um)	SS	SF	TT	FS	FF
Vth	10	10	0.39	0.38	0.36	0.34	0.32
	0.12	0.04	0.46	0.41	0.36	0.31	0.26
	10	0.04	0.43	0.41	0.38	0.35	0.32
	0.12	10	0.2	0.17	0.14	0.11	0.08
Idsat	10	10	7.83E-05	8.42E-05	9.01E-05	9.58E-05	1.02E-04
	0.12	0.04	5.54E-05	6.47E-05	7.40E-05	8.32E-05	9.24E-05
	10	0.04	5.23E-03	5.59E-03	5.96E-03	6.31E-03	6.68E-03
	0.12	10	8.73E-07	1.04E-06	1.21E-06	1.38E-06	1.56E-06

Table 2.5 1.1v Standard Vt NMOS Corner Model Spec

2.3.2: 1.1V Standard Vt PMOS

Binning Scheme:
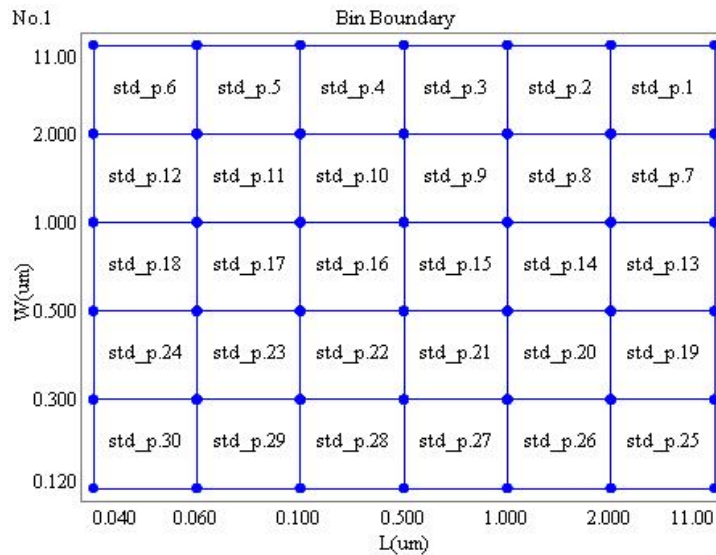
Model Spec:

W(um)	L(um)	Vth	Idsat
10	10	-0.3	-6.48E-05
0.12	0.04	-0.4	-4.27E-05
10	0.04	-0.43	-3.06E-03
0.12	10	-0.22	-8.67E-07

Table 2.6 1.1v Standard Vt PMOS Model Spec

Corner Model SPEC

Target	W (um)	L (um)	SS	FS	TT	SF	FF
Vth	10	10	-0.33	-0.31	-0.3	-0.28	-0.27
	0.12	0.04	-0.49	-0.45	-0.4	-0.36	-0.31
	10	0.04	-0.48	-0.46	-0.43	-0.41	-0.38
	0.12	10	-0.28	-0.25	-0.22	-0.19	-0.16
Idsat	10	10	-5.63E-05	-6.06E-05	-6.48E-05	-6.89E-05	-7.33E-05
	0.12	0.04	-3.22E-05	-3.56E-05	-4.27E-05	-4.81E-05	-5.34E-05
	10	0.04	-2.69E-03	0.00E+00	-3.06E-03	-3.24E-03	-3.42E-03
	0.12	10	-6.34E-07	-7.49E-07	-8.67E-07	-9.84E-07	-1.10E-06

Table 2.7 1.1v Standard Vt PMOS Corner Model Spec

2.3.3: 1.1V Low Vt NMOS

Binning Scheme
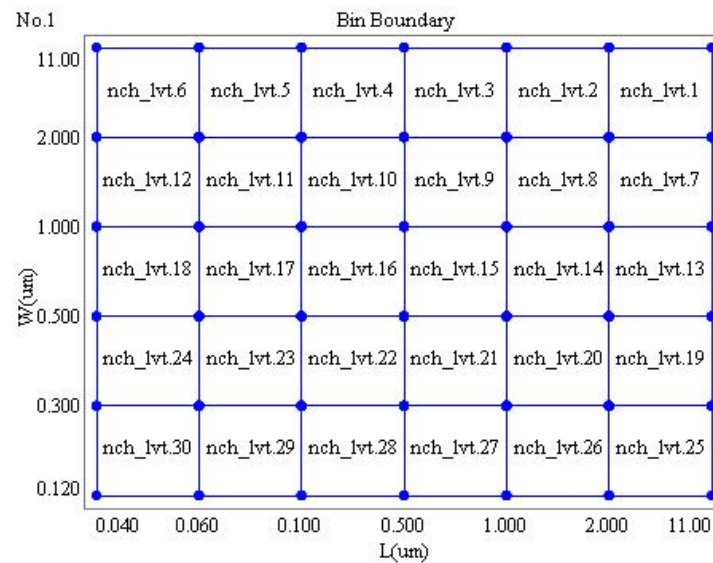
SPEC Table

W(um)	L(um)	Vth	Idsat
10	10	0.26	1.17E-04
0.12	0.04	0.26	9.78E-05
10	0.04	0.28	7.76E-03
0.12	10	0.05	1.53E-06

Table 2.8 1.1v Low Vt NMOS Model Spec

Corner Model SPEC

Target	W (um)	L (um)	TT_LVT	FF_LVT	SS_LVT	FS_LVT	SF_LVT
Vth	10	10	0.26	0.22	0.29	0.24	0.27
	0.12	0.04	0.26	0.16	0.36	0.21	0.31
	10	0.04	0.28	0.23	0.34	0.25	0.31
	0.12	10	0.05	-0.01	0.11	0.02	0.08
Idsat	10	10	1.17E-04	1.32E-04	1.02E-04	1.24E-04	1.09E-04
	0.12	0.04	9.78E-05	1.23E-04	7.34E-05	1.10E-04	8.55E-05
	10	0.04	7.76E-03	8.69E-03	6.82E-03	8.22E-03	7.29E-03
	0.12	10	1.53E-06	1.95E-06	1.12E-06	1.75E-06	1.32E-06

Table 2.9 1.1v Low Vt NMOS Corner Model Spec

2.3.4: 1.1V Low Vt PMOS

Binning Scheme
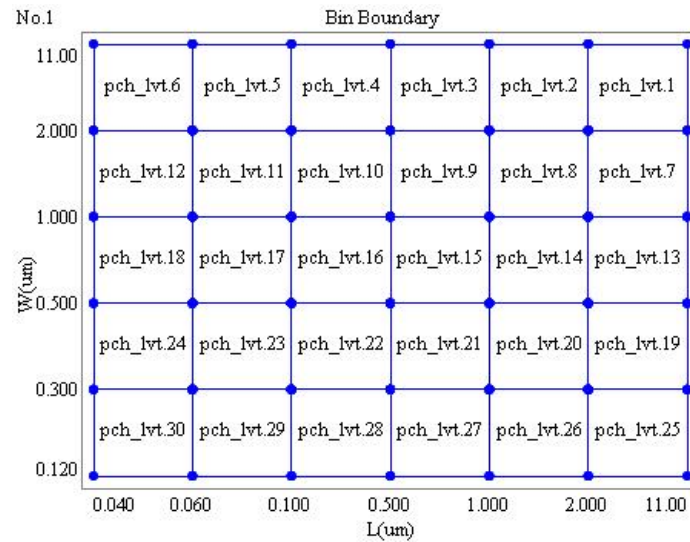
SPEC Table

W(um)	L(um)	Vth	Idsat
10	10	-0.21	-8.67E-05
0.12	0.04	-0.31	-5.15E-05
10	0.04	-0.34	-3.69E-03
0.12	10	-0.13	-1.13E-06

Table 2.10 1.1v Low Vt PMOS Model Spec

Corner Model SPEC

Target	W (um)	L (um)	TT_LVT	FF_LVT	SS_LVT	FS_LVT	SF_LVT
Vth	10	10	-0.21	-0.18	-0.24	-0.22	-0.2
	0.12	0.04	-0.31	-0.21	-0.41	-0.36	-0.26
	10	0.04	-0.34	-0.29	-0.39	-0.36	-0.31
	0.12	10	-0.13	-0.07	-0.19	-0.16	-0.1
Idsat	10	10	-8.67E-05	-9.83E-05	-7.56E-05	-8.12E-05	-9.24E-05
	0.12	0.04	-5.15E-05	-6.42E-05	-3.86E-05	-4.50E-05	-5.78E-05
	10	0.04	-3.69E-03	-4.13E-03	-3.24E-03	-3.46E-03	-3.91E-03
	0.12	10	-1.13E-06	-1.44E-06	-8.27E-07	-9.79E-07	-1.29E-06

Table 2.11 1.1v Low Vt PMOS Corner Model Spec

2.3.5: 1.1V High Vt NMOS

Binning Scheme
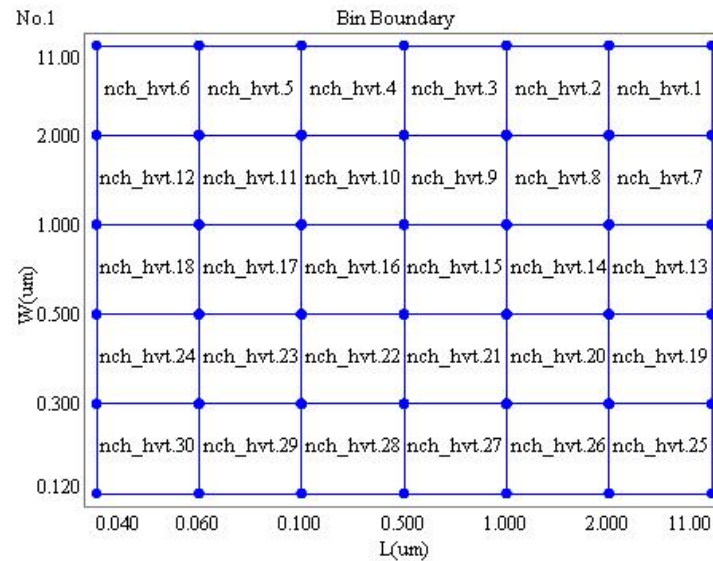
SPEC Table

W(um)	L(um)	Vth	Idsat
10	10	0.43	6.81E-05
0.12	0.04	0.46	5.01E-05
10	0.04	0.48	3.97E-03
0.12	10	0.2	9.42E-07

Table 2.12 1.1v High Vt NMOS Model Spec

Corner Model SPEC

Target	W (um)	L (um)	TT_HVT	FF_HVT	SS_HVT	FS_HVT	SF_HVT
Vth	10	10	0.43	0.39	0.46	0.41	0.45
	0.12	0.04	0.46	0.37	0.55	0.42	0.51
	10	0.04	0.48	0.43	0.53	0.46	0.51
	0.12	10	0.2	0.14	0.26	0.17	0.23
Idsat	10	10	6.81E-05	7.73E-05	5.95E-05	7.25E-05	6.37E-05
	0.12	0.04	5.01E-05	6.26E-05	3.76E-05	5.63E-05	4.38E-05
	10	0.04	3.97E-03	4.45E-03	3.50E-03	4.21E-03	3.74E-03
	0.12	10	9.42E-07	1.20E-06	6.88E-07	1.07E-06	8.10E-07

Table 2.13 1.1v High Vt NMOS Corner Model Spec

2.3.6: 1.1V High Vt PMOS

Binning Scheme
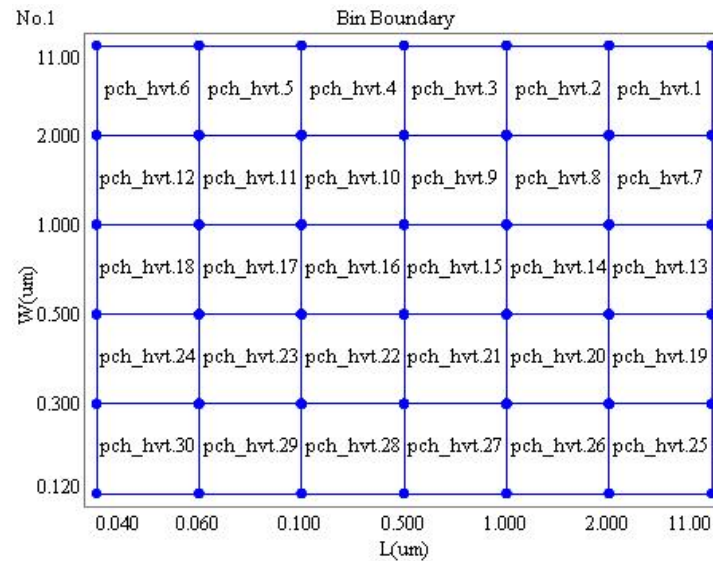
SPEC Table

W(um)	L(um)	Vth	Idsat
10	10	-0.38	-4.76E-05
0.12	0.04	-0.49	-3.00E-05
10	0.04	-0.52	-2.00E-03
0.12	10	-0.3	-6.52E-07

Table 2.14 1.1v High Vt PMOS Model Spec

Corner Model SPEC

Target	W (um)	L (um)	TT_HVT	FF_HVT	SS_HVT	FS_HVT	SF_HVT
Table Vth	10	10	-0.38	-0.35	-0.4	-0.39	-0.36
	0.12	0.04	-0.49	-0.42	-0.58	-0.53	-0.45
	10	0.04	-0.52	-0.47	-0.57	-0.54	-0.49
	0.12	10	-0.3	-0.24	-0.35	-0.33	-0.27
2 Idsat 1 5	10	10	-4.76E-05	-5.38E-05	-4.14E-05	-4.45E-05	-5.06E-05
	0.12	0.04	-3.00E-05	-3.75E-05	-2.25E-05	-2.62E-05	-3.37E-05
	10	0.04	-2.00E-03	-2.24E-03	-1.76E-03	-1.87E-03	-2.12E-03
	0.12	10	-6.52E-07	-8.27E-07	-4.77E-07	-5.63E-07	-7.39E-07

1.Table 2.15 1v High Vt PMOS Corner Model Spec

2.3.7: 1.1V Native NMOS

Binning Scheme
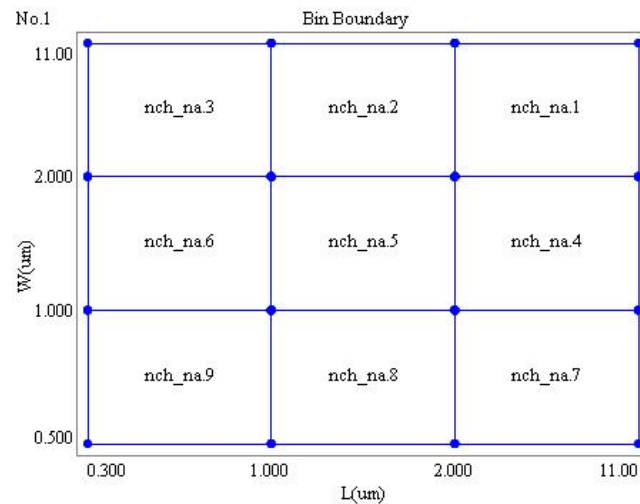
SPEC Table

W(um)	L(um)	Vth	Idsat
10	10	0.05	2.26E-04
0.5	0.3	-0.07	2.39E-04
10	0.3	-2.71E-03	4.59E-03
0.5	10	-0.16	1.20E-05

Table 2.16 1.1v Native NMOS Model Spec

Corner Model SPEC

Target	W (um)	L (um)	TT_NA	FF_NA	SS_NA	FS_NA	SF_NA
Vth	10	10	0.05	0.01	0.08	0.03	0.07
	0.5	0.3	-0.07	-0.15	-9.87E-03	-0.11	-0.03
	10	0.3	-2.71E-03	-0.06	0.06	-0.03	0.03
	0.5	10	-0.16	-0.2	-0.12	-0.18	-0.14
Idsat	10	10	2.26E-04	2.46E-04	2.06E-04	2.36E-04	2.16E-04
	0.5	0.3	2.39E-04	2.75E-04	2.03E-04	2.57E-04	2.19E-04
	10	0.3	4.59E-03	5.14E-03	4.04E-03	4.87E-03	4.32E-03
	0.5	10	1.20E-05	1.35E-05	1.06E-05	1.27E-05	1.13E-05

Table 2.17 1.1v Native NMOS Corner Model Spec

2.3.8: 1.8V IO NMOS

Binning Scheme
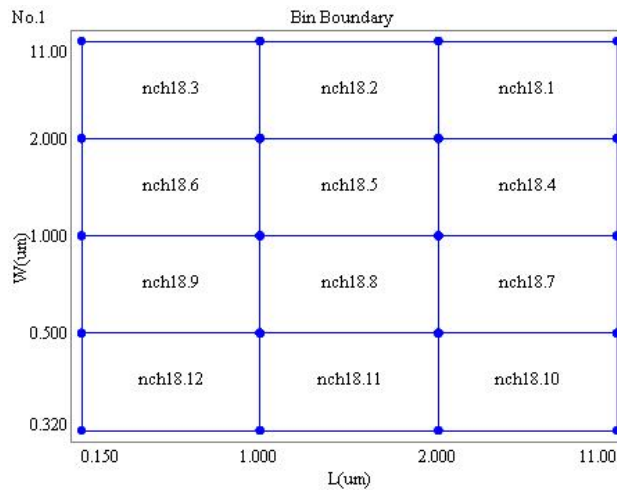
SPEC Table

W(um)	L(um)	Vth	Idsat
10	10	0.43	2.39E-04
0.32	0.15	0.45	2.20E-04
10	0.15	0.49	6.79E-03
0.32	10	0.32	7.86E-06

Table 2.18 1.8v NMOS Model Spec

Corner Model SPEC

Target	W (um)	L (um)	TT_18	FF_18	SS_18	FS_18	SF_18
Vth	10	10	0.43	0.39	0.47	0.41	0.45
	0.32	0.15	0.45	0.36	0.54	0.4	0.49
	10	0.15	0.49	0.42	0.55	0.46	0.52
	0.32	10	0.32	0.26	0.38	0.29	0.35
Idsat	10	10	2.39E-04	2.69E-04	2.08E-04	2.54E-04	2.23E-04
	0.32	0.15	2.20E-04	2.59E-04	1.80E-04	2.39E-04	2.00E-04
	10	0.15	6.79E-03	7.59E-03	5.95E-03	7.17E-03	6.36E-03
	0.32	10	7.86E-06	9.43E-06	6.29E-06	8.64E-06	7.07E-06

Table 2.19 1.8v NMOS Corner Model Spec

2.3.9: 1.8V IO PMOS

Binning Scheme
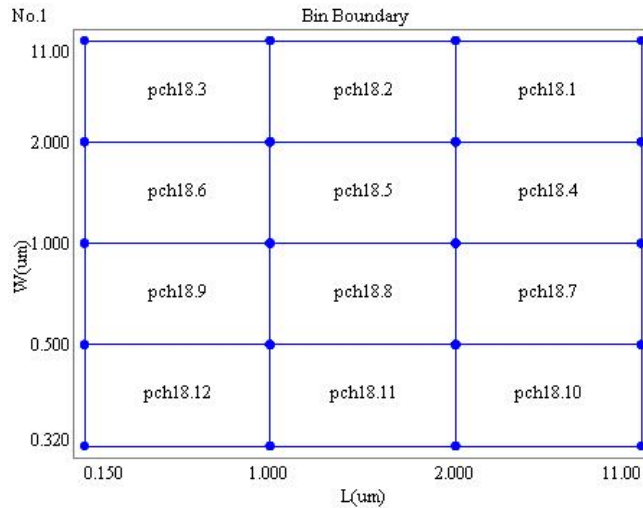
SPEC Table

W(um)	L(um)	Vth	Idsat
10	10	-0.37	-1.04E-04
0.12	0.04	-0.49	-1.02E-04
10	0.04	-0.51	-3.00E-03
0.12	10	-0.37	-3.76E-06

Table 2.20 1.8v PMOS Model Spec

Corner Model SPEC

Target	W (um)	L (um)	TT_18	FF_18	SS_18	FS_18	SF_18
Vth	10	10	-0.37	-0.33	-0.4	-0.39	-0.35
	0.32	0.15	-0.49	-0.41	-0.57	-0.53	-0.45
	10	0.15	-0.51	-0.44	-0.58	-0.54	-0.48
	0.32	10	-0.37	-0.32	-0.42	-0.39	-0.34
Idsat	10	10	-1.04E-04	-1.19E-04	-8.81E-05	-9.59E-05	-1.11E-04
	0.32	0.15	-1.02E-04	-1.20E-04	-8.34E-05	-9.26E-05	-1.11E-04
	10	0.15	-3.00E-03	-3.40E-03	-2.56E-03	-2.77E-03	-3.19E-03
	0.32	10	-3.76E-06	-4.51E-06	-3.01E-06	-3.38E-06	-4.13E-06

Table 2.21 1.8v PMOS Corner Model Spec

2.3.10: 1.8V Native NMOS

Binning Scheme
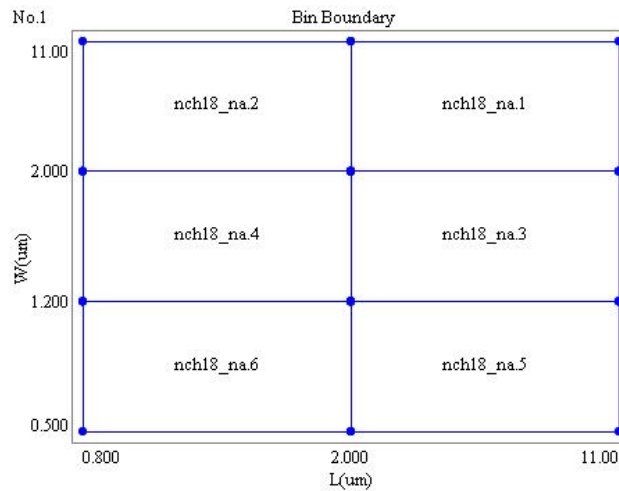
SPEC Table

W(um)	L(um)	Vth	Idsat
10	10	6.69E-03	5.03E-04
0.5	0.8	-0.05	2.41E-04
10	0.8	-0.02	4.72E-03
0.5	10	-0.11	2.54E-05

Table 2.22 1.8v Native NMOS Model Spec

Corner Model SPEC

Target	W (um)	L (um)	TT_NA18	FF_NA18	SS_NA18	FS_NA18	SF_NA18
Vth	10	10	6.69E-03	-0.04	0.06	-0.02	0.03
	0.5	0.8	-0.05	-0.14	0.04	-0.1	-7.54E-03
	10	0.8	-0.02	-0.1	0.05	-0.06	0.01
	0.5	10	-0.11	-0.17	-0.05	-0.14	-0.08
Idsat	10	10	5.03E-04	5.38E-04	4.67E-04	5.20E-04	4.85E-04
	0.5	0.8	2.41E-04	2.78E-04	2.05E-04	2.59E-04	2.23E-04
	10	0.8	4.72E-03	5.29E-03	4.16E-03	5.01E-03	4.44E-03
	0.5	10	2.54E-05	2.86E-05	2.21E-05	2.70E-05	2.37E-05

Table 2.23 1.8v Native NMOS Corner Model Spec

2.4 MOSFET Statistical Model and Mismatch Model

2.4.1: Statistical SPICE Model

Due to the lack of wafer data for PCA (Principle Component Analysis), the 3σ of Idsat, Vth and the key model parameters such as Tox, XL and XW are obtained from corner SPEC. Correlation coefficients between key model parameters are obtained by fitting the 3σ of Idsat, Vth.
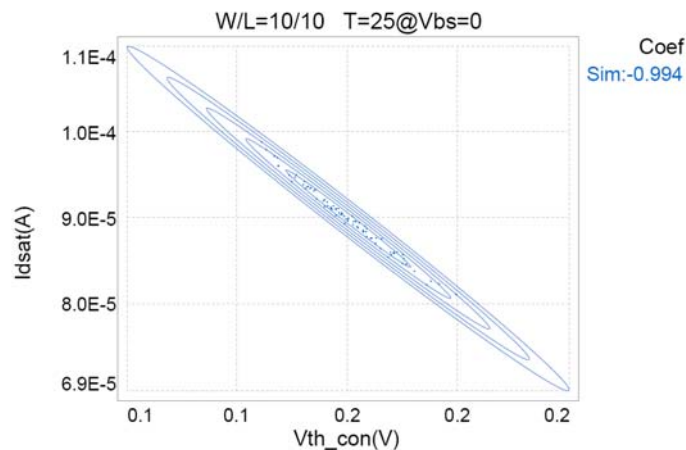
2.4.2: Mismatch Model

Mismatch model is also available, TOX, XL, XW and Vth0 are used to account for the local random variation.
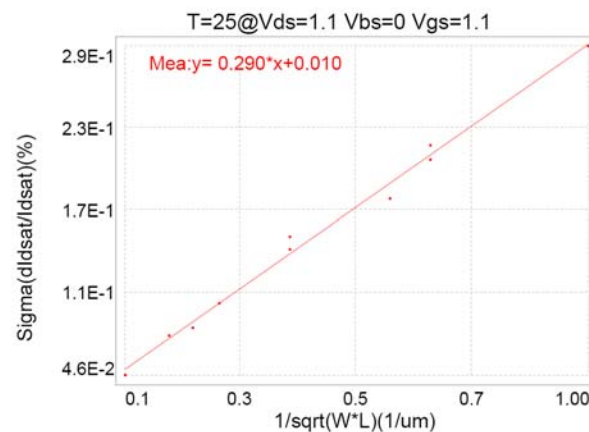
3 BJT Models

There are total of 8 bipolar models are developed with two types, Vertical NPN and Vertical PNP, each with models for 3 emitter size and a scalable model. The model nominal temperature is 25℃, while the valid temperature varied from -40 to 125℃. BJT Device list is shown below:

	2∗2	5∗5	10∗10	Scalable model
PNP	pnp2	pnp5	pnp10	pnp_scalable
NPN	npn2	npn5	npn10	npn_scalable

Table 3.1 Bipolar model list

3.1 BJT Intrinsic Models

3.1.1: Vertical PNP

Skew Table and Corner SPEC

Parameters	TYPICAL PNP10	TYPICAL PNP5	TYPICAL PNP2	SLOW %	FAST %
BF	1.022	1.226	1.851	-10	10
IS(A)	8.491E-18	2.440E-18	5.047E-19	-20	20
NF	1.015	1.015	1.015	0.30	-0.30
RE(Ohm)	3.48	6.52	9.56	20	-20
RB(Ohm)	88.42	92.64	140.5	20	-20
RC(Ohm)	7.12	8.58	10.01	20	-20
RBM(Ohm)	0.1	0.1	0.1	20	-20
CJE(F)	1.17e-13	2.848E-14	5.1E-15	10	-10
CJC(F)	2.55e-13	5.512E-14	3.8E-14	10	-10

Table 3.2   Skew parameters table for vertical PNP models

3.1.2: Vertical NPN

Skew Table and Corner SPEC

Parameters	TYPICAL NPN10	TYPICAL NPN5	TYPICAL NPN2	SLOW %	FAST %
BF	4.049	4.560	5.064	-10	10
IS(A)	1.995E-17	5.569E-18	1.085E-18	-20	20
NF	1.014	1.014	1.014	0.3	-0.3
RE(Ohm)	4.312	6.512	8.386	20	-20
RB(Ohm)	112.22	176.08	323.5	20	-20
RC(Ohm)	5.98	7.26	13.42	20	-20
RBM(Ohm)	0.1	0.1	0.1	20	-20
CJE(F)	1.2e-13	2.88E-14	5.38E-15	10	-10
CJC(F)	2.74e-13	1.480E-13	8.29E-14	10	-10

Table 3.3   Skew parameters table for vertical NPN models

3.2 BJT Statistical Model

Due to the lack of wafer data for PCA (Principle Component Analysis), the 3σ of skewed model parameters such as IS, BF, etc are obtained from corner model parameters.

4 Diode Models

There are total of 10 diode models developed for this project, the device list is shown below:

	1.1v standard	1.1v high vt	1.1v low vt	1.8v	1.1v native	1.8v native
Lib name	dio	dio_hvt	dio_lvt	dio_18	dio_na	dio_na18
N+/PW	ndio	ndio_hvt	ndio_lvt	ndio_18	ndio_na	ndio_na18
P+/NW	pdio	pdio_hvt	pdio_lvt	pdio_18		

Table 4.1 List of junction diode models

4.1 Intrinsic Diode Models

Skew table

Parameters	Typical N+P Diode	Typical P+N Diode	SLOW %	FAST %
IS(A/m2)	1.985E-7	1.658E-7	-20	20
ISW(A/m2)	7.240E-13	6.075E-13	-60	60
N	1.241	1.224	0.3	-0.3
RS(Ohm)	8.701E-11	1.1E-10	15	-15
CJO(F/m2)	1.177E-3	1.308E-3	8	-8
CJSW(F/m2)	6.562E-11	7.604E-11	8	-8

Table 4.2 Skew parameters table for 1.1V Standard Vt junction diodes.

Parameters	Typical N+P Diode	Typical P+N Diode	SLOW %	FAST %
IS(A/m2)	1.897E-7	1.343E-7	-20	20
ISW(A/m2)	5.987E-13	4.216E-13	-60	60
N	1.199	1.116	0.3	-0.3
RS(Ohm)	9.016E-11	1.307E-10	15	-15
CJO(F/m2)	7.978E-4	1.349E-3	8	-8
CJSW(F/m2)	4.4E-11	7.636E-11	8	-8

Table 4.3 Skew parameters table for 1.1V high Vt junction diodes

Parameters	Typical N+P Diode	Typical P+N Diode	SLOW%	FAST%
IS(A/m2)	2.392E-7	1.658E-7	-20	20
ISW(A/m2)	4.460E-13	6.075E-13	-60	60

N	1.326	1.224	0.3	-0.3
RS(Ohm)	1.424E-10	1E-10	15	-15
CJO(F/m2)	1.177E-3	1.308E-3	8	-8
CJSW(F/m2)	6.562E-11	8.253E-11	8	-8

Table 4.4 Skew parameters table for 1.1V low Vt junction diodes.

Parameters	Typical N+P Diode	Typical P+N Diode	SLOW %	FAST %
IS(A/m2)	5.386E-7	4.319E-7	-20	20
ISW(A/m2)	3.452E-12	1.835E-12	-60	60
N	1.232	1.224	0.3	-0.3
RS(Ohm)	1E-10	1.100E-10	15	-15
CJO(F/m2)	1.154E-3	1.352E-3	8	-8
CJSW(F/m2)	1.761E-10	8.582E-11	8	-8

Table 4.5 Skew parameters table for 1.8V junction diodes.

Parameters	Typical N+P Diode	SLOW%	FAST%
IS(A/m2)	7.893E-7	-20	20
ISW(A/m2)	1.068E-12	-60	60
N	1.225	0.3	-0.3
RS(Ohm)	1.200E-10	15	-15
CJO(F/m2)	1.668E-4	8	-8
CJSW(F/m2)	1.60E-10	8	-8

Table 4.6 Skew parameters table for 1.1V Native junction diodes.

Parameters	Typical N+P Diode	SLOW%	FAST%
IS(A/m2)	1.076E-6	-20	20
ISW(A/m2)	1.670E-12	-60	60
N	1.224	0.3	-0.3
RS(Ohm)	1.210E-10	15	15
CJO(F/m2)	1.668E-4	8	-8
CJSW(F/m2)	2.344E-10	8	-8

Table 4.7 Skew parameters table for 1.8V Native junction diodes.

4.2 Statistical Diode Models

Due to the lack of wafer data for PCA (Principle Component Analysis), the 3σ of skewed model parameters such as IS, N, etc are obtained from corner model parameters.

5   Resistor Models

There are total of 30 resistor models developed for this project, including 10 2-terminal resistors, 10 3-terminal resistors and 11 metal resistors. The device list is shown below:

Model name	structure	rsh value
resnwsti	N-well Resistor under STI	1000
resnwoxide	N-well Resistor under Oxide	450
ressndiff	N+ Diffused Resistor (salicide)	18
resspdiff	P+ Diffused Resistor (salicide)	15
ressnpoly	N+ Poly Resistor (salicide)	15
ressppoly	P+ Poly Resistor (salicide)	15
resnsndiff	N+ Diffused Resistor (w/o salicide)	100
resnspdiff	P+ Diffused Resistor (w/o salicide)	200
resnsnpoly	N+ Poly Resistor (w/o salicide)	200
resnsppoly	P+ Poly Resistor (w/o salicide)	600

Table 5.1 list of 2-terminal resistor model

Model name	structure	rsh value
resnwsti_m	NW diff(under STI)	1000
resnwoxide_m	NW diff(under OD)	450
ressndiff _m	N+diff w/i silicide	18
resspdiff _m	P+diff w/i silicide	15
ressnpoly_dis	N+Poly w/i silicide	15
ressppoly_dis	P+Poly w/i silicide	15
resnsndiff_m	N+diff w/o silicide	100
resnspdiff_m	P+diff w/o silicide	200
resnsnpoly_dis	N+Poly w/o silicide	200
resnsppoly_dis	P+Poly w/o silicide	600

Table 5.2 list of 3-terminal resistor model

Model name	structure	rsh value
resm1	Metal 1 Resistor	0.0736
resm2	Metal 2 Resistor	0.0604
resm3	Metal 3 Resistor	0.0604
resm4	Metal 4 Resistor	0.0604
resm5	Metal 5 Resistor	0.0604
resm6	Metal 6 Resistor	0.0604
resm7	Metal 7 Resistor	0.0604
resm8	Metal 8 Resistor	0.0214
resm9	Metal 9 Resistor	0.0214
resm10	Metal 10 Resistor	0.0214
resm11	Metal 11 Resistor	0.021

Table 5.3 list of metal resistor model

6   Capacitor Models

6.1 MOS Capacitor

Model name	structure
s1p8v_nch18_mac	Mosfet capacitance for 1.8v nmos
s1p8v_pch18_mac	Mosfet capacitance for 1.8v pmos
s1v_nch_mac	Mosfet capacitance for 1.1v nmos
s1v_nch_mac	Mosfet capacitance for 1.1v pmos

Table 6.1 list of MOS capacitor model

6.2 MIM Capacitor

Model name	structure
mimcap	MiM capacitance Model

Table 6.2 list of MIM capacitor model

7   Inductor Models

Device	Model name
inductor	ind_m

Table 7.1 list of inductor model