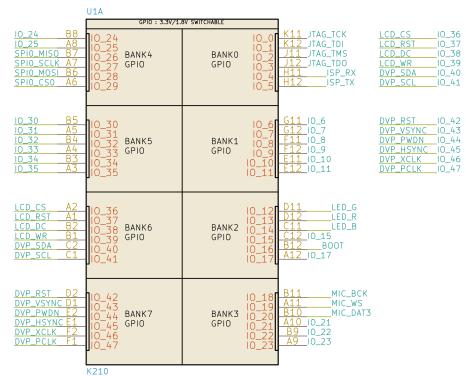
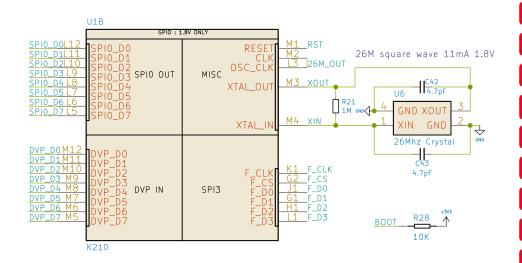
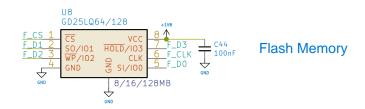
Core System

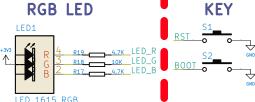


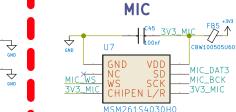




Note:

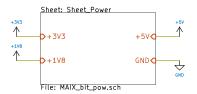
BOOT(IO16) pull low to enter ISP mode, download from IO4,5 SPI3 Support XIP SPI0/1/3 for Master, SPI2 for slave 3.3V IO speed 80M, 1.8V IO speed 208M. Simple test PWM is faster than 300MHz.



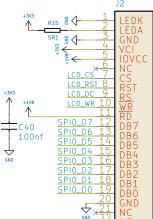


1:RIGHT 0:LEFT

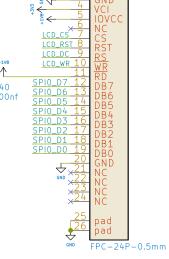
Power



TF Card



8bit MCU LCD

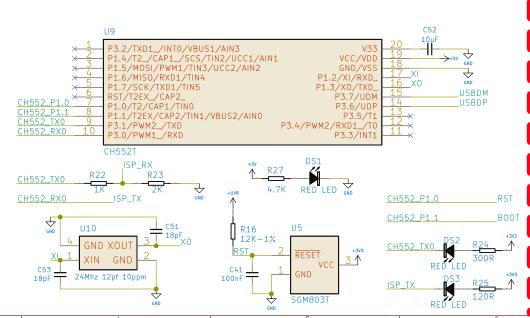


USB to UART IC

SIP20 SIP

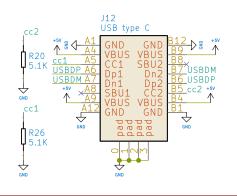
DVP_PWDN

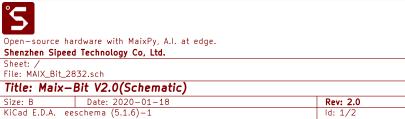
ISP DOWNLOAD



USB Port

DVP Carmera





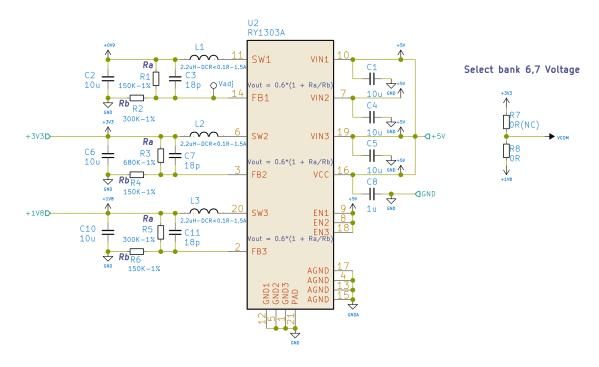
DVP_SCL_R13 2K DVP_SDA R14 2k

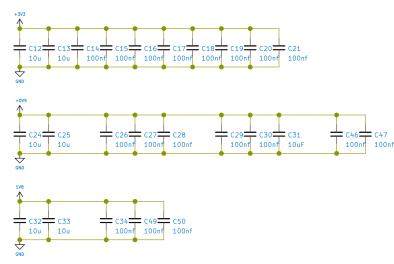
GND 10-8

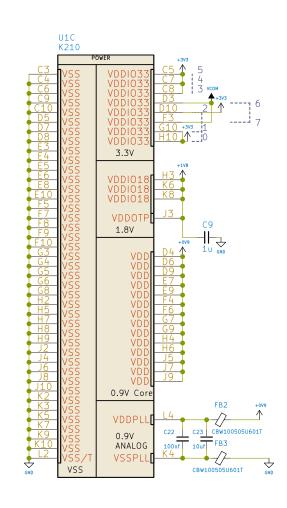
_IO_6 _ISP_TX _ISP_RX _JTAG_TDO _JTAG_TMS

Connector

DCDC&LDO









Open—source hardware with MaixPy, A.I. at edge.
Shenzhen Sipeed Technology Co, Ltd.

Sheet: /Sheet_Power/ File: MAIX_bit_pow.sch

Title: Maix-Bit V2.0(Schematic)

- 1	Size: B	Date: 2020-01-18	Rev: 2.0
	KiCad E.D.A. e	eschema (5.1.6)-1	ld: 2/2