TÉCNICO LISBOA

CIRCUIT THEORY AND ELECTRONICS FUNDAMENTALS

[MEAER]

INTEGRATED MASTER'S DEGREE IN AEROSPACE ENGINEERING

LABORATORY 2

RC CIRCUIT ANALYSIS

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1 Introduction

In this laboratory, we analysed in a theoretical approach as well as using software simulation, a first-order forced circuit, in particular, RC with Forced Sinusoidal Voltage. With this method, software simulation and theoretical analysis can be stacked up against each other more easily. It allowed us to deal with important concepts such as the **impedance** (and its inverse, admittance), **phasors** (with amplitudes and phases), as well as **stationary, transient and frequency response** analysis. In Figure 1 the stated circuit is presented.

A theoretical analysis of the circuit will be presented using Nodal Analysis giving us some insights on the stationary behaviour of the circuit (2.1), before the time starts counting ($t < 0$). Also, Nodal Analysis is used in its phasor form to derive the forced solution for node voltages. Later, we superimposed both solutions referred and studied the response of the circuit regarding the change in frequency (either its Magnitude, as well as, Phase).

At the same time, the circuit is analysed by computational simulation tools, via *Ngspice*, and the results are compared to the theoretical results obtained, in Section 2. The conclusions of this study are outlined in Section 3.

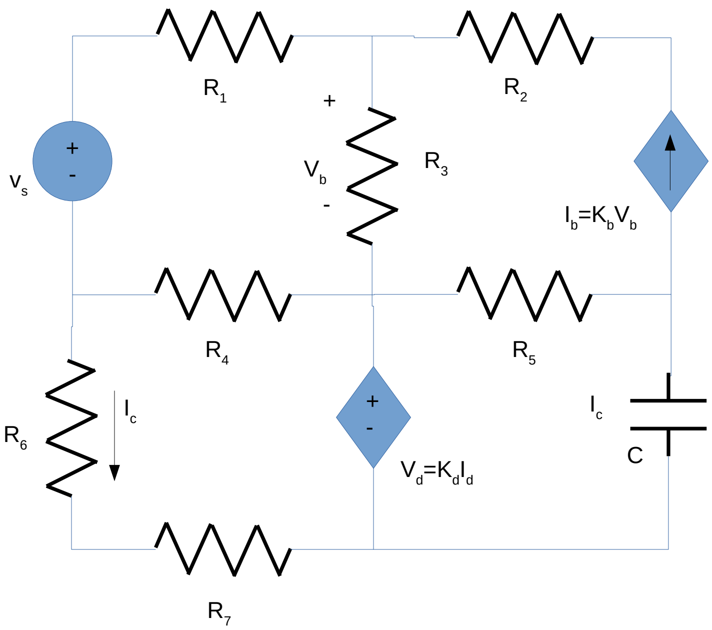

Figure 1: RC Circuit.

2 Theoretical and Simulation Analysis

In order to compare *side by side*, we'll discuss the theoretical and simulation analysis at the same time.

2.1 Stationary Analysis

For $t < 0$, we have a stationary *regime* which means that v_i and i_i are constants. In this case, as $i_c = C\frac{dv_c}{dt}$, we end up with i_c to be zero, *i.e.* an Open Circuit (OC).

The nodes are identified in the figure below. We considered V_4 to be the Ground Node.

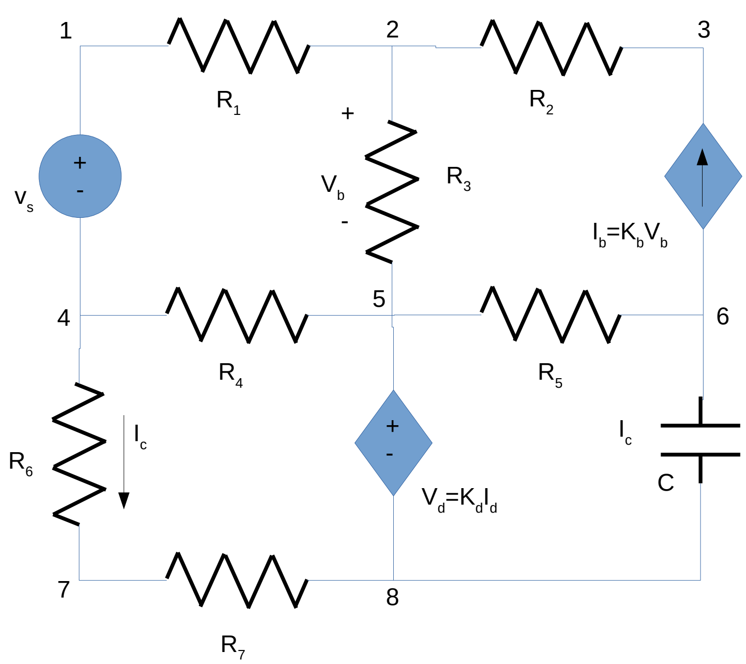

Figure 2: RC Circuit with Node Identification

We hence have, after computing Nodal Analysis,

$$\begin{bmatrix} 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -K_dG_6 & 1 & 0 & K_dG_6 & -1 \\ G_1 & -(G_1+G_2+G_3) & G_2 & 0 & G_3 & 0 & 0 & 0 \\ 0 & K_b+G_2 & -G_2 & 0 & -K_b & 0 & 0 & 0 \\ 0 & -K_b & 0 & 0 & G_5+K_b & -G_5 & 0 & 0 \\ 0 & 0 & 0 & G_6 & 0 & -G_6-G_7 & G_7 & 0 \\ 0 & G_3 & 0 & G4 & -(G_3+G_4+G_5) & G_5 & G_7 & -G_7 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ V_7 \\ V_8 \end{bmatrix} = \begin{bmatrix} 0 \\ V_s \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Regarding the computer-aided analysis (and remembering the already discussed, in the previous laboratory, *technique* of the addition of a *dummy* 0V-voltage source), we also have results, presented below:

Name	Value [mA or V]
V1	5.133225
V2	4.938703
V3	4.525145
V4	-0.000000
V5	4.966942
V6	5.595679
V7	-2.056243
V8	-3.102805
@IR1	0.193116
@IR2	-0.202180
@IR3	-0.009064
@IR4	1.199425
@IR5	-0.202180
@IR6	1.006309
@IR7	1.006309
@Ib	-0.202180
@IVs	0.193116
@IVd	1.006309

Table 1: Theoretical Results for $t < 0$

Name	Value [A or V]
@gb[i]	-2.02180e-04
@r1[i]	1.931161e-04
@r2[i]	-2.02180e-04
@r3[i]	-9.06371e-06
@r4[i]	1.199425e-03
@r5[i]	-2.02180e-04
@r6[i]	1.006309e-03
@r7[i]	1.006309e-03
v(1)	5.133225e+00
v(2)	4.938703e+00
v(3)	4.525145e+00
v(5)	4.966942e+00
v(6)	5.595679e+00
v(7)	-2.05624e+00
v(8)	-3.10280e+00
ne	-2.05624e+00

Table 2: Simulated Results for $t < 0$

We can see that, as expected, all results are equal.

The important result derived from this subsection is the voltage drop $V_6 - V_8$, which we'll impose later on as an Initial Condition (IC).

2.2 Equivalent Resistance

In this case we applied *Thévenin's* Equivalent Method to discover R_{eq} as seen from the capacitor. As we have Dependent Sources, it is not enough just to *shut down* Independent Sources.

In fact, one has to add, either an Independent Voltage Source or an Independent Current Source to the terminals of the OC.

We chose an Independent Current Source applying a current of $1A$ to easen the derivation (as $R_{eq} = V_x/I_x$).

After running Nodal Analysis we arrive at the theoretical results expressed in Tables 3:

Name	Value [V, A and Ω]
Vx	3109.793846
Ix	1.000000
Req	3109.793846

Table 3: Equivalent Resistance

2.3 Natural Solution

Using the results from the equivalent resistance calculated on Section 2.2 we can plot the natural solution of the voltage at V6 using the equivalent RC circuit, by doing:

$$v_{Cn} = [V_0 - V_\infty]e^{-(t-t_0)/\tau} + V_\infty$$

We know that $V_0 = V_{6_0} - V_{8_0}$ and that $V_\infty = 0$: The final *regime* is stationary, implying that, $\frac{dv}{dt} = 0$ for the natural solution. By the capacitor equation $i_c = C\frac{dv}{dt} = 0$, which means that no current passes through the capacitor nor the resistor. By Ohm's Law , one must conclude that $V_\infty = 0$. Since that by each node and simulation analysis, $V_{8n} = 0$, :

$$v_{6n} = v_{Cn} + v_{8n} = (V_{6_0} - V_{8_0})e^{-t/\tau}$$

Where $\tau = R_{eq}C$, represents the relaxation time.

Name	**Value [A or V]**
@gb[i]	0.000000e+00
@r1[i]	0.000000e+00
@r2[i]	0.000000e+00
@r3[i]	0.000000e+00
@r4[i]	0.000000e+00
@r5[i]	-2.79713e-03
@r6[i]	0.000000e+00
@r7[i]	0.000000e+00
v(1)	0.000000e+00
v(2)	0.000000e+00
v(3)	0.000000e+00
v(5)	0.000000e+00
v(6)	8.698484e+00
v(7)	0.000000e+00
v(8)	0.000000e+00
ne	0.000000e+00

Table 4: Simulation Results for Natural Solution Determination

The table shown above presents the values that are going to be used from now on regarding the ICs for the simulation analysis, and were generated using the professor's suggestion.

This step was imperative in order to determine the ICs regarding the transient analysis that will follow and also to calculate R_{eq}, which is useful to compare the natural solution analysis between both methods. The result for R_{eq}, which can be calculated by doing $\frac{v(6)}{|@r5[i]|}$, is equal to the one obtained in the theoretical analysis, as shown previously.

It is important to note that the value of v(6) given by the table is the subtraction of the values of v(6) and v(8) from table 2.

We can see, by comparing the plots below (Figures 5 and 6), that we achieved really satisfactory results. From a mere comparison of the figures, we can see that both have the same **shape** (negative exponential), they start at the **same voltage** and they almost touch zero, with a naked eye approach, at the **same time** (τ is equal in both graphs).

With a greater detail, one can compare the values of the coordinates of the points on each graphs to see that they match up.

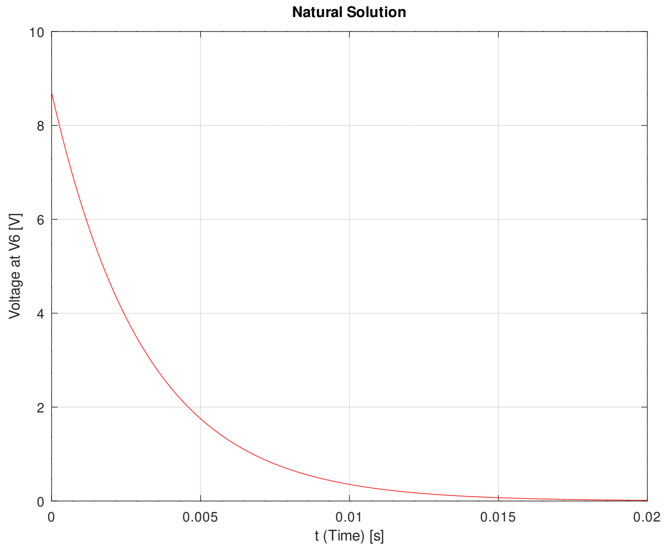

Figure 3: Theoretical Natural Solution

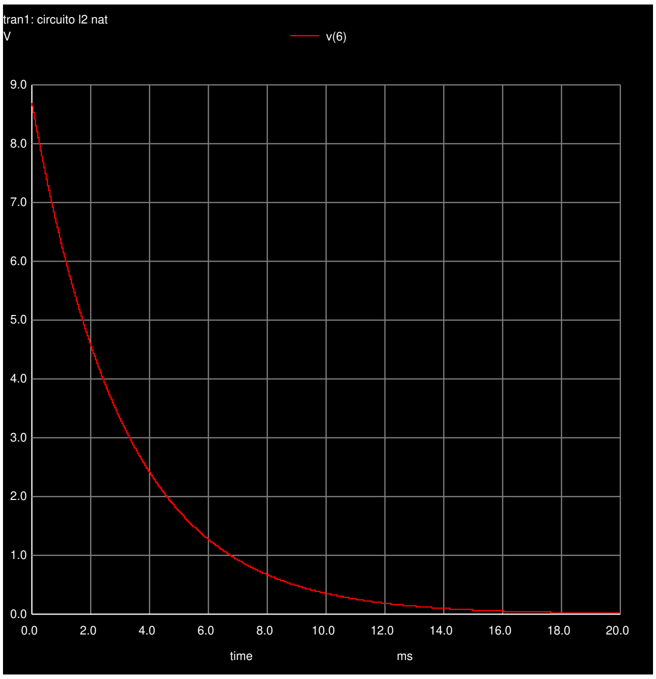

Figure 4: Simulation Natural Solution

2.4 Superimposed Natural and Forced Solutions

In a theoretical approach, we'll procede the analysis using the concept of phasors and its Nodal Analysis. We are now dealing with complex voltages of the form $\tilde{V_i} = V_i e^{j(\omega t - \phi_i)}$, where $V_i \equiv$ amplitude, $j \equiv$ imaginary quantity, $\omega \equiv$ angular frequency and $\phi_i \equiv$ phase.

One must remember that when we force a sinusoidal signal, the whole circuit will vibrate with the same frequency so, for the node analysis, the part corresponding to the time dependency can be ommited for the sake of simplicity and we can solve the system using phasors of the form $\tilde{V_i} = V_i e^{-j\phi_i}$. Then, the final real solutions can be derived by:

$$V_i = |\tilde{V_i}| sin(\omega t - \phi_i) \tag{1}$$

Once Phasor Node Analysis is apllied to the circuit, one ends up with the following complex matrix system:

$$\begin{bmatrix} 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -K_d G_6 & 1 & 0 & K_d G_6 & -1 \\ G_1 & -(G_1+G_2+G_3) & G_2 & 0 & G_3 & 0 & 0 & 0 \\ 0 & K_b + G_2 & -G_2 & 0 & -K_b & 0 & 0 & 0 \\ 0 & -K_b & 0 & 0 & G_5 + K_b & -G_5 - Y_c & 0 & Y_c \\ 0 & 0 & 0 & G_6 & 0 & 0 & -G_6 - G_7 & G_7 \\ 0 & -G_3 & 0 & -G4 & G_3 + G_4 + G_5 & G_5 - Y_c & -G_7 & G_7 + Y_c \end{bmatrix} \begin{bmatrix} \tilde{V_1} \\ \tilde{V_2} \\ \tilde{V_3} \\ \tilde{V_4} \\ \tilde{V_5} \\ \tilde{V_6} \\ \tilde{V_7} \\ \tilde{V_8} \end{bmatrix} = \begin{bmatrix} 0 \\ \tilde{V_s} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

where $Y_c \equiv j\omega C \equiv$ admittance of a capacitor.

Solving the above system gives off the following forced phasor voltages:

Name	Value [A or V]	Phase [Deg]
V1	1.000000	0.000000
V2	0.962105	-0.000000
V3	0.881540	-0.000000
V4	0.000000	90.000000
V5	0.967606	-0.000000
V6	0.606217	-171.829563
V7	0.400575	180.000000
V8	0.604455	180.000000

Table 5: Forced Complex Amplitudes

From that, by superimposing the Natural and Forced solution we have the plot 5.
On the *Ngspice* case, we just have to add a sinusoidal voltage source of the form

$$v_s(t) = V_s sin(2\pi f t)$$

where $f = 1kHz$.
Applying transient analysis, *Ngspice* plots as seen in figure 6.

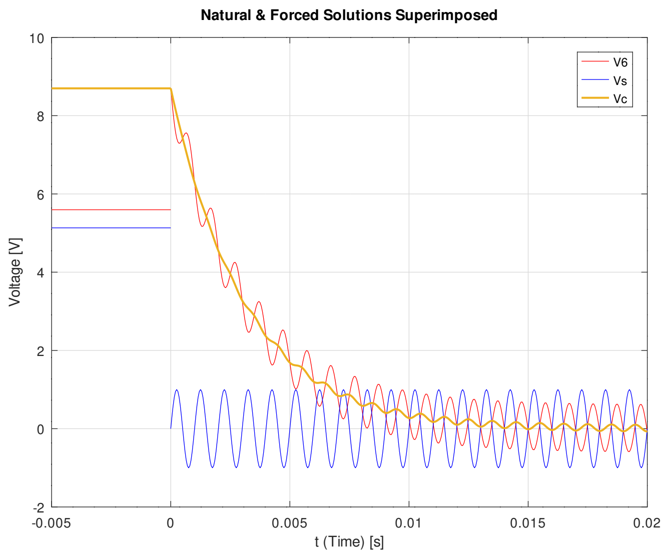

Figure 5: Theoretical Superimposed Solution

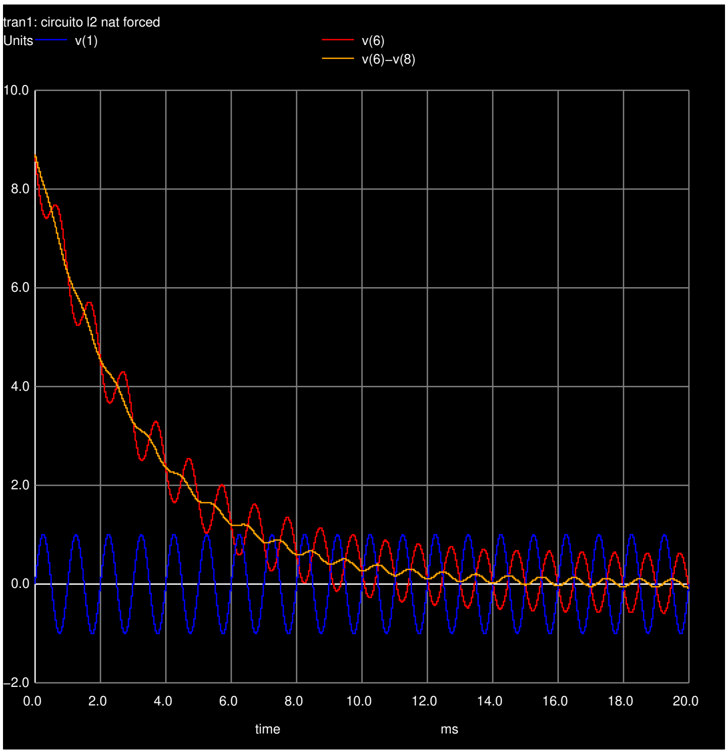

Figure 6: Simulation Superimposed Solution

It is interesting to identify, among other *phenomena*, the fact that, for $t \to \infty$, we have a pure sinusoidal signal on V_6 with the same frequency as the imposed one (which was expectable since that the natural solution part of $V_c \to 0$ and so, for the amplitudes $V_6 \to V_8$).

Besides, there is no discontinuity on v_c, which is expectable since there cannot be a voltage drop change on the capacitor for the same time sequence, bearing that energy stored in this element must be continuous.

If we compare some values of the three voltages examined, one can state that there is an enourmous amount of precision. Also, the phases and starting values are equivalent between both analysis. This leads, as previously achieved, to an excelent similarity using the two different methods.

2.5 Frequency Response

In this last subsection, we study the behaviour of $V_c = V_6 - V_8$, V_s and V_6 in both a theoretical point of view as well as simulation, when the frequency changes.

Before analysing the plot results, one has to remember that we have a logarithmic scale on the x-axis (frequency) and a decibel scale on the y-axis (amplitude voltage), for convenience.

When it comes to amplitudes the resultant theoretical graph is,

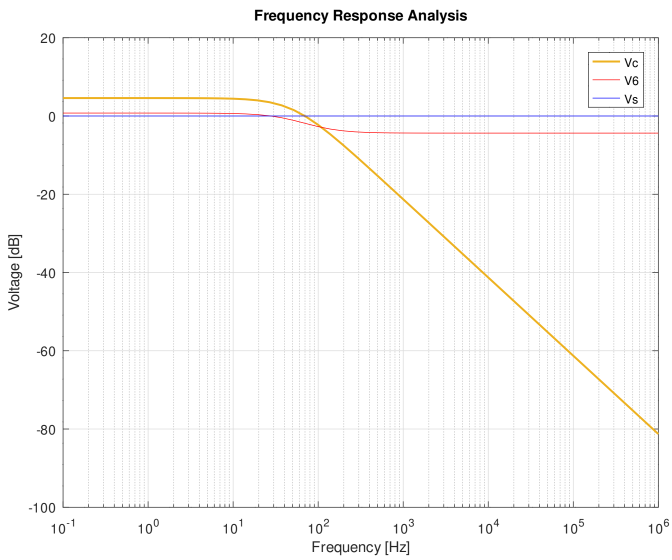

Figure 7: Theoretical Amplitude Response

Note that since the amplitude of V_s is independent of the frequency, as expected, its value in decibels remains equal to 0. Since the RC circuit acts as a low-pass filter[1] its voltage drop remains almost constant until a certain turning point. This turning point is denominated the cut-off frequency, and in this case its value is:

$$f_{CO} = \frac{1}{2\pi R_{eq} C}$$

From this value on, the amplitude of the voltage drop in the capacitor decreases exponentially, denoted by the linear decrease on the logarithmic scale plot.

For the *Ngspice* simulation, we do the same kind of analysis, varying the frequency of the AC current source from 0.1Hz to 1MHz, giving off the following results:

[1] A low-pass filter allows low frequencies to *pass* while *cutting off* high frequencies

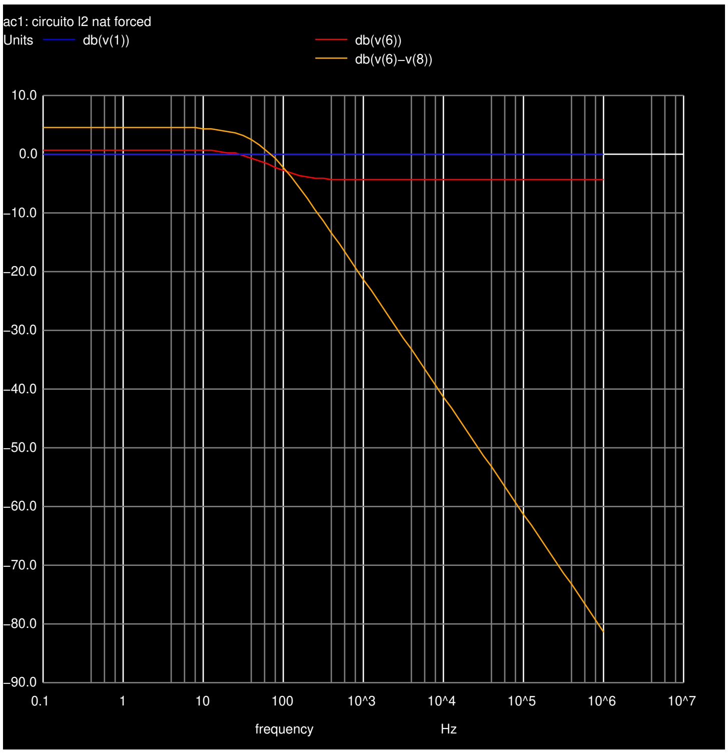

Figure 8: Simulation Amplitude Response

Once again, the results can be compared to confirm an excellent similarity.

Regarding the phases, we have plotted both analysis displayed in Figures 9 and 10. The x-label is a logarithmic scale of the frequency as in the previous plots, but now the y-label is a degree angle scale.

It is interesting to analyse the variation of phase in both V_c and V_6, as the frequency of the input signal increases. For extremely low frequencies, the AC signal is almost DC. The impedance of the capacitor is therefore, tending to infinity, which is equivalent to say, that V_c branch is open-circuted. The expected phase diference between voltages at the capacitor and the voltage source is zero ($\phi_S - \phi_C = 0$). On the other hand, if we take extremely high frequencies, one should expect the capacitor impedance to go to 0. The branch becomes "short-circuited" and it is expectable that the voltage at the capacitor are completely out of phase, not keeping up with the changes at the voltage source. Bear in mind that because $i = C\frac{dv}{dt}$, if the current through the resistor is extremely high, the change of V_c with respect to time becomes high as well.

For the final two graphs, as observed below, there are no significant differences between the simulation and the theory.

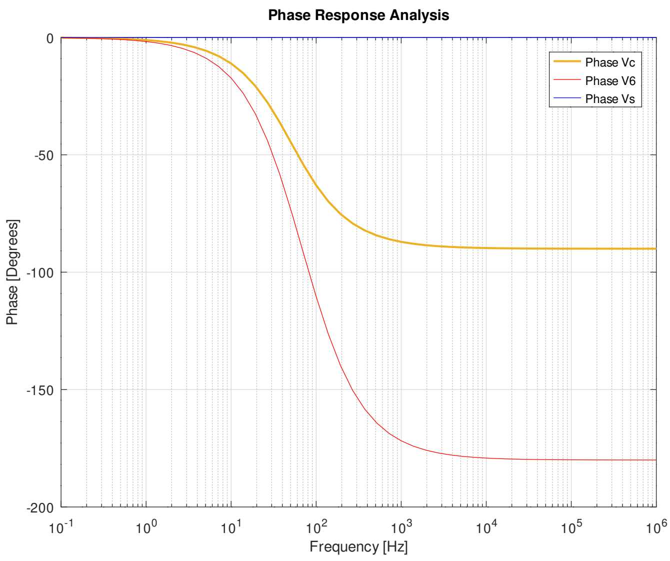

Figure 9: Theoretical Phase Response

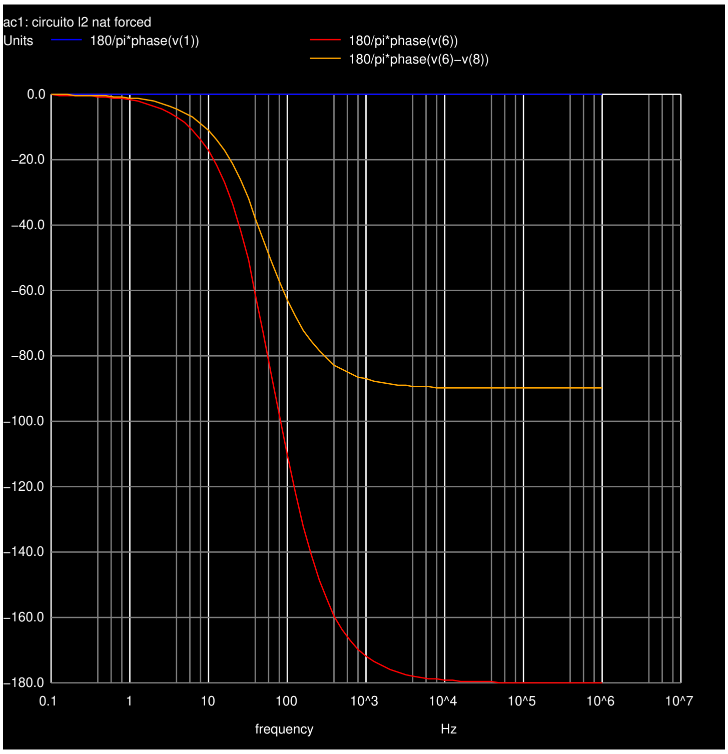

Figure 10: Simulation Phase Response

3 Final Conclusion and General Notes

As a conclusion, we can state that there is a major degree of similarity between both analysis. This was expected due to the fact that the circuit is linear and that the overall component complexity is reduced (in fact, this circuit belongs to one of the simplest circuit categories one can have - a 1st order forced circuit). The model used by *Ngspice* is almost entirely equal to the one we used on the theoretical analysis. This was the main reason as to why we were able to obtain near-zero errors, related only to the approximations both tools had to make.

Although difficult to conceptualise, the understanding of the effects studied in this laboratory was greatly aided by the use of the simulation tool. Seeing what was expected to happen was able to give some insights as to how some of the variables intertwined. The graphs were also a great tool to visualize what was happening. Some concepts as the **filter** were better understood by examining the frequency response of the capacitor. Another important notion was the understanding of **charge/discharge** on a capacitor.

In conclusion, it was an extremely important step, if not a necessary one, to deepen the knowledge on these types of circuits, in particular, a RC one.