TÉCNICO LISBOA

CIRCUIT THEORY AND ELECTRONICS FUNDAMENTALS

[MEAER]

INTEGRATED MASTER'S DEGREE IN AEROSPACE ENGINEERING

LABORATORY 4

BJT AMPLIFIER

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1 Introduction

In this laboratory, we analysed in a theoretical approach as well as using software simulation, an Amplifier made of Bipolar Junction Transistors. It was composed of two different stages: a Gain Stage (with the objective of having the maximum gain possible, as we'll discuss in greater detail) and an Output Stage (whose objective is to lower the impedance of the Amplifier, to allow a better connection to the Load). In this report, a software simulation and theoretical analysis will be stacked up against each other. This assignment allowed us to deal with important concepts such as **BJTs Transistors** and its diverse utility in circuits. In Figure **??** the stated circuit is presented.

A theoretical analysis of the circuit will be presented combining Operating Point (DC), which allows us to derive important values for the incremental analysis (AC). Also, regarding BJTs it is important to notice that there were used two different models, both of them by Philips: BC557A (PNP) and BC547A (NPN).

Simultaneously, the circuit is analysed by computational simulation tools, via *Ngspice*, and the results are compared to the theoretical results obtained, in Section 2. The conclusions of this study are outlined in Section 4.

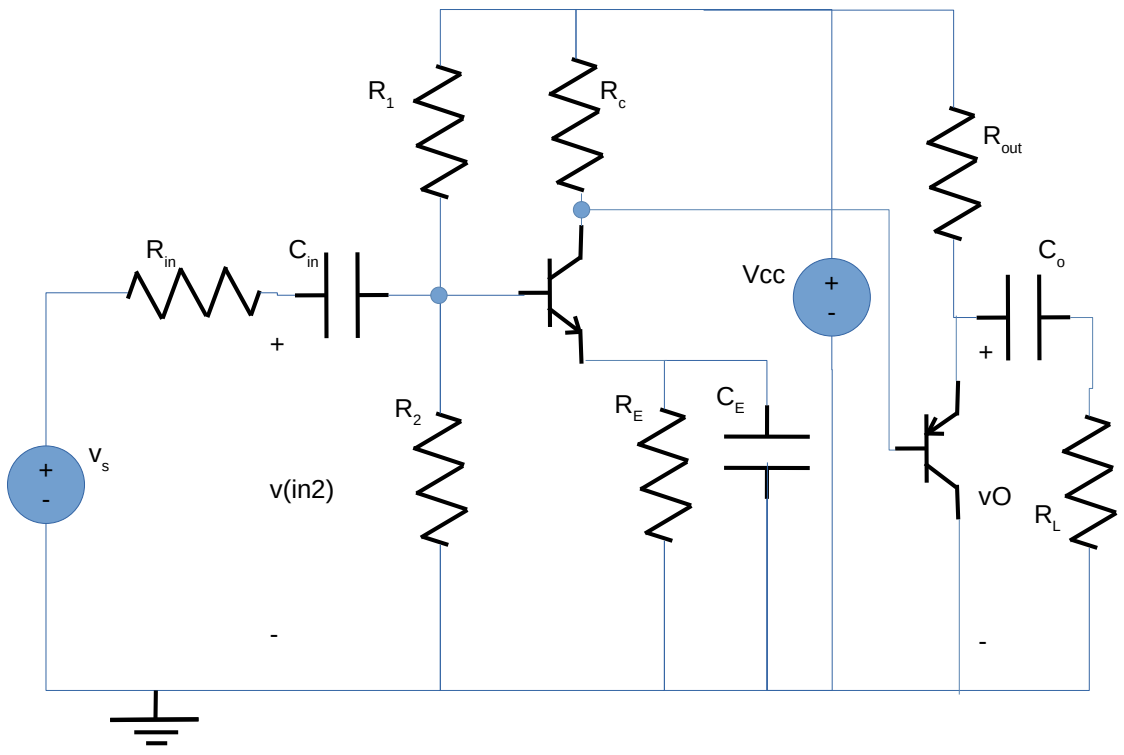


Figure 1: BJT Amplifier

2 Theoretical and Simulation Analysis

In order to compare *side by side*, we'll discuss the theoretical and simulation analysis at the same time.

However, one has to present and analyse the two stages in order to fully understand the simulation. The constants values used are expressed in the table below.

Name	Value	Units
R_1	33.7	$k\Omega$ [kOhms]
R_2	3.6	$k\Omega$ [kOhms]
R_C	3.8	$k\Omega$ [kOhms]
R_E	200	Ω [Ohms]
R_{out}	400	Ω [Ohms]
C_{in}	800	μF [μFarads]
C_E	800	μF [μFarads]
C_o	600	μF [μFarads]

Table 1: Constants Values

2.1 Gain Stage

Firstly, we must discuss the first half of the circuit that was used. Its goal is to ensure a high input voltage so the input signal is not degradated or distorted throughout the circuit. It also has an elevated gain associated, so this is the part that is responsible for the signal amplification.

A scheme of this circuit is presented below.

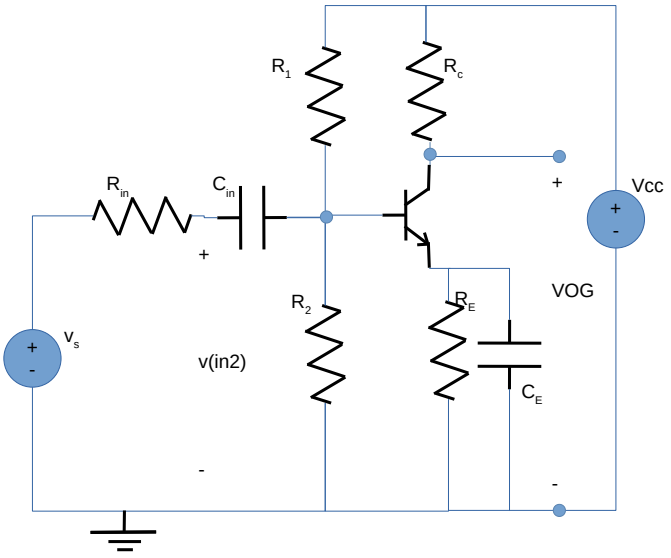


Figure 2: Gain Stage

As one can see, there are 3 types of elements: a NPN BJT, resistors and capacitors.

The first capacitor, C_{in}, is a coupling capacitor, as it acts as a DC Block, so that V_{in} doesn't impose a DC component of 0, that would change the OP of the transistor.

The second capacitor, C_E, acts as a bypass capacitor, for it ensures that for low frequencies all the current flows through R_E, and for high frequencies, it passes through the capacitor.

Generally, the output impedance of this stage (Z_{O1}) is high, when compared with the load, being the major reason why one cannot use just this stage, and we need another one.

2.2 Output Stage

As we could see in the previous section, the Gain Stage has a high Z_{O1}. For that reason, we connect a second circuit to the output of the Gain Stage, that presents a low output impedance.

A scheme of this stage is presented below,

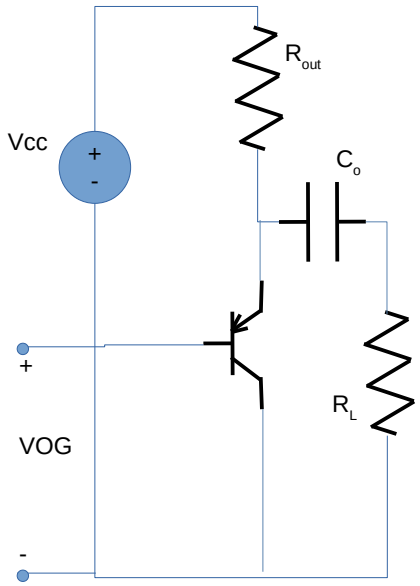


Figure 3: Output Stage

As one can see, this circuit presents similar components, however, with mild differences.

Instead of a NPN BJT, we use a PNP BJT, because it has a higher β_F, which lowers the output impedance (which is what we want). Besides, it illustrates the use of another BJT transistor.

Another capacitor, C_o, is used with a similar goal as the previous coupling capacitor. If we didn't use such component, the gain stage would impose a DC voltage of 0 to the second stage, which would ruin the transistor's OP.

As we'll see, we end up with a lower output impedance in this stage (when compared to the load) and a higher input impedance (when compared to the output impedance of the gain stage).

When combining both stages, we need to ensure that there is a compatibility between the impedances. In fact, by the voltage divider law, to make sure no voltage signal is lost, the input impedance of the second stage should be much greater than the output impedance of the first one.

In conclusion, when we merge these two circuits, we end up with our BJT Amplifier as seen in Figure 1.

2.3 Theoretical Analysis

Firstly, it is important to run an OP analysis of the circuit in order to compute the voltage drops within each of the transistors to ensure they are operating in the forward active region (FAR). To confirm this, the voltages between the emitter and collector as well as between emitter and base (for each of the transistors) were calculated and compared, confirming FAR as seen in the tables below:

Name	Value
V(CE)	3.641357
V(BEON)	0.700000
V(CE) greater than V(BEON)	Yes

Table 2: NPN voltages and FAR confirmation

Name	Value
V(EC)	4.761510
V(EBON)	0.700000
V(EC) greater than V(EBON)	Yes

Table 3: PNP voltages and FAR confirmation

As we can see, since V(CE) is greater than V(BEON), (as well as V(EC) with V(EBON)), the forward active region is confirmed for each of the transistors, meaning it's safe to operate in these conditions.

As we'll be able to see in section 2.4, the theoretical and simulation results match up considerably well, not only at checking the FAR but also when comparing the values.

2.3.1 Impedances

On the Theoretical side, we will evaluate the four impedances associated with the two stages (Z_{I1}, Z_{O1}, Z_{I2} and Z_{O2}) as well as the two gains associated with each stage (A_{V1} and A_{V2}). To do so, we need to perform an Operating Point Analysis to find the values necessary for the Incremental Analysis.

Regarding the first stage (Gain Stage), the input and output impedances ($\{Z_{I1}$, $Z_{O1}\}$, respectively) can be derived by KVL and KCL, leading us to the following expressions:

$$Z_{I1} = R_B // r_{\pi 1} \tag{1}$$

where $R_B = R_1 // R_2$.

Because of the presence of the bypass capacitor and also because in this theorectical approach it is assumed the capacitors are short-circuited (high-frequency analysis), $R_E \simeq 0$. This first stage input impedance matches also with the total input impedance of the circuit, as this stage is load-independent.

On the other hand, the first stage output impedance can be obtained by:

$$Z_{O1} = r_o // R_C \tag{2}$$

Regarding the second stage, by analysing the circuit we get:

$$Z_{I2} = \frac{(g_{m2} + g_{\pi 2} + g_{o2} + g_{E2})}{g_{\pi 2}(g_{\pi 2} + g_{o2} + g_{E2})} \tag{3}$$

$$Z_{O2} = \frac{1}{(g_{m2} + g_{\pi 2} + g_{o2} + g_{E2})} \tag{4}$$

And finally, the total output impedance:

$$Z_{OT} = \frac{v_o}{i_o} = \frac{1}{g_{o2} + g_{m2}\frac{r_{\pi 2}}{r_{\pi 2}+Z_{O1}} + g_{E2} + \frac{1}{r_{\pi 2}+Z_{O1}}} \tag{5}$$

The 4 values are presented below,

Impedances	**Ohms (Ω)**
Z_{I1}	1290.209759
Z_{O1}	3411.452239
Z_{I2}	37245.135442
Z_{O2}	1.375831
Z_{OT}	15.566019

Table 4: Theoretical Impedances

As a result of the compromise between the cost and overall performance, the total output impedance was unpurposely sacrified, which is of course not what we would desire (especially because the speaker impedance is 8 Ω).

As one can see, regarding the compatibility between both stages (remembering that Z_{O1} needs to be much lower than Z_{I2}), we have pretty satisfactory results. This is needed so that there is no signal degradation or loss between these stages. It's clear that V_{in2} needs to be as close as possible to V_{O2}, confirmed if we apply a voltage divider with $Z_{I2} >> Z_{O1}$:

$$V_{in2} = \frac{Z_{I2}}{Z_{I2} + Z_{O1}} V_{O2}. \tag{6}$$

2.3.2 Gain

In order to calculate the total gain (A_V) we performed a simple multiplication, so that we have $A_V = A_{V1}A_{V2}$. Although being an approximation, the real interaction between both stages is negligible, and because of that we can compute the gain as if it was the total gain of both separate stages.

We present a compilation of the values below,

Gain	**Value**
G_1	-264.565721
G_2	0.991532
G_T	-252.275561
$G_{T_{dB}}$	48.037504

Table 5: Theoretical upper gain bound results

Gain	**Value**
G_1	-17.126226
G_2	0.991532
G_T	-16.330643
$G_{T_{dB}}$	24.260066

Table 6: Theoretical lower gain bound results

Note that the first approximation considers C_E to be short-circuited and the second one that C_E behaves as an open circuit. The simulation results should bear within these two boundaries (as they actually do, see table 10) since the capacitor is never either *SC* or *OC*. These bounds as well as an approximation for the real gain will be plotted in Section 2.5.

In order to acquire a better comparison between theory and simulation, besides this aproach, that considers the gain to be constant through all the frequencies , we also performed the *Time constant method* for the lower cut-off frequency.

We calculate the lower cut-off frequency ($\omega_L = 2\pi f_{CO_L}$) as,

$$\omega_L = 1/R_{eq_i}C_i + 1/R_{eq_e}C_e + 1/R_{eq_o}C_o \implies f_{CO_L} = 2\pi w_L \tag{7}$$

where $R_{eq} \equiv$ equivalent resistor as seen by each capacitor when the others are short-circuits.

We have,

$$R_{eq_{in}} = R_{in} + Z_{I1} \tag{8}$$

$$R_{eq_e} = R_E//(\frac{1}{\frac{1}{R_s||R_B+r_\pi} + \frac{g_m r_\pi}{R_s||R_B+r_\pi}}) \simeq R_E//(\frac{r_\pi + R_s||R_B}{r_\pi}\frac{1}{g_m}) \simeq 1/g_m \tag{9}$$

$$R_{eq_o} = R_L + Z_O \tag{10}$$

One could also do the reciprocal, but with the capacitors as open circuits in order to determine the higher cut-off frequency. Like that, we just have to consider as approximation, a slope of $+20dB/dec$, until f_{CO_L} is reached (which gives a better approximation than the constant gain one).

The theoretical value of the lower cut-off frequency is presented in the table below and will be better analysed and compared in Section 2.5.

Name	**Value [Hz]**
Lower CO freq	28.296662

Table 7: Theoretical Lower Cut-off frequency

2.4 Simulation Analysis

On the Simulation Side, we are interested in the two impedances associated with the circuit as a whole (Z_I and Z_O), both cut-off frequencies (f_{CO_L} and f_{CO_H}), the bandwidth (interval between the cut-off frequencies) and the total gain (A_V) measured in the bandpass region. The measurement of these parameters and the overall performance of the circuit is outlined in 3.

We also confirm whether the BJTs are on the Forward Active Region (FAR), by comparing V_{CE} and V_{BE} for the NPN (and, analogously, V_{EC} and V_{EB} for PNP).

The confirmation is presented below:

Name	Value
V(CE)	3.41849
V(BE)	0.667515
V(CE) greater than V(BE)	Yes

Table 8: NPN voltages and FAR confirmation

Name	Value
V(EC)	4.59901
V(EB)	0.730487
V(EC) greater than V(EB)	Yes

Table 9: PNP voltages and FAR confirmation

Regarding the results obtained, we present them in the table below:

Name	Value	Units
Gain (dB)	36.1292	dB
Gain	63.8749	
Lower CO Freq	19.9157	Hz
Higher CO Freq	1.37412E+06	Hz
Bandwidth	1.3741E+06	Hz

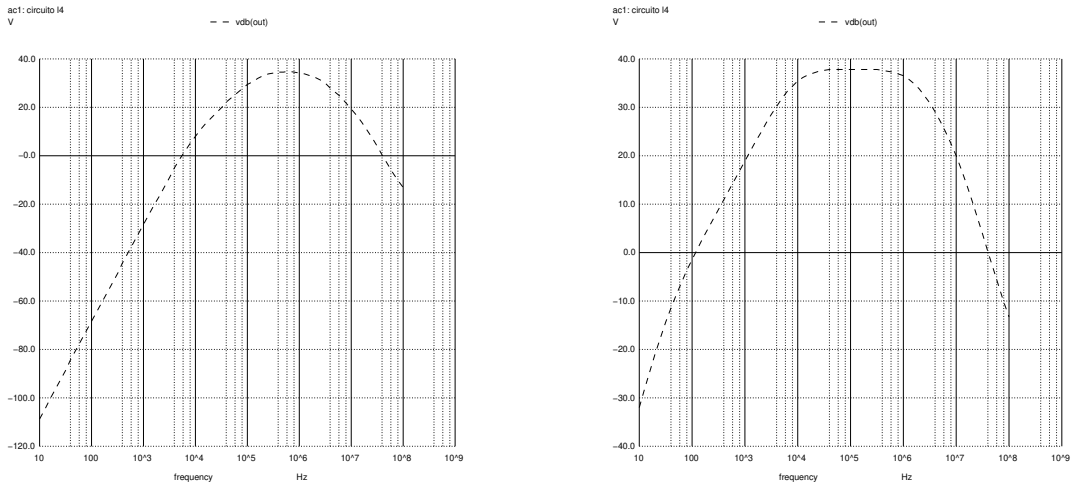
Table 10: Simulation results

These results are to be explained and compared to the theoretical approach further into the report. But as quick note, we can see, as previously mentioned, that the value of the Gain, in dB, is within the theoretical boundaries prediction.

2.4.1 Coupling Capacitors

The understanding of the Coupling Capacitors' behaviour is crucial in order to analyse this circuit. In our BJT amplifier circuit there are two coupling capacitors (C_O and C_{in}) but, since their functions are analogous, we shall focus on the capacitor C_{in}.

Below, we present 2 figures of the frequency response analysis, just by changing the parameter C_{in} in a drastical way.



(a) C_i low ($1nF$) (b) C_i high ($1F$)

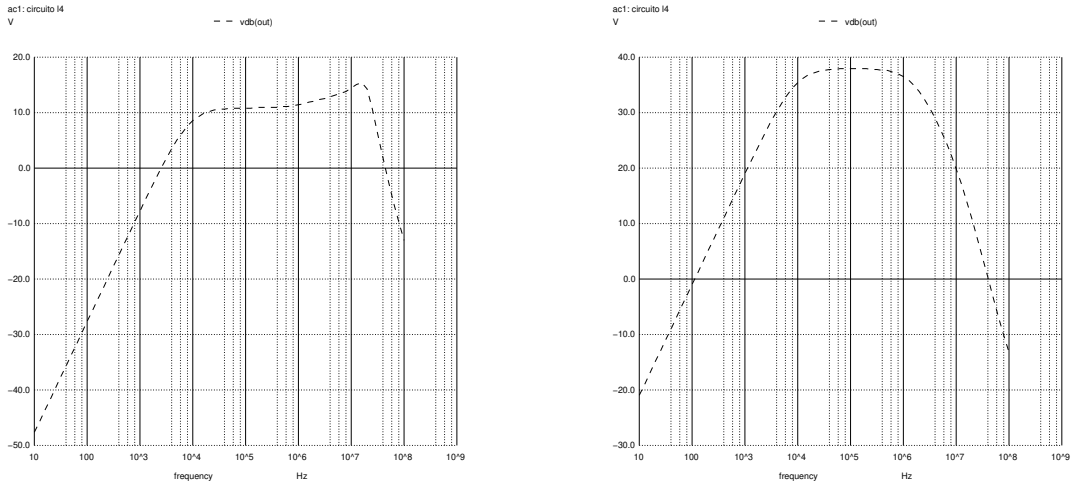
Figure 4: C_{in} influence

As one can realise, the increase of the capacitance *pushes* the cutoff frequency to the left, anticipating it, without changing the higher cut-off frequency, which leads to a larger bandwidth (desired).

This is not surprising because, as discussed previously, as $\omega \to 0$, $Z(C_{in}) \to \inf$, so this capacitor prevents the transistor from entering on either the saturation or cut-off regions, by blocking the DC component of the AUDIO IN source, as previously discussed. This helps mantaining the OP of the transistor, so that it can operate at lower frequencies, as C_{in} increases.

2.4.2 Bypass Capacitor

Below, we present 2 figures of the frequency response analysis, just by changing the parameter C_E.



(a) Low C_E effect on Gain ($1nF$) (b) High C_E effect on Gain ($1F$)

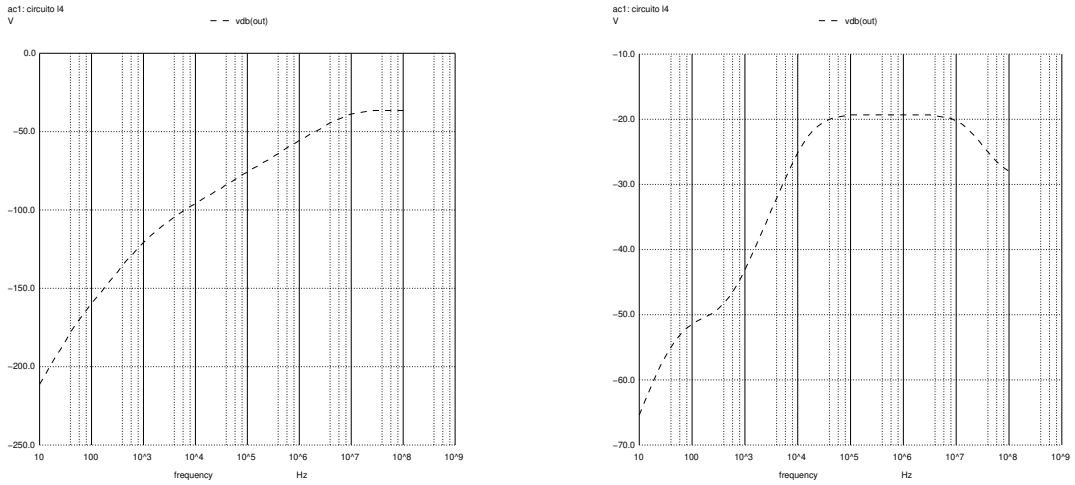
Figure 5: C_E influence

Besides that, by placing the bypass capacitor in parallel with R_E, this resistor becomes short for medium and high frequencies - remember the capacitor impedance is $\frac{1}{j\omega C}$. Because the amplifier's first stage gain is inversely dependent on this resistance, the bypass capacitor plays an extremelly important role in maximizing the gain for medium and high frequencies.

2.4.3 R_C

Finally, it is relevant to analyse the influence of R_C on the total Gain of the circuit.

We also present assymptotical situations in order to fully understand that behaviour.



(a) Low R_C effect (on the Gain) (10Ω)

(b) High R_C effect on Gain ($10k\Omega$)

Figure 6: R_C influence (on the Gain)

As one can see, not only the gain increases with R_C but also *antecipates* the passband. This behaviour was already previewed by the theorectical anlysis on the gain, as it is proportional to R_C. Note that for extremely large resistance, a bizarre and slightly unpredictable behaviour occurs.

Moreover, it is important, in order to guarantee a high compatibility with AUDIO IN and speakers, to simulate the input and output impedances of the circuit. This good compatibility is ensured with a very high input impedance (Z_I) and a very low output impedance (Z_O). The simulation results are expressed in the following tables:

Name	**Value [Ω]**
Input Imp	-1233.56 + 277.901 j
Absolute Value	1264.47

Table 11: Simulation Input Impedance

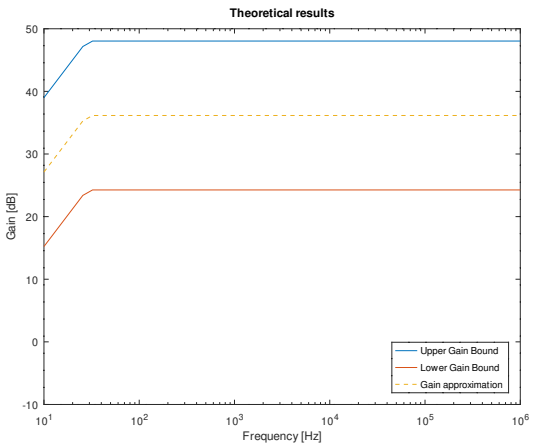
Name	**Value [Ω]**
Output Imp	21.8078 + 0.737428 j
Absolute value	21.8203

Table 12: Simulation Output Impedance

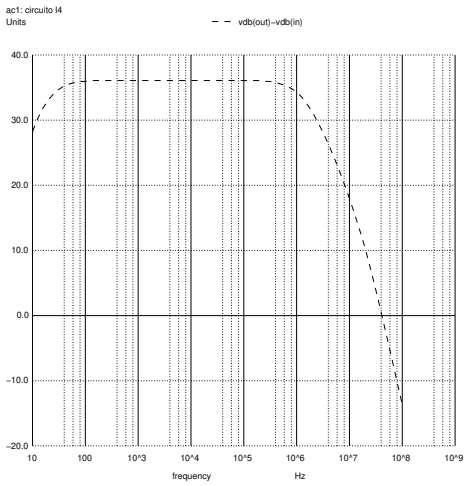
As with the theoretical analysis, this simulation also gives off a slightly high output inpedance (which should ideally be lower than the load's 8 Ω). As stated this fact results from the compromise needed for the merit figure.

2.5 Comparison

We are now ready to make a global comparison of the two approaches, with the chosen values for the constants. Below, we present both the theoretical and simulation graphs of the gain:



(a) Theoretical Gain



(b) Simulation Gain

Figure 7: Gain

In this case, the comparison of the shape can only be done on the left side, since we don't have the theoretical higher cut-off frequency. For this reason, there's no point in plotting the theoretical gain any further than $1MHz$.

One should bear in mind that the theorectical analysis either considers the capacitors are short-circuited or are open-circuited (this approximation is made when for this analysis, the value of R_E is either 0 or R_E in Table 1, respectively). For this reason, two estimates were made (Figure 7) - in blue the capacitors are considered short-circuited; in orange the capacitors are considered open-circuited; in yellow dashed it is represented the medium-value plot, that can be considered as a rough approximation of the real gain. This theorectical approach does not guarantee a specific value for the overall gain, however it gives us a region of acceptable gains. The simulation gain obtained is satisfyingly in this prediction region.

The overall shape of the graphs is similar, noting that the theoretical one can be thought of as assymptotical rather than a precise approach. In fact, as we imposed its shape, accordingly to the one given by *Ngspice*, it is not sensible to variations that might occur (as the appearance of a *second step* in 6b).

In a greater detail analysis, when remembering the values presented in the previous subsections - Z_I and Z_O, A_v and f_{CO_L} -, despite the obvious differences, the comparison is satisfactory. Comparing the order of magnitude, when putting values side by side, they are within reasonable intervals of similarity. In fact, the lower cut-off frequencies (from tables 7 and 10) are really close, especially when you remember they are to be plotted in a logscale graph.

In conclusion, the theoretical approach gives a rough perspective of the overall work conditions of the amplifier, which is good in a first *sketch*.

3 Merit Results

From the results obtained through the Ngspice simulation (see Section 2.5) and considering we used the data shown in Section 1, we can compute the price and the merit using the *formulae* given in the lab assignment:

Name	Value
price	2242.01
merit	1965.69

Table 13: Total Price and Merit

For our strategy, we opted to firstly understand what each component would produce when its values changed dramatically . So we analysed the circuit *assymptotically* in order to acquire a bigger picture of the influence of each component.

After understanding that, we then made small adjustments to further perfect our results, which in turn made the merit figure rise. In this approach, we left the cost as a second thought.

To conclude, we began decreasing the cost until we found out the perfect compromise for us, giving the results shown in table 13.

4 Final Conclusion and General Notes

As a conclusion, we can state that, alike the previous lab assignment, there is not a major degree of similarity between both analysis, in terms of precision. This was expected due to the fact that the circuit is non-linear and the model used by *Ngspice* is far more complex than the theoretical model used - the Incremental Analysis one, presented on classes, only includes 2 resistors and a dependent current source. Despite these differences, as previously discussed, the theoretical model gives an overview of the behaviour, so it is useful when we don't have any simulation tools available or even to quickly verify the simulation results obtained.

With all this in mind, this laboratory enabled us to deepen our knowledge regarding BJTs and how they can be implemented to develop circuits with various purposes - in our case, an AUDIO Amplifier, even thought the real model amplifiers are far more complex than the circuit implemented, achieving gains of around 115 dB. Besides, we used new concepts such as the *Time constant method*, the incremental models, the input and output impedances and the gain (these, eventhough already familiar, allowed us to gain flexibility and easiness).

Regarding our results, especially the simulation ones, the main goal was to have a high gain and a large enough bandwidth that would cover at least 20Hz to 20kHz, since this is the human hearing range. We can state that we obtained results that more than cover said range and would be suitable for a real audio amplifier. Given that, one possible improvement to our circuit would be to increase the gain even more, which we were not able to do.