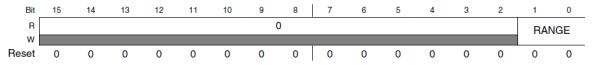
1. Clock Frequency after Reset on S32K144 Cortex M4F

Clock divider values after reset [1]

The default configuration out of reset has the CPU clocked by the Fast IRC (FIRC_CLK). The clocks (for example, CORE_CLK, FLASH_CLK, and BUS_CLK) are configured in the SCG module (see Memory Map/Register Definition).

Fast IRC Configuration Register (SCG_FIRCCFG)



SCG_FIRCCFG field descriptions

Field	Description
31–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
RANGE	Frequency Range
	See chip-specific information for supported frequency ranges.
>	00 Fast IRC is trimmed to 48 MHz
	01 Fast IRC is trimmed to 52 MHz
	10 Fast IRC is trimmed to 56 MHz
	11 Fast IRC is trimmed to 60 MHz

2. Code

At the moment to initialize Systick interrupt: Period is 20.8333ns (assuming FIRC @ 48 MHz clock) Maximum is 2^24-1 = 16777215 = 16,777215 e+6 Minimum is determined by length of ISR

SysTick_Init(16000000); period value sets busy wait count to 16 000 000

```
Tick(T) = 20.8333ns
Maximum Reload value (MRV)= RVR-1 = 16 000 000 -1 = 15 999 999
```

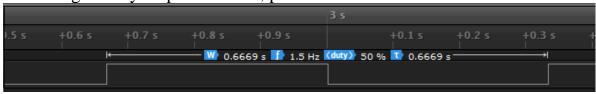
The periodic Systick_Handler is asserted as calculated below:

```
Systick(ISR) = Tick(T) * (RVR-1)
= (20.8333ns)(15 999 999) = 0,3333327791667s
```

3. Measurements

• Utilized board: S32K144 EVB.

Saleae logic analyzer put on J6-01, port PD0.



```
T = 0.6669s
T/2 = 0.3334
```

4. Reference:

[1] NXP STAFF Document Number: S32K1XXRM Rev. 6, 12/2017