ICM45686 eMD driver

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Chapter 1

Overview

1.1 Introduction

This documentation aims at guiding user into using the eMD driver. The driver is divided into several modules, each having a specific purpose:

- **Transport**: Abstraction layer to communicate with device.
- **Basic Driver**: Basic API to drive the device.
- **Driver Advanced**: High-level API for advanced functionalities.
- **EDMP**: API to drive eDMP features.
- **EDMP Wearable**: API to drive eDMP Wearable features such as B2S.
- **SELFTEST**: API to execute self-test procedure.

Chapter 2

Deprecated List

Member inv_imu_serif_type_t

Kept for retrocompatibility. Replaced with `uint32_t` type in `inv_imu_transport_t` struct.

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Chapter 5

File Index

5.1 File List

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Chapter 6

Module Documentation

6.1 Defs

Registers and driver-related definitions and descriptions.

Files

- file inv_imu_defs.h

Classes

- struct inv_imu_sensor_data_t

  Sensor data from registers.
- union fifo_header_t

  Describe the content of the FIFO header.
- union fifo_comp_header_t

  Describe the content of the FIFO header for compressed packets.
- union fifo_header2_t

  Describe the content of the second FIFO header.
- union fifo_comp_decode_t

  Describe the content of the FIFO Compression Decoding Tag.
- struct fifo_configx_t

  Required registers to configure FIFO.
- struct intx_configx_t

  Required registers to configure interrupts.
- struct intx_statusx_t

  Registers to retrieve interrupts status.
- struct inv_imu_int_pin_config_t

  Interrupts pin configuration.

Macros

- #define INV_IMU_OK 0

  Success.
- #define INV_IMU_ERROR -1

  Unspecified error.
- #define INV_IMU_ERROR_TRANSPORT -3

  Error occurred at transport level.
- #define INV_IMU_ERROR_TIMEOUT -4

  Action did not complete in the expected time window.
- #define INV_IMU_ERROR_BAD_ARG -11

  Invalid argument provided.
- #define INV_IMU_ERROR_EDMP_ODR -126

  EDMP ODR decimator reconfiguration is needed.
- #define INV_IMU_ERROR_EDMP_BUF_EMPTY -127

  EDMP buffer is empty.
- #define INV_IMU_DISABLE (0U)
- #define INV_IMU_ENABLE (1U)
- #define ACC_STARTUP_TIME_US 10000
- #define GYR_STARTUP_TIME_US 70000
- #define ACCEL_DATA_SIZE 6
- #define GYRO_DATA_SIZE 6
- #define TEMP_DATA_SIZE 2
- #define FIFO_HEADER_SIZE 1
- #define FIFO_TEMP_DATA_SIZE 1
- #define FIFO_TS_FSYNC_SIZE 2
- #define FIFO_TEMP_HIGH_RES_SIZE 1
- #define FIFO_ACCEL_GYRO_HIGH_RES_SIZE 3
- #define FIFO_ES0_6B_DATA_SIZE 6
- #define FIFO_ES0_9B_DATA_SIZE 9
- #define FIFO_ES1_DATA_SIZE 6
- #define INVALID_VALUE_FIFO ((int16_t)0x8000)
- #define INVALID_VALUE_FIFO_1B ((int8_t)0x80)
- #define OUT_OF_BOUND_TEMP_NEG_FIFO_1B ((int8_t)0x81)
- #define OUT_OF_BOUND_TEMP_POS_FIFO_1B ((int8_t)0x7F)
- #define FIFO_COMP_X2_COMPRESSION 0
- #define FIFO_COMP_X3_COMPRESSION 1
- #define FIFO_COMP_X4_COMPRESSION 2
- #define FIFO_COMP_1_SAMPLE_IN_FRAME 0
- #define FIFO_COMP_2_SAMPLES_IN_FRAME 1
- #define FIFO_COMP_3_SAMPLES_IN_FRAME 2
- #define FIFO_COMP_4_SAMPLES_IN_FRAME 3
- #define INT5_TO_INT8(in) (((in) < 16) ? ((int8_t)(in)) : ((int8_t)(in)-32))

  Converts an integer from a 5-bits signed to a 8-bits signed.
- #define INT4_TO_INT8(in) (((in) < 8) ? ((int8_t)(in)) : ((int8_t)(in)-16))

  Converts an integer from a 4-bits signed to a 8-bits signed.
- #define EDMP_INT_SRC_ACCEL_DRDY_MASK 0x01
- #define EDMP_INT_SRC_GYRO_DRDY_MASK 0x02
- #define EDMP_INT_SRC_EXT_INT_DRDY_MASK 0x04
- #define EDMP_INT_SRC_EXT_ODR_DRDY_MASK 0x08
- #define EDMP_INT_SRC_WOM_DRDY_MASK 0x10
- #define EDMP_INT_SRC_ON_DEMAND_MASK 0x20
- #define TAP_TMAX_400HZ 198

- #define TAP_TMAX_800HZ 396
- #define TAP_TMIN_400HZ 66
- #define TAP_TMIN_800HZ 132
- #define TAP_SMUDGE_REJECT_THR_400HZ 34
- #define TAP_SMUDGE_REJECT_THR_800HZ 68
- #define STC_RESULTS_ACCEL_X_MASK 0x0001
- #define STC_RESULTS_ACCEL_Y_MASK 0x0002
- #define STC_RESULTS_ACCEL_Z_MASK 0x0004
- #define STC_RESULTS_GYRO_X_MASK 0x0008
- #define STC_RESULTS_GYRO_Y_MASK 0x0010
- #define STC_RESULTS_GYRO_Z_MASK 0x0020
- #define STC_RESULTS_ST_STATUS_MASK 0x00C0
- #define STC_RESULTS_ACCEL_SC_MASK 0x0300
- #define STC_RESULTS_GYRO_SC_MASK 0x0C00
- #define SELFTESTCAL_INIT_EN_MASK 0x0001
- #define SELFTESTCAL_INIT_EN 0x0001
- #define SELFTESTCAL_INIT_DIS 0x0000
- #define SELFTEST_ACCEL_EN_MASK 0x0002
- #define SELFTEST_ACCEL_EN 0x0002
- #define SELFTEST_ACCEL_DIS 0x0000
- #define SELFTEST_GYRO_EN_MASK 0x0004
- #define SELFTEST_GYRO_EN 0x0004
- #define SELFTEST_GYRO_DIS 0x0000
- #define SELFTEST_AVERAGE_TIME_MASK 0x0380
- #define SELFTEST_ACCEL_THRESH_MASK 0x1C00
- #define SELFTEST_GYRO_THRESH_MASK 0xE000

Enumerations

- enum inv_imu_int_num_t { INV_IMU_INT1 , INV_IMU_INT2 }

  Interrupt number.
- enum pwr_mgmt0_gyro_mode_t { PWR_MGMT0_GYRO_MODE_LN = 0x03 , PWR_MGMT0_GYRO_MODE_LP = 0x02 , PWR_MGMT0_GYRO_MODE_STANDBY = 0x01 , PWR_MGMT0_GYRO_MODE_OFF = 0x00 }
- enum pwr_mgmt0_accel_mode_t { PWR_MGMT0_ACCEL_MODE_LN = 0x03 , PWR_MGMT0_ACCEL_MODE_LP = 0x02 , PWR_MGMT0_ACCEL_MODE_OFF = 0x00 }
- enum intx_config2_intx_drive_t { INTX_CONFIG2_INTX_DRIVE_PP = 0x00 , INTX_CONFIG2_INTX_DRIVE_OD = 0x01 }
- enum intx_config2_intx_mode_t { INTX_CONFIG2_INTX_MODE_PULSE = 0x00 , INTX_CONFIG2_INTX_MODE_LATCH = 0x01 }
- enum intx_config2_intx_polarity_t { INTX_CONFIG2_INTX_POLARITY_LOW = 0x00 , INTX_CONFIG2_INTX_POLARITY_HIG = 0x01 }
- enum accel_config0_accel_ui_fs_sel_t { ACCEL_CONFIG0_ACCEL_UI_FS_SEL_2_G = 0x4 , ACCEL_CONFIG0_ACCEL_UI = 0x3 , ACCEL_CONFIG0_ACCEL_UI_FS_SEL_8_G = 0x2 , ACCEL_CONFIG0_ACCEL_UI_FS_SEL_16_G = 0x1 }
- enum accel_config0_accel_odr_t { ACCEL_CONFIG0_ACCEL_ODR_1_5625_HZ = 0xF , ACCEL_CONFIG0_ACCEL_ODR_3_125_HZ = 0xE , ACCEL_CONFIG0_ACCEL_ODR_6_25_HZ = 0xD , ACCEL_CONFIG0_ACCEL_ODR_12_5_HZ = 0xC , ACCEL_CONFIG0_ACCEL_ODR_25_HZ = 0xB , ACCEL_CONFIG0_ACCEL_ODR_50_HZ = 0xA , ACCEL_CONFIG0_ACCEL_ODR_100_HZ = 0x9 , ACCEL_CONFIG0_ACCEL_ODR_200_HZ = 0x8 , ACCEL_CONFIG0_ACCEL_ODR_400_HZ = 0x7 , ACCEL_CONFIG0_ACCEL_ODR_800_HZ = 0x6 , ACCEL_CONFIG0_ACCEL_ODR_1600_HZ = 0x5 , ACCEL_CONFIG0_ACCEL_ODR_3200_HZ = 0x4 , ACCEL_CONFIG0_ACCEL_ODR_6400_HZ = 0x3 }

- enum gyro_config0_gyro_ui_fs_sel_t { GYRO_CONFIG0_GYRO_UI_FS_SEL_15_625_DPS = 8 , GYRO_CONFIG0_GYRO_UI_FS_SEL_31_25_DPS = 7 , GYRO_CONFIG0_GYRO_UI_FS_SEL_62_5_DPS = 6 , GYRO_CONFIG0_GYRO_UI_FS_SEL_125_DPS = 5 , GYRO_CONFIG0_GYRO_UI_FS_SEL_250_DPS = 4 , GYRO_CONFIG0_GYRO_UI_FS_SEL_500_DPS = 3 , GYRO_CONFIG0_GYRO_UI_FS_SEL_1000_DPS = 2 , GYRO_CONFIG0_GYRO_UI_FS_SEL_2000_DPS = 1 }
- enum gyro_config0_gyro_odr_t { GYRO_CONFIG0_GYRO_ODR_1_5625_HZ = 0xF , GYRO_CONFIG0_GYRO_ODR_3_125_HZ = 0xE , GYRO_CONFIG0_GYRO_ODR_6_25_HZ = 0xD , GYRO_CONFIG0_GYRO_ODR_12_5_HZ = 0xC , GYRO_CONFIG0_GYRO_ODR_25_HZ = 0xB , GYRO_CONFIG0_GYRO_ODR_50_HZ = 0xA , GYRO_CONFIG0_GYRO_ODR_100_HZ = 0x9 , GYRO_CONFIG0_GYRO_ODR_200_HZ = 0x8 , GYRO_CONFIG0_GYRO_ODR_400_HZ = 0x7 , GYRO_CONFIG0_GYRO_ODR_800_HZ = 0x6 , GYRO_CONFIG0_GYRO_ODR_1600_HZ = 0x5 , GYRO_CONFIG0_GYRO_ODR_3200_HZ = 0x4 , GYRO_CONFIG0_GYRO_ODR_6400_HZ = 0x3 }
- enum fifo_config0_fifo_mode_t { FIFO_CONFIG0_FIFO_MODE_SNAPSHOT = 0x02 , FIFO_CONFIG0_FIFO_MODE_STREAM = 0x01 , FIFO_CONFIG0_FIFO_MODE_BYPASS = 0x00 }
- enum fifo_config0_fifo_depth_t { FIFO_CONFIG0_FIFO_DEPTH_MAX = 0x1E , FIFO_CONFIG0_FIFO_DEPTH_APEX = 0x07 , FIFO_CONFIG0_FIFO_DEPTH_GAF = 0x04 }
- enum fifo_config2_fifo_wr_wm_gt_th_t { FIFO_CONFIG2_FIFO_WR_WM_EQ_OR_GT_TH = 0x1 , FIFO_CONFIG2_FIFO_WR_WM_EQ_TH = 0x0 }
- enum fifo_config4_fifo_comp_nc_flow_cfg_t { FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_EVERY_128_FR = 0x5 , FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_E = 0x4 , FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_EVERY_32_FR = 0x3 , FIFO_CONFIG4_FIFO_COMP_NC_FLOW_C = 0x2 , FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_EVERY_8_FR = 0x1 , FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_DIS = 0x0 }
- enum fifo_config4_fifo_es0_6b_9b_t { FIFO_CONFIG4_FIFO_ES0_9B = 0x1 , FIFO_CONFIG4_FIFO_ES0_6B = 0x0 }
- enum tmst_wom_config_tmst_resol_t { TMST_WOM_CONFIG_TMST_RESOL_16_US = 0x01 , TMST_WOM_CONFIG_TMST = 0x00 }
- enum tmst_wom_config_wom_mode_t { TMST_WOM_CONFIG_WOM_MODE_CMP_PREV = 0x01 , TMST_WOM_CONFIG_WOM_MODE_CMP_INIT = 0x00 }
- enum tmst_wom_config_wom_int_mode_t { TMST_WOM_CONFIG_WOM_INT_MODE_ANDED = 0x01 , TMST_WOM_CONFIG_WOM_INT_MODE_ORED = 0x00 }
- enum tmst_wom_config_wom_int_dur_t { TMST_WOM_CONFIG_WOM_INT_DUR_1_SMPL = 0x00 , TMST_WOM_CONFIG_WOM_INT_DUR_2_SMPL = 0x01 , TMST_WOM_CONFIG_WOM_INT_DUR_3_SMPL = 0x02 , TMST_WOM_CONFIG_WOM_INT_DUR_4_SMPL = 0x03 }
- enum fsync_config0_ap_fsync_sel_t { FSYNC_CONFIG0_AP_FSYNC_NO = 0x0 , FSYNC_CONFIG0_AP_FSYNC_TEMP = 0x1 , FSYNC_CONFIG0_AP_FSYNC_C = 0x2 , FSYNC_CONFIG0_AP_FSYNC_GYRO_Y = 0x3 , FSYNC_CONFIG0_AP_FSYNC_GYRO_Z = 0x4 , FSYNC_CONFIG0_AP_FSYNC_ACCEL_X = 0x5 , FSYNC_CONFIG0_AP_FSYNC_ACCEL_Y = 0x6 , FSYNC_CONFIG0_AP_FSYNC_ACCEL_Z = 0x7 }
- enum dmp_ext_sen_odr_cfg_ext_odr_t { DMP_EXT_SEN_ODR_CFG_EXT_ODR_3_25_HZ = 0x00 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_6_25_HZ = 0x01 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_12_5_HZ = 0x02 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_25_HZ = 0x03 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_50_HZ = 0x04 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_100_HZ = 0x05 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_200_HZ = 0x06 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_400_HZ = 0x07 }
- enum dmp_ext_sen_odr_cfg_apex_odr_t { DMP_EXT_SEN_ODR_CFG_APEX_ODR_25_HZ = 0x00 , DMP_EXT_SEN_ODR_CFG_APEX_ODR_50_HZ = 0x01 , DMP_EXT_SEN_ODR_CFG_APEX_ODR_100_HZ = 0x02 , DMP_EXT_SEN_ODR_CFG_APEX_ODR_200_HZ = 0x03 , DMP_EXT_SEN_ODR_CFG_APEX_ODR_400_HZ = 0x04 , DMP_EXT_SEN_ODR_CFG_APEX_ODR_800_HZ = 0x05 }

- enum odr_decimate_config_gyro_fifo_odr_dec_t {
  ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_1 = 0x0 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_2
  = 0x1 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_4 = 0x2 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_
  = 0x3 ,
  ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_16 = 0x4 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_32
  = 0x5 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_64 = 0x6 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC
  = 0x7 ,
  ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_256 = 0x8 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_512
  = 0x9 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_1024 = 0xA , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_D
  = 0xB ,
  ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_4096 = 0xC }
- enum odr_decimate_config_accel_fifo_odr_dec_t {
  ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_1 = 0x0 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_2
  = 0x1 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_4 = 0x2 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DE
  = 0x3 ,
  ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_16 = 0x4 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_32
  = 0x5 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_64 = 0x6 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_D
  = 0x7 ,
  ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_256 = 0x8 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_5
  = 0x9 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_1024 = 0xA , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_
  = 0xB ,
  ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_4096 = 0xC }
- enum intf_config1_ovrd_ap_spi_34_mode_ovrd_val_t { INTF_CONFIG1_OVRD_AP_SPI_34_MODE_OVRD_VAL_3_WIRE
  = 0x0 , INTF_CONFIG1_OVRD_AP_SPI_34_MODE_OVRD_VAL_4_WIRE = 0x1 }
- enum intf_config1_ovrd_ap_spi_mode_ovrd_val_t { INTF_CONFIG1_OVRD_AP_SPI_MODE_OVRD_VAL_0_OR_3
  = 0x0 , INTF_CONFIG1_OVRD_AP_SPI_MODE_OVRD_VAL_1_OR_2 = 0x1 }
- enum drive_config0_pads_i2c_slew_t { DRIVE_CONFIG0_PADS_I2C_SLEW_TYP_20NS = 0x0 ,
  DRIVE_CONFIG0_PADS_I2C_SLEW_TYP_7NS = 0x2 }
- enum drive_config0_pads_spi_slew_t {
  DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_38NS = 0x0 , DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_14NS
  = 0x1 , DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_10NS = 0x2 , DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_7NS
  = 0x3 ,
  DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_5NS = 0x4 , DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_4NS
  = 0x5 , DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_0_5NS = 0x6 }
- enum ioc_pad_scenario_ovrd_pads_int2_cfg_ovrd_val_t { IOC_PAD_SCENARIO_OVRD_INT2_CFG_OVRD_VAL_INT2
  = 0 , IOC_PAD_SCENARIO_OVRD_INT2_CFG_OVRD_VAL_DRDY_INTR = 3 }
- enum reg_misc1_osc_id_ovrd_t {
  REG_MISC1_OSC_ID_OVRD_OFF = 0x0 , REG_MISC1_OSC_ID_OVRD_EDOSC = 0x1 , REG_MISC1_OSC_ID_OVRD_RC
  = 0x2 , REG_MISC1_OSC_ID_OVRD_PLL = 0x4 ,
  REG_MISC1_OSC_ID_OVRD_EXT_CLK = 0x8 }
- enum fs_sel_aux_gyro_fs_sel_t {
  FS_SEL_AUX_GYRO_FS_SEL_15_625_DPS = 8 , FS_SEL_AUX_GYRO_FS_SEL_31_25_DPS = 7 ,
  FS_SEL_AUX_GYRO_FS_SEL_62_5_DPS = 6 , FS_SEL_AUX_GYRO_FS_SEL_125_DPS = 5 ,
  FS_SEL_AUX_GYRO_FS_SEL_250_DPS = 4 , FS_SEL_AUX_GYRO_FS_SEL_500_DPS = 3 ,
  FS_SEL_AUX_GYRO_FS_SEL_1000_DPS = 2 , FS_SEL_AUX_GYRO_FS_SEL_2000_DPS = 1 }
- enum fs_sel_aux_accel_fs_sel_t { FS_SEL_AUX_ACCEL_FS_SEL_2_G = 0x4 , FS_SEL_AUX_ACCEL_FS_SEL_4_G
  = 0x3 , FS_SEL_AUX_ACCEL_FS_SEL_8_G = 0x2 , FS_SEL_AUX_ACCEL_FS_SEL_16_G = 0x1 }
- enum smc_control_0_accel_lp_clk_sel_t { SMC_CONTROL_0_ACCEL_LP_CLK_RCOSC = 0x01 ,
  SMC_CONTROL_0_ACCEL_LP_CLK_WUOSC = 0x00 }
- enum sreg_ctrl_sreg_data_endian_sel_t { SREG_CTRL_SREG_DATA_BIG_ENDIAN = 0x01 , SREG_CTRL_SREG_DATA_LIT
  = 0x00 }
- enum ipreg_sys1_reg_166_gyro_src_ctrl_sel_t { IPREG_SYS1_REG_166_GYRO_SRC_CTRL_INTERPOLATOR_ON_FIR_O
  = 0x2 , IPREG_SYS1_REG_166_GYRO_SRC_CTRL_INTERPOLATOR_OFF_FIR_ON = 0x1 , IPREG_SYS1_REG_166_GYR
  = 0x0 }
- enum ipreg_sys1_reg_170_gyro_lp_avg_sel_t {
  IPREG_SYS1_REG_170_GYRO_LP_AVG_64 = 0xC , IPREG_SYS1_REG_170_GYRO_LP_AVG_32 = 0xB
  , IPREG_SYS1_REG_170_GYRO_LP_AVG_20 = 0xA , IPREG_SYS1_REG_170_GYRO_LP_AVG_18 =
  0x9 ,

IPREG_SYS1_REG_170_GYRO_LP_AVG_16 = 0x8 , IPREG_SYS1_REG_170_GYRO_LP_AVG_11 = 0x7 , IPREG_SYS1_REG_170_GYRO_LP_AVG_10 = 0x6 , IPREG_SYS1_REG_170_GYRO_LP_AVG_8 = 0x5 ,
IPREG_SYS1_REG_170_GYRO_LP_AVG_7 = 0x4 , IPREG_SYS1_REG_170_GYRO_LP_AVG_5 = 0x3 , IPREG_SYS1_REG_170_GYRO_LP_AVG_4 = 0x2 , IPREG_SYS1_REG_170_GYRO_LP_AVG_2 = 0x1 , IPREG_SYS1_REG_170_GYRO_LP_AVG_1 = 0x0 }

- enum ipreg_sys1_reg_172_gyro_ui_lpfbw_sel_t { IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_128 = 0x06 , IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_64 = 0x05 , IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_32 = 0x04 , IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_16 = 0x03 ,
IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_8 = 0x02 , IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_4 = 0x01 , IPREG_SYS1_REG_172_GYRO_UI_LPFBW_NO_FILTER = 0x00 }
- enum ipreg_sys2_reg_123_accel_src_ctrl_sel_t { IPREG_SYS2_REG_123_ACCEL_SRC_CTRL_INTERPOLATOR_ON_FIR_ = 0x2 , IPREG_SYS2_REG_123_ACCEL_SRC_CTRL_INTERPOLATOR_OFF_FIR_ON = 0x1 , IPREG_SYS2_REG_123_ACC = 0x0 }
- enum ipreg_sys2_reg_129_accel_lp_avg_sel_t { IPREG_SYS2_REG_129_ACCEL_LP_AVG_64 = 0xC , IPREG_SYS2_REG_129_ACCEL_LP_AVG_32 = 0xB , IPREG_SYS2_REG_129_ACCEL_LP_AVG_20 = 0xA , IPREG_SYS2_REG_129_ACCEL_LP_AVG_18 = 0x9 ,
IPREG_SYS2_REG_129_ACCEL_LP_AVG_16 = 0x8 , IPREG_SYS2_REG_129_ACCEL_LP_AVG_11 = 0x7 , IPREG_SYS2_REG_129_ACCEL_LP_AVG_10 = 0x6 , IPREG_SYS2_REG_129_ACCEL_LP_AVG_8 = 0x5 ,
IPREG_SYS2_REG_129_ACCEL_LP_AVG_7 = 0x4 , IPREG_SYS2_REG_129_ACCEL_LP_AVG_5 = 0x3 , IPREG_SYS2_REG_129_ACCEL_LP_AVG_4 = 0x2 , IPREG_SYS2_REG_129_ACCEL_LP_AVG_2 = 0x1 , IPREG_SYS2_REG_129_ACCEL_LP_AVG_1 = 0x0 }
- enum ipreg_sys2_reg_131_accel_ui_lpfbw_t { IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_128 = 0x06 , IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_64 = 0x05 , IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_32 = 0x04 , IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_ = 0x03 ,
IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_8 = 0x02 , IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_4 = 0x01 , IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_NO_FILTER = 0x00 }
- enum selftest_average_time_t { SELFTEST_AVG_TIME_10_MS = 0x0000 , SELFTEST_AVG_TIME_20_MS = 0x0080 , SELFTEST_AVG_TIME_40_MS = 0x0100 , SELFTEST_AVG_TIME_80_MS = 0x0180 ,
SELFTEST_AVG_TIME_160_MS = 0x0200 , SELFTEST_AVG_TIME_320_MS = 0x0280 }
- enum selftest_accel_threshold_t { SELFTEST_ACCEL_THRESHOLD_5_PERCENT = 0x0000 , SELFTEST_ACCEL_THRESHOLD_10_PERCENT = 0x0400 , SELFTEST_ACCEL_THRESHOLD_15_PERCENT = 0x0800 , SELFTEST_ACCEL_THRESHOLD_20_PERCENT = 0x0c00 ,
SELFTEST_ACCEL_THRESHOLD_25_PERCENT = 0x1000 , SELFTEST_ACCEL_THRESHOLD_30_PERCENT = 0x1400 , SELFTEST_ACCEL_THRESHOLD_40_PERCENT = 0x1800 , SELFTEST_ACCEL_THRESHOLD_50_PERCENT = 0x1c00 }
- enum selftest_gyro_threshold_t { SELFTEST_GYRO_THRESHOLD_5_PERCENT = 0x0000 , SELFTEST_GYRO_THRESHOLD_10_PERCENT = 0x2000 , SELFTEST_GYRO_THRESHOLD_15_PERCENT = 0x4000 , SELFTEST_GYRO_THRESHOLD_20_PERCENT = 0x6000 ,
SELFTEST_GYRO_THRESHOLD_25_PERCENT = 0x8000 , SELFTEST_GYRO_THRESHOLD_30_PERCENT = 0xa000 , SELFTEST_GYRO_THRESHOLD_40_PERCENT = 0xc000 , SELFTEST_GYRO_THRESHOLD_50_PERCENT = 0xe000 }
- enum stc_patch_params_t { SELFTEST_PATCH_EN_ACCEL_PHASE1 = 0x0001 , SELFTEST_PATCH_EN_ACCEL_PHASE2 = 0x0002 , SELFTEST_PATCH_EN_GYRO1_PHASE1 = 0x0004 , SELFTEST_PATCH_EN_GYRO1_PHASE2 = 0x0008 }

6.1.1 Detailed Description

Registers and driver-related definitions and descriptions.

6.1.2 Macro Definition Documentation

6.1.2.1 ACC_STARTUP_TIME_US

```
#define ACC_STARTUP_TIME_US 10000
```

6.1.2.2 ACCEL_DATA_SIZE

```
#define ACCEL_DATA_SIZE 6
```

6.1.2.3 EDMP_INT_SRC_ACCEL_DRDY_MASK

```
#define EDMP_INT_SRC_ACCEL_DRDY_MASK 0x01
```

6.1.2.4 EDMP_INT_SRC_EXT_INT_DRDY_MASK

```
#define EDMP_INT_SRC_EXT_INT_DRDY_MASK 0x04
```

6.1.2.5 EDMP_INT_SRC_EXT_ODR_DRDY_MASK

```
#define EDMP_INT_SRC_EXT_ODR_DRDY_MASK 0x08
```

6.1.2.6 EDMP_INT_SRC_GYRO_DRDY_MASK

```
#define EDMP_INT_SRC_GYRO_DRDY_MASK 0x02
```

6.1.2.7 EDMP_INT_SRC_ON_DEMAND_MASK

```
#define EDMP_INT_SRC_ON_DEMAND_MASK 0x20
```

6.1.2.8 EDMP_INT_SRC_WOM_DRDY_MASK

```
#define EDMP_INT_SRC_WOM_DRDY_MASK 0x10
```

6.1.2.9 FIFO_ACCEL_GYRO_HIGH_RES_SIZE

```
#define FIFO_ACCEL_GYRO_HIGH_RES_SIZE 3
```

6.1.2.10 FIFO_COMP_1_SAMPLE_IN_FRAME

```
#define FIFO_COMP_1_SAMPLE_IN_FRAME 0
```

6.1.2.11 FIFO_COMP_2_SAMPLES_IN_FRAME

```
#define FIFO_COMP_2_SAMPLES_IN_FRAME 1
```

6.1.2.12 FIFO_COMP_3_SAMPLES_IN_FRAME

```
#define FIFO_COMP_3_SAMPLES_IN_FRAME 2
```

6.1.2.13 FIFO_COMP_4_SAMPLES_IN_FRAME

```
#define FIFO_COMP_4_SAMPLES_IN_FRAME 3
```

6.1.2.14 FIFO_COMP_X2_COMPRESSION

```
#define FIFO_COMP_X2_COMPRESSION 0
```

6.1.2.15 FIFO_COMP_X3_COMPRESSION

```
#define FIFO_COMP_X3_COMPRESSION 1
```

6.1.2.16 FIFO_COMP_X4_COMPRESSION

```
#define FIFO_COMP_X4_COMPRESSION 2
```

6.1.2.17 FIFO_ES0_6B_DATA_SIZE

```
#define FIFO_ES0_6B_DATA_SIZE 6
```

6.1.2.18 FIFO_ES0_9B_DATA_SIZE

```
#define FIFO_ES0_9B_DATA_SIZE 9
```

6.1.2.19 FIFO_ES1_DATA_SIZE

```
#define FIFO_ES1_DATA_SIZE 6
```

6.1.2.20 FIFO_HEADER_SIZE

```
#define FIFO_HEADER_SIZE 1
```

6.1.2.21 FIFO_TEMP_DATA_SIZE

```
#define FIFO_TEMP_DATA_SIZE 1
```

6.1.2.22 FIFO_TEMP_HIGH_RES_SIZE

```
#define FIFO_TEMP_HIGH_RES_SIZE 1
```

6.1.2.23 FIFO_TS_FSYNC_SIZE

```
#define FIFO_TS_FSYNC_SIZE 2
```

6.1.2.24 GYR_STARTUP_TIME_US

```
#define GYR_STARTUP_TIME_US 70000
```

6.1.2.25 GYRO_DATA_SIZE

```
#define GYRO_DATA_SIZE 6
```

6.1.2.26 INT4_TO_INT8

```
#define INT4_TO_INT8(
              in ) (((in) < 8) ?  ((int8_t)(in)) :  ((int8_t)(in)-16))
```

Converts an integer from a 4-bits signed to a 8-bits signed.

6.1.2.27 INT5_TO_INT8

```
#define INT5_TO_INT8(
              in ) (((in) < 16) ?  ((int8_t)(in)) :  ((int8_t)(in)-32))
```

Converts an integer from a 5-bits signed to a 8-bits signed.

6.1.2.28 INV_IMU_DISABLE

```
#define INV_IMU_DISABLE (0U)
```

6.1.2.29 INV_IMU_ENABLE

```
#define INV_IMU_ENABLE (1U)
```

6.1.2.30 INV_IMU_ERROR

```
#define INV_IMU_ERROR -1
```

Unspecified error.

6.1.2.31 INV_IMU_ERROR_BAD_ARG

```
#define INV_IMU_ERROR_BAD_ARG -11
```

Invalid argument provided.

6.1.2.32 INV_IMU_ERROR_EDMP_BUF_EMPTY

```
#define INV_IMU_ERROR_EDMP_BUF_EMPTY -127
```

EDMP buffer is empty.

6.1.2.33 INV_IMU_ERROR_EDMP_ODR

```
#define INV_IMU_ERROR_EDMP_ODR -126
```

EDMP ODR decimator reconfiguration is needed.

6.1.2.34 INV_IMU_ERROR_TIMEOUT

```
#define INV_IMU_ERROR_TIMEOUT -4
```

Action did not complete in the expected time window.

6.1.2.35 INV_IMU_ERROR_TRANSPORT

```
#define INV_IMU_ERROR_TRANSPORT -3
```

Error occurred at transport level.

6.1.2.36 INV_IMU_OK

```
#define INV_IMU_OK 0
```

Success.

6.1.2.37 INVALID_VALUE_FIFO

```
#define INVALID_VALUE_FIFO ((int16_t)0x8000)
```

6.1.2.38 INVALID_VALUE_FIFO_1B

```
#define INVALID_VALUE_FIFO_1B ((int8_t)0x80)
```

6.1.2.39 OUT_OF_BOUND_TEMP_NEG_FIFO_1B

```
#define OUT_OF_BOUND_TEMP_NEG_FIFO_1B ((int8_t)0x81)
```

6.1.2.40 OUT_OF_BOUND_TEMP_POS_FIFO_1B

```
#define OUT_OF_BOUND_TEMP_POS_FIFO_1B ((int8_t)0x7F)
```

6.1.2.41 SELFTEST_ACCEL_DIS

```
#define SELFTEST_ACCEL_DIS 0x0000
```

6.1.2.42 SELFTEST_ACCEL_EN

```
#define SELFTEST_ACCEL_EN 0x0002
```

6.1.2.43 SELFTEST_ACCEL_EN_MASK

```
#define SELFTEST_ACCEL_EN_MASK 0x0002
```

6.1.2.44 SELFTEST_ACCEL_THRESH_MASK

```
#define SELFTEST_ACCEL_THRESH_MASK 0x1C00
```

6.1.2.45 SELFTEST_AVERAGE_TIME_MASK

```
#define SELFTEST_AVERAGE_TIME_MASK 0x0380
```

6.1.2.46 SELFTEST_GYRO_DIS

```
#define SELFTEST_GYRO_DIS 0x0000
```

6.1.2.47 SELFTEST_GYRO_EN

```
#define SELFTEST_GYRO_EN 0x0004
```

6.1.2.48 SELFTEST_GYRO_EN_MASK

```
#define SELFTEST_GYRO_EN_MASK 0x0004
```

6.1.2.49 SELFTEST_GYRO_THRESH_MASK

```
#define SELFTEST_GYRO_THRESH_MASK 0xE000
```

6.1.2.50 SELFTESTCAL_INIT_DIS

```
#define SELFTESTCAL_INIT_DIS 0x0000
```

6.1.2.51 SELFTESTCAL_INIT_EN

```
#define SELFTESTCAL_INIT_EN 0x0001
```

6.1.2.52 SELFTESTCAL_INIT_EN_MASK

```
#define SELFTESTCAL_INIT_EN_MASK 0x0001
```

6.1.2.53 STC_RESULTS_ACCEL_SC_MASK

```
#define STC_RESULTS_ACCEL_SC_MASK 0x0300
```

6.1.2.54 STC_RESULTS_ACCEL_X_MASK

```
#define STC_RESULTS_ACCEL_X_MASK 0x0001
```

6.1.2.55 STC_RESULTS_ACCEL_Y_MASK

```
#define STC_RESULTS_ACCEL_Y_MASK 0x0002
```

6.1.2.56 STC_RESULTS_ACCEL_Z_MASK

```
#define STC_RESULTS_ACCEL_Z_MASK 0x0004
```

6.1.2.57 STC_RESULTS_GYRO_SC_MASK

```
#define STC_RESULTS_GYRO_SC_MASK 0x0C00
```

6.1.2.58 STC_RESULTS_GYRO_X_MASK

```
#define STC_RESULTS_GYRO_X_MASK 0x0008
```

6.1.2.59 STC_RESULTS_GYRO_Y_MASK

```
#define STC_RESULTS_GYRO_Y_MASK 0x0010
```

6.1.2.60 STC_RESULTS_GYRO_Z_MASK

```
#define STC_RESULTS_GYRO_Z_MASK 0x0020
```

6.1.2.61 STC_RESULTS_ST_STATUS_MASK

```
#define STC_RESULTS_ST_STATUS_MASK 0x00C0
```

6.1.2.62 TAP_SMUDGE_REJECT_THR_400HZ

```
#define TAP_SMUDGE_REJECT_THR_400HZ 34
```

6.1.2.63 TAP_SMUDGE_REJECT_THR_800HZ

```
#define TAP_SMUDGE_REJECT_THR_800HZ 68
```

6.1.2.64 TAP_TMAX_400HZ

```
#define TAP_TMAX_400HZ 198
```

6.1.2.65 TAP_TMAX_800HZ

```
#define TAP_TMAX_800HZ 396
```

6.1.2.66 TAP_TMIN_400HZ

```
#define TAP_TMIN_400HZ 66
```

6.1.2.67 TAP_TMIN_800HZ

```
#define TAP_TMIN_800HZ 132
```

6.1.2.68 TEMP_DATA_SIZE

```
#define TEMP_DATA_SIZE 2
```

6.1.3 Enumeration Type Documentation

6.1.3.1 accel_config0_accel_odr_t

```
enum accel_config0_accel_odr_t
```

Enumerator

ACCEL_CONFIG0_ACCEL_ODR_1_5625_HZ	
ACCEL_CONFIG0_ACCEL_ODR_3_125_HZ	
ACCEL_CONFIG0_ACCEL_ODR_6_25_HZ	
ACCEL_CONFIG0_ACCEL_ODR_12_5_HZ	
ACCEL_CONFIG0_ACCEL_ODR_25_HZ	
ACCEL_CONFIG0_ACCEL_ODR_50_HZ	
ACCEL_CONFIG0_ACCEL_ODR_100_HZ	
ACCEL_CONFIG0_ACCEL_ODR_200_HZ	
ACCEL_CONFIG0_ACCEL_ODR_400_HZ	
ACCEL_CONFIG0_ACCEL_ODR_800_HZ	
ACCEL_CONFIG0_ACCEL_ODR_1600_HZ	
ACCEL_CONFIG0_ACCEL_ODR_3200_HZ	
ACCEL_CONFIG0_ACCEL_ODR_6400_HZ	

6.1.3.2 accel_config0_accel_ui_fs_sel_t

`enum accel_config0_accel_ui_fs_sel_t`

Enumerator

ACCEL_CONFIG0_ACCEL_UI_FS_SEL_2_G	
ACCEL_CONFIG0_ACCEL_UI_FS_SEL_4_G	
ACCEL_CONFIG0_ACCEL_UI_FS_SEL_8_G	
ACCEL_CONFIG0_ACCEL_UI_FS_SEL_16_G	

6.1.3.3 dmp_ext_sen_odr_cfg_apex_odr_t

`enum dmp_ext_sen_odr_cfg_apex_odr_t`

Enumerator

DMP_EXT_SEN_ODR_CFG_APEX_ODR_25_HZ	
DMP_EXT_SEN_ODR_CFG_APEX_ODR_50_HZ	
DMP_EXT_SEN_ODR_CFG_APEX_ODR_100_HZ	
DMP_EXT_SEN_ODR_CFG_APEX_ODR_200_HZ	
DMP_EXT_SEN_ODR_CFG_APEX_ODR_400_HZ	
DMP_EXT_SEN_ODR_CFG_APEX_ODR_800_HZ	

6.1.3.4 dmp_ext_sen_odr_cfg_ext_odr_t

enum dmp_ext_sen_odr_cfg_ext_odr_t

Enumerator

DMP_EXT_SEN_ODR_CFG_EXT_ODR_3_25_HZ	
DMP_EXT_SEN_ODR_CFG_EXT_ODR_6_25_HZ	
DMP_EXT_SEN_ODR_CFG_EXT_ODR_12_5_HZ	
DMP_EXT_SEN_ODR_CFG_EXT_ODR_25_HZ	
DMP_EXT_SEN_ODR_CFG_EXT_ODR_50_HZ	
DMP_EXT_SEN_ODR_CFG_EXT_ODR_100_HZ	
DMP_EXT_SEN_ODR_CFG_EXT_ODR_200_HZ	
DMP_EXT_SEN_ODR_CFG_EXT_ODR_400_HZ	

6.1.3.5 drive_config0_pads_i2c_slew_t

enum drive_config0_pads_i2c_slew_t

Enumerator

DRIVE_CONFIG0_PADS_I2C_SLEW_TYP_20NS	
DRIVE_CONFIG0_PADS_I2C_SLEW_TYP_7NS	

6.1.3.6 drive_config0_pads_spi_slew_t

enum drive_config0_pads_spi_slew_t

Enumerator

DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_38NS	
DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_14NS	
DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_10NS	
DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_7NS	
DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_5NS	
DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_4NS	
DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_0_5NS	

6.1.3.7 fifo_config0_fifo_depth_t

enum fifo_config0_fifo_depth_t

Enumerator

FIFO_CONFIG0_FIFO_DEPTH_MAX	
FIFO_CONFIG0_FIFO_DEPTH_APEX	
FIFO_CONFIG0_FIFO_DEPTH_GAF	

6.1.3.8 fifo_config0_fifo_mode_t

`enum fifo_config0_fifo_mode_t`

Enumerator

FIFO_CONFIG0_FIFO_MODE_SNAPSHOT	
FIFO_CONFIG0_FIFO_MODE_STREAM	
FIFO_CONFIG0_FIFO_MODE_BYPASS	

6.1.3.9 fifo_config2_fifo_wr_wm_gt_th_t

`enum fifo_config2_fifo_wr_wm_gt_th_t`

Enumerator

FIFO_CONFIG2_FIFO_WR_WM_EQ_OR_GT_TH	
FIFO_CONFIG2_FIFO_WR_WM_EQ_TH	

6.1.3.10 fifo_config4_fifo_comp_nc_flow_cfg_t

`enum fifo_config4_fifo_comp_nc_flow_cfg_t`

Enumerator

FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_EVERY_128_FR	
FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_EVERY_64_FR	
FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_EVERY_32_FR	
FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_EVERY_16_FR	
FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_EVERY_8_FR	
FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_DIS	

6.1.3.11 fifo_config4_fifo_es0_6b_9b_t

enum fifo_config4_fifo_es0_6b_9b_t

Enumerator

FIFO_CONFIG4_FIFO_ES0_9B	
FIFO_CONFIG4_FIFO_ES0_6B	

6.1.3.12 fs_sel_aux_accel_fs_sel_t

enum fs_sel_aux_accel_fs_sel_t

Enumerator

FS_SEL_AUX_ACCEL_FS_SEL_2_G	
FS_SEL_AUX_ACCEL_FS_SEL_4_G	
FS_SEL_AUX_ACCEL_FS_SEL_8_G	
FS_SEL_AUX_ACCEL_FS_SEL_16_G	

6.1.3.13 fs_sel_aux_gyro_fs_sel_t

enum fs_sel_aux_gyro_fs_sel_t

Enumerator

FS_SEL_AUX_GYRO_FS_SEL_15_625_DPS	
FS_SEL_AUX_GYRO_FS_SEL_31_25_DPS	
FS_SEL_AUX_GYRO_FS_SEL_62_5_DPS	
FS_SEL_AUX_GYRO_FS_SEL_125_DPS	
FS_SEL_AUX_GYRO_FS_SEL_250_DPS	
FS_SEL_AUX_GYRO_FS_SEL_500_DPS	
FS_SEL_AUX_GYRO_FS_SEL_1000_DPS	
FS_SEL_AUX_GYRO_FS_SEL_2000_DPS	

6.1.3.14 fsync_config0_ap_fsync_sel_t

enum fsync_config0_ap_fsync_sel_t

Enumerator

FSYNC_CONFIG0_AP_FSYNC_NO	
FSYNC_CONFIG0_AP_FSYNC_TEMP	
FSYNC_CONFIG0_AP_FSYNC_GYRO_X	
FSYNC_CONFIG0_AP_FSYNC_GYRO_Y	
FSYNC_CONFIG0_AP_FSYNC_GYRO_Z	
FSYNC_CONFIG0_AP_FSYNC_ACCEL↩ _X	
FSYNC_CONFIG0_AP_FSYNC_ACCEL↩ _Y	
FSYNC_CONFIG0_AP_FSYNC_ACCEL↩ _Z	

6.1.3.15 gyro_config0_gyro_odr_t

enum gyro_config0_gyro_odr_t

Enumerator

GYRO_CONFIG0_GYRO_ODR_1_5625_HZ	
GYRO_CONFIG0_GYRO_ODR_3_125_HZ	
GYRO_CONFIG0_GYRO_ODR_6_25_HZ	
GYRO_CONFIG0_GYRO_ODR_12_5_HZ	
GYRO_CONFIG0_GYRO_ODR_25_HZ	
GYRO_CONFIG0_GYRO_ODR_50_HZ	
GYRO_CONFIG0_GYRO_ODR_100_HZ	
GYRO_CONFIG0_GYRO_ODR_200_HZ	
GYRO_CONFIG0_GYRO_ODR_400_HZ	
GYRO_CONFIG0_GYRO_ODR_800_HZ	
GYRO_CONFIG0_GYRO_ODR_1600_HZ	
GYRO_CONFIG0_GYRO_ODR_3200_HZ	
GYRO_CONFIG0_GYRO_ODR_6400_HZ	

6.1.3.16 gyro_config0_gyro_ui_fs_sel_t

enum gyro_config0_gyro_ui_fs_sel_t

Enumerator

GYRO_CONFIG0_GYRO_UI_FS_SEL_15_625_DPS	
GYRO_CONFIG0_GYRO_UI_FS_SEL_31_25_DPS	
GYRO_CONFIG0_GYRO_UI_FS_SEL_62_5_DPS	
GYRO_CONFIG0_GYRO_UI_FS_SEL_125_DPS	
GYRO_CONFIG0_GYRO_UI_FS_SEL_250_DPS	

Enumerator

GYRO_CONFIG0_GYRO_UI_FS_SEL_500_DPS	
GYRO_CONFIG0_GYRO_UI_FS_SEL_1000_DPS	
GYRO_CONFIG0_GYRO_UI_FS_SEL_2000_DPS	

6.1.3.17 intf_config1_ovrd_ap_spi_34_mode_ovrd_val_t

`enum intf_config1_ovrd_ap_spi_34_mode_ovrd_val_t`

Enumerator

INTF_CONFIG1_OVRD_AP_SPI_34_MODE_OVRD_VAL_3_WIRE	
INTF_CONFIG1_OVRD_AP_SPI_34_MODE_OVRD_VAL_4_WIRE	

6.1.3.18 intf_config1_ovrd_ap_spi_mode_ovrd_val_t

`enum intf_config1_ovrd_ap_spi_mode_ovrd_val_t`

Enumerator

INTF_CONFIG1_OVRD_AP_SPI_MODE_OVRD_VAL_0_OR↩ _3	
INTF_CONFIG1_OVRD_AP_SPI_MODE_OVRD_VAL_1_OR↩ _2	

6.1.3.19 intx_config2_intx_drive_t

`enum intx_config2_intx_drive_t`

Enumerator

INTX_CONFIG2_INTX_DRIVE_PP	
INTX_CONFIG2_INTX_DRIVE_OD	

6.1.3.20 intx_config2_intx_mode_t

`enum intx_config2_intx_mode_t`

Enumerator

INTX_CONFIG2_INTX_MODE_PULSE	
INTX_CONFIG2_INTX_MODE_LATCH	

6.1.3.21 intx_config2_intx_polarity_t

`enum intx_config2_intx_polarity_t`

Enumerator

INTX_CONFIG2_INTX_POLARITY_LOW	
INTX_CONFIG2_INTX_POLARITY_HIGH	

6.1.3.22 inv_imu_int_num_t

`enum inv_imu_int_num_t`

Interrupt number.

Enumerator

INV_IMU_INT1	
INV_IMU_INT2	

6.1.3.23 ioc_pad_scenario_ovrd_pads_int2_cfg_ovrd_val_t

`enum ioc_pad_scenario_ovrd_pads_int2_cfg_ovrd_val_t`

Enumerator

IOC_PAD_SCENARIO_OVRD_INT2_CFG_OVRD_VAL_INT2	
IOC_PAD_SCENARIO_OVRD_INT2_CFG_OVRD_VAL_DRDY_INTR	

6.1.3.24 ipreg_sys1_reg_166_gyro_src_ctrl_sel_t

`enum ipreg_sys1_reg_166_gyro_src_ctrl_sel_t`

Enumerator

IPREG_SYS1_REG_166_GYRO_SRC_CTRL_INTERPOLATOR_ON_FIR_ON	
IPREG_SYS1_REG_166_GYRO_SRC_CTRL_INTERPOLATOR_OFF_FIR_ON	
IPREG_SYS1_REG_166_GYRO_SRC_CTRL_INTERPOLATOR_OFF_FIR_OFF	

6.1.3.25 ipreg_sys1_reg_170_gyro_lp_avg_sel_t

`enum ipreg_sys1_reg_170_gyro_lp_avg_sel_t`

Enumerator

IPREG_SYS1_REG_170_GYRO_LP_AVG_64	
IPREG_SYS1_REG_170_GYRO_LP_AVG_32	
IPREG_SYS1_REG_170_GYRO_LP_AVG_20	
IPREG_SYS1_REG_170_GYRO_LP_AVG_18	
IPREG_SYS1_REG_170_GYRO_LP_AVG_16	
IPREG_SYS1_REG_170_GYRO_LP_AVG_11	
IPREG_SYS1_REG_170_GYRO_LP_AVG_10	
IPREG_SYS1_REG_170_GYRO_LP_AVG_8	
IPREG_SYS1_REG_170_GYRO_LP_AVG_7	
IPREG_SYS1_REG_170_GYRO_LP_AVG_5	
IPREG_SYS1_REG_170_GYRO_LP_AVG_4	
IPREG_SYS1_REG_170_GYRO_LP_AVG_2	
IPREG_SYS1_REG_170_GYRO_LP_AVG_1	

6.1.3.26 ipreg_sys1_reg_172_gyro_ui_lpfbw_sel_t

`enum ipreg_sys1_reg_172_gyro_ui_lpfbw_sel_t`

Enumerator

IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_128	
IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_64	
IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_32	
IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_16	
IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_8	
IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_4	
IPREG_SYS1_REG_172_GYRO_UI_LPFBW_NO_FILTER	

6.1.3.27 ipreg_sys2_reg_123_accel_src_ctrl_sel_t

enum ipreg_sys2_reg_123_accel_src_ctrl_sel_t

Enumerator

IPREG_SYS2_REG_123_ACCEL_SRC_CTRL_INTERPOLATOR_ON_FIR_ON	
IPREG_SYS2_REG_123_ACCEL_SRC_CTRL_INTERPOLATOR_OFF_FIR_ON	
IPREG_SYS2_REG_123_ACCEL_SRC_CTRL_INTERPOLATOR_OFF_FIR_OFF	

6.1.3.28 ipreg_sys2_reg_129_accel_lp_avg_sel_t

enum ipreg_sys2_reg_129_accel_lp_avg_sel_t

Enumerator

IPREG_SYS2_REG_129_ACCEL_LP_AVG_64	
IPREG_SYS2_REG_129_ACCEL_LP_AVG_32	
IPREG_SYS2_REG_129_ACCEL_LP_AVG_20	
IPREG_SYS2_REG_129_ACCEL_LP_AVG_18	
IPREG_SYS2_REG_129_ACCEL_LP_AVG_16	
IPREG_SYS2_REG_129_ACCEL_LP_AVG_11	
IPREG_SYS2_REG_129_ACCEL_LP_AVG_10	
IPREG_SYS2_REG_129_ACCEL_LP_AVG_8	
IPREG_SYS2_REG_129_ACCEL_LP_AVG_7	
IPREG_SYS2_REG_129_ACCEL_LP_AVG_5	
IPREG_SYS2_REG_129_ACCEL_LP_AVG_4	
IPREG_SYS2_REG_129_ACCEL_LP_AVG_2	
IPREG_SYS2_REG_129_ACCEL_LP_AVG_1	

6.1.3.29 ipreg_sys2_reg_131_accel_ui_lpfbw_t

enum ipreg_sys2_reg_131_accel_ui_lpfbw_t

Enumerator

IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_128	
IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_64	
IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_32	
IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_16	
IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_8	
IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_4	
IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_NO_FILTER	

6.1.3.30 odr_decimate_config_accel_fifo_odr_dec_t

enum odr_decimate_config_accel_fifo_odr_dec_t

Enumerator

ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_1	
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_2	
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_4	
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_8	
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_16	
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_32	
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_64	
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_128	
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_256	
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_512	
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_1024	
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_2048	
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_4096	

6.1.3.31 odr_decimate_config_gyro_fifo_odr_dec_t

enum odr_decimate_config_gyro_fifo_odr_dec_t

Enumerator

ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_1	
ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_2	
ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_4	
ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_8	
ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_16	
ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_32	
ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_64	
ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_128	
ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_256	
ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_512	
ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_1024	
ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_2048	
ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_4096	

6.1.3.32 pwr_mgmt0_accel_mode_t

enum pwr_mgmt0_accel_mode_t

Enumerator

PWR_MGMT0_ACCEL_MODE_LN	
PWR_MGMT0_ACCEL_MODE_LP	
PWR_MGMT0_ACCEL_MODE_OFF	

6.1.3.33 pwr_mgmt0_gyro_mode_t

`enum pwr_mgmt0_gyro_mode_t`

Enumerator

PWR_MGMT0_GYRO_MODE_LN	
PWR_MGMT0_GYRO_MODE_LP	
PWR_MGMT0_GYRO_MODE_STANDBY	
PWR_MGMT0_GYRO_MODE_OFF	

6.1.3.34 reg_misc1_osc_id_ovrd_t

`enum reg_misc1_osc_id_ovrd_t`

Enumerator

REG_MISC1_OSC_ID_OVRD_OFF	
REG_MISC1_OSC_ID_OVRD_EDOSC	
REG_MISC1_OSC_ID_OVRD_RCOSC	
REG_MISC1_OSC_ID_OVRD_PLL	
REG_MISC1_OSC_ID_OVRD_EXT_CLK	

6.1.3.35 selftest_accel_threshold_t

`enum selftest_accel_threshold_t`

Enumerator

SELFTEST_ACCEL_THRESHOLD_5_PERCENT	
SELFTEST_ACCEL_THRESHOLD_10_PERCENT	
SELFTEST_ACCEL_THRESHOLD_15_PERCENT	
SELFTEST_ACCEL_THRESHOLD_20_PERCENT	
SELFTEST_ACCEL_THRESHOLD_25_PERCENT	
SELFTEST_ACCEL_THRESHOLD_30_PERCENT	
SELFTEST_ACCEL_THRESHOLD_40_PERCENT	
SELFTEST_ACCEL_THRESHOLD_50_PERCENT	

6.1.3.36 selftest_average_time_t

enum selftest_average_time_t

Enumerator

SELFTEST_AVG_TIME_10_MS	
SELFTEST_AVG_TIME_20_MS	
SELFTEST_AVG_TIME_40_MS	
SELFTEST_AVG_TIME_80_MS	
SELFTEST_AVG_TIME_160_MS	
SELFTEST_AVG_TIME_320_MS	

6.1.3.37 selftest_gyro_threshold_t

enum selftest_gyro_threshold_t

Enumerator

SELFTEST_GYRO_THRESHOLD_5_PERCENT	
SELFTEST_GYRO_THRESHOLD_10_PERCENT	
SELFTEST_GYRO_THRESHOLD_15_PERCENT	
SELFTEST_GYRO_THRESHOLD_20_PERCENT	
SELFTEST_GYRO_THRESHOLD_25_PERCENT	
SELFTEST_GYRO_THRESHOLD_30_PERCENT	
SELFTEST_GYRO_THRESHOLD_40_PERCENT	
SELFTEST_GYRO_THRESHOLD_50_PERCENT	

6.1.3.38 smc_control_0_accel_lp_clk_sel_t

enum smc_control_0_accel_lp_clk_sel_t

Enumerator

SMC_CONTROL_0_ACCEL_LP_CLK_RCOSC	
SMC_CONTROL_0_ACCEL_LP_CLK_WUOSC	

6.1.3.39 sreg_ctrl_sreg_data_endian_sel_t

enum sreg_ctrl_sreg_data_endian_sel_t

Enumerator

SREG_CTRL_SREG_DATA_BIG_ENDIAN	
SREG_CTRL_SREG_DATA_LITTLE_ENDIAN	

6.1.3.40 stc_patch_params_t

enum stc_patch_params_t

Enumerator

SELFTEST_PATCH_EN_ACCEL_PHASE1	
SELFTEST_PATCH_EN_ACCEL_PHASE2	
SELFTEST_PATCH_EN_GYRO1_PHASE1	
SELFTEST_PATCH_EN_GYRO1_PHASE2	

6.1.3.41 tmst_wom_config_tmst_resol_t

enum tmst_wom_config_tmst_resol_t

Enumerator

TMST_WOM_CONFIG_TMST_RESOL_16_US	
TMST_WOM_CONFIG_TMST_RESOL_1_US	

6.1.3.42 tmst_wom_config_wom_int_dur_t

enum tmst_wom_config_wom_int_dur_t

Enumerator

TMST_WOM_CONFIG_WOM_INT_DUR_1_SMPL	
TMST_WOM_CONFIG_WOM_INT_DUR_2_SMPL	
TMST_WOM_CONFIG_WOM_INT_DUR_3_SMPL	
TMST_WOM_CONFIG_WOM_INT_DUR_4_SMPL	

6.1.3.43 tmst_wom_config_wom_int_mode_t

enum tmst_wom_config_wom_int_mode_t

Enumerator

TMST_WOM_CONFIG_WOM_INT_MODE_ANDED	
TMST_WOM_CONFIG_WOM_INT_MODE_ORED	

6.1.3.44 tmst_wom_config_wom_mode_t

enum tmst_wom_config_wom_mode_t

Enumerator

TMST_WOM_CONFIG_WOM_MODE_CMP_PREV	
TMST_WOM_CONFIG_WOM_MODE_CMP_INIT	

6.2 Basic Driver

Basic API to drive the device.

Files

- file inv_imu_driver.h

Classes

- struct inv_imu_device_t
  Basic driver configuration structure.
- union inv_imu_fifo_data_t
  One frame of FIFO header+data.
- struct inv_imu_int_state_t
  Interrupts definition.
- struct inv_imu_fifo_config_t
  Basic FIFO configuration.

Macros

- #define FORMAT_16_BITS_DATA(is_big_endian, pIn8, pOut16) *(pOut16) = ((is_big_endian) == 1) ? ((p↩ In8)[0] << 8) | (pIn8)[1] : ((pIn8)[1] << 8) | (pIn8)[0]
  Macro to convert 2 bytes in 1 half-word depending on IMU endianness.

Functions

- void inv_imu_sleep_us (inv_imu_device_t *s, uint32_t us)

  Sleep function.
- int inv_imu_soft_reset (inv_imu_device_t *s)

  Performs a soft reset of the device.
- int inv_imu_get_who_am_i (inv_imu_device_t *s, uint8_t *who_am_i)

  return WHOAMI value
- int inv_imu_set_accel_mode (inv_imu_device_t *s, pwr_mgmt0_accel_mode_t accel_mode)

  Configure accel mode.
- int inv_imu_set_gyro_mode (inv_imu_device_t *s, pwr_mgmt0_gyro_mode_t gyro_mode)

  Configure gyro mode.
- int inv_imu_set_accel_frequency (inv_imu_device_t *s, const accel_config0_accel_odr_t frequency)

  Configure accel Output Data Rate.
- int inv_imu_set_gyro_frequency (inv_imu_device_t *s, const gyro_config0_gyro_odr_t frequency)

  Configure gyro Output Data Rate.
- int inv_imu_set_accel_fsr (inv_imu_device_t *s, accel_config0_accel_ui_fs_sel_t accel_fsr)

  Set accel full scale range.
- int inv_imu_set_gyro_fsr (inv_imu_device_t *s, gyro_config0_gyro_ui_fs_sel_t gyro_fsr)

  Set gyro full scale range.
- int inv_imu_set_accel_lp_avg (inv_imu_device_t *s, ipreg_sys2_reg_129_accel_lp_avg_sel_t acc_avg)

  Set accel Low-Power averaging value.
- int inv_imu_set_gyro_lp_avg (inv_imu_device_t *s, ipreg_sys1_reg_170_gyro_lp_avg_sel_t gyr_avg)

  Set gyro Low-Power averaging value.
- int inv_imu_set_accel_ln_bw (inv_imu_device_t *s, ipreg_sys2_reg_131_accel_ui_lpfbw_t acc_bw)

  Set accel Low-Noise bandwidth value.
- int inv_imu_set_gyro_ln_bw (inv_imu_device_t *s, ipreg_sys1_reg_172_gyro_ui_lpfbw_sel_t gyr_bw)

  Set gyro Low-Noise bandwidth value.
- int inv_imu_get_register_data (inv_imu_device_t *s, inv_imu_sensor_data_t *data)

  Get current sensor data from the registers.
- int inv_imu_set_fifo_config (inv_imu_device_t *s, const inv_imu_fifo_config_t *fifo_config)

  Configures the FIFO to the specified state.
- int inv_imu_get_fifo_config (inv_imu_device_t *s, inv_imu_fifo_config_t *fifo_config)

  Gets the current FIFO configuration.
- int inv_imu_flush_fifo (inv_imu_device_t *s)

  Flush FIFO content.
- int inv_imu_get_frame_count (inv_imu_device_t *s, uint16_t *frame_count)

  Get FIFO frame count.
- int inv_imu_get_fifo_frame (inv_imu_device_t *s, inv_imu_fifo_data_t *data)

  Get one frame of FIFO data.
- int inv_imu_set_config_int (inv_imu_device_t *s, const inv_imu_int_num_t num, const inv_imu_int_state_t *it)

  Configure interrupts source.
- int inv_imu_get_config_int (inv_imu_device_t *s, const inv_imu_int_num_t num, inv_imu_int_state_t *it)

  Retrieve interrupts configuration.
- int inv_imu_set_pin_config_int (inv_imu_device_t *s, const inv_imu_int_num_t num, const inv_imu_int_pin_config_t *conf)

  Configure pin behavior.
- int inv_imu_get_int_status (inv_imu_device_t *s, const inv_imu_int_num_t num, inv_imu_int_state_t *it)

  Read interrupt 1 status.
- int inv_imu_get_endianness (inv_imu_device_t *s)

Read the UI endianness and set the inv_device endianness field.

- int inv_imu_select_accel_lp_clk (inv_imu_device_t *s, smc_control_0_accel_lp_clk_sel_t clk_sel)

  Select which clock to use when in Low Power mode.

- const char * inv_imu_get_version (void)

  Return driver version x.y.z-suffix as a char array.

6.2.1 Detailed Description

Basic API to drive the device.

6.2.2 Macro Definition Documentation

6.2.2.1 FORMAT_16_BITS_DATA

```
#define FORMAT_16_BITS_DATA(
              is_big_endian,
              pIn8,
              pOut16 )  *(pOut16) = ((is_big_endian) == 1) ?  ((pIn8)[0] << 8) | (pIn8)[1] :
((pIn8)[1] << 8) | (pIn8)[0]
```

Macro to convert 2 bytes in 1 half-word depending on IMU endianness.

6.2.3 Function Documentation

6.2.3.1 inv_imu_flush_fifo()

```
int inv_imu_flush_fifo (
             inv_imu_device_t * s )
```

Flush FIFO content.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.2.3.2 inv_imu_get_config_int()

```
int inv_imu_get_config_int (
            inv_imu_device_t * s,
            const inv_imu_int_num_t num,
            inv_imu_int_state_t * it )
```

Retrieve interrupts configuration.

Parameters

in	*s*	Pointer to device.
in	*num*	Interrupt number
out	*it*	State of each interrupt

Returns

0 on success, negative value on error.

6.2.3.3 inv_imu_get_endianness()

```
int inv_imu_get_endianness (
            inv_imu_device_t * s )
```

Read the UI endianness and set the inv_device endianness field.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.2.3.4 inv_imu_get_fifo_config()

```
int inv_imu_get_fifo_config (
            inv_imu_device_t * s,
            inv_imu_fifo_config_t * fifo_config )
```

Gets the current FIFO configuration.

Parameters

in	*s*	Pointer to device.
in	*fifo_config*	Structure containing the FIFO configuration.

Returns

0 on success, negative value on error.

6.2.3.5 inv_imu_get_fifo_frame()

```
int inv_imu_get_fifo_frame (
            inv_imu_device_t * s,
            inv_imu_fifo_data_t * data )
```

Get one frame of FIFO data.

Parameters

in	*s*	Pointer to device.
out	*data*	Accel, gyro and temperature data from the top frame on the FIFO.

Returns

0 on success, negative value on error.

6.2.3.6 inv_imu_get_frame_count()

```
int inv_imu_get_frame_count (
            inv_imu_device_t * s,
            uint16_t * frame_count )
```

Get FIFO frame count.

Parameters

in	*s*	Pointer to device.
out	*frame_count*	The number of frames in the FIFO.

Returns

0 on success, negative value on error.

6.2.3.7 inv_imu_get_int_status()

```
int inv_imu_get_int_status (
            inv_imu_device_t * s,
```

```
        const inv_imu_int_num_t num,
        inv_imu_int_state_t * it )
```

Read interrupt 1 status.

Parameters

in	*s*	Pointer to device.
in	*num*	Interrupt number
out	*it*	Status of each interrupt.

Returns

0 on success, negative value on error.

6.2.3.8 inv_imu_get_register_data()

```
int inv_imu_get_register_data (
            inv_imu_device_t * s,
            inv_imu_sensor_data_t * data )
```

Get current sensor data from the registers.

Parameters

in	*s*	Pointer to device.
out	*data*	Current accel, gyro and temperature data from the registers.

Returns

0 on success, negative value on error.

6.2.3.9 inv_imu_get_version()

```
const char* inv_imu_get_version (
            void  )
```

Return driver version x.y.z-suffix as a char array.

Returns

Driver version as char array "x.y.z-suffix"

6.2.3.10 inv_imu_get_who_am_i()

```
int inv_imu_get_who_am_i (
            inv_imu_device_t * s,
            uint8_t * who_am_i )
```

return WHOAMI value

Parameters

in	*s*	Pointer to device.
out	*who_↩ am_i*	WHOAMI for device

Returns

0 on success, negative value on error

6.2.3.11 inv_imu_select_accel_lp_clk()

```
int inv_imu_select_accel_lp_clk (
            inv_imu_device_t * s,
            smc_control_0_accel_lp_clk_sel_t clk_sel )
```

Select which clock to use when in Low Power mode.

Use SMC_CONTROL_0_ACCEL_LP_CLK_RCOSC for Low Power (LP) mode. Use SMC_CONTROL_0_↩ ACCEL_LP_CLK_WUOSC for Ultra Low Power (ULP) mode.

Note

In ULP mode, sensor registers are not available and the host must retrieve data from the FIFO.

Parameters

in	*s*	Pointer to device.
in	*clk_sel*	Selected clock.

Returns

0 on success, negative value on error.

6.2.3.12 inv_imu_set_accel_frequency()

```
int inv_imu_set_accel_frequency (
            inv_imu_device_t * s,
            const accel_config0_accel_odr_t frequency )
```

Configure accel Output Data Rate.

Parameters

in	*s*	Pointer to device.
in	*frequency*	The requested frequency.

Returns

0 on success, negative value on error.

6.2.3.13 inv_imu_set_accel_fsr()

```
int inv_imu_set_accel_fsr (
            inv_imu_device_t * s,
            accel_config0_accel_ui_fs_sel_t accel_fsr )
```

Set accel full scale range.

Parameters

in	*s*	Pointer to device.
in	*accel_fsr*	Requested full scale range.

Returns

0 on success, negative value on error.

6.2.3.14 inv_imu_set_accel_ln_bw()

```
int inv_imu_set_accel_ln_bw (
            inv_imu_device_t * s,
            ipreg_sys2_reg_131_accel_ui_lpfbw_t acc_bw )
```

Set accel Low-Noise bandwidth value.

Parameters

in	*s*	Pointer to device.
in	*acc_bw*	Requested bandwidth value

Returns

0 on success, negative value on error.

6.2.3.15 inv_imu_set_accel_lp_avg()

```
int inv_imu_set_accel_lp_avg (
            inv_imu_device_t * s,
            ipreg_sys2_reg_129_accel_lp_avg_sel_t acc_avg )
```

Set accel Low-Power averaging value.

Parameters

in	*s*	Pointer to device.
in	*acc_avg*	Requested averaging value

Returns

0 on success, negative value on error.

6.2.3.16 inv_imu_set_accel_mode()

```
int inv_imu_set_accel_mode (
            inv_imu_device_t * s,
            pwr_mgmt0_accel_mode_t accel_mode )
```

Configure accel mode.

Parameters

in	*s*	Pointer to transport structure.
in	*accel_mode*	The requested mode.

Returns

0 on success, negative value on error.

6.2.3.17 inv_imu_set_config_int()

```
int inv_imu_set_config_int (
            inv_imu_device_t * s,
            const inv_imu_int_num_t num,
            const inv_imu_int_state_t * it )
```

Configure interrupts source.

Parameters

in	*s*	Pointer to device.
in	*num*	Interrupt number
in	*it*	State of each interrupt

Returns

0 on success, negative value on error.

6.2.3.18 inv_imu_set_fifo_config()

```
int inv_imu_set_fifo_config (
            inv_imu_device_t * s,
            const inv_imu_fifo_config_t * fifo_config )
```

Configures the FIFO to the specified state.

Parameters

in	*s*	Pointer to device.
in	*fifo_config*	Structure containing the FIFO configuration.

Returns

0 on success, negative value on error.

6.2.3.19 inv_imu_set_gyro_frequency()

```
int inv_imu_set_gyro_frequency (
            inv_imu_device_t * s,
            const gyro_config0_gyro_odr_t frequency )
```

Configure gyro Output Data Rate.

Parameters

in	*s*	Pointer to device.
in	*frequency*	The requested frequency.

Returns

0 on success, negative value on error.

6.2.3.20 inv_imu_set_gyro_fsr()

```
int inv_imu_set_gyro_fsr (
            inv_imu_device_t * s,
            gyro_config0_gyro_ui_fs_sel_t gyro_fsr )
```

Set gyro full scale range.

Parameters

in	*s*	Pointer to device.
in	*gyro_fsr*	Requested full scale range.

Returns

0 on success, negative value on error.

6.2.3.21 inv_imu_set_gyro_ln_bw()

```
int inv_imu_set_gyro_ln_bw (
            inv_imu_device_t * s,
            ipreg_sys1_reg_172_gyro_ui_lpfbw_sel_t gyr_bw )
```

Set gyro Low-Noise bandwidth value.

Parameters

in	*s*	Pointer to device.
in	*gyr_bw*	Requested bandwidth value

Returns

0 on success, negative value on error.

6.2.3.22 inv_imu_set_gyro_lp_avg()

```
int inv_imu_set_gyro_lp_avg (
            inv_imu_device_t * s,
            ipreg_sys1_reg_170_gyro_lp_avg_sel_t gyr_avg )
```

Set gyro Low-Power averaging value.

Parameters

in	*s*	Pointer to device.
in	*gyr_avg*	Requested averaging value

Returns

0 on success, negative value on error.

6.2.3.23 inv_imu_set_gyro_mode()

```
int inv_imu_set_gyro_mode (
            inv_imu_device_t * s,
            pwr_mgmt0_gyro_mode_t gyro_mode )
```

Configure gyro mode.

Parameters

in	*s*	Pointer to transport structure.
in	*gyro_mode*	The requested mode.

Returns

0 on success, negative value on error.

6.2.3.24 inv_imu_set_pin_config_int()

```
int inv_imu_set_pin_config_int (
            inv_imu_device_t * s,
            const inv_imu_int_num_t num,
            const inv_imu_int_pin_config_t * conf )
```

Configure pin behavior.

Parameters

in	*s*	Pointer to device.
in	*num*	Interrupt number
in	*conf*	Structure with the requested configuration.

Returns

0 on success, negative value on error.

6.2.3.25 inv_imu_sleep_us()

```
void inv_imu_sleep_us (
            inv_imu_device_t * s,
            uint32_t us )
```

Sleep function.

Parameters

in	*s*	Pointer to device.
in	*us*	Time to sleep in microseconds.

6.2.3.26 inv_imu_soft_reset()

```
int inv_imu_soft_reset (
            inv_imu_device_t * s )
```

Performs a soft reset of the device.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3 Driver Advanced

High-level API for advanced functionalities.

Files

- file inv_imu_driver_advanced.h

Classes

- struct inv_imu_sensor_event_t
  Sensor event structure definition.
- struct inv_imu_adv_var_t
  Definition of extended variables.
- struct inv_imu_adv_fifo_config_t
  FIFO configuration structure.

Macros

- #define FIFO_MIRRORING_SIZE 16 ∗ 258 /∗ packet size ∗ max_count = 4kB ∗/
  Maximum buffer size mirrored from FIFO.

Enumerations

- enum inv_imu_sensor_id_t {
  INV_SENSOR_ACCEL , INV_SENSOR_GYRO , INV_SENSOR_FSYNC_EVENT , INV_SENSOR_TEMPERATURE
  ,
  INV_SENSOR_EDMP_PEDOMETER_EVENT , INV_SENSOR_EDMP_PEDOMETER_COUNT , INV_SENSOR_EDMP_TILT
  , INV_SENSOR_EDMP_FF ,
  INV_SENSOR_EDMP_LOWG , INV_SENSOR_EDMP_HIGHG , INV_SENSOR_EDMP_SMD , INV_SENSOR_EDMP_TAP
  ,
  INV_SENSOR_EDMP_R2W_WAKE , INV_SENSOR_EDMP_R2W_SLEEP , INV_SENSOR_ES0 ,
  INV_SENSOR_ES1 ,
  INV_SENSOR_MAX }

  Sensor identifier enumeration.

Functions

- int inv_imu_adv_init (inv_imu_device_t *s)

  Initializes device.
- int inv_imu_adv_device_reset (inv_imu_device_t *s)

  Performs a soft reset of the device.
- int inv_imu_adv_enable_accel_lp (inv_imu_device_t *s)

  Enable accel in low power mode.
- int inv_imu_adv_enable_accel_ln (inv_imu_device_t *s)

  Enable accel in low noise mode.
- int inv_imu_adv_disable_accel (inv_imu_device_t *s)

  Disable accel.
- int inv_imu_adv_enable_gyro_ln (inv_imu_device_t *s)

  Enable gyro in low noise mode.
- int inv_imu_adv_enable_gyro_lp (inv_imu_device_t *s)

  Enable gyro in low power mode.
- int inv_imu_adv_disable_gyro (inv_imu_device_t *s)

  Disable gyro.
- int inv_imu_adv_get_data_from_registers (inv_imu_device_t *s)

  Read all registers containing data (temperature, accelerometer and gyroscope).
- int inv_imu_adv_reset_fifo (inv_imu_device_t *s)

  reset IMU fifo
- int inv_imu_adv_get_fifo_config (inv_imu_device_t *s, inv_imu_adv_fifo_config_t *conf)

  Retrieve FIFO configuration.
- int inv_imu_adv_set_fifo_config (inv_imu_device_t *s, const inv_imu_adv_fifo_config_t *conf)

  Set FIFO configuration.
- int inv_imu_adv_get_data_from_fifo (inv_imu_device_t *s, uint8_t fifo_data[FIFO_MIRRORING_SIZE], uint16_t *fifo_count)

  Read all available packets from the FIFO.
- int inv_imu_adv_parse_fifo_data (inv_imu_device_t *s, const uint8_t fifo_data[FIFO_MIRRORING_SIZE], const uint16_t fifo_count)

  Parse packets from FIFO buffer.
- uint32_t inv_imu_adv_convert_odr_bitfield_to_us (uint32_t odr_bitfield)

  Converts accel_config0_accel_odr_t or gyro_config0_gyro_odr_t enums to period expressed in us.
- int inv_imu_adv_get_accel_fsr (inv_imu_device_t *s, accel_config0_accel_ui_fs_sel_t *accel_fsr)

  Access accel full scale range.
- int inv_imu_adv_get_gyro_fsr (inv_imu_device_t *s, gyro_config0_gyro_ui_fs_sel_t *gyro_fsr)

  Access gyro full scale range.

- int inv_imu_adv_set_timestamp_resolution (inv_imu_device_t *s, const tmst_wom_config_tmst_resol_t timestamp_resol)

  Set timestamp resolution.
- uint32_t inv_imu_adv_get_timestamp_resolution_us (inv_imu_device_t *s)

  Get timestamp resolution.
- int inv_imu_adv_configure_wom (inv_imu_device_t *s, const uint8_t wom_x_th, const uint8_t wom_y_th, const uint8_t wom_z_th, tmst_wom_config_wom_int_mode_t wom_int, tmst_wom_config_wom_int_dur_t wom_dur)

  Enable Wake On Motion.
- int inv_imu_adv_enable_wom (inv_imu_device_t *s)

  Enable Wake On Motion.
- int inv_imu_adv_disable_wom (inv_imu_device_t *s)

  Disable Wake On Motion.
- int inv_imu_adv_set_endianness (inv_imu_device_t *s, sreg_ctrl_sreg_data_endian_sel_t endianness)

  Set the UI endianness and set the inv_device endianness field.
- int inv_imu_adv_power_up_sram (inv_imu_device_t *s)

  Power-up the SRAM.
- int inv_imu_adv_power_down_sram (inv_imu_device_t *s)

  Power-down the SRAM.

6.3.1 Detailed Description

High-level API for advanced functionalities.

6.3.2 Macro Definition Documentation

6.3.2.1 FIFO_MIRRORING_SIZE

```
#define FIFO_MIRRORING_SIZE 16 * 258 /* packet size * max_count = 4kB */
```

Maximum buffer size mirrored from FIFO.

6.3.3 Enumeration Type Documentation

6.3.3.1 inv_imu_sensor_id_t

```
enum inv_imu_sensor_id_t
```

Sensor identifier enumeration.

Enumerator

INV_SENSOR_ACCEL	
INV_SENSOR_GYRO	
INV_SENSOR_FSYNC_EVENT	
INV_SENSOR_TEMPERATURE	
INV_SENSOR_EDMP_PEDOMETER_EVENT	
INV_SENSOR_EDMP_PEDOMETER_COUNT	
INV_SENSOR_EDMP_TILT	
INV_SENSOR_EDMP_FF	
INV_SENSOR_EDMP_LOWG	
INV_SENSOR_EDMP_HIGHG	
INV_SENSOR_EDMP_SMD	
INV_SENSOR_EDMP_TAP	
INV_SENSOR_EDMP_R2W_WAKE	
INV_SENSOR_EDMP_R2W_SLEEP	
INV_SENSOR_ES0	
INV_SENSOR_ES1	
INV_SENSOR_MAX	

6.3.4 Function Documentation

6.3.4.1 inv_imu_adv_configure_wom()

```
int inv_imu_adv_configure_wom (
              inv_imu_device_t * s,
              const uint8_t wom_x_th,
              const uint8_t wom_y_th,
              const uint8_t wom_z_th,
              tmst_wom_config_wom_int_mode_t wom_int,
              tmst_wom_config_wom_int_dur_t wom_dur )
```

Enable Wake On Motion.

Parameters

in	*s*	Pointer to device.
in	*wom_x_th*	Threshold for X axis with 1g/256 resolution (wom_x_th = mg ∗ 256 / 1000).
in	*wom_y_th*	Threshold for Y axis with 1g/256 resolution (wom_y_th = mg ∗ 256 / 1000).
in	*wom_z_th*	Threshold for Z axis with 1g/256 resolution (wom_z_th = mg ∗ 256 / 1000).
in	*wom_int*	Mode used to generate interrupt (AND/OR).
in	*wom_dur*	Number of overthreshold events to wait before generating interrupt.

Returns

0 on success, negative value on error.

6.3.4.2 inv_imu_adv_convert_odr_bitfield_to_us()

```
uint32_t inv_imu_adv_convert_odr_bitfield_to_us (
            uint32_t odr_bitfield )
```

Converts accel_config0_accel_odr_t or gyro_config0_gyro_odr_t enums to period expressed in us.

Parameters

in	*odr_bitfield*	An accel_config0_accel_odr_t or gyro_config0_gyro_odr_t enum

Returns

The corresponding period expressed in us

6.3.4.3 inv_imu_adv_device_reset()

```
int inv_imu_adv_device_reset (
            inv_imu_device_t * s )
```

Performs a soft reset of the device.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.4 inv_imu_adv_disable_accel()

```
int inv_imu_adv_disable_accel (
            inv_imu_device_t * s )
```

Disable accel.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.5 inv_imu_adv_disable_gyro()

```
int inv_imu_adv_disable_gyro (
            inv_imu_device_t * s )
```

Disable gyro.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.6 inv_imu_adv_disable_wom()

```
int inv_imu_adv_disable_wom (
            inv_imu_device_t * s )
```

Disable Wake On Motion.

note : Fifo water-mark interrupt is re-enabled when WoM is disabled.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.7 inv_imu_adv_enable_accel_ln()

```
int inv_imu_adv_enable_accel_ln (
            inv_imu_device_t * s )
```

Enable accel in low noise mode.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.8 inv_imu_adv_enable_accel_lp()

```
int inv_imu_adv_enable_accel_lp (
            inv_imu_device_t * s )
```

Enable accel in low power mode.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.9 inv_imu_adv_enable_gyro_ln()

```
int inv_imu_adv_enable_gyro_ln (
            inv_imu_device_t * s )
```

Enable gyro in low noise mode.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.10 inv_imu_adv_enable_gyro_lp()

```
int inv_imu_adv_enable_gyro_lp (
            inv_imu_device_t * s )
```

Enable gyro in low power mode.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.11 inv_imu_adv_enable_wom()

```
int inv_imu_adv_enable_wom (
            inv_imu_device_t * s )
```

Enable Wake On Motion.

note : WoM requests to have the accelerometer enabled to work. As a consequence Fifo water-mark interrupt is disabled to only trigger WoM interrupts. To have good performance, it's recommended to set accelerometer ODR (Output Data Rate) to 20ms and the accelerometer in Low Power Mode.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.12 inv_imu_adv_get_accel_fsr()

```
int inv_imu_adv_get_accel_fsr (
            inv_imu_device_t * s,
            accel_config0_accel_ui_fs_sel_t * accel_fsr )
```

Access accel full scale range.

Parameters

in	*s*	Pointer to device.
out	*accel_fsr*	Current full scale range.

Returns

0 on success, negative value on error.

6.3.4.13 inv_imu_adv_get_data_from_fifo()

```
int inv_imu_adv_get_data_from_fifo (
            inv_imu_device_t * s,
            uint8_t fifo_data[FIFO_MIRRORING_SIZE],
            uint16_t * fifo_count )
```

Read all available packets from the FIFO.

Parameters

in	*s*	Pointer to device.
out	*fifo_data*	Pointer to FIFO data buffer.
out	*fifo_count*	Number of packet read in FIFO.

Returns

0 on success, negative value on error.

6.3.4.14 inv_imu_adv_get_data_from_registers()

```
int inv_imu_adv_get_data_from_registers (
            inv_imu_device_t * s )
```

Read all registers containing data (temperature, accelerometer and gyroscope).

It will then call `sensor_event_cb` function provided in the `inv_imu_device_t` for each packet.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.15 inv_imu_adv_get_fifo_config()

```
int inv_imu_adv_get_fifo_config (
            inv_imu_device_t * s,
            inv_imu_adv_fifo_config_t * conf )
```

Retrieve FIFO configuration.

Parameters

in	*s*	Pointer to device.
in	*conf*	Structure that will be filled with current configuration.

Returns

0 on success, negative value on error.

6.3.4.16 inv_imu_adv_get_gyro_fsr()

```
int inv_imu_adv_get_gyro_fsr (
            inv_imu_device_t * s,
            gyro_config0_gyro_ui_fs_sel_t * gyro_fsr )
```

Access gyro full scale range.

Parameters

in	*s*	Pointer to device.
out	*gyro_fsr*	Current full scale range.

Returns

0 on success, negative value on error.

6.3.4.17 inv_imu_adv_get_timestamp_resolution_us()

```
uint32_t inv_imu_adv_get_timestamp_resolution_us (
            inv_imu_device_t * s )
```

Get timestamp resolution.

Parameters

in	*s*	Pointer to device.

Returns

Timestamp resolution in us, negative value on error

6.3.4.18 inv_imu_adv_init()

```
int inv_imu_adv_init (
            inv_imu_device_t * s )
```

Initializes device.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.19 inv_imu_adv_parse_fifo_data()

```
int inv_imu_adv_parse_fifo_data (
            inv_imu_device_t * s,
            const uint8_t fifo_data[FIFO_MIRRORING_SIZE],
            const uint16_t fifo_count )
```

Parse packets from FIFO buffer.

For each packet function builds a sensor event containing packet data and validity information. Then it calls sensor↩ _event_cb funtion passed in parameter of inv_imu_init function for each packet.

Parameters

in	*s*	Pointer to device.
in	*fifo_data*	Pointer to FIFO data buffer.
in	*fifo_count*	Number of packet read in FIFO.

Returns

0 on success, negative value on error.

6.3.4.20 inv_imu_adv_power_down_sram()

```
int inv_imu_adv_power_down_sram (
            inv_imu_device_t * s )
```

Power-down the SRAM.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.21 inv_imu_adv_power_up_sram()

```
int inv_imu_adv_power_up_sram (
            inv_imu_device_t * s )
```

Power-up the SRAM.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.22 inv_imu_adv_reset_fifo()

```
int inv_imu_adv_reset_fifo (
            inv_imu_device_t * s )
```

reset IMU fifo

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.3.4.23 inv_imu_adv_set_endianness()

```
int inv_imu_adv_set_endianness (
            inv_imu_device_t * s,
            sreg_ctrl_sreg_data_endian_sel_t endianness )
```

Set the UI endianness and set the inv_device endianness field.

Parameters

in	*s*	Pointer to device.
in	*endianness*	Requested endianness value.

Returns

0 on success, negative value on error.

6.3.4.24 inv_imu_adv_set_fifo_config()

```
int inv_imu_adv_set_fifo_config (
            inv_imu_device_t * s,
            const inv_imu_adv_fifo_config_t * conf )
```

Set FIFO configuration.

Parameters

in	*s*	Pointer to device.
in	*conf*	Structure containing the requested configuration.

Returns

0 on success, negative value on error.

6.3.4.25 inv_imu_adv_set_timestamp_resolution()

```
int inv_imu_adv_set_timestamp_resolution (
            inv_imu_device_t * s,
            const tmst_wom_config_tmst_resol_t timestamp_resol )
```

Set timestamp resolution.

Parameters

in	*s*	Pointer to device.
in	*timestamp_resol*	Requested timestamp resolution

Returns

0 on success, negative value on error.

6.4 EDMP

API to drive eDMP features.

Files

- file inv_imu_edmp.h

Classes

- struct inv_imu_edmp_int_state_t
  APEX interrupts definition.
- struct int_apex_statusx_t
  Registers to retrieve interrupts status for APEX.
- struct int_apex_configx_t
  Registers to configure interrupts for APEX.
- struct edmp_apex_enx_t
  Registers to enable APEX features.
- struct inv_imu_edmp_apex_parameters_t
  IMU APEX inputs parameters definition.
- struct inv_imu_edmp_pedometer_data_t
  Pedometer outputs.
- struct inv_imu_edmp_tap_data_t
  Tap outputs.

Macros

- #define INV_IMU_WRITE_EDMP_SRAM(s, name, val) inv_imu_write_sram(s, (uint32_t)name, name##_↩ SIZE, val)
  Writes in EDMP SRAM.
- #define INV_IMU_READ_EDMP_SRAM(s, name, val) inv_imu_read_sram(s, (uint32_t)name, name##_↩ SIZE, val)
  Reads in EDMP SRAM.

Enumerations

- enum inv_imu_edmp_int_t { INV_IMU_EDMP_INT0 = 0 , INV_IMU_EDMP_INT1 , INV_IMU_EDMP_INT2 }
  EDMP input interrupt lines definition.
- enum inv_imu_edmp_activity_class_t { INV_IMU_EDMP_UNKNOWN = 0 , INV_IMU_EDMP_WALK = 1 , INV_IMU_EDMP_RUN = 2 }
  Pedometer activity class.
- enum inv_imu_edmp_tap_num_t { INV_IMU_EDMP_TAP_DOUBLE = 0x02 , INV_IMU_EDMP_TAP_SINGLE = 0x01 }
  Tap number definition.
- enum inv_imu_edmp_tap_axis_t { INV_IMU_EDMP_TAP_AXIS_Z = 0x02 , INV_IMU_EDMP_TAP_AXIS_Y = 0x01 , INV_IMU_EDMP_TAP_AXIS_X = 0x00 }
  Tap axis definition.
- enum inv_imu_edmp_tap_dir_t { INV_IMU_EDMP_TAP_DIR_POSITIVE = 0x01 , INV_IMU_EDMP_TAP_DIR_NEGATIVE = 0x00 }
  Tap direction definition.

Functions

- int inv_imu_edmp_set_frequency (inv_imu_device_t *s, const dmp_ext_sen_odr_cfg_apex_odr_t frequency)

  Configure EDMP Output Data Rate.
- int inv_imu_edmp_init_apex (inv_imu_device_t *s)

  Initialize EDMP APEX algorithms.
- int inv_imu_edmp_recompute_apex_decimation (inv_imu_device_t *s)

  Recompute EDMP APEX algorithms internal decimator based on new EDMP output Data Rate configured with `inv_imu_edmp_set_frequency`.
- int inv_imu_edmp_get_apex_parameters (inv_imu_device_t *s, inv_imu_edmp_apex_parameters_t *p)

  Returns current EDMP parameters for APEX algorithms.
- int inv_imu_edmp_set_apex_parameters (inv_imu_device_t *s, const inv_imu_edmp_apex_parameters_t *p)

  Configures EDMP parameters for APEX algorithms.
- int inv_imu_edmp_get_config_int_apex (inv_imu_device_t *s, inv_imu_edmp_int_state_t *it)

  Retrieve interrupts configuration.
- int inv_imu_edmp_set_config_int_apex (inv_imu_device_t *s, const inv_imu_edmp_int_state_t *it)

  Configure APEX interrupt.
- int inv_imu_edmp_enable (inv_imu_device_t *s)

  Enable EDMP.
- int inv_imu_edmp_disable (inv_imu_device_t *s)

  Disable EDMP.
- int inv_imu_edmp_enable_pedometer (inv_imu_device_t *s)

  Enable APEX algorithm Pedometer.
- int inv_imu_edmp_disable_pedometer (inv_imu_device_t *s)

  Disable APEX algorithm Pedometer.
- int inv_imu_edmp_enable_smd (inv_imu_device_t *s)

  Enable APEX algorithm Significant Motion Detection.
- int inv_imu_edmp_disable_smd (inv_imu_device_t *s)

  Disable APEX algorithm Significant Motion Detection.
- int inv_imu_edmp_enable_tilt (inv_imu_device_t *s)

  Enable APEX algorithm Tilt.
- int inv_imu_edmp_disable_tilt (inv_imu_device_t *s)

  Disable APEX algorithm Tilt.
- int inv_imu_edmp_enable_r2w (inv_imu_device_t *s)

  Enable APEX algorithm R2W.
- int inv_imu_edmp_disable_r2w (inv_imu_device_t *s)

  Disable APEX algorithm R2W.
- int inv_imu_edmp_enable_tap (inv_imu_device_t *s)

  Enable APEX algorithm Tap.
- int inv_imu_edmp_disable_tap (inv_imu_device_t *s)

  Disable APEX algorithm Tap.
- int inv_imu_edmp_enable_ff (inv_imu_device_t *s)

  Enable APEX algorithm Free Fall.
- int inv_imu_edmp_disable_ff (inv_imu_device_t *s)

  Disable APEX algorithm Free Fall.
- int inv_imu_edmp_get_int_apex_status (inv_imu_device_t *s, inv_imu_edmp_int_state_t *it)

  Read APEX interrupt status.
- int inv_imu_edmp_get_pedometer_data (inv_imu_device_t *s, inv_imu_edmp_pedometer_data_t *data)

  Retrieve pedometer outputs.
- int inv_imu_edmp_get_ff_data (inv_imu_device_t *s, uint16_t *freefall_duration)

  Retrieve APEX free fall outputs and format them.

- int inv_imu_edmp_get_tap_data (inv_imu_device_t *s, inv_imu_edmp_tap_data_t *data)

  Retrieve tap outputs.
- int inv_imu_edmp_mask_int_src (inv_imu_device_t *s, inv_imu_edmp_int_t edmp_int_nb, uint8_t int_mask)

  Mask requested interrupt sources for edmp interrupt line passed in parameter.
- int inv_imu_edmp_unmask_int_src (inv_imu_device_t *s, inv_imu_edmp_int_t edmp_int_nb, uint8_t int_mask)

  Unmask requested interrupt sources for edmp interrupt line passed in parameter.
- int inv_imu_edmp_configure (inv_imu_device_t *s)

  Setup EDMP to execute code in ROM.
- int inv_imu_edmp_run_ondemand (inv_imu_device_t *s, inv_imu_edmp_int_t edmp_int_nb)

  Run EDMP using the on-demand mechanism.
- int inv_imu_edmp_wait_for_idle (inv_imu_device_t *s)

  Wait until EDMP idle bit is set (means EDMP execution is completed).

6.4.1 Detailed Description

API to drive eDMP features.

6.4.2 Macro Definition Documentation

6.4.2.1 INV_IMU_READ_EDMP_SRAM

```
#define INV_IMU_READ_EDMP_SRAM(
              s,
              name,
              val ) inv_imu_read_sram(s, (uint32_t)name, name##_SIZE, val)
```

Reads in EDMP SRAM.

Parameters

in	*s*	Pointer to device.
in	*name*	Name of the parameter.
in	*val*	Value to be read.

Returns

0 on success, negative value on error.

6.4.2.2 INV_IMU_WRITE_EDMP_SRAM

```
#define INV_IMU_WRITE_EDMP_SRAM(
              s,
```

```
name,
val )  inv_imu_write_sram(s, (uint32_t)name, name##_SIZE, val)
```

Writes in EDMP SRAM.

Parameters

in	*s*	Pointer to device.
in	*name*	Name of the parameter.
in	*val*	Value to be written.

Returns

0 on success, negative value on error.

6.4.3 Enumeration Type Documentation

6.4.3.1 inv_imu_edmp_activity_class_t

```
enum inv_imu_edmp_activity_class_t
```

Pedometer activity class.

Enumerator

INV_IMU_EDMP_UNKNOWN	
INV_IMU_EDMP_WALK	
INV_IMU_EDMP_RUN	

6.4.3.2 inv_imu_edmp_int_t

```
enum inv_imu_edmp_int_t
```

EDMP input interrupt lines definition.

Enumerator

INV_IMU_EDMP_INT0	
INV_IMU_EDMP_INT1	
INV_IMU_EDMP_INT2	

6.4.3.3 inv_imu_edmp_tap_axis_t

`enum inv_imu_edmp_tap_axis_t`

Tap axis definition.

Enumerator

INV_IMU_EDMP_TAP_AXIS_Z	
INV_IMU_EDMP_TAP_AXIS_Y	
INV_IMU_EDMP_TAP_AXIS_X	

6.4.3.4 inv_imu_edmp_tap_dir_t

`enum inv_imu_edmp_tap_dir_t`

Tap direction definition.

Enumerator

INV_IMU_EDMP_TAP_DIR_POSITIVE	
INV_IMU_EDMP_TAP_DIR_NEGATIVE	

6.4.3.5 inv_imu_edmp_tap_num_t

`enum inv_imu_edmp_tap_num_t`

Tap number definition.

Enumerator

INV_IMU_EDMP_TAP_DOUBLE	
INV_IMU_EDMP_TAP_SINGLE	

6.4.4 Function Documentation

6.4.4.1 inv_imu_edmp_configure()

```
int inv_imu_edmp_configure (
            inv_imu_device_t * s )
```

Setup EDMP to execute code in ROM.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.4.4.2 inv_imu_edmp_disable()

```
int inv_imu_edmp_disable (
            inv_imu_device_t * s )
```

Disable EDMP.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.4.4.3 inv_imu_edmp_disable_ff()

```
int inv_imu_edmp_disable_ff (
            inv_imu_device_t * s )
```

Disable APEX algorithm Free Fall.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.4.4.4 inv_imu_edmp_disable_pedometer()

```
int inv_imu_edmp_disable_pedometer (
            inv_imu_device_t * s )
```

Disable APEX algorithm Pedometer.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.4.4.5 inv_imu_edmp_disable_r2w()

```
int inv_imu_edmp_disable_r2w (
            inv_imu_device_t * s )
```

Disable APEX algorithm R2W.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.4.4.6 inv_imu_edmp_disable_smd()

```
int inv_imu_edmp_disable_smd (
            inv_imu_device_t * s )
```

Disable APEX algorithm Significant Motion Detection.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.4.4.7 inv_imu_edmp_disable_tap()

```
int inv_imu_edmp_disable_tap (
            inv_imu_device_t * s )
```

Disable APEX algorithm Tap.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.4.4.8 inv_imu_edmp_disable_tilt()

```
int inv_imu_edmp_disable_tilt (
            inv_imu_device_t * s )
```

Disable APEX algorithm Tilt.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.4.4.9 inv_imu_edmp_enable()

```
int inv_imu_edmp_enable (
            inv_imu_device_t * s )
```

Enable EDMP.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.4.4.10 inv_imu_edmp_enable_ff()

```
int inv_imu_edmp_enable_ff (
            inv_imu_device_t * s )
```

Enable APEX algorithm Free Fall.

Parameters

in	*s*	Pointer to device.

Returns

0 on success INV_IMU_ERROR_EDMP_ODR if user should have called inv_imu_edmp_recompute_apex_decimatio other negative value on error.

6.4.4.11 inv_imu_edmp_enable_pedometer()

```
int inv_imu_edmp_enable_pedometer (
            inv_imu_device_t * s )
```

Enable APEX algorithm Pedometer.

Parameters

in	*s*	Pointer to device.

Returns

0 on success INV_IMU_ERROR_EDMP_ODR if user should have called inv_imu_edmp_recompute_apex_decimatio other negative value on error.

6.4.4.12 inv_imu_edmp_enable_r2w()

```
int inv_imu_edmp_enable_r2w (
            inv_imu_device_t * s )
```

Enable APEX algorithm R2W.

Parameters

in	*s*	Pointer to device.

Returns

0 on success INV_IMU_ERROR_EDMP_ODR if user should have called inv_imu_edmp_recompute_apex_decimatio other negative value on error.

6.4.4.13 inv_imu_edmp_enable_smd()

```
int inv_imu_edmp_enable_smd (
            inv_imu_device_t * s )
```

Enable APEX algorithm Significant Motion Detection.

Parameters

in	*s*	Pointer to device.

Returns

0 on success INV_IMU_ERROR_EDMP_ODR if user should have called inv_imu_edmp_recompute_apex_decimatio other negative value on error.

6.4.4.14 inv_imu_edmp_enable_tap()

```
int inv_imu_edmp_enable_tap (
            inv_imu_device_t * s )
```

Enable APEX algorithm Tap.

Parameters

in	*s*	Pointer to device.

Returns

0 on success INV_IMU_ERROR_EDMP_ODR if user should have called inv_imu_edmp_recompute_apex_decimatio other negative value on error.

6.4.4.15 inv_imu_edmp_enable_tilt()

```
int inv_imu_edmp_enable_tilt (
            inv_imu_device_t * s )
```

Enable APEX algorithm Tilt.

Parameters

in	*s*	Pointer to device.

Returns

0 on success INV_IMU_ERROR_EDMP_ODR if user should have called inv_imu_edmp_recompute_apex_decimatio other negative value on error.

6.4.4.16 inv_imu_edmp_get_apex_parameters()

```
int inv_imu_edmp_get_apex_parameters (
            inv_imu_device_t * s,
            inv_imu_edmp_apex_parameters_t * p )
```

Returns current EDMP parameters for APEX algorithms.

Parameters

in	*s*	Pointer to device.
out	*p*	The current parameters read from registers.

Returns

0 on success, negative value on error.

6.4.4.17 inv_imu_edmp_get_config_int_apex()

```
int inv_imu_edmp_get_config_int_apex (
            inv_imu_device_t * s,
            inv_imu_edmp_int_state_t * it )
```

Retrieve interrupts configuration.

Parameters

in	*s*	Pointer to device.
out	*it*	Configuration of each APEX interrupt.

Returns

0 on success, negative value on error.

6.4.4.18 inv_imu_edmp_get_ff_data()

```
int inv_imu_edmp_get_ff_data (
            inv_imu_device_t * s,
            uint16_t * freefall_duration )
```

Retrieve APEX free fall outputs and format them.

Parameters

in	*s*	Pointer to device.
out	*freefall_duration*	Duration in number of sample.

Returns

0 on success, negative value on error.

6.4.4.19 inv_imu_edmp_get_int_apex_status()

```
int inv_imu_edmp_get_int_apex_status (
            inv_imu_device_t * s,
            inv_imu_edmp_int_state_t * it )
```

Read APEX interrupt status.

Parameters

in	*s*	Pointer to device.
out	*it*	Status of each APEX interrupt.

Returns

0 on success, negative value on error.

6.4.4.20 inv_imu_edmp_get_pedometer_data()

```
int inv_imu_edmp_get_pedometer_data (
              inv_imu_device_t * s,
              inv_imu_edmp_pedometer_data_t * data )
```

Retrieve pedometer outputs.

Parameters

in	*s*	Pointer to device.
out	*data*	Pedometer step count and activity data value.

Returns

0 on success, negative value on error.

Return values

INV_IMU_ERROR_EDMP_BUF_EMPTY	if step count buffer is empty.

6.4.4.21 inv_imu_edmp_get_tap_data()

```
int inv_imu_edmp_get_tap_data (
              inv_imu_device_t * s,
              inv_imu_edmp_tap_data_t * data )
```

Retrieve tap outputs.

Parameters

in	*s*	Pointer to device.
out	*data*	Tap number and direction.

Returns

0 on success, negative value on error.

6.4.4.22 inv_imu_edmp_init_apex()

```
int inv_imu_edmp_init_apex (
              inv_imu_device_t * s )
```

Initialize EDMP APEX algorithms.

This function should be called before calling any other function (except for `inv_imu_edmp_set_frequency`).

Warning

This function will power-up the SRAM. For power consumption consideration, you can manually call `inv_imu_adv_power_down_sram` if you don't need to preserve SRAM content.

This function will reset all interrupt masks previously set with `inv_imu_edmp_unmask_int_src` and exit with `EDMP_INT_SRC_ACCEL_DRDY_MASK` unmasked on `INV_IMU_EDMP_INT0`.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error or if EDMP is enabled.

6.4.4.23 inv_imu_edmp_mask_int_src()

```
int inv_imu_edmp_mask_int_src (
              inv_imu_device_t * s,
              inv_imu_edmp_int_t edmp_int_nb,
              uint8_t int_mask )
```

Mask requested interrupt sources for edmp interrupt line passed in parameter.

Parameters

in	*s*	Pointer to device.
in	*edmp_int_nb*	EDMP input interrupt line number that should be configured.
in	*int_mask*	Interrupt sources to mask.

Returns

0 on success, negative value on error.

6.4.4.24 inv_imu_edmp_recompute_apex_decimation()

```
int inv_imu_edmp_recompute_apex_decimation (
              inv_imu_device_t * s )
```

Recompute EDMP APEX algorithms internal decimator based on new EDMP output Data Rate configured with `inv_imu_edmp_set_frequency`.

Warning

It is up to application level to save/restore previously configured APEX parameters, if any, with `inv_imu_edmp_set_apex_parameters`.

EDMP must be disabled before calling this function.

This function will reset all interrupt masks previously set with `inv_imu_edmp_unmask_int_src` and exit with `EDMP_INT_SRC_ACCEL_DRDY_MASK` unmasked on `INV_IMU_EDMP_INT0`.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error or if EDMP is enabled.

6.4.4.25 inv_imu_edmp_run_ondemand()

```
int inv_imu_edmp_run_ondemand (
            inv_imu_device_t * s,
            inv_imu_edmp_int_t edmp_int_nb )
```

Run EDMP using the on-demand mechanism.

Parameters

in	*s*	Pointer to device.
in	*edmp_int_nb*	EDMP input interrupt line.

Returns

0 on success, negative value on error.

6.4.4.26 inv_imu_edmp_set_apex_parameters()

```
int inv_imu_edmp_set_apex_parameters (
            inv_imu_device_t * s,
            const inv_imu_edmp_apex_parameters_t * p )
```

Configures EDMP parameters for APEX algorithms.

Warning

This function should be called only when all EDMP algorithms are disabled.

Parameters

in	*s*	Pointer to device.
in	*p*	The requested input parameters.

Returns

0 on success, negative value on error.

6.4.4.27 inv_imu_edmp_set_config_int_apex()

```
int inv_imu_edmp_set_config_int_apex (
            inv_imu_device_t * s,
            const inv_imu_edmp_int_state_t * it )
```

Configure APEX interrupt.

Parameters

in	*s*	Pointer to device.
in	*it*	State of each APEX interrupt to configure.

Returns

0 on success, negative value on error.

6.4.4.28 inv_imu_edmp_set_frequency()

```
int inv_imu_edmp_set_frequency (
            inv_imu_device_t * s,
            const dmp_ext_sen_odr_cfg_apex_odr_t frequency )
```

Configure EDMP Output Data Rate.

Warning

Accel frequency must be higher or equal to EDMP frequency.

If inv_imu_edmp_init_apex() was already called, application should call `inv_imu_edmp_recompute_apex_decimatio` afterwards if APEX algorithms are to be run.

Parameters

in	*s*	Pointer to device.
in	*frequency*	The requested frequency.

Returns

0 on success, negative value on error.

6.4.4.29 inv_imu_edmp_unmask_int_src()

```
int inv_imu_edmp_unmask_int_src (
              inv_imu_device_t * s,
              inv_imu_edmp_int_t edmp_int_nb,
              uint8_t int_mask )
```

Unmask requested interrupt sources for edmp interrupt line passed in parameter.

Parameters

in	*s*	Pointer to device.
in	*edmp_int_nb*	EDMP input interrupt line number that should be configured.
in	*int_mask*	Interrupt sources to unmask.

Returns

0 on success, negative value on error.

6.4.4.30 inv_imu_edmp_wait_for_idle()

```
int inv_imu_edmp_wait_for_idle (
              inv_imu_device_t * s )
```

Wait until EDMP idle bit is set (means EDMP execution is completed).

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.5 EDMP Wearable

High-level functions to drive eDMP Wearable features.

Files

- file inv_imu_edmp_wearable.h

Classes

- struct inv_imu_edmp_b2s_parameters_t

  IMU B2S parameters definition.

Functions

- int inv_imu_edmp_b2s_init (inv_imu_device_t *s)

  Initialize B2S algorithm.
- int inv_imu_edmp_b2s_get_parameters (inv_imu_device_t *s, inv_imu_edmp_b2s_parameters_t *b2s_params)

  Get current B2S configuration settings.
- int inv_imu_edmp_b2s_set_parameters (inv_imu_device_t *s, const inv_imu_edmp_b2s_parameters_t *b2s_params)

  Set new B2S configuration settings.
- int inv_imu_edmp_b2s_enable (inv_imu_device_t *s)

  Enable APEX algorithm B2S.
- int inv_imu_edmp_b2s_disable (inv_imu_device_t *s)

  Disable APEX algorithm B2S.

6.5.1 Detailed Description

High-level functions to drive eDMP Wearable features.

6.5.2 Function Documentation

6.5.2.1 inv_imu_edmp_b2s_disable()

```
int inv_imu_edmp_b2s_disable (
            inv_imu_device_t * s )
```

Disable APEX algorithm B2S.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.5.2.2 inv_imu_edmp_b2s_enable()

```
int inv_imu_edmp_b2s_enable (
            inv_imu_device_t * s )
```

Enable APEX algorithm B2S.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.5.2.3 inv_imu_edmp_b2s_get_parameters()

```
int inv_imu_edmp_b2s_get_parameters (
            inv_imu_device_t * s,
            inv_imu_edmp_b2s_parameters_t * b2s_params )
```

Get current B2S configuration settings.

Parameters

in	*s*	Pointer to device.
out	*b2s_params*	Pointer to B2S configuration structure, which will hold current B2S configuration.

Returns

0 on success, negative value on error.

6.5.2.4 inv_imu_edmp_b2s_init()

```
int inv_imu_edmp_b2s_init (
            inv_imu_device_t * s )
```

Initialize B2S algorithm.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

6.5.2.5 inv_imu_edmp_b2s_set_parameters()

```
int inv_imu_edmp_b2s_set_parameters (
            inv_imu_device_t * s,
            const inv_imu_edmp_b2s_parameters_t * b2s_params )
```

Set new B2S configuration settings.

Parameters

in	*s*	Pointer to device.
in	*b2s_params*	Pointer to B2S configuration structure, which contains new B2S configuration.

Returns

0 on success, negative value on error.

6.6 Self-test

API to execute self-test procedure.

Files

- file inv_imu_selftest.h

Classes

- struct inv_imu_selftest_parameters_t

  Self-Test parameters.
- struct inv_imu_selftest_output_t

  Self-test outputs.

Macros

- #define INV_IMU_ST_STATUS_SUCCESS 1

  Indicates test is successful.
- #define INV_IMU_ST_STATUS_FAIL -1

  Indicates test is failing.
- #define INV_IMU_ST_STATUS_NOT_RUN 0

  Indicates test has not run.

Functions

- int inv_imu_selftest_init_params (inv_imu_device_t ∗s, inv_imu_selftest_parameters_t ∗st_params)

  Provide recommended parameters to execute self-test.
- int inv_imu_selftest (inv_imu_device_t ∗s, const inv_imu_selftest_parameters_t ∗st_params, inv_imu_selftest_output_t ∗st_output)

  Perform hardware self-test for Accel and/or Gyro.

6.6.1 Detailed Description

API to execute self-test procedure.

6.6.2 Macro Definition Documentation

6.6.2.1 INV_IMU_ST_STATUS_FAIL

```
#define INV_IMU_ST_STATUS_FAIL -1
```

Indicates test is failing.

6.6.2.2 INV_IMU_ST_STATUS_NOT_RUN

```
#define INV_IMU_ST_STATUS_NOT_RUN 0
```

Indicates test has not run.

6.6.2.3 INV_IMU_ST_STATUS_SUCCESS

```
#define INV_IMU_ST_STATUS_SUCCESS 1
```

Indicates test is successful.

6.6.3 Function Documentation

6.6.3.1 inv_imu_selftest()

```
int inv_imu_selftest (
            inv_imu_device_t * s,
            const inv_imu_selftest_parameters_t * st_params,
            inv_imu_selftest_output_t * st_output )
```

Perform hardware self-test for Accel and/or Gyro.

Parameters

in	*s*	Pointer to device.
in	*st_params*	Self-test parameters to be used.
out	*st_output*	Output from Self-test operation.

Returns

0 on success, negative value on error.

6.6.3.2 inv_imu_selftest_init_params()

```
int inv_imu_selftest_init_params (
            inv_imu_device_t * s,
            inv_imu_selftest_parameters_t * st_params )
```

Provide recommended parameters to execute self-test.

Parameters

in	*s*	Pointer to device.
in	*st_params*	Structure filled with recommended params.

Returns

0 on success, negative value on error.

6.7 Transport

Abstraction layer to communicate with device.

Files

- file inv_imu_transport.h

Classes

- struct inv_imu_transport_t

  Structure dedicated to transport layer transport interface.

Macros

- #define UI_I2C 0

  identifies I2C interface.
- #define UI_SPI4 1

  identifies 4-wire SPI interface.
- #define UI_SPI3 2

  identifies 3-wire SPI interface.

Typedefs

- typedef int(∗ inv_imu_read_reg_t) (uint8_t reg, uint8_t ∗buf, uint32_t len)

  Function pointer to read register(s).
- typedef int(∗ inv_imu_write_reg_t) (uint8_t reg, const uint8_t ∗buf, uint32_t len)

  Function pointer to write register(s).
- typedef uint32_t inv_imu_serif_type_t

  Serif type definition.

Functions

- int inv_imu_read_reg (void ∗t, uint32_t reg, uint32_t len, uint8_t ∗buf)

  Reads data from a register on IMU.
- int inv_imu_write_reg (void ∗t, uint32_t reg, uint32_t len, const uint8_t ∗buf)

  Writes data to a register on IMU.
- int inv_imu_read_sram (void ∗t, uint32_t addr, uint32_t len, uint8_t ∗buf)

  Reads data from SRAM on IMU.
- int inv_imu_write_sram (void ∗t, uint32_t addr, uint32_t len, const uint8_t ∗buf)

  Writes data to SRAM on IMU.

6.7.1 Detailed Description

Abstraction layer to communicate with device.

6.7.2 Macro Definition Documentation

6.7.2.1 UI_I2C

```
#define UI_I2C 0
```

identifies I2C interface.

6.7.2.2 UI_SPI3

```
#define UI_SPI3 2
```

identifies 3-wire SPI interface.

6.7.2.3 UI_SPI4

```
#define UI_SPI4 1
```

identifies 4-wire SPI interface.

6.7.3 Typedef Documentation

6.7.3.1 inv_imu_read_reg_t

```
typedef int(* inv_imu_read_reg_t) (uint8_t reg, uint8_t *buf, uint32_t len)
```

Function pointer to read register(s).

Parameters

in	*reg*	Register address to be read.
out	*buf*	Output data from the register.
in	*len*	Number of byte to be read.

Returns

0 on success, negative value on error.

6.7.3.2 inv_imu_serif_type_t

```
typedef uint32_t inv_imu_serif_type_t
```

Serif type definition.

Deprecated Kept for retrocompatibility. Replaced with `uint32_t` type in `inv_imu_transport_t` struct.

6.7.3.3 inv_imu_write_reg_t

```
typedef int(* inv_imu_write_reg_t) (uint8_t reg, const uint8_t *buf, uint32_t len)
```

Function pointer to write register(s).

Parameters

in	*reg*	Register address to be written.
in	*buf*	Input data to write.
in	*len*	Number of byte to be written.

Returns

0 on success, negative value on error.

6.7.4 Function Documentation

6.7.4.1 inv_imu_read_reg()

```
int inv_imu_read_reg (
            void * t,
            uint32_t reg,
            uint32_t len,
            uint8_t * buf )
```

Reads data from a register on IMU.

Parameters

in	*t*	Pointer to transport (as void ∗ so it can be called from any module).
in	*reg*	Register address to be read.
in	*len*	Number of byte to be read.
out	*buf*	Output data from the register.

Returns

0 on success, negative value on error.

6.7.4.2 inv_imu_read_sram()

```
int inv_imu_read_sram (
            void * t,
            uint32_t addr,
            uint32_t len,
            uint8_t * buf )
```

Reads data from SRAM on IMU.

Parameters

in	*t*	Pointer to transport (as void * so it can be called from any module).
in	*addr*	Address to be read.
in	*len*	Number of byte to be read.
out	*buf*	Output data from the register.

Returns

0 on success, negative value on error.

6.7.4.3 inv_imu_write_reg()

```
int inv_imu_write_reg (
            void * t,
            uint32_t reg,
            uint32_t len,
            const uint8_t * buf )
```

Writes data to a register on IMU.

Parameters

in	*t*	Pointer to transport (as void * so it can be called from any module).
in	*reg*	Register address to be written.
in	*len*	Number of byte to be written.
in	*buf*	Input data to write.

Returns

0 on success, negative value on error.

6.7.4.4 inv_imu_write_sram()

```
int inv_imu_write_sram (
            void * t,
            uint32_t addr,
            uint32_t len,
            const uint8_t * buf )
```

Writes data to SRAM on IMU.

Parameters

in	*t*	Pointer to transport (as void * so it can be called from any module).
in	*addr*	Address to be written.
in	*len*	Number of byte to be written.
in	*buf*	Input data to write.

Returns

0 on success, negative value on error.

Chapter 7

Class Documentation

7.1 accel_config0_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t accel_odr: 4
- uint8_t accel_ui_fs_sel: 3
- uint8_t resv_1: 1

7.1.1 Member Data Documentation

7.1.1.1 accel_odr

`uint8_t accel_config0_t::accel_odr`

7.1.1.2 accel_ui_fs_sel

`uint8_t accel_config0_t::accel_ui_fs_sel`

7.1.1.3 resv_1

`uint8_t accel_config0_t::resv_1`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.2 accel_wom_x_thr_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t wom_x_th: 8

7.2.1 Member Data Documentation

7.2.1.1 wom_x_th

`uint8_t accel_wom_x_thr_t::wom_x_th`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.3 accel_wom_y_thr_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t wom_y_th: 8

7.3.1 Member Data Documentation

7.3.1.1 wom_y_th

`uint8_t accel_wom_y_thr_t::wom_y_th`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.4 accel_wom_z_thr_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t wom_z_th: 8

7.4.1 Member Data Documentation

7.4.1.1 wom_z_th

`uint8_t accel_wom_z_thr_t::wom_z_th`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.5 apex_buffer_mgmt_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t step_count_edmp_wptr: 2
- uint8_t step_count_host_rptr: 2
- uint8_t ff_duration_edmp_wptr: 2
- uint8_t ff_duration_host_rptr: 2

7.5.1 Member Data Documentation

7.5.1.1 ff_duration_edmp_wptr

`uint8_t apex_buffer_mgmt_t::ff_duration_edmp_wptr`

7.5.1.2 ff_duration_host_rptr

```
uint8_t apex_buffer_mgmt_t::ff_duration_host_rptr
```

7.5.1.3 step_count_edmp_wptr

```
uint8_t apex_buffer_mgmt_t::step_count_edmp_wptr
```

7.5.1.4 step_count_host_rptr

```
uint8_t apex_buffer_mgmt_t::step_count_host_rptr
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.6 dmp_ext_sen_odr_cfg_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t apex_odr: 3
- uint8_t ext_odr: 3
- uint8_t ext_sensor_en: 1
- uint8_t resv_1: 1

7.6.1 Member Data Documentation

7.6.1.1 apex_odr

```
uint8_t dmp_ext_sen_odr_cfg_t::apex_odr
```

7.6.1.2 ext_odr

```
uint8_t dmp_ext_sen_odr_cfg_t::ext_odr
```

7.6.1.3 ext_sensor_en

```
uint8_t dmp_ext_sen_odr_cfg_t::ext_sensor_en
```

7.6.1.4 resv_1

```
uint8_t dmp_ext_sen_odr_cfg_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.7 drive_config0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t virtual_access_aux2_en: 1
- uint8_t pads_spi_slew: 3
- uint8_t pads_i2c_slew: 3
- uint8_t resv_1: 1

7.7.1 Member Data Documentation

7.7.1.1 pads_i2c_slew

```
uint8_t drive_config0_t::pads_i2c_slew
```

7.7.1.2 pads_spi_slew

```
uint8_t drive_config0_t::pads_spi_slew
```

7.7.1.3 resv_1

```
uint8_t drive_config0_t::resv_1
```

7.7.1.4 virtual_access_aux2_en

```
uint8_t drive_config0_t::virtual_access_aux2_en
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.8 drive_config1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t pads_i3c_sdr_slew: 3
- uint8_t pads_i3c_ddr_slew: 3
- uint8_t resv_1: 2

7.8.1 Member Data Documentation

7.8.1.1 pads_i3c_ddr_slew

```
uint8_t drive_config1_t::pads_i3c_ddr_slew
```

7.8.1.2 pads_i3c_sdr_slew

```
uint8_t drive_config1_t::pads_i3c_sdr_slew
```

7.8.1.3 resv_1

```
uint8_t drive_config1_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.9 drive_config2_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t pads_slew: 3
- uint8_t resv_1: 5

7.9.1 Member Data Documentation

7.9.1.1 pads_slew

```
uint8_t drive_config2_t::pads_slew
```

7.9.1.2 resv_1

```
uint8_t drive_config2_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.10 edmp_apex_en0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t tap_en: 1
- uint8_t reserved0: 1
- uint8_t reserved1: 1
- uint8_t tilt_en: 1
- uint8_t pedo_en: 1
- uint8_t ff_en: 1
- uint8_t r2w_en: 1
- uint8_t smd_en: 1

7.10.1 Member Data Documentation

7.10.1.1 ff_en

```
uint8_t edmp_apex_en0_t::ff_en
```

7.10.1.2 pedo_en

```
uint8_t edmp_apex_en0_t::pedo_en
```

7.10.1.3 r2w_en

```
uint8_t edmp_apex_en0_t::r2w_en
```

7.10.1.4 reserved0

```
uint8_t edmp_apex_en0_t::reserved0
```

7.10.1.5 reserved1

```
uint8_t edmp_apex_en0_t::reserved1
```

7.10.1.6 smd_en

```
uint8_t edmp_apex_en0_t::smd_en
```

7.10.1.7 tap_en

```
uint8_t edmp_apex_en0_t::tap_en
```

7.10.1.8 tilt_en

```
uint8_t edmp_apex_en0_t::tilt_en
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.11 edmp_apex_en1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t soft_hard_iron_corr_en: 1
- uint8_t init_en: 1
- uint8_t power_save_en: 1
- uint8_t basic_smd_en: 1
- uint8_t resv_1: 1
- uint8_t feature3_en: 1
- uint8_t edmp_enable: 1
- uint8_t resv_2: 1

7.11.1 Member Data Documentation

7.11.1.1 basic_smd_en

```
uint8_t edmp_apex_en1_t::basic_smd_en
```

7.11.1.2 edmp_enable

```
uint8_t edmp_apex_en1_t::edmp_enable
```

7.11.1.3 feature3_en

```
uint8_t edmp_apex_en1_t::feature3_en
```

7.11.1.4 init_en

```
uint8_t edmp_apex_en1_t::init_en
```

7.11.1.5 power_save_en

```
uint8_t edmp_apex_en1_t::power_save_en
```

7.11.1.6 resv_1

```
uint8_t edmp_apex_en1_t::resv_1
```

7.11.1.7 resv_2

```
uint8_t edmp_apex_en1_t::resv_2
```

7.11.1.8 soft_hard_iron_corr_en

```
uint8_t edmp_apex_en1_t::soft_hard_iron_corr_en
```

The documentation for this struct was generated from the following file:

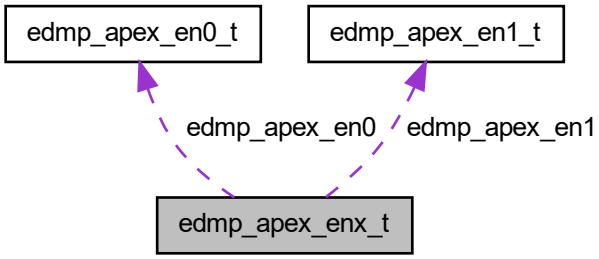
- inv_imu_regmap_le.h

7.12 edmp_apex_enx_t Struct Reference

Registers to enable APEX features.

`#include <inv_imu_edmp.h>`

Collaboration diagram for edmp_apex_enx_t:



Public Attributes

- edmp_apex_en0_t edmp_apex_en0
- edmp_apex_en1_t edmp_apex_en1

7.12.1 Detailed Description

Registers to enable APEX features.

7.12.2 Member Data Documentation

7.12.2.1 edmp_apex_en0

`edmp_apex_en0_t edmp_apex_enx_t::edmp_apex_en0`

7.12.2.2 edmp_apex_en1

`edmp_apex_en1_t edmp_apex_enx_t::edmp_apex_en1`

The documentation for this struct was generated from the following file:

- inv_imu_edmp.h

7.13 edmp_sp_start_addr_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t edmp_sp_start_addr: 8

7.13.1 Member Data Documentation

7.13.1.1 edmp_sp_start_addr

`uint8_t edmp_sp_start_addr_t::edmp_sp_start_addr`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.14 fifo_comp_decode_t Union Reference

Describe the content of the FIFO Compression Decoding Tag.

`#include <inv_imu_defs.h>`

Public Attributes

- uint8_t Byte
- struct {
  uint8_t valid_samples_a: 4
  uint8_t valid_samples_g: 4
  } bits

7.14.1 Detailed Description

Describe the content of the FIFO Compression Decoding Tag.

7.14.2 Member Data Documentation

7.14.2.1

```
struct { ... } fifo_comp_decode_t::bits
```

7.14.2.2 Byte

```
uint8_t fifo_comp_decode_t::Byte
```

7.14.2.3 valid_samples_a

```
uint8_t fifo_comp_decode_t::valid_samples_a
```

7.14.2.4 valid_samples_g

```
uint8_t fifo_comp_decode_t::valid_samples_g
```

The documentation for this union was generated from the following file:

- inv_imu_defs.h

7.15 fifo_comp_header_t Union Reference

Describe the content of the FIFO header for compressed packets.

```
#include <inv_imu_defs.h>
```

Public Attributes

- uint8_t Byte
- struct {
  uint8_t tot_sample: 2
  uint8_t comp_ratio: 2
  uint8_t comp_frame: 1
  uint8_t gyro_bit: 1
  uint8_t accel_bit: 1
  uint8_t ext_header: 1
  } bits

7.15.1 Detailed Description

Describe the content of the FIFO header for compressed packets.

7.15.2 Member Data Documentation

7.15.2.1 accel_bit

```
uint8_t fifo_comp_header_t::accel_bit
```

7.15.2.2

```
struct { ... } fifo_comp_header_t::bits
```

7.15.2.3 Byte

```
uint8_t fifo_comp_header_t::Byte
```

7.15.2.4 comp_frame

```
uint8_t fifo_comp_header_t::comp_frame
```

7.15.2.5 comp_ratio

```
uint8_t fifo_comp_header_t::comp_ratio
```

7.15.2.6 ext_header

```
uint8_t fifo_comp_header_t::ext_header
```

7.15.2.7 gyro_bit

```
uint8_t fifo_comp_header_t::gyro_bit
```

7.15.2.8 tot_sample

```
uint8_t fifo_comp_header_t::tot_sample
```

The documentation for this union was generated from the following file:

- inv_imu_defs.h

7.16 fifo_config0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t fifo_depth: 6
- uint8_t fifo_mode: 2

7.16.1 Member Data Documentation

7.16.1.1 fifo_depth

```
uint8_t fifo_config0_t::fifo_depth
```

7.16.1.2 fifo_mode

```
uint8_t fifo_config0_t::fifo_mode
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.17 fifo_config2_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t resv_1: 3
- uint8_t fifo_wr_wm_gt_th: 1
- uint8_t resv_2: 3
- uint8_t fifo_flush: 1

7.17.1 Member Data Documentation

7.17.1.1 fifo_flush

```
uint8_t fifo_config2_t::fifo_flush
```

7.17.1.2 fifo_wr_wm_gt_th

```
uint8_t fifo_config2_t::fifo_wr_wm_gt_th
```

7.17.1.3 resv_1

```
uint8_t fifo_config2_t::resv_1
```

7.17.1.4 resv_2

```
uint8_t fifo_config2_t::resv_2
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.18 fifo_config3_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t fifo_if_en: 1
- uint8_t fifo_accel_en: 1
- uint8_t fifo_gyro_en: 1
- uint8_t fifo_hires_en: 1
- uint8_t fifo_es0_en: 1
- uint8_t fifo_es1_en: 1
- uint8_t resv_1: 2

7.18.1 Member Data Documentation

7.18.1.1 fifo_accel_en

```
uint8_t fifo_config3_t::fifo_accel_en
```

7.18.1.2 fifo_es0_en

```
uint8_t fifo_config3_t::fifo_es0_en
```

7.18.1.3 fifo_es1_en

```
uint8_t fifo_config3_t::fifo_es1_en
```

7.18.1.4 fifo_gyro_en

```
uint8_t fifo_config3_t::fifo_gyro_en
```

7.18.1.5 fifo_hires_en

```
uint8_t fifo_config3_t::fifo_hires_en
```

7.18.1.6 fifo_if_en

```
uint8_t fifo_config3_t::fifo_if_en
```

7.18.1.7 resv_1

```
uint8_t fifo_config3_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.19 fifo_config4_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t fifo_es0_6b_9b: 1
- uint8_t fifo_tmst_fsync_en: 1
- uint8_t fifo_comp_en: 1
- uint8_t fifo_comp_nc_flow_cfg: 3
- uint8_t resv_1: 2

7.19.1 Member Data Documentation

7.19.1.1 fifo_comp_en

```
uint8_t fifo_config4_t::fifo_comp_en
```

7.19.1.2 fifo_comp_nc_flow_cfg

```
uint8_t fifo_config4_t::fifo_comp_nc_flow_cfg
```

7.19.1.3 fifo_es0_6b_9b

```
uint8_t fifo_config4_t::fifo_es0_6b_9b
```

7.19.1.4 fifo_tmst_fsync_en

```
uint8_t fifo_config4_t::fifo_tmst_fsync_en
```

7.19.1.5 resv_1

```
uint8_t fifo_config4_t::resv_1
```

The documentation for this struct was generated from the following file:

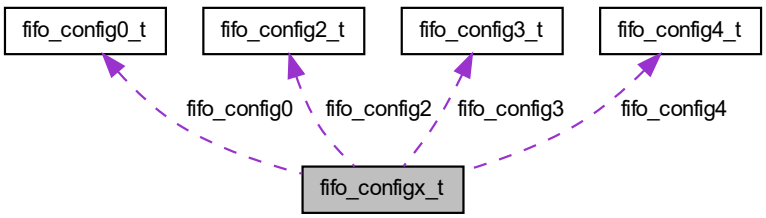
- inv_imu_regmap_le.h

7.20 fifo_configx_t Struct Reference

Required registers to configure FIFO.

```
#include <inv_imu_defs.h>
```

Collaboration diagram for fifo_configx_t:



Public Attributes

- fifo_config0_t fifo_config0
- uint8_t fifo_config1_0
- uint8_t fifo_config1_1
- fifo_config2_t fifo_config2
- fifo_config3_t fifo_config3
- fifo_config4_t fifo_config4

7.20.1 Detailed Description

Required registers to configure FIFO.

7.20.2 Member Data Documentation

7.20.2.1 fifo_config0

```
fifo_config0_t fifo_configx_t::fifo_config0
```

7.20.2.2 fifo_config1_0

```
uint8_t fifo_configx_t::fifo_config1_0
```

7.20.2.3 fifo_config1_1

```
uint8_t fifo_configx_t::fifo_config1_1
```

7.20.2.4 fifo_config2

```
fifo_config2_t fifo_configx_t::fifo_config2
```

7.20.2.5 fifo_config3

```
fifo_config3_t fifo_configx_t::fifo_config3
```

7.20.2.6 fifo_config4

```
fifo_config4_t fifo_configx_t::fifo_config4
```

The documentation for this struct was generated from the following file:

- inv_imu_defs.h

7.21 fifo_data_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t fifo_data: 8

7.21.1 Member Data Documentation

7.21.1.1 fifo_data

`uint8_t fifo_data_t::fifo_data`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.22 fifo_header2_t Union Reference

Describe the content of the second FIFO header.

`#include <inv_imu_defs.h>`

Public Attributes

- uint8_t Byte
- struct {
  uint8_t es0_en: 1
  uint8_t es1_en: 1
  uint8_t es0_vld: 1
  uint8_t es1_vld: 1
  uint8_t es0_6b_9b: 1
  uint8_t unused1: 1
  uint8_t unused2: 1
  uint8_t unused3: 1
  } bits

7.22.1 Detailed Description

Describe the content of the second FIFO header.

7.22.2 Member Data Documentation

7.22.2.1

```
struct { ... } fifo_header2_t::bits
```

7.22.2.2 Byte

```
uint8_t fifo_header2_t::Byte
```

7.22.2.3 es0_6b_9b

```
uint8_t fifo_header2_t::es0_6b_9b
```

7.22.2.4 es0_en

```
uint8_t fifo_header2_t::es0_en
```

7.22.2.5 es0_vld

```
uint8_t fifo_header2_t::es0_vld
```

7.22.2.6 es1_en

```
uint8_t fifo_header2_t::es1_en
```

7.22.2.7 es1_vld

```
uint8_t fifo_header2_t::es1_vld
```

7.22.2.8 unused1

```
uint8_t fifo_header2_t::unused1
```

7.22.2.9 unused2

```
uint8_t fifo_header2_t::unused2
```

7.22.2.10 unused3

```
uint8_t fifo_header2_t::unused3
```

The documentation for this union was generated from the following file:

- inv_imu_defs.h

7.23 fifo_header_t Union Reference

Describe the content of the FIFO header.

```
#include <inv_imu_defs.h>
```

Public Attributes

- uint8_t Byte
- struct {
    uint8_t gyro_odr_different: 1
    uint8_t accel_odr_different: 1
    uint8_t fsync_bit: 1
    uint8_t timestamp_bit: 1
    uint8_t twentybits_bit: 1
    uint8_t gyro_bit: 1
    uint8_t accel_bit: 1
    uint8_t ext_header: 1
  } bits

7.23.1 Detailed Description

Describe the content of the FIFO header.

7.23.2 Member Data Documentation

7.23.2.1 accel_bit

```
uint8_t fifo_header_t::accel_bit
```

7.23.2.2 accel_odr_different

```
uint8_t fifo_header_t::accel_odr_different
```

7.23.2.3

```
struct { ... } fifo_header_t::bits
```

7.23.2.4 Byte

```
uint8_t fifo_header_t::Byte
```

7.23.2.5 ext_header

```
uint8_t fifo_header_t::ext_header
```

7.23.2.6 fsync_bit

```
uint8_t fifo_header_t::fsync_bit
```

7.23.2.7 gyro_bit

```
uint8_t fifo_header_t::gyro_bit
```

7.23.2.8 gyro_odr_different

```
uint8_t fifo_header_t::gyro_odr_different
```

7.23.2.9 timestamp_bit

```
uint8_t fifo_header_t::timestamp_bit
```

7.23.2.10 twentybits_bit

```
uint8_t fifo_header_t::twentybits_bit
```

The documentation for this union was generated from the following file:

- inv_imu_defs.h

7.24 fifo_sram_sleep_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t fifo_gsleep_shared_sram: 2
- uint8_t resv_1: 6

7.24.1 Member Data Documentation

7.24.1.1 fifo_gsleep_shared_sram

```
uint8_t fifo_sram_sleep_t::fifo_gsleep_shared_sram
```

7.24.1.2 resv_1

```
uint8_t fifo_sram_sleep_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.25 fs_sel_aux1_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t accel_aux1_fs_sel: 3
- uint8_t gyro_aux1_fs_sel: 4
- uint8_t resv_1: 1

7.25.1 Member Data Documentation

7.25.1.1 accel_aux1_fs_sel

`uint8_t fs_sel_aux1_t::accel_aux1_fs_sel`

7.25.1.2 gyro_aux1_fs_sel

`uint8_t fs_sel_aux1_t::gyro_aux1_fs_sel`

7.25.1.3 resv_1

`uint8_t fs_sel_aux1_t::resv_1`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.26 fs_sel_aux2_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t accel_aux2_fs_sel: 3
- uint8_t gyro_aux2_fs_sel: 4
- uint8_t resv_1: 1

7.26.1 Member Data Documentation

7.26.1.1 accel_aux2_fs_sel

```
uint8_t fs_sel_aux2_t::accel_aux2_fs_sel
```

7.26.1.2 gyro_aux2_fs_sel

```
uint8_t fs_sel_aux2_t::gyro_aux2_fs_sel
```

7.26.1.3 resv_1

```
uint8_t fs_sel_aux2_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.27 fsync_config0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t ap_fsync_sel: 3
- uint8_t ap_fsync_flag_clear_sel: 1
- uint8_t resv_1: 4

7.27.1 Member Data Documentation

7.27.1.1 ap_fsync_flag_clear_sel

```
uint8_t fsync_config0_t::ap_fsync_flag_clear_sel
```

7.27.1.2 ap_fsync_sel

```
uint8_t fsync_config0_t::ap_fsync_sel
```

7.27.1.3 resv_1

```
uint8_t fsync_config0_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.28 fsync_config1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t aux1_fsync_sel: 3
- uint8_t aux1_fsync_flag_clear_sel: 1
- uint8_t resv_1: 4

7.28.1 Member Data Documentation

7.28.1.1 aux1_fsync_flag_clear_sel

```
uint8_t fsync_config1_t::aux1_fsync_flag_clear_sel
```

7.28.1.2 aux1_fsync_sel

```
uint8_t fsync_config1_t::aux1_fsync_sel
```

7.28.1.3 resv_1

```
uint8_t fsync_config1_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.29 gyro_config0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t gyro_odr: 4
- uint8_t gyro_ui_fs_sel: 4

7.29.1 Member Data Documentation

7.29.1.1 gyro_odr

```
uint8_t gyro_config0_t::gyro_odr
```

7.29.1.2 gyro_ui_fs_sel

```
uint8_t gyro_config0_t::gyro_ui_fs_sel
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.30 i2cm_command_0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t burstlen_0: 4
- uint8_t r_w_0: 2
- uint8_t ch_sel_0: 1
- uint8_t endflag_0: 1

7.30.1 Member Data Documentation

7.30.1.1 burstlen_0

```
uint8_t i2cm_command_0_t::burstlen_0
```

7.30.1.2 ch_sel_0

```
uint8_t i2cm_command_0_t::ch_sel_0
```

7.30.1.3 endflag_0

```
uint8_t i2cm_command_0_t::endflag_0
```

7.30.1.4 r_w_0

```
uint8_t i2cm_command_0_t::r_w_0
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.31 i2cm_command_1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t burstlen_1: 4
- uint8_t r_w_1: 2
- uint8_t ch_sel_1: 1
- uint8_t endflag_1: 1

7.31.1 Member Data Documentation

7.31.1.1 burstlen_1

```
uint8_t i2cm_command_1_t::burstlen_1
```

7.31.1.2 ch_sel_1

```
uint8_t i2cm_command_1_t::ch_sel_1
```

7.31.1.3 endflag_1

```
uint8_t i2cm_command_1_t::endflag_1
```

7.31.1.4 r_w_1

```
uint8_t i2cm_command_1_t::r_w_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.32 i2cm_command_2_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t burstlen_2: 4
- uint8_t r_w_2: 2
- uint8_t ch_sel_2: 1
- uint8_t endflag_2: 1

7.32.1 Member Data Documentation

7.32.1.1 burstlen_2

```
uint8_t i2cm_command_2_t::burstlen_2
```

7.32.1.2 ch_sel_2

```
uint8_t i2cm_command_2_t::ch_sel_2
```

7.32.1.3 endflag_2

```
uint8_t i2cm_command_2_t::endflag_2
```

7.32.1.4 r_w_2

```
uint8_t i2cm_command_2_t::r_w_2
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.33 i2cm_command_3_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t burstlen_3: 4
- uint8_t r_w_3: 2
- uint8_t ch_sel_3: 1
- uint8_t endflag_3: 1

7.33.1 Member Data Documentation

7.33.1.1 burstlen_3

```
uint8_t i2cm_command_3_t::burstlen_3
```

7.33.1.2 ch_sel_3

```
uint8_t i2cm_command_3_t::ch_sel_3
```

7.33.1.3 endflag_3

```
uint8_t i2cm_command_3_t::endflag_3
```

7.33.1.4 r_w_3

```
uint8_t i2cm_command_3_t::r_w_3
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.34 i2cm_control_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_go: 1
- uint8_t resv_1: 2
- uint8_t i2cm_speed: 1
- uint8_t resv_2: 2
- uint8_t i2cm_restart_en: 1
- uint8_t resv_3: 1

7.34.1 Member Data Documentation

7.34.1.1 i2cm_go

```
uint8_t i2cm_control_t::i2cm_go
```

7.34.1.2 i2cm_restart_en

```
uint8_t i2cm_control_t::i2cm_restart_en
```

7.34.1.3 i2cm_speed

```
uint8_t i2cm_control_t::i2cm_speed
```

7.34.1.4 resv_1

```
uint8_t i2cm_control_t::resv_1
```

7.34.1.5 resv_2

```
uint8_t i2cm_control_t::resv_2
```

7.34.1.6 resv_3

```
uint8_t i2cm_control_t::resv_3
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.35 i2cm_dev_profile0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t rd_address_0: 8

7.35.1 Member Data Documentation

7.35.1.1 rd_address_0

```
uint8_t i2cm_dev_profile0_t::rd_address_0
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.36 i2cm_dev_profile1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t dev_id_0: 7
- uint8_t resv_1: 1

7.36.1 Member Data Documentation

7.36.1.1 dev_id_0

```
uint8_t i2cm_dev_profile1_t::dev_id_0
```

7.36.1.2 resv_1

```
uint8_t i2cm_dev_profile1_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.37 i2cm_dev_profile2_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t rd_address_1: 8

7.37.1 Member Data Documentation

7.37.1.1 rd_address_1

```
uint8_t i2cm_dev_profile2_t::rd_address_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.38 i2cm_dev_profile3_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t dev_id_1: 7
- uint8_t resv_1: 1

7.38.1 Member Data Documentation

7.38.1.1 dev_id_1

```
uint8_t i2cm_dev_profile3_t::dev_id_1
```

7.38.1.2 resv_1

```
uint8_t i2cm_dev_profile3_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.39 i2cm_ext_dev_status_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t i2cm_ext_dev_status: 4
- uint8_t resv_1: 4

7.39.1 Member Data Documentation

7.39.1.1 i2cm_ext_dev_status

`uint8_t i2cm_ext_dev_status_t::i2cm_ext_dev_status`

7.39.1.2 resv_1

`uint8_t i2cm_ext_dev_status_t::resv_1`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.40 i2cm_rd_data0_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t i2cm_rd_data0: 8

7.40.1 Member Data Documentation

7.40.1.1 i2cm_rd_data0

```
uint8_t i2cm_rd_data0_t::i2cm_rd_data0
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.41 i2cm_rd_data10_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data10: 8

7.41.1 Member Data Documentation

7.41.1.1 i2cm_rd_data10

```
uint8_t i2cm_rd_data10_t::i2cm_rd_data10
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.42 i2cm_rd_data11_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data11: 8

7.42.1 Member Data Documentation

7.42.1.1 i2cm_rd_data11

```
uint8_t i2cm_rd_data11_t::i2cm_rd_data11
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.43 i2cm_rd_data12_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data12: 8

7.43.1 Member Data Documentation

7.43.1.1 i2cm_rd_data12

```
uint8_t i2cm_rd_data12_t::i2cm_rd_data12
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.44 i2cm_rd_data13_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data13: 8

7.44.1 Member Data Documentation

7.44.1.1 i2cm_rd_data13

```
uint8_t i2cm_rd_data13_t::i2cm_rd_data13
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.45 i2cm_rd_data14_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data14: 8

7.45.1 Member Data Documentation

7.45.1.1 i2cm_rd_data14

```
uint8_t i2cm_rd_data14_t::i2cm_rd_data14
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.46 i2cm_rd_data15_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data15: 8

7.46.1 Member Data Documentation

7.46.1.1 i2cm_rd_data15

```
uint8_t i2cm_rd_data15_t::i2cm_rd_data15
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.47 i2cm_rd_data16_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data16: 8

7.47.1 Member Data Documentation

7.47.1.1 i2cm_rd_data16

```
uint8_t i2cm_rd_data16_t::i2cm_rd_data16
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.48 i2cm_rd_data17_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data17: 8

7.48.1 Member Data Documentation

7.48.1.1 i2cm_rd_data17

```
uint8_t i2cm_rd_data17_t::i2cm_rd_data17
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.49 i2cm_rd_data18_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data18: 8

7.49.1 Member Data Documentation

7.49.1.1 i2cm_rd_data18

```
uint8_t i2cm_rd_data18_t::i2cm_rd_data18
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.50 i2cm_rd_data19_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data19: 8

7.50.1 Member Data Documentation

7.50.1.1 i2cm_rd_data19

```
uint8_t i2cm_rd_data19_t::i2cm_rd_data19
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.51 i2cm_rd_data1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data1: 8

7.51.1 Member Data Documentation

7.51.1.1 i2cm_rd_data1

```
uint8_t i2cm_rd_data1_t::i2cm_rd_data1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.52 i2cm_rd_data20_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data20: 8

7.52.1 Member Data Documentation

7.52.1.1 i2cm_rd_data20

```
uint8_t i2cm_rd_data20_t::i2cm_rd_data20
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.53 i2cm_rd_data2_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data2: 8

7.53.1 Member Data Documentation

7.53.1.1 i2cm_rd_data2

```
uint8_t i2cm_rd_data2_t::i2cm_rd_data2
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.54 i2cm_rd_data3_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data3: 8

7.54.1 Member Data Documentation

7.54.1.1 i2cm_rd_data3

```
uint8_t i2cm_rd_data3_t::i2cm_rd_data3
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.55 i2cm_rd_data4_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data4: 8

7.55.1 Member Data Documentation

7.55.1.1 i2cm_rd_data4

```
uint8_t i2cm_rd_data4_t::i2cm_rd_data4
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.56 i2cm_rd_data5_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data5: 8

7.56.1 Member Data Documentation

7.56.1.1 i2cm_rd_data5

```
uint8_t i2cm_rd_data5_t::i2cm_rd_data5
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.57 i2cm_rd_data6_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data6: 8

7.57.1 Member Data Documentation

7.57.1.1 i2cm_rd_data6

```
uint8_t i2cm_rd_data6_t::i2cm_rd_data6
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.58 i2cm_rd_data7_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_rd_data7: 8

7.58.1 Member Data Documentation

7.58.1.1 i2cm_rd_data7

`uint8_t i2cm_rd_data7_t::i2cm_rd_data7`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.59 i2cm_rd_data8_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t i2cm_rd_data8: 8

7.59.1 Member Data Documentation

7.59.1.1 i2cm_rd_data8

`uint8_t i2cm_rd_data8_t::i2cm_rd_data8`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.60 i2cm_rd_data9_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t i2cm_rd_data9: 8

7.60.1 Member Data Documentation

7.60.1.1 i2cm_rd_data9

```
uint8_t i2cm_rd_data9_t::i2cm_rd_data9
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.61 i2cm_status_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_busy: 1
- uint8_t i2cm_done: 1
- uint8_t i2cm_timeout_err: 1
- uint8_t i2cm_srst_err: 1
- uint8_t i2cm_scl_err: 1
- uint8_t i2cm_sda_err: 1
- uint8_t resv_1: 2

7.61.1 Member Data Documentation

7.61.1.1 i2cm_busy

```
uint8_t i2cm_status_t::i2cm_busy
```

7.61.1.2 i2cm_done

```
uint8_t i2cm_status_t::i2cm_done
```

7.61.1.3 i2cm_scl_err

```
uint8_t i2cm_status_t::i2cm_scl_err
```

7.61.1.4 i2cm_sda_err

```
uint8_t i2cm_status_t::i2cm_sda_err
```

7.61.1.5 i2cm_srst_err

```
uint8_t i2cm_status_t::i2cm_srst_err
```

7.61.1.6 i2cm_timeout_err

```
uint8_t i2cm_status_t::i2cm_timeout_err
```

7.61.1.7 resv_1

```
uint8_t i2cm_status_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.62 i2cm_wr_data0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t i2cm_wr_data0: 8

7.62.1 Member Data Documentation

7.62.1.1 i2cm_wr_data0

```
uint8_t i2cm_wr_data0_t::i2cm_wr_data0
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.63 i2cm_wr_data1_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t i2cm_wr_data1: 8

7.63.1 Member Data Documentation

7.63.1.1 i2cm_wr_data1

`uint8_t i2cm_wr_data1_t::i2cm_wr_data1`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.64 i2cm_wr_data2_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t i2cm_wr_data2: 8

7.64.1 Member Data Documentation

7.64.1.1 i2cm_wr_data2

`uint8_t i2cm_wr_data2_t::i2cm_wr_data2`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.65 i2cm_wr_data3_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t i2cm_wr_data3: 8

7.65.1 Member Data Documentation

7.65.1.1 i2cm_wr_data3

`uint8_t i2cm_wr_data3_t::i2cm_wr_data3`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.66 i2cm_wr_data4_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t i2cm_wr_data4: 8

7.66.1 Member Data Documentation

7.66.1.1 i2cm_wr_data4

`uint8_t i2cm_wr_data4_t::i2cm_wr_data4`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.67 i2cm_wr_data5_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t i2cm_wr_data5: 8

7.67.1 Member Data Documentation

7.67.1.1 i2cm_wr_data5

`uint8_t i2cm_wr_data5_t::i2cm_wr_data5`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.68 int1_config0_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t int1_status_en_fifo_full: 1
- uint8_t int1_status_en_fifo_ths: 1
- uint8_t int1_status_en_drdy: 1
- uint8_t int1_status_en_aux1_drdy: 1
- uint8_t int1_status_en_ap_fsync: 1
- uint8_t int1_status_en_ap_agc_rdy: 1
- uint8_t int1_status_en_aux1_agc_rdy: 1
- uint8_t int1_status_en_reset_done: 1

7.68.1 Member Data Documentation

7.68.1.1 int1_status_en_ap_agc_rdy

`uint8_t int1_config0_t::int1_status_en_ap_agc_rdy`

7.68.1.2 int1_status_en_ap_fsync

```
uint8_t int1_config0_t::int1_status_en_ap_fsync
```

7.68.1.3 int1_status_en_aux1_agc_rdy

```
uint8_t int1_config0_t::int1_status_en_aux1_agc_rdy
```

7.68.1.4 int1_status_en_aux1_drdy

```
uint8_t int1_config0_t::int1_status_en_aux1_drdy
```

7.68.1.5 int1_status_en_drdy

```
uint8_t int1_config0_t::int1_status_en_drdy
```

7.68.1.6 int1_status_en_fifo_full

```
uint8_t int1_config0_t::int1_status_en_fifo_full
```

7.68.1.7 int1_status_en_fifo_ths

```
uint8_t int1_config0_t::int1_status_en_fifo_ths
```

7.68.1.8 int1_status_en_reset_done

```
uint8_t int1_config0_t::int1_status_en_reset_done
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.69 int1_config1_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t int1_status_en_pll_rdy: 1
- uint8_t int1_status_en_wom_x: 1
- uint8_t int1_status_en_wom_y: 1
- uint8_t int1_status_en_wom_z: 1
- uint8_t int1_status_en_i3c_protocol_err: 1
- uint8_t int1_status_en_i2cm_done: 1
- uint8_t int1_status_en_apex_event: 1
- uint8_t resv_1: 1

7.69.1 Member Data Documentation

7.69.1.1 int1_status_en_apex_event

`uint8_t int1_config1_t::int1_status_en_apex_event`

7.69.1.2 int1_status_en_i2cm_done

`uint8_t int1_config1_t::int1_status_en_i2cm_done`

7.69.1.3 int1_status_en_i3c_protocol_err

`uint8_t int1_config1_t::int1_status_en_i3c_protocol_err`

7.69.1.4 int1_status_en_pll_rdy

`uint8_t int1_config1_t::int1_status_en_pll_rdy`

7.69.1.5 int1_status_en_wom_x

```
uint8_t int1_config1_t::int1_status_en_wom_x
```

7.69.1.6 int1_status_en_wom_y

```
uint8_t int1_config1_t::int1_status_en_wom_y
```

7.69.1.7 int1_status_en_wom_z

```
uint8_t int1_config1_t::int1_status_en_wom_z
```

7.69.1.8 resv_1

```
uint8_t int1_config1_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.70 int1_config2_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int1_polarity: 1
- uint8_t int1_mode: 1
- uint8_t int1_drive: 1
- uint8_t resv_1: 5

7.70.1 Member Data Documentation

7.70.1.1 int1_drive

```
uint8_t int1_config2_t::int1_drive
```

7.70.1.2 int1_mode

```
uint8_t int1_config2_t::int1_mode
```

7.70.1.3 int1_polarity

```
uint8_t int1_config2_t::int1_polarity
```

7.70.1.4 resv_1

```
uint8_t int1_config2_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.71 int1_status0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int1_status_fifo_full: 1
- uint8_t int1_status_fifo_ths: 1
- uint8_t int1_status_drdy: 1
- uint8_t int1_status_aux1_drdy: 1
- uint8_t int1_status_ap_fsync: 1
- uint8_t int1_status_ap_agc_rdy: 1
- uint8_t int1_status_aux1_agc_rdy: 1
- uint8_t int1_status_reset_done: 1

7.71.1 Member Data Documentation

7.71.1.1 int1_status_ap_agc_rdy

```
uint8_t int1_status0_t::int1_status_ap_agc_rdy
```

7.71.1.2 int1_status_ap_fsync

```
uint8_t int1_status0_t::int1_status_ap_fsync
```

7.71.1.3 int1_status_aux1_agc_rdy

```
uint8_t int1_status0_t::int1_status_aux1_agc_rdy
```

7.71.1.4 int1_status_aux1_drdy

```
uint8_t int1_status0_t::int1_status_aux1_drdy
```

7.71.1.5 int1_status_drdy

```
uint8_t int1_status0_t::int1_status_drdy
```

7.71.1.6 int1_status_fifo_full

```
uint8_t int1_status0_t::int1_status_fifo_full
```

7.71.1.7 int1_status_fifo_ths

```
uint8_t int1_status0_t::int1_status_fifo_ths
```

7.71.1.8 int1_status_reset_done

```
uint8_t int1_status0_t::int1_status_reset_done
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.72 int1_status1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int1_status_pll_rdy: 1
- uint8_t int1_status_wom_x: 1
- uint8_t int1_status_wom_y: 1
- uint8_t int1_status_wom_z: 1
- uint8_t int1_status_i3c_protocol_err: 1
- uint8_t int1_status_i2cm_done: 1
- uint8_t int1_status_apex_event: 1
- uint8_t resv_1: 1

7.72.1 Member Data Documentation

7.72.1.1 int1_status_apex_event

```
uint8_t int1_status1_t::int1_status_apex_event
```

7.72.1.2 int1_status_i2cm_done

```
uint8_t int1_status1_t::int1_status_i2cm_done
```

7.72.1.3 int1_status_i3c_protocol_err

```
uint8_t int1_status1_t::int1_status_i3c_protocol_err
```

7.72.1.4 int1_status_pll_rdy

```
uint8_t int1_status1_t::int1_status_pll_rdy
```

7.72.1.5 int1_status_wom_x

```
uint8_t int1_status1_t::int1_status_wom_x
```

7.72.1.6 int1_status_wom_y

```
uint8_t int1_status1_t::int1_status_wom_y
```

7.72.1.7 int1_status_wom_z

```
uint8_t int1_status1_t::int1_status_wom_z
```

7.72.1.8 resv_1

```
uint8_t int1_status1_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.73 int2_config0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int2_status_en_fifo_full: 1
- uint8_t int2_status_en_fifo_ths: 1
- uint8_t int2_status_en_drdy: 1
- uint8_t int2_status_en_aux1_drdy: 1
- uint8_t int2_status_en_ap_fsync: 1
- uint8_t int2_status_en_ap_agc_rdy: 1
- uint8_t int2_status_en_aux1_agc_rdy: 1
- uint8_t int2_status_en_reset_done: 1

7.73.1 Member Data Documentation

7.73.1.1 int2_status_en_ap_agc_rdy

```
uint8_t int2_config0_t::int2_status_en_ap_agc_rdy
```

7.73.1.2 int2_status_en_ap_fsync

```
uint8_t int2_config0_t::int2_status_en_ap_fsync
```

7.73.1.3 int2_status_en_aux1_agc_rdy

```
uint8_t int2_config0_t::int2_status_en_aux1_agc_rdy
```

7.73.1.4 int2_status_en_aux1_drdy

```
uint8_t int2_config0_t::int2_status_en_aux1_drdy
```

7.73.1.5 int2_status_en_drdy

```
uint8_t int2_config0_t::int2_status_en_drdy
```

7.73.1.6 int2_status_en_fifo_full

```
uint8_t int2_config0_t::int2_status_en_fifo_full
```

7.73.1.7 int2_status_en_fifo_ths

```
uint8_t int2_config0_t::int2_status_en_fifo_ths
```

7.73.1.8 int2_status_en_reset_done

```
uint8_t int2_config0_t::int2_status_en_reset_done
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.74 int2_config1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int2_status_en_pll_rdy: 1
- uint8_t int2_status_en_wom_x: 1
- uint8_t int2_status_en_wom_y: 1
- uint8_t int2_status_en_wom_z: 1
- uint8_t int2_status_en_i3c_protocol_err: 1
- uint8_t int2_status_en_i2cm_done: 1
- uint8_t int2_status_en_apex_event: 1
- uint8_t resv_1: 1

7.74.1 Member Data Documentation

7.74.1.1 int2_status_en_apex_event

```
uint8_t int2_config1_t::int2_status_en_apex_event
```

7.74.1.2 int2_status_en_i2cm_done

```
uint8_t int2_config1_t::int2_status_en_i2cm_done
```

7.74.1.3 int2_status_en_i3c_protocol_err

```
uint8_t int2_config1_t::int2_status_en_i3c_protocol_err
```

7.74.1.4 int2_status_en_pll_rdy

```
uint8_t int2_config1_t::int2_status_en_pll_rdy
```

7.74.1.5 int2_status_en_wom_x

```
uint8_t int2_config1_t::int2_status_en_wom_x
```

7.74.1.6 int2_status_en_wom_y

```
uint8_t int2_config1_t::int2_status_en_wom_y
```

7.74.1.7 int2_status_en_wom_z

```
uint8_t int2_config1_t::int2_status_en_wom_z
```

7.74.1.8 resv_1

```
uint8_t int2_config1_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.75 int2_config2_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int2_polarity: 1
- uint8_t int2_mode: 1
- uint8_t int2_drive: 1
- uint8_t resv_1: 5

7.75.1 Member Data Documentation

7.75.1.1 int2_drive

```
uint8_t int2_config2_t::int2_drive
```

7.75.1.2 int2_mode

```
uint8_t int2_config2_t::int2_mode
```

7.75.1.3 int2_polarity

```
uint8_t int2_config2_t::int2_polarity
```

7.75.1.4 resv_1

```
uint8_t int2_config2_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.76 int2_status0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int2_status_fifo_full: 1
- uint8_t int2_status_fifo_ths: 1
- uint8_t int2_status_drdy: 1
- uint8_t int2_status_aux1_drdy: 1
- uint8_t int2_status_ap_fsync: 1
- uint8_t int2_status_ap_agc_rdy: 1
- uint8_t int2_status_aux1_agc_rdy: 1
- uint8_t int2_status_reset_done: 1

7.76.1 Member Data Documentation

7.76.1.1 int2_status_ap_agc_rdy

```
uint8_t int2_status0_t::int2_status_ap_agc_rdy
```

7.76.1.2 int2_status_ap_fsync

```
uint8_t int2_status0_t::int2_status_ap_fsync
```

7.76.1.3 int2_status_aux1_agc_rdy

```
uint8_t int2_status0_t::int2_status_aux1_agc_rdy
```

7.76.1.4 int2_status_aux1_drdy

```
uint8_t int2_status0_t::int2_status_aux1_drdy
```

7.76.1.5 int2_status_drdy

```
uint8_t int2_status0_t::int2_status_drdy
```

7.76.1.6 int2_status_fifo_full

```
uint8_t int2_status0_t::int2_status_fifo_full
```

7.76.1.7 int2_status_fifo_ths

```
uint8_t int2_status0_t::int2_status_fifo_ths
```

7.76.1.8 int2_status_reset_done

```
uint8_t int2_status0_t::int2_status_reset_done
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.77 int2_status1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int2_status_pll_rdy: 1
- uint8_t int2_status_wom_x: 1
- uint8_t int2_status_wom_y: 1
- uint8_t int2_status_wom_z: 1
- uint8_t int2_status_i3c_protocol_err: 1
- uint8_t int2_status_i2cm_done: 1
- uint8_t int2_status_apex_event: 1
- uint8_t resv_1: 1

7.77.1 Member Data Documentation

7.77.1.1 int2_status_apex_event

```
uint8_t int2_status1_t::int2_status_apex_event
```

7.77.1.2 int2_status_i2cm_done

```
uint8_t int2_status1_t::int2_status_i2cm_done
```

7.77.1.3 int2_status_i3c_protocol_err

```
uint8_t int2_status1_t::int2_status_i3c_protocol_err
```

7.77.1.4 int2_status_pll_rdy

```
uint8_t int2_status1_t::int2_status_pll_rdy
```

7.77.1.5 int2_status_wom_x

```
uint8_t int2_status1_t::int2_status_wom_x
```

7.77.1.6 int2_status_wom_y

```
uint8_t int2_status1_t::int2_status_wom_y
```

7.77.1.7 int2_status_wom_z

```
uint8_t int2_status1_t::int2_status_wom_z
```

7.77.1.8 resv_1

```
uint8_t int2_status1_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.78 int_apex_config0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_status_mask_pin_tap_detect: 1
- uint8_t int_status_mask_pin_high_g_det: 1
- uint8_t int_status_mask_pin_low_g_det: 1
- uint8_t int_status_mask_pin_tilt_det: 1
- uint8_t int_status_mask_pin_step_cnt_ovfl: 1
- uint8_t int_status_mask_pin_step_det: 1
- uint8_t int_status_mask_pin_ff_det: 1
- uint8_t int_status_mask_pin_r2w_wake_det: 1

7.78.1 Member Data Documentation

7.78.1.1 int_status_mask_pin_ff_det

```
uint8_t int_apex_config0_t::int_status_mask_pin_ff_det
```

7.78.1.2 int_status_mask_pin_high_g_det

```
uint8_t int_apex_config0_t::int_status_mask_pin_high_g_det
```

7.78.1.3 int_status_mask_pin_low_g_det

```
uint8_t int_apex_config0_t::int_status_mask_pin_low_g_det
```

7.78.1.4 int_status_mask_pin_r2w_wake_det

```
uint8_t int_apex_config0_t::int_status_mask_pin_r2w_wake_det
```

7.78.1.5 int_status_mask_pin_step_cnt_ovfl

```
uint8_t int_apex_config0_t::int_status_mask_pin_step_cnt_ovfl
```

7.78.1.6 int_status_mask_pin_step_det

```
uint8_t int_apex_config0_t::int_status_mask_pin_step_det
```

7.78.1.7 int_status_mask_pin_tap_detect

```
uint8_t int_apex_config0_t::int_status_mask_pin_tap_detect
```

7.78.1.8 int_status_mask_pin_tilt_det

```
uint8_t int_apex_config0_t::int_status_mask_pin_tilt_det
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.79 int_apex_config1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_status_mask_pin_r2w_sleep_det: 1
- uint8_t int_status_mask_pin_smd_det: 1
- uint8_t int_status_mask_pin_selftest_done: 1
- uint8_t resv_1: 1
- uint8_t int_status_mask_pin_sa_done: 1
- uint8_t int_status_mask_pin_basic_smd: 1
- uint8_t resv_2: 2

7.79.1 Member Data Documentation

7.79.1.1 int_status_mask_pin_basic_smd

```
uint8_t int_apex_config1_t::int_status_mask_pin_basic_smd
```

7.79.1.2 int_status_mask_pin_r2w_sleep_det

```
uint8_t int_apex_config1_t::int_status_mask_pin_r2w_sleep_det
```

7.79.1.3 int_status_mask_pin_sa_done

```
uint8_t int_apex_config1_t::int_status_mask_pin_sa_done
```

7.79.1.4 int_status_mask_pin_selftest_done

```
uint8_t int_apex_config1_t::int_status_mask_pin_selftest_done
```

7.79.1.5 int_status_mask_pin_smd_det

```
uint8_t int_apex_config1_t::int_status_mask_pin_smd_det
```

7.79.1.6 resv_1

```
uint8_t int_apex_config1_t::resv_1
```

7.79.1.7 resv_2

```
uint8_t int_apex_config1_t::resv_2
```

The documentation for this struct was generated from the following file:

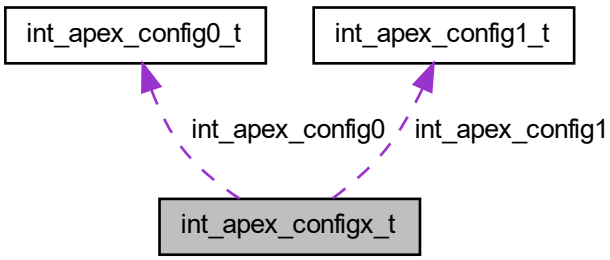
- inv_imu_regmap_le.h

7.80 int_apex_configx_t Struct Reference

Registers to configure interrupts for APEX.

```
#include <inv_imu_edmp.h>
```

Collaboration diagram for int_apex_configx_t:



Public Attributes

- int_apex_config0_t int_apex_config0
- int_apex_config1_t int_apex_config1

7.80.1 Detailed Description

Registers to configure interrupts for APEX.

7.80.2 Member Data Documentation

7.80.2.1 int_apex_config0

```
int_apex_config0_t int_apex_configx_t::int_apex_config0
```

7.80.2.2 int_apex_config1

```
int_apex_config1_t int_apex_configx_t::int_apex_config1
```

The documentation for this struct was generated from the following file:

- inv_imu_edmp.h

7.81 int_apex_status0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_status_tap_det: 1
- uint8_t int_status_high_g_det: 1
- uint8_t int_status_low_g_det: 1
- uint8_t int_status_tilt_det: 1
- uint8_t int_status_step_cnt_ovfl: 1
- uint8_t int_status_step_det: 1
- uint8_t int_status_ff_det: 1
- uint8_t int_status_r2w_wake_det: 1

7.81.1 Member Data Documentation

7.81.1.1 int_status_ff_det

```
uint8_t int_apex_status0_t::int_status_ff_det
```

7.81.1.2 int_status_high_g_det

```
uint8_t int_apex_status0_t::int_status_high_g_det
```

7.81.1.3 int_status_low_g_det

```
uint8_t int_apex_status0_t::int_status_low_g_det
```

7.81.1.4 int_status_r2w_wake_det

```
uint8_t int_apex_status0_t::int_status_r2w_wake_det
```

7.81.1.5 int_status_step_cnt_ovfl

```
uint8_t int_apex_status0_t::int_status_step_cnt_ovfl
```

7.81.1.6 int_status_step_det

```
uint8_t int_apex_status0_t::int_status_step_det
```

7.81.1.7 int_status_tap_det

```
uint8_t int_apex_status0_t::int_status_tap_det
```

7.81.1.8 int_status_tilt_det

```
uint8_t int_apex_status0_t::int_status_tilt_det
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.82 int_apex_status1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_status_r2w_sleep_det: 1
- uint8_t int_status_smd_det: 1
- uint8_t int_status_selftest_done: 1
- uint8_t resv_1: 1
- uint8_t int_status_sa_done: 1
- uint8_t int_status_basic_smd: 1
- uint8_t resv_2: 2

7.82.1 Member Data Documentation

7.82.1.1 int_status_basic_smd

```
uint8_t int_apex_status1_t::int_status_basic_smd
```

7.82.1.2 int_status_r2w_sleep_det

```
uint8_t int_apex_status1_t::int_status_r2w_sleep_det
```

7.82.1.3 int_status_sa_done

```
uint8_t int_apex_status1_t::int_status_sa_done
```

7.82.1.4 int_status_selftest_done

```
uint8_t int_apex_status1_t::int_status_selftest_done
```

7.82.1.5 int_status_smd_det

```
uint8_t int_apex_status1_t::int_status_smd_det
```

7.82.1.6 resv_1

```
uint8_t int_apex_status1_t::resv_1
```

7.82.1.7 resv_2

```
uint8_t int_apex_status1_t::resv_2
```

The documentation for this struct was generated from the following file:

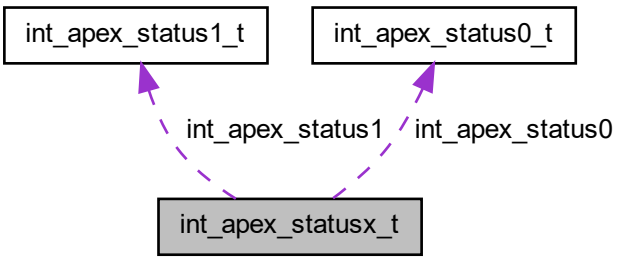
- inv_imu_regmap_le.h

7.83 int_apex_statusx_t Struct Reference

Registers to retrieve interrupts status for APEX.

```
#include <inv_imu_edmp.h>
```

Collaboration diagram for int_apex_statusx_t:



Public Attributes

- int_apex_status0_t int_apex_status0
- int_apex_status1_t int_apex_status1

7.83.1 Detailed Description

Registers to retrieve interrupts status for APEX.

7.83.2 Member Data Documentation

7.83.2.1 int_apex_status0

```
int_apex_status0_t int_apex_statusx_t::int_apex_status0
```

7.83.2.2 int_apex_status1

```
int_apex_status1_t int_apex_statusx_t::int_apex_status1
```

The documentation for this struct was generated from the following file:

- inv_imu_edmp.h

7.84 int_aux2_config_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_en_aux2_agc_rdy: 1
- uint8_t int_en_aux2_reset_done: 1
- uint8_t int_en_aux2_pll_rdy: 1
- uint8_t int_en_aux2_drdy: 1
- uint8_t resv_1: 4

7.84.1 Member Data Documentation

7.84.1.1 int_en_aux2_agc_rdy

```
uint8_t int_aux2_config_t::int_en_aux2_agc_rdy
```

7.84.1.2 int_en_aux2_drdy

```
uint8_t int_aux2_config_t::int_en_aux2_drdy
```

7.84.1.3 int_en_aux2_pll_rdy

```
uint8_t int_aux2_config_t::int_en_aux2_pll_rdy
```

7.84.1.4 int_en_aux2_reset_done

```
uint8_t int_aux2_config_t::int_en_aux2_reset_done
```

7.84.1.5 resv_1

```
uint8_t int_aux2_config_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.85 int_aux2_status_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_status_aux2_agc_rdy: 1
- uint8_t int_status_aux2_reset_done: 1
- uint8_t int_status_aux2_pll_rdy: 1
- uint8_t int_status_aux2_drdy: 1
- uint8_t resv_1: 4

7.85.1 Member Data Documentation

7.85.1.1 int_status_aux2_agc_rdy

```
uint8_t int_aux2_status_t::int_status_aux2_agc_rdy
```

7.85.1.2 int_status_aux2_drdy

```
uint8_t int_aux2_status_t::int_status_aux2_drdy
```

7.85.1.3 int_status_aux2_pll_rdy

```
uint8_t int_aux2_status_t::int_status_aux2_pll_rdy
```

7.85.1.4 int_status_aux2_reset_done

```
uint8_t int_aux2_status_t::int_status_aux2_reset_done
```

7.85.1.5 resv_1

```
uint8_t int_aux2_status_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.86 int_i2cm_source_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_status_i2cm_ioc_ext_trig_en: 1
- uint8_t int_status_i2cm_smc_ext_odr_en: 1
- uint8_t resv_1: 6

7.86.1 Member Data Documentation

7.86.1.1 int_status_i2cm_ioc_ext_trig_en

```
uint8_t int_i2cm_source_t::int_status_i2cm_ioc_ext_trig_en
```

7.86.1.2 int_status_i2cm_smc_ext_odr_en

```
uint8_t int_i2cm_source_t::int_status_i2cm_smc_ext_odr_en
```

7.86.1.3 resv_1

```
uint8_t int_i2cm_source_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.87 int_pulse_min_off_intf0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int0_tdeassert_disable: 3
- uint8_t resv_1: 5

7.87.1 Member Data Documentation

7.87.1.1 int0_tdeassert_disable

```
uint8_t int_pulse_min_off_intf0_t::int0_tdeassert_disable
```

7.87.1.2 resv_1

```
uint8_t int_pulse_min_off_intf0_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.88 int_pulse_min_off_intf1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int1_tdeassert_disable: 3
- uint8_t resv_1: 5

7.88.1 Member Data Documentation

7.88.1.1 int1_tdeassert_disable

```
uint8_t int_pulse_min_off_intf1_t::int1_tdeassert_disable
```

7.88.1.2 resv_1

```
uint8_t int_pulse_min_off_intf1_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.89 int_pulse_min_on_intf0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int0_tpulse_duration: 3
- uint8_t resv_1: 5

7.89.1 Member Data Documentation

7.89.1.1 int0_tpulse_duration

```
uint8_t int_pulse_min_on_intf0_t::int0_tpulse_duration
```

7.89.1.2 resv_1

```
uint8_t int_pulse_min_on_intf0_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.90 int_pulse_min_on_intf1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int1_tpulse_duration: 3
- uint8_t resv_1: 5

7.90.1 Member Data Documentation

7.90.1.1 int1_tpulse_duration

```
uint8_t int_pulse_min_on_intf1_t::int1_tpulse_duration
```

7.90.1.2 resv_1

```
uint8_t int_pulse_min_on_intf1_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.91 intf_aux_config_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t aux1_spi_mode: 1
- uint8_t aux1_spi_34_mode: 1
- uint8_t aux2_spi_mode: 1
- uint8_t resv_1: 5

7.91.1 Member Data Documentation

7.91.1.1 aux1_spi_34_mode

`uint8_t intf_aux_config_t::aux1_spi_34_mode`

7.91.1.2 aux1_spi_mode

`uint8_t intf_aux_config_t::aux1_spi_mode`

7.91.1.3 aux2_spi_mode

`uint8_t intf_aux_config_t::aux2_spi_mode`

7.91.1.4 resv_1

`uint8_t intf_aux_config_t::resv_1`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.92 intf_config0_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t ap_spi_mode: 1
- uint8_t ap_spi_34_mode: 1
- uint8_t resv_1: 3
- uint8_t virtual_access_aux1_en: 1
- uint8_t resv_2: 2

7.92.1 Member Data Documentation

7.92.1.1 ap_spi_34_mode

```
uint8_t intf_config0_t::ap_spi_34_mode
```

7.92.1.2 ap_spi_mode

```
uint8_t intf_config0_t::ap_spi_mode
```

7.92.1.3 resv_1

```
uint8_t intf_config0_t::resv_1
```

7.92.1.4 resv_2

```
uint8_t intf_config0_t::resv_2
```

7.92.1.5 virtual_access_aux1_en

```
uint8_t intf_config0_t::virtual_access_aux1_en
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.93 intf_config1_ovrd_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t ap_spi_mode_ovrd_val: 1
- uint8_t ap_spi_mode_ovrd: 1
- uint8_t ap_spi_34_mode_ovrd_val: 1
- uint8_t ap_spi_34_mode_ovrd: 1
- uint8_t resv_1: 4

7.93.1 Member Data Documentation

7.93.1.1 ap_spi_34_mode_ovrd

`uint8_t intf_config1_ovrd_t::ap_spi_34_mode_ovrd`

7.93.1.2 ap_spi_34_mode_ovrd_val

`uint8_t intf_config1_ovrd_t::ap_spi_34_mode_ovrd_val`

7.93.1.3 ap_spi_mode_ovrd

`uint8_t intf_config1_ovrd_t::ap_spi_mode_ovrd`

7.93.1.4 ap_spi_mode_ovrd_val

`uint8_t intf_config1_ovrd_t::ap_spi_mode_ovrd_val`

7.93.1.5 resv_1

`uint8_t intf_config1_ovrd_t::resv_1`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.94 intf_config_ovrd_aux1_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t aux1_spi_mode_ovrd_val: 1
- uint8_t aux1_spi_mode_ovrd: 1
- uint8_t aux1_spi_34_mode_ovrd_val: 1
- uint8_t aux1_spi_34_mode_ovrd: 1
- uint8_t aux1_ireg_auto_addr_inc_dis: 1
- uint8_t resv_1: 3

7.94.1 Member Data Documentation

7.94.1.1 aux1_ireg_auto_addr_inc_dis

`uint8_t intf_config_ovrd_aux1_t::aux1_ireg_auto_addr_inc_dis`

7.94.1.2 aux1_spi_34_mode_ovrd

`uint8_t intf_config_ovrd_aux1_t::aux1_spi_34_mode_ovrd`

7.94.1.3 aux1_spi_34_mode_ovrd_val

`uint8_t intf_config_ovrd_aux1_t::aux1_spi_34_mode_ovrd_val`

7.94.1.4 aux1_spi_mode_ovrd

`uint8_t intf_config_ovrd_aux1_t::aux1_spi_mode_ovrd`

7.94.1.5 aux1_spi_mode_ovrd_val

`uint8_t intf_config_ovrd_aux1_t::aux1_spi_mode_ovrd_val`

7.94.1.6 resv_1

```
uint8_t intf_config_ovrd_aux1_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.95 intf_config_ovrd_aux2_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t aux2_spi_mode_ovrd_val: 1
- uint8_t aux2_spi_mode_ovrd: 1
- uint8_t aux2_ireg_auto_addr_inc_dis: 1
- uint8_t resv_1: 5

7.95.1 Member Data Documentation

7.95.1.1 aux2_ireg_auto_addr_inc_dis

```
uint8_t intf_config_ovrd_aux2_t::aux2_ireg_auto_addr_inc_dis
```

7.95.1.2 aux2_spi_mode_ovrd

```
uint8_t intf_config_ovrd_aux2_t::aux2_spi_mode_ovrd
```

7.95.1.3 aux2_spi_mode_ovrd_val

```
uint8_t intf_config_ovrd_aux2_t::aux2_spi_mode_ovrd_val
```

7.95.1.4 resv_1

```
uint8_t intf_config_ovrd_aux2_t::resv_1
```

The documentation for this struct was generated from the following file:

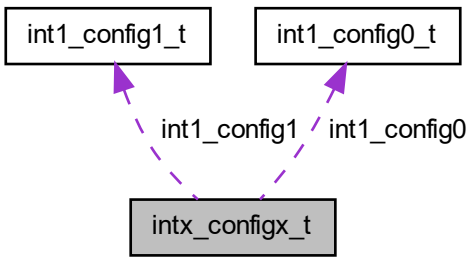
- inv_imu_regmap_le.h

7.96 intx_configx_t Struct Reference

Required registers to configure interrupts.

```
#include <inv_imu_defs.h>
```

Collaboration diagram for intx_configx_t:



Public Attributes

- int1_config0_t int1_config0
- int1_config1_t int1_config1

7.96.1 Detailed Description

Required registers to configure interrupts.

This structure applies to INT1 and INT2 as bit location are the same.

7.96.2 Member Data Documentation

7.96.2.1 int1_config0

```
int1_config0_t intx_configx_t::int1_config0
```

7.96.2.2 int1_config1

```
int1_config1_t intx_configx_t::int1_config1
```

The documentation for this struct was generated from the following file:

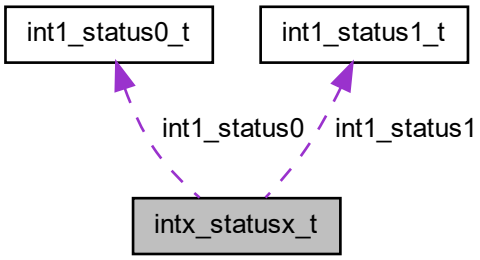
- inv_imu_defs.h

7.97 intx_statusx_t Struct Reference

Registers to retrieve interrupts status.

```
#include <inv_imu_defs.h>
```

Collaboration diagram for intx_statusx_t:



Public Attributes

- int1_status0_t int1_status0
- int1_status1_t int1_status1

7.97.1 Detailed Description

Registers to retrieve interrupts status.

This structure applies to INT1 and INT2 as bit location are the same.

7.97.2 Member Data Documentation

7.97.2.1 int1_status0

```
int1_status0_t intx_statusx_t::int1_status0
```

7.97.2.2 int1_status1

```
int1_status1_t intx_statusx_t::int1_status1
```

The documentation for this struct was generated from the following file:

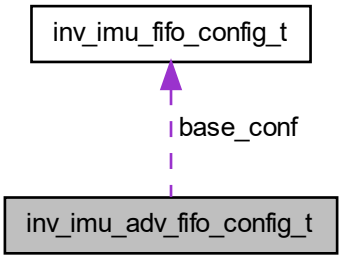
- inv_imu_defs.h

7.98 inv_imu_adv_fifo_config_t Struct Reference

FIFO configuration structure.

```
#include <inv_imu_driver_advanced.h>
```

Collaboration diagram for inv_imu_adv_fifo_config_t:



Public Attributes

- inv_imu_fifo_config_t base_conf
  Basic FIFO configuration.
- fifo_config2_fifo_wr_wm_gt_th_t fifo_wr_wm_gt_th
  Condition to trig watermark interrupt.
- uint8_t tmst_fsync_en
  Enable Timestamp or FSYNC delay in FIFO.
- uint8_t es1_en
  Enable External Sensor 1 to be pushed in FIFO.
- uint8_t es0_en
  Enable External Sensor 0 to be pushed in FIFO.
- fifo_config4_fifo_es0_6b_9b_t es0_6b_9b
  Size of the External Sensor 0 data (6 bytes or 9 bytes)
- uint8_t comp_en
  Enable FIFO compression.
- fifo_config4_fifo_comp_nc_flow_cfg_t comp_nc_flow_cfg
  Rate at which an uncompressed frame is generated.
- odr_decimate_config_gyro_fifo_odr_dec_t gyro_dec
  Decimation rate for gyro.
- odr_decimate_config_accel_fifo_odr_dec_t accel_dec
  Decimation rate for accel.

7.98.1 Detailed Description

FIFO configuration structure.

7.98.2 Member Data Documentation

7.98.2.1 accel_dec

```
odr_decimate_config_accel_fifo_odr_dec_t inv_imu_adv_fifo_config_t::accel_dec
```

Decimation rate for accel.

7.98.2.2 base_conf

```
inv_imu_fifo_config_t inv_imu_adv_fifo_config_t::base_conf
```

Basic FIFO configuration.

7.98.2.3 comp_en

`uint8_t inv_imu_adv_fifo_config_t::comp_en`

Enable FIFO compression.

7.98.2.4 comp_nc_flow_cfg

`fifo_config4_fifo_comp_nc_flow_cfg_t inv_imu_adv_fifo_config_t::comp_nc_flow_cfg`

Rate at which an uncompressed frame is generated.

7.98.2.5 es0_6b_9b

`fifo_config4_fifo_es0_6b_9b_t inv_imu_adv_fifo_config_t::es0_6b_9b`

Size of the External Sensor 0 data (6 bytes or 9 bytes)

7.98.2.6 es0_en

`uint8_t inv_imu_adv_fifo_config_t::es0_en`

Enable External Sensor 0 to be pushed in FIFO.

7.98.2.7 es1_en

`uint8_t inv_imu_adv_fifo_config_t::es1_en`

Enable External Sensor 1 to be pushed in FIFO.

7.98.2.8 fifo_wr_wm_gt_th

`fifo_config2_fifo_wr_wm_gt_th_t inv_imu_adv_fifo_config_t::fifo_wr_wm_gt_th`

Condition to trig watermark interrupt.

7.98.2.9 gyro_dec

```
odr_decimate_config_gyro_fifo_odr_dec_t inv_imu_adv_fifo_config_t::gyro_dec
```

Decimation rate for gyro.

7.98.2.10 tmst_fsync_en

```
uint8_t inv_imu_adv_fifo_config_t::tmst_fsync_en
```

Enable Timestamp or FSYNC delay in FIFO.

The documentation for this struct was generated from the following file:

- inv_imu_driver_advanced.h

7.99 inv_imu_adv_var_t Struct Reference

Definition of extended variables.

```
#include <inv_imu_driver_advanced.h>
```

Public Attributes

- void(∗ sensor_event_cb)(inv_imu_sensor_event_t ∗event)
  Callback executed when a new sensor event is available.
- uint8_t fifo_is_used
  Keeps track of FIFO usage.
- uint8_t fifo_comp_en
  Indicates if FIFO compression is enabled.
- fifo_config0_fifo_mode_t fifo_mode
  Current fifo mode.
- int16_t accel_baseline [3]
  Baseline for the accel.
- int16_t gyro_baseline [3]
  Baseline for the gyro.
- int16_t temp_baseline
  Baseline for the temperature sensor.
- uint8_t accel_baseline_found
  Flag indicating accel baseline has been found.
- uint8_t gyro_baseline_found
  Flag indicating gyro baseline has been found.
- uint8_t temp_baseline_found
  Flag indicating temperature baseline has been found.

7.99.1 Detailed Description

Definition of extended variables.

7.99.2 Member Data Documentation

7.99.2.1 accel_baseline

```
int16_t inv_imu_adv_var_t::accel_baseline[3]
```

Baseline for the accel.

7.99.2.2 accel_baseline_found

```
uint8_t inv_imu_adv_var_t::accel_baseline_found
```

Flag indicating accel baseline has been found.

7.99.2.3 fifo_comp_en

```
uint8_t inv_imu_adv_var_t::fifo_comp_en
```

Indicates if FIFO compression is enabled.

7.99.2.4 fifo_is_used

```
uint8_t inv_imu_adv_var_t::fifo_is_used
```

Keeps track of FIFO usage.

7.99.2.5 fifo_mode

```
fifo_config0_fifo_mode_t inv_imu_adv_var_t::fifo_mode
```

Current fifo mode.

Required by AN-000364

7.99.2.6 gyro_baseline

```
int16_t inv_imu_adv_var_t::gyro_baseline[3]
```

Baseline for the gyro.

7.99.2.7 gyro_baseline_found

```
uint8_t inv_imu_adv_var_t::gyro_baseline_found
```

Flag indicating gyro baseline has been found.

7.99.2.8 sensor_event_cb

```
void(* inv_imu_adv_var_t::sensor_event_cb) (inv_imu_sensor_event_t *event)
```

Callback executed when a new sensor event is available.

Parameters

in	*event*	Pointer to the sensor event.

7.99.2.9 temp_baseline

```
int16_t inv_imu_adv_var_t::temp_baseline
```

Baseline for the temperature sensor.

7.99.2.10 temp_baseline_found

```
uint8_t inv_imu_adv_var_t::temp_baseline_found
```

Flag indicating temperature baseline has been found.

The documentation for this struct was generated from the following file:

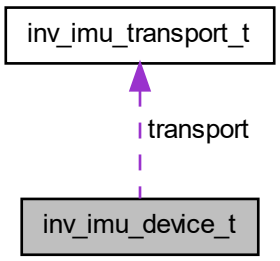
- inv_imu_driver_advanced.h

7.100 inv_imu_device_t Struct Reference

Basic driver configuration structure.

`#include <inv_imu_driver.h>`

Collaboration diagram for inv_imu_device_t:



Public Attributes

- inv_imu_transport_t transport

  Transport structure.
- uint8_t fifo_frame_size

  The calculated FIFO frame size in Bytes.
- uint8_t endianness_data

  Keeps track of data endianness mode 0 : data in Sensor Registers and FIFO are in Little Endian format 1 : data in Sensor Registers and FIFO are in Big Endian format.
- uint64_t adv_var [6]

  Memory area reserved for advanced module.

7.100.1 Detailed Description

Basic driver configuration structure.

7.100.2 Member Data Documentation

7.100.2.1 adv_var

```
uint64_t inv_imu_device_t::adv_var[6]
```

Memory area reserved for advanced module.

(only required when using advanced feature set).

Note

In case advanced module is not used, this field can be removed.

7.100.2.2 endianness_data

```
uint8_t inv_imu_device_t::endianness_data
```

Keeps track of data endianness mode 0 : data in Sensor Registers and FIFO are in Little Endian format 1 : data in Sensor Registers and FIFO are in Big Endian format.

7.100.2.3 fifo_frame_size

```
uint8_t inv_imu_device_t::fifo_frame_size
```

The calculated FIFO frame size in Bytes.

7.100.2.4 transport

```
inv_imu_transport_t inv_imu_device_t::transport
```

Transport structure.

The documentation for this struct was generated from the following file:

- inv_imu_driver.h

7.101 inv_imu_edmp_apex_parameters_t Struct Reference

IMU APEX inputs parameters definition.

```
#include <inv_imu_edmp.h>
```

Public Attributes

- uint32_t ped_amp_th
- uint16_t ped_step_cnt_th
- uint16_t ped_step_det_th
- uint16_t ped_sb_timer_th
- uint32_t ped_hi_en_th
- uint8_t ped_sensitivity_mode
- uint32_t ped_low_en_amp_th
- uint16_t tilt_wait_time
- uint8_t smd_sensitivity
- uint32_t r2w_sleep_time_out
- uint32_t r2w_sleep_gesture_delay
- uint32_t r2w_mounting_matrix
- uint32_t r2w_gravity_filter_gain
- uint32_t r2w_motion_th_angle_cosine
- uint32_t r2w_motion_th_timer_fast
- uint32_t r2w_motion_th_timer_slow
- uint32_t r2w_motion_prev_gravity_timeout
- uint32_t r2w_last_gravity_motion_timer
- uint32_t r2w_last_gravity_timeout
- uint32_t r2w_gesture_validity_timeout
- uint16_t lowg_peak_th
- uint16_t lowg_peak_th_hyst
- uint16_t lowg_time_th
- uint16_t highg_peak_th
- uint16_t highg_peak_th_hyst
- uint16_t highg_time_th
- uint32_t ff_min_duration
- uint32_t ff_max_duration
- uint32_t ff_debounce_duration
- uint8_t tap_min_jerk
- uint16_t tap_tmax
- uint8_t tap_tmin
- uint8_t tap_max_peak_tol
- uint8_t tap_smudge_reject_th
- uint8_t tap_tavg
- int32_t soft_iron_sensitivity_matrix [9]
- int32_t hard_iron_offset [3]
- uint32_t power_save_time
- uint8_t power_save_en

7.101.1 Detailed Description

IMU APEX inputs parameters definition.

Note

Refer to the datasheet for details on how to configure these parameters.

7.101.2 Member Data Documentation

7.101.2.1 ff_debounce_duration

```
uint32_t inv_imu_edmp_apex_parameters_t::ff_debounce_duration
```

7.101.2.2 ff_max_duration

```
uint32_t inv_imu_edmp_apex_parameters_t::ff_max_duration
```

7.101.2.3 ff_min_duration

```
uint32_t inv_imu_edmp_apex_parameters_t::ff_min_duration
```

7.101.2.4 hard_iron_offset

```
int32_t inv_imu_edmp_apex_parameters_t::hard_iron_offset[3]
```

7.101.2.5 highg_peak_th

```
uint16_t inv_imu_edmp_apex_parameters_t::highg_peak_th
```

7.101.2.6 highg_peak_th_hyst

```
uint16_t inv_imu_edmp_apex_parameters_t::highg_peak_th_hyst
```

7.101.2.7 highg_time_th

```
uint16_t inv_imu_edmp_apex_parameters_t::highg_time_th
```

7.101.2.8 lowg_peak_th

```
uint16_t inv_imu_edmp_apex_parameters_t::lowg_peak_th
```

7.101.2.9 lowg_peak_th_hyst

```
uint16_t inv_imu_edmp_apex_parameters_t::lowg_peak_th_hyst
```

7.101.2.10 lowg_time_th

```
uint16_t inv_imu_edmp_apex_parameters_t::lowg_time_th
```

7.101.2.11 ped_amp_th

```
uint32_t inv_imu_edmp_apex_parameters_t::ped_amp_th
```

7.101.2.12 ped_hi_en_th

```
uint32_t inv_imu_edmp_apex_parameters_t::ped_hi_en_th
```

7.101.2.13 ped_low_en_amp_th

```
uint32_t inv_imu_edmp_apex_parameters_t::ped_low_en_amp_th
```

7.101.2.14 ped_sb_timer_th

```
uint16_t inv_imu_edmp_apex_parameters_t::ped_sb_timer_th
```

7.101.2.15 ped_sensitivity_mode

```
uint8_t inv_imu_edmp_apex_parameters_t::ped_sensitivity_mode
```

7.101.2.16 ped_step_cnt_th

```
uint16_t inv_imu_edmp_apex_parameters_t::ped_step_cnt_th
```

7.101.2.17 ped_step_det_th

```
uint16_t inv_imu_edmp_apex_parameters_t::ped_step_det_th
```

7.101.2.18 power_save_en

```
uint8_t inv_imu_edmp_apex_parameters_t::power_save_en
```

7.101.2.19 power_save_time

```
uint32_t inv_imu_edmp_apex_parameters_t::power_save_time
```

7.101.2.20 r2w_gesture_validity_timeout

```
uint32_t inv_imu_edmp_apex_parameters_t::r2w_gesture_validity_timeout
```

7.101.2.21 r2w_gravity_filter_gain

```
uint32_t inv_imu_edmp_apex_parameters_t::r2w_gravity_filter_gain
```

7.101.2.22 r2w_last_gravity_motion_timer

```
uint32_t inv_imu_edmp_apex_parameters_t::r2w_last_gravity_motion_timer
```

7.101.2.23 r2w_last_gravity_timeout

```
uint32_t inv_imu_edmp_apex_parameters_t::r2w_last_gravity_timeout
```

7.101.2.24 r2w_motion_prev_gravity_timeout

```
uint32_t inv_imu_edmp_apex_parameters_t::r2w_motion_prev_gravity_timeout
```

7.101.2.25 r2w_motion_th_angle_cosine

```
uint32_t inv_imu_edmp_apex_parameters_t::r2w_motion_th_angle_cosine
```

7.101.2.26 r2w_motion_th_timer_fast

```
uint32_t inv_imu_edmp_apex_parameters_t::r2w_motion_th_timer_fast
```

7.101.2.27 r2w_motion_th_timer_slow

```
uint32_t inv_imu_edmp_apex_parameters_t::r2w_motion_th_timer_slow
```

7.101.2.28 r2w_mounting_matrix

```
uint32_t inv_imu_edmp_apex_parameters_t::r2w_mounting_matrix
```

7.101.2.29 r2w_sleep_gesture_delay

```
uint32_t inv_imu_edmp_apex_parameters_t::r2w_sleep_gesture_delay
```

7.101.2.30 r2w_sleep_time_out

```
uint32_t inv_imu_edmp_apex_parameters_t::r2w_sleep_time_out
```

7.101.2.31 smd_sensitivity

```
uint8_t inv_imu_edmp_apex_parameters_t::smd_sensitivity
```

7.101.2.32 soft_iron_sensitivity_matrix

```
int32_t inv_imu_edmp_apex_parameters_t::soft_iron_sensitivity_matrix[9]
```

7.101.2.33 tap_max_peak_tol

```
uint8_t inv_imu_edmp_apex_parameters_t::tap_max_peak_tol
```

7.101.2.34 tap_min_jerk

```
uint8_t inv_imu_edmp_apex_parameters_t::tap_min_jerk
```

7.101.2.35 tap_smudge_reject_th

```
uint8_t inv_imu_edmp_apex_parameters_t::tap_smudge_reject_th
```

7.101.2.36 tap_tavg

```
uint8_t inv_imu_edmp_apex_parameters_t::tap_tavg
```

7.101.2.37 tap_tmax

```
uint16_t inv_imu_edmp_apex_parameters_t::tap_tmax
```

7.101.2.38 tap_tmin

```
uint8_t inv_imu_edmp_apex_parameters_t::tap_tmin
```

7.101.2.39 tilt_wait_time

```
uint16_t inv_imu_edmp_apex_parameters_t::tilt_wait_time
```

The documentation for this struct was generated from the following file:

- inv_imu_edmp.h

7.102 inv_imu_edmp_b2s_parameters_t Struct Reference

IMU B2S parameters definition.

`#include <inv_imu_edmp_wearable.h>`

Public Attributes

- uint32_t b2s_mounting_matrix

  Specifies mounting matrix to be applied to B2S raw data Set bit 2 : swap X/Y ; flip Z Set bit 1 : flip X ; flip Z Set bit 0 : flip Y ; flip Z.

7.102.1 Detailed Description

IMU B2S parameters definition.

7.102.2 Member Data Documentation

7.102.2.1 b2s_mounting_matrix

`uint32_t inv_imu_edmp_b2s_parameters_t::b2s_mounting_matrix`

Specifies mounting matrix to be applied to B2S raw data Set bit 2 : swap X/Y ; flip Z Set bit 1 : flip X ; flip Z Set bit 0 : flip Y ; flip Z.

The documentation for this struct was generated from the following file:

- inv_imu_edmp_wearable.h

7.103 inv_imu_edmp_int_state_t Struct Reference

APEX interrupts definition.

`#include <inv_imu_edmp.h>`

Public Attributes

- uint8_t INV_TAP
- uint8_t INV_HIGHG
- uint8_t INV_LOWG
- uint8_t INV_TILT_DET
- uint8_t INV_STEP_CNT_OVFL
- uint8_t INV_STEP_DET
- uint8_t INV_FF
- uint8_t INV_R2W
- uint8_t INV_B2S
- uint8_t INV_R2W_SLEEP
- uint8_t INV_B2S_REV
- uint8_t INV_SMD
- uint8_t INV_SELF_TEST
- uint8_t INV_SEC_AUTH

7.103.1 Detailed Description

APEX interrupts definition.

7.103.2 Member Data Documentation

7.103.2.1 INV_B2S

```
uint8_t inv_imu_edmp_int_state_t::INV_B2S
```

7.103.2.2 INV_B2S_REV

```
uint8_t inv_imu_edmp_int_state_t::INV_B2S_REV
```

7.103.2.3 INV_FF

```
uint8_t inv_imu_edmp_int_state_t::INV_FF
```

7.103.2.4 INV_HIGHG

```
uint8_t inv_imu_edmp_int_state_t::INV_HIGHG
```

7.103.2.5 INV_LOWG

```
uint8_t inv_imu_edmp_int_state_t::INV_LOWG
```

7.103.2.6 INV_R2W

```
uint8_t inv_imu_edmp_int_state_t::INV_R2W
```

7.103.2.7 INV_R2W_SLEEP

uint8_t inv_imu_edmp_int_state_t::INV_R2W_SLEEP

7.103.2.8 INV_SEC_AUTH

uint8_t inv_imu_edmp_int_state_t::INV_SEC_AUTH

7.103.2.9 INV_SELF_TEST

uint8_t inv_imu_edmp_int_state_t::INV_SELF_TEST

7.103.2.10 INV_SMD

uint8_t inv_imu_edmp_int_state_t::INV_SMD

7.103.2.11 INV_STEP_CNT_OVFL

uint8_t inv_imu_edmp_int_state_t::INV_STEP_CNT_OVFL

7.103.2.12 INV_STEP_DET

uint8_t inv_imu_edmp_int_state_t::INV_STEP_DET

7.103.2.13 INV_TAP

uint8_t inv_imu_edmp_int_state_t::INV_TAP

7.103.2.14 INV_TILT_DET

```
uint8_t inv_imu_edmp_int_state_t::INV_TILT_DET
```

The documentation for this struct was generated from the following file:

- inv_imu_edmp.h

7.104 inv_imu_edmp_pedometer_data_t Struct Reference

Pedometer outputs.

```
#include <inv_imu_edmp.h>
```

Public Attributes

- uint16_t step_cnt
  Number of steps.
- uint8_t step_cadence
  Walk/Run cadency in number of samples.
- inv_imu_edmp_activity_class_t activity_class
  Detected activity.

7.104.1 Detailed Description

Pedometer outputs.

7.104.2 Member Data Documentation

7.104.2.1 activity_class

```
inv_imu_edmp_activity_class_t inv_imu_edmp_pedometer_data_t::activity_class
```

Detected activity.

7.104.2.2 step_cadence

```
uint8_t inv_imu_edmp_pedometer_data_t::step_cadence
```

Walk/Run cadency in number of samples.

Number of samples between two steps with u6.2 format (8-bits unsigned in Q2). cadency (steps/s) = EDMP_↩ ODR_HZ / (step_cadence ∗ 0.25)

7.104.2.3 step_cnt

```
uint16_t inv_imu_edmp_pedometer_data_t::step_cnt
```

Number of steps.

The documentation for this struct was generated from the following file:

- inv_imu_edmp.h

7.105 inv_imu_edmp_tap_data_t Struct Reference

Tap outputs.

```
#include <inv_imu_edmp.h>
```

Public Attributes

- inv_imu_edmp_tap_num_t num
- inv_imu_edmp_tap_axis_t axis
- inv_imu_edmp_tap_dir_t direction
- uint8_t double_tap_timing

7.105.1 Detailed Description

Tap outputs.

7.105.2 Member Data Documentation

7.105.2.1 axis

```
inv_imu_edmp_tap_axis_t inv_imu_edmp_tap_data_t::axis
```

7.105.2.2 direction

```
inv_imu_edmp_tap_dir_t inv_imu_edmp_tap_data_t::direction
```

7.105.2.3 double_tap_timing

```
uint8_t inv_imu_edmp_tap_data_t::double_tap_timing
```

7.105.2.4 num

```
inv_imu_edmp_tap_num_t inv_imu_edmp_tap_data_t::num
```

The documentation for this struct was generated from the following file:

- inv_imu_edmp.h

7.106 inv_imu_fifo_config_t Struct Reference

Basic FIFO configuration.

```
#include <inv_imu_driver.h>
```

Public Attributes

- uint8_t gyro_en
  Enable Gyro in FIFO.
- uint8_t accel_en
  Enable Accel in FIFO.
- uint8_t hires_en
  Enable High Resolution mode (20-bits long data)
- uint16_t fifo_wm_th
  Watermark threshold value.
- fifo_config0_fifo_mode_t fifo_mode
  Operating mode of the FIFO.
- fifo_config0_fifo_depth_t fifo_depth
  FIFO size.

7.106.1 Detailed Description

Basic FIFO configuration.

7.106.2 Member Data Documentation

7.106.2.1 accel_en

```
uint8_t inv_imu_fifo_config_t::accel_en
```

Enable Accel in FIFO.

7.106.2.2 fifo_depth

```
fifo_config0_fifo_depth_t inv_imu_fifo_config_t::fifo_depth
```

FIFO size.

7.106.2.3 fifo_mode

```
fifo_config0_fifo_mode_t inv_imu_fifo_config_t::fifo_mode
```

Operating mode of the FIFO.

7.106.2.4 fifo_wm_th

```
uint16_t inv_imu_fifo_config_t::fifo_wm_th
```

Watermark threshold value.

7.106.2.5 gyro_en

```
uint8_t inv_imu_fifo_config_t::gyro_en
```

Enable Gyro in FIFO.

7.106.2.6 hires_en

```
uint8_t inv_imu_fifo_config_t::hires_en
```

Enable High Resolution mode (20-bits long data)

The documentation for this struct was generated from the following file:

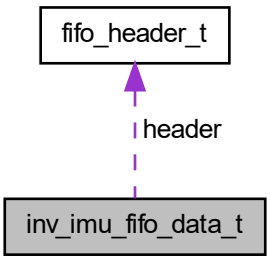
- inv_imu_driver.h

7.107 inv_imu_fifo_data_t Union Reference

One frame of FIFO header+data.

`#include <inv_imu_driver.h>`

Collaboration diagram for inv_imu_fifo_data_t:



Public Attributes

- fifo_header_t header
- struct {
  fifo_header_t header
  int16_t sensor_data [3]
  int8_t temp_data
  } byte_8

- struct {
  fifo_header_t header
  int16_t accel_data [3]
  int16_t gyro_data [3]
  int8_t temp_data
  uint16_t timestamp
  } byte_16

- struct {
  fifo_header_t header
  int32_t accel_data [3]
  int32_t gyro_data [3]
  int16_t temp_data
  uint16_t timestamp
  } byte_20

7.107.1 Detailed Description

One frame of FIFO header+data.

7.107.2 Member Data Documentation

7.107.2.1 accel_data [1/2]

```
int16_t inv_imu_fifo_data_t::accel_data[3]
```

7.107.2.2 accel_data [2/2]

```
int32_t inv_imu_fifo_data_t::accel_data[3]
```

7.107.2.3

```
struct { ... } inv_imu_fifo_data_t::byte_16
```

7.107.2.4

```
struct { ... } inv_imu_fifo_data_t::byte_20
```

7.107.2.5

```
struct { ... } inv_imu_fifo_data_t::byte_8
```

7.107.2.6 gyro_data [1/2]

```
int16_t inv_imu_fifo_data_t::gyro_data[3]
```

7.107.2.7 gyro_data [2/2]

```
int32_t inv_imu_fifo_data_t::gyro_data[3]
```

7.107.2.8 header

```
fifo_header_t inv_imu_fifo_data_t::header
```

7.107.2.9 sensor_data

```
int16_t inv_imu_fifo_data_t::sensor_data[3]
```

7.107.2.10 temp_data [1/2]

```
int8_t inv_imu_fifo_data_t::temp_data
```

7.107.2.11 temp_data [2/2]

```
int16_t inv_imu_fifo_data_t::temp_data
```

7.107.2.12 timestamp

```
uint16_t inv_imu_fifo_data_t::timestamp
```

The documentation for this union was generated from the following file:

- inv_imu_driver.h

7.108 inv_imu_int_pin_config_t Struct Reference

Interrupts pin configuration.

```
#include <inv_imu_defs.h>
```

Public Attributes

- intx_config2_intx_polarity_t int_polarity
- intx_config2_intx_mode_t int_mode
- intx_config2_intx_drive_t int_drive

7.108.1 Detailed Description

Interrupts pin configuration.

7.108.2 Member Data Documentation

7.108.2.1 int_drive

```
intx_config2_intx_drive_t inv_imu_int_pin_config_t::int_drive
```

7.108.2.2 int_mode

```
intx_config2_intx_mode_t inv_imu_int_pin_config_t::int_mode
```

7.108.2.3 int_polarity

```
intx_config2_intx_polarity_t inv_imu_int_pin_config_t::int_polarity
```

The documentation for this struct was generated from the following file:

- inv_imu_defs.h

7.109 inv_imu_int_state_t Struct Reference

Interrupts definition.

```
#include <inv_imu_driver.h>
```

Public Attributes

- uint8_t INV_FIFO_FULL
- uint8_t INV_FIFO_THS
- uint8_t INV_UI_DRDY
- uint8_t INV_OIS1
- uint8_t INV_UI_FSYNC
- uint8_t INV_AGC_RDY
- uint8_t INV_OIS1_AGC_RDY
- uint8_t INV_RESET_DONE
- uint8_t INV_PLL_RDY
- uint8_t INV_WOM_X
- uint8_t INV_WOM_Y
- uint8_t INV_WOM_Z
- uint8_t INV_I3C_PROT_ERR
- uint8_t INV_I2CM_DONE
- uint8_t INV_EDMP_EVENT

7.109.1 Detailed Description

Interrupts definition.

7.109.2 Member Data Documentation

7.109.2.1 INV_AGC_RDY

```
uint8_t inv_imu_int_state_t::INV_AGC_RDY
```

7.109.2.2 INV_EDMP_EVENT

```
uint8_t inv_imu_int_state_t::INV_EDMP_EVENT
```

7.109.2.3 INV_FIFO_FULL

```
uint8_t inv_imu_int_state_t::INV_FIFO_FULL
```

7.109.2.4 INV_FIFO_THS

```
uint8_t inv_imu_int_state_t::INV_FIFO_THS
```

7.109.2.5 INV_I2CM_DONE

```
uint8_t inv_imu_int_state_t::INV_I2CM_DONE
```

7.109.2.6 INV_I3C_PROT_ERR

```
uint8_t inv_imu_int_state_t::INV_I3C_PROT_ERR
```

7.109.2.7 INV_OIS1

uint8_t inv_imu_int_state_t::INV_OIS1

7.109.2.8 INV_OIS1_AGC_RDY

uint8_t inv_imu_int_state_t::INV_OIS1_AGC_RDY

7.109.2.9 INV_PLL_RDY

uint8_t inv_imu_int_state_t::INV_PLL_RDY

7.109.2.10 INV_RESET_DONE

uint8_t inv_imu_int_state_t::INV_RESET_DONE

7.109.2.11 INV_UI_DRDY

uint8_t inv_imu_int_state_t::INV_UI_DRDY

7.109.2.12 INV_UI_FSYNC

uint8_t inv_imu_int_state_t::INV_UI_FSYNC

7.109.2.13 INV_WOM_X

uint8_t inv_imu_int_state_t::INV_WOM_X

7.109.2.14 INV_WOM_Y

uint8_t inv_imu_int_state_t::INV_WOM_Y

7.109.2.15 INV_WOM_Z

```
uint8_t inv_imu_int_state_t::INV_WOM_Z
```

The documentation for this struct was generated from the following file:

- inv_imu_driver.h

7.110 inv_imu_selftest_output_t Struct Reference

Self-test outputs.

```
#include <inv_imu_selftest.h>
```

Public Attributes

- int8_t accel_status
  Global accel self-test status.
- int8_t gyro_status
  Global gyro self-test status.
- int8_t ax_status
  AX self-test status.
- int8_t ay_status
  AY self-test status.
- int8_t az_status
  AZ self-test status.
- int8_t gx_status
  GX self-test status.
- int8_t gy_status
  GY self-test status.
- int8_t gz_status
  GZ self-test status.

7.110.1 Detailed Description

Self-test outputs.

7.110.2 Member Data Documentation

7.110.2.1 accel_status

```
int8_t inv_imu_selftest_output_t::accel_status
```

Global accel self-test status.

1 for success, 0 otherwise.

7.110.2.2 ax_status

```
int8_t inv_imu_selftest_output_t::ax_status
```

AX self-test status.

1 for success, 0 otherwise.

7.110.2.3 ay_status

```
int8_t inv_imu_selftest_output_t::ay_status
```

AY self-test status.

1 for success, 0 otherwise.

7.110.2.4 az_status

```
int8_t inv_imu_selftest_output_t::az_status
```

AZ self-test status.

1 for success, 0 otherwise.

7.110.2.5 gx_status

```
int8_t inv_imu_selftest_output_t::gx_status
```

GX self-test status.

1 for success, 0 otherwise.

7.110.2.6 gy_status

```
int8_t inv_imu_selftest_output_t::gy_status
```

GY self-test status.

1 for success, 0 otherwise.

7.110.2.7 gyro_status

```
int8_t inv_imu_selftest_output_t::gyro_status
```

Global gyro self-test status.

1 for success, 0 otherwise.

7.110.2.8 gz_status

```
int8_t inv_imu_selftest_output_t::gz_status
```

GZ self-test status.

1 for success, 0 otherwise.

The documentation for this struct was generated from the following file:

- inv_imu_selftest.h

7.111 inv_imu_selftest_parameters_t Struct Reference

Self-Test parameters.

```
#include <inv_imu_selftest.h>
```

Public Attributes

- uint8_t accel_en
  If set, enable accel self-test.
- uint8_t gyro_en
  If set, enable gyro self-test.
- selftest_average_time_t avg_time
  Averaging time used to perform self-test.
- selftest_accel_threshold_t accel_limit
  Tolerance between factory trim and accel self-test response.
- selftest_gyro_threshold_t gyro_limit
  Tolerance between factory trim and gyro self-test response.
- uint32_t patch_settings
  Mechanism for adding patches to self-test operations.

7.111.1 Detailed Description

Self-Test parameters.

7.111.2 Member Data Documentation

7.111.2.1 accel_en

```
uint8_t inv_imu_selftest_parameters_t::accel_en
```

If set, enable accel self-test.

7.111.2.2 accel_limit

`selftest_accel_threshold_t inv_imu_selftest_parameters_t::accel_limit`

Tolerance between factory trim and accel self-test response.

7.111.2.3 avg_time

`selftest_average_time_t inv_imu_selftest_parameters_t::avg_time`

Averaging time used to perform self-test.

7.111.2.4 gyro_en

`uint8_t inv_imu_selftest_parameters_t::gyro_en`

If set, enable gyro self-test.

7.111.2.5 gyro_limit

`selftest_gyro_threshold_t inv_imu_selftest_parameters_t::gyro_limit`

Tolerance between factory trim and gyro self-test response.

7.111.2.6 patch_settings

`uint32_t inv_imu_selftest_parameters_t::patch_settings`

Mechanism for adding patches to self-test operations.

The documentation for this struct was generated from the following file:

- inv_imu_selftest.h

7.112 inv_imu_sensor_data_t Struct Reference

Sensor data from registers.

`#include <inv_imu_defs.h>`

Public Attributes

- int16_t accel_data [3]
- int16_t gyro_data [3]
- int16_t temp_data

7.112.1 Detailed Description

Sensor data from registers.

7.112.2 Member Data Documentation

7.112.2.1 accel_data

```
int16_t inv_imu_sensor_data_t::accel_data[3]
```

7.112.2.2 gyro_data

```
int16_t inv_imu_sensor_data_t::gyro_data[3]
```

7.112.2.3 temp_data

```
int16_t inv_imu_sensor_data_t::temp_data
```

The documentation for this struct was generated from the following file:

- inv_imu_defs.h

7.113 inv_imu_sensor_event_t Struct Reference

Sensor event structure definition.

```
#include <inv_imu_driver_advanced.h>
```

Public Attributes

- int sensor_mask

  Specifies which sensors are available in the event (defined by inv_imu_sensor_id_t as a mask)
- uint16_t timestamp_fsync

  Value of the FIFO timestamp (if FIFO is used)
- int16_t accel [3]

  Accel raw data.
- int16_t gyro [3]

  Gyro raw data.
- int16_t temperature

  Temperature raw data.
- int8_t accel_high_res [3]

  High-res portion of the accel raw data (if using high-res mode)
- int8_t gyro_high_res [3]

  High-res portion of the accel raw data (if using high-res mode)
- uint8_t es0 [9]

  Buffer for external sensor 0 connected to EDMP.
- uint8_t es1 [6]

  Buffer for external sensor 1 connected to EDMP.

7.113.1 Detailed Description

Sensor event structure definition.

7.113.2 Member Data Documentation

7.113.2.1 accel

```
int16_t inv_imu_sensor_event_t::accel[3]
```

Accel raw data.

7.113.2.2 accel_high_res

```
int8_t inv_imu_sensor_event_t::accel_high_res[3]
```

High-res portion of the accel raw data (if using high-res mode)

7.113.2.3 es0

```
uint8_t inv_imu_sensor_event_t::es0[9]
```

Buffer for external sensor 0 connected to EDMP.

7.113.2.4 es1

```
uint8_t inv_imu_sensor_event_t::es1[6]
```

Buffer for external sensor 1 connected to EDMP.

7.113.2.5 gyro

```
int16_t inv_imu_sensor_event_t::gyro[3]
```

Gyro raw data.

7.113.2.6 gyro_high_res

```
int8_t inv_imu_sensor_event_t::gyro_high_res[3]
```

High-res portion of the accel raw data (if using high-res mode)

7.113.2.7 sensor_mask

```
int inv_imu_sensor_event_t::sensor_mask
```

Specifies which sensors are available in the event (defined by inv_imu_sensor_id_t as a mask)

7.113.2.8 temperature

```
int16_t inv_imu_sensor_event_t::temperature
```

Temperature raw data.

7.113.2.9 timestamp_fsync

```
uint16_t inv_imu_sensor_event_t::timestamp_fsync
```

Value of the FIFO timestamp (if FIFO is used)

The documentation for this struct was generated from the following file:

- inv_imu_driver_advanced.h

7.114 inv_imu_transport_t Struct Reference

Structure dedicated to transport layer transport interface.

```
#include <inv_imu_transport.h>
```

Public Attributes

- inv_imu_read_reg_t read_reg
  Function pointer to read register(s).
- inv_imu_write_reg_t write_reg
  Function pointer to write register(s).
- uint32_t serif_type
  Serial interface type.
- void(∗ sleep_us)(uint32_t us)
  Callback to sleep function.

7.114.1 Detailed Description

Structure dedicated to transport layer transport interface.

7.114.2 Member Data Documentation

7.114.2.1 read_reg

```
inv_imu_read_reg_t inv_imu_transport_t::read_reg
```

Function pointer to read register(s).

7.114.2.2 serif_type

```
uint32_t inv_imu_transport_t::serif_type
```

Serial interface type.

7.114.2.3 sleep_us

```
void(* inv_imu_transport_t::sleep_us) (uint32_t us)
```

Callback to sleep function.

Parameters

in	*us*	Time to sleep in microseconds.

7.114.2.4 write_reg

```
inv_imu_write_reg_t inv_imu_transport_t::write_reg
```

Function pointer to write register(s).

The documentation for this struct was generated from the following file:

- inv_imu_transport.h

7.115 ioc_pad_scenario_aux_ovrd_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t aux1_enable_ovrd_val: 1
- uint8_t aux1_enable_ovrd: 1
- uint8_t aux1_mode_ovrd_val: 2
- uint8_t aux1_mode_ovrd: 1
- uint8_t aux2_enable_ovrd_val: 1
- uint8_t aux2_enable_ovrd: 1
- uint8_t resv_1: 1

7.115.1 Member Data Documentation

7.115.1.1 aux1_enable_ovrd

```
uint8_t ioc_pad_scenario_aux_ovrd_t::aux1_enable_ovrd
```

7.115.1.2 aux1_enable_ovrd_val

```
uint8_t ioc_pad_scenario_aux_ovrd_t::aux1_enable_ovrd_val
```

7.115.1.3 aux1_mode_ovrd

```
uint8_t ioc_pad_scenario_aux_ovrd_t::aux1_mode_ovrd
```

7.115.1.4 aux1_mode_ovrd_val

```
uint8_t ioc_pad_scenario_aux_ovrd_t::aux1_mode_ovrd_val
```

7.115.1.5 aux2_enable_ovrd

```
uint8_t ioc_pad_scenario_aux_ovrd_t::aux2_enable_ovrd
```

7.115.1.6 aux2_enable_ovrd_val

```
uint8_t ioc_pad_scenario_aux_ovrd_t::aux2_enable_ovrd_val
```

7.115.1.7 resv_1

```
uint8_t ioc_pad_scenario_aux_ovrd_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.116 ioc_pad_scenario_ovrd_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t pads_int2_cfg_ovrd_val: 2
- uint8_t pads_int2_cfg_ovrd: 1
- uint8_t resv_1: 5

7.116.1 Member Data Documentation

7.116.1.1 pads_int2_cfg_ovrd

```
uint8_t ioc_pad_scenario_ovrd_t::pads_int2_cfg_ovrd
```

7.116.1.2 pads_int2_cfg_ovrd_val

```
uint8_t ioc_pad_scenario_ovrd_t::pads_int2_cfg_ovrd_val
```

7.116.1.3 resv_1

```
uint8_t ioc_pad_scenario_ovrd_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.117 ioc_pad_scenario_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t aux1_enable: 1
- uint8_t aux1_mode: 2
- uint8_t aux2_enable: 1
- uint8_t pads_int2_cfg: 2
- uint8_t resv_1: 2

7.117.1 Member Data Documentation

7.117.1.1 aux1_enable

```
uint8_t ioc_pad_scenario_t::aux1_enable
```

7.117.1.2 aux1_mode

```
uint8_t ioc_pad_scenario_t::aux1_mode
```

7.117.1.3 aux2_enable

```
uint8_t ioc_pad_scenario_t::aux2_enable
```

7.117.1.4 pads_int2_cfg

```
uint8_t ioc_pad_scenario_t::pads_int2_cfg
```

7.117.1.5 resv_1

```
uint8_t ioc_pad_scenario_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.118 ipreg_bar_reg_57_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t resv_1: 5
- uint8_t io_opt1: 1
- uint8_t io_opt0: 1
- uint8_t resv_2: 1

7.118.1 Member Data Documentation

7.118.1.1 io_opt0

```
uint8_t ipreg_bar_reg_57_t::io_opt0
```

7.118.1.2 io_opt1

```
uint8_t ipreg_bar_reg_57_t::io_opt1
```

7.118.1.3 resv_1

```
uint8_t ipreg_bar_reg_57_t::resv_1
```

7.118.1.4 resv_2

```
uint8_t ipreg_bar_reg_57_t::resv_2
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.119 ipreg_bar_reg_58_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t io_opt2: 1
- uint8_t resv_1: 2
- uint8_t pads_ap_cs_pe_trim_d2a: 1
- uint8_t pads_ap_cs_pud_trim_d2a: 1
- uint8_t resv_2: 1
- uint8_t pads_ap_sclk_pe_trim_d2a: 1
- uint8_t pads_ap_sclk_pud_trim_d2a: 1

7.119.1 Member Data Documentation

7.119.1.1 io_opt2

```
uint8_t ipreg_bar_reg_58_t::io_opt2
```

7.119.1.2 pads_ap_cs_pe_trim_d2a

```
uint8_t ipreg_bar_reg_58_t::pads_ap_cs_pe_trim_d2a
```

7.119.1.3 pads_ap_cs_pud_trim_d2a

```
uint8_t ipreg_bar_reg_58_t::pads_ap_cs_pud_trim_d2a
```

7.119.1.4 pads_ap_sclk_pe_trim_d2a

```
uint8_t ipreg_bar_reg_58_t::pads_ap_sclk_pe_trim_d2a
```

7.119.1.5 pads_ap_sclk_pud_trim_d2a

```
uint8_t ipreg_bar_reg_58_t::pads_ap_sclk_pud_trim_d2a
```

7.119.1.6 resv_1

```
uint8_t ipreg_bar_reg_58_t::resv_1
```

7.119.1.7 resv_2

```
uint8_t ipreg_bar_reg_58_t::resv_2
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.120 ipreg_bar_reg_59_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t resv_1: 1
- uint8_t pads_ap_sdi_pe_trim_d2a: 1
- uint8_t pads_ap_sdi_pud_trim_d2a: 1
- uint8_t resv_2: 1
- uint8_t pads_ap_sdo_pe_trim_d2a: 1
- uint8_t pads_ap_sdo_pud_trim_d2a: 1
- uint8_t resv_3: 1
- uint8_t pads_pin7_pe_trim_d2a: 1

7.120.1 Member Data Documentation

7.120.1.1 pads_ap_sdi_pe_trim_d2a

`uint8_t ipreg_bar_reg_59_t::pads_ap_sdi_pe_trim_d2a`

7.120.1.2 pads_ap_sdi_pud_trim_d2a

`uint8_t ipreg_bar_reg_59_t::pads_ap_sdi_pud_trim_d2a`

7.120.1.3 pads_ap_sdo_pe_trim_d2a

`uint8_t ipreg_bar_reg_59_t::pads_ap_sdo_pe_trim_d2a`

7.120.1.4 pads_ap_sdo_pud_trim_d2a

`uint8_t ipreg_bar_reg_59_t::pads_ap_sdo_pud_trim_d2a`

7.120.1.5 pads_pin7_pe_trim_d2a

```
uint8_t ipreg_bar_reg_59_t::pads_pin7_pe_trim_d2a
```

7.120.1.6 resv_1

```
uint8_t ipreg_bar_reg_59_t::resv_1
```

7.120.1.7 resv_2

```
uint8_t ipreg_bar_reg_59_t::resv_2
```

7.120.1.8 resv_3

```
uint8_t ipreg_bar_reg_59_t::resv_3
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.121 ipreg_bar_reg_60_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t pads_pin7_cs_pud_trim_d2a: 1
- uint8_t resv_1: 1
- uint8_t pads_aux1_cs_pe_trim_d2a: 1
- uint8_t pads_aux1_cs_pud_trim_d2a: 1
- uint8_t pads_aux_sclk_tp2_from_pad_disable_trim_d2a: 1
- uint8_t pads_aux1_sclk_pe_trim_d2a: 1
- uint8_t pads_aux1_sclk_pud_trim_d2a: 1
- uint8_t resv_2: 1

7.121.1 Member Data Documentation

7.121.1.1 pads_aux1_cs_pe_trim_d2a

```
uint8_t ipreg_bar_reg_60_t::pads_aux1_cs_pe_trim_d2a
```

7.121.1.2 pads_aux1_cs_pud_trim_d2a

```
uint8_t ipreg_bar_reg_60_t::pads_aux1_cs_pud_trim_d2a
```

7.121.1.3 pads_aux1_sclk_pe_trim_d2a

```
uint8_t ipreg_bar_reg_60_t::pads_aux1_sclk_pe_trim_d2a
```

7.121.1.4 pads_aux1_sclk_pud_trim_d2a

```
uint8_t ipreg_bar_reg_60_t::pads_aux1_sclk_pud_trim_d2a
```

7.121.1.5 pads_aux_sclk_tp2_from_pad_disable_trim_d2a

```
uint8_t ipreg_bar_reg_60_t::pads_aux_sclk_tp2_from_pad_disable_trim_d2a
```

7.121.1.6 pads_pin7_cs_pud_trim_d2a

```
uint8_t ipreg_bar_reg_60_t::pads_pin7_cs_pud_trim_d2a
```

7.121.1.7 resv_1

```
uint8_t ipreg_bar_reg_60_t::resv_1
```

7.121.1.8 resv_2

```
uint8_t ipreg_bar_reg_60_t::resv_2
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.122 ipreg_bar_reg_61_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t pads_aux1_sdi_pe_trim_d2a: 1
- uint8_t pads_aux1_sdi_pud_trim_d2a: 1
- uint8_t resv_1: 1
- uint8_t pads_aux1_sdo_pe_trim_d2a: 1
- uint8_t pads_aux1_sdo_pud_trim_d2a: 1
- uint8_t resv_2: 1
- uint8_t pads_int1_pe_trim_d2a: 1
- uint8_t pads_int1_pud_trim_d2a: 1

7.122.1 Member Data Documentation

7.122.1.1 pads_aux1_sdi_pe_trim_d2a

```
uint8_t ipreg_bar_reg_61_t::pads_aux1_sdi_pe_trim_d2a
```

7.122.1.2 pads_aux1_sdi_pud_trim_d2a

```
uint8_t ipreg_bar_reg_61_t::pads_aux1_sdi_pud_trim_d2a
```

7.122.1.3 pads_aux1_sdo_pe_trim_d2a

```
uint8_t ipreg_bar_reg_61_t::pads_aux1_sdo_pe_trim_d2a
```

7.122.1.4 pads_aux1_sdo_pud_trim_d2a

```
uint8_t ipreg_bar_reg_61_t::pads_aux1_sdo_pud_trim_d2a
```

7.122.1.5 pads_int1_pe_trim_d2a

```
uint8_t ipreg_bar_reg_61_t::pads_int1_pe_trim_d2a
```

7.122.1.6 pads_int1_pud_trim_d2a

```
uint8_t ipreg_bar_reg_61_t::pads_int1_pud_trim_d2a
```

7.122.1.7 resv_1

```
uint8_t ipreg_bar_reg_61_t::resv_1
```

7.122.1.8 resv_2

```
uint8_t ipreg_bar_reg_61_t::resv_2
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.123 ipreg_bar_reg_62_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t resv_1: 1
- uint8_t pads_int2_pe_trim_d2a: 1
- uint8_t pads_int2_pud_trim_d2a: 1
- uint8_t resv_2: 5

7.123.1 Member Data Documentation

7.123.1.1 pads_int2_pe_trim_d2a

```
uint8_t ipreg_bar_reg_62_t::pads_int2_pe_trim_d2a
```

7.123.1.2 pads_int2_pud_trim_d2a

```
uint8_t ipreg_bar_reg_62_t::pads_int2_pud_trim_d2a
```

7.123.1.3 resv_1

```
uint8_t ipreg_bar_reg_62_t::resv_1
```

7.123.1.4 resv_2

```
uint8_t ipreg_bar_reg_62_t::resv_2
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.124 ipreg_misc_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t resv_1: 1
- uint8_t edmp_idle: 1
- uint8_t resv_2: 6

7.124.1 Member Data Documentation

7.124.1.1 edmp_idle

```
uint8_t ipreg_misc_t::edmp_idle
```

7.124.1.2 resv_1

```
uint8_t ipreg_misc_t::resv_1
```

7.124.1.3 resv_2

```
uint8_t ipreg_misc_t::resv_2
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.125 ipreg_sys1_reg_166_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t resv_1: 3
- uint8_t gyro_afsr_mode: 2
- uint8_t gyro_src_ctrl: 2
- uint8_t resv_2: 1

7.125.1 Member Data Documentation

7.125.1.1 gyro_afsr_mode

```
uint8_t ipreg_sys1_reg_166_t::gyro_afsr_mode
```

7.125.1.2 gyro_src_ctrl

```
uint8_t ipreg_sys1_reg_166_t::gyro_src_ctrl
```

7.125.1.3 resv_1

```
uint8_t ipreg_sys1_reg_166_t::resv_1
```

7.125.1.4 resv_2

```
uint8_t ipreg_sys1_reg_166_t::resv_2
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.126 ipreg_sys1_reg_168_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t gyro_afsr_shared: 1
- uint8_t gyro_ois_m6_byp: 1
- uint8_t resv_1: 6

7.126.1 Member Data Documentation

7.126.1.1 gyro_afsr_shared

```
uint8_t ipreg_sys1_reg_168_t::gyro_afsr_shared
```

7.126.1.2 gyro_ois_m6_byp

```
uint8_t ipreg_sys1_reg_168_t::gyro_ois_m6_byp
```

7.126.1.3 resv_1

```
uint8_t ipreg_sys1_reg_168_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.127 ipreg_sys1_reg_170_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t resv_1: 1
- uint8_t gyro_lp_avg_sel: 4
- uint8_t gyro_ois_hpfbw_sel: 3

7.127.1 Member Data Documentation

7.127.1.1 gyro_lp_avg_sel

```
uint8_t ipreg_sys1_reg_170_t::gyro_lp_avg_sel
```

7.127.1.2 gyro_ois_hpfbw_sel

```
uint8_t ipreg_sys1_reg_170_t::gyro_ois_hpfbw_sel
```

7.127.1.3 resv_1

```
uint8_t ipreg_sys1_reg_170_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.128 ipreg_sys1_reg_171_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t gyro_ois_lpf1bw_sel: 3
- uint8_t gyro_ois_lpf2bw_sel: 3
- uint8_t resv_1: 2

7.128.1 Member Data Documentation

7.128.1.1 gyro_ois_lpf1bw_sel

`uint8_t ipreg_sys1_reg_171_t::gyro_ois_lpf1bw_sel`

7.128.1.2 gyro_ois_lpf2bw_sel

`uint8_t ipreg_sys1_reg_171_t::gyro_ois_lpf2bw_sel`

7.128.1.3 resv_1

`uint8_t ipreg_sys1_reg_171_t::resv_1`

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.129 ipreg_sys1_reg_172_t Struct Reference

`#include <inv_imu_regmap_le.h>`

Public Attributes

- uint8_t gyro_ui_lpfbw_sel: 3
- uint8_t resv_1: 4
- uint8_t gyro_ois_hpf1_byp: 1

7.129.1 Member Data Documentation

7.129.1.1 gyro_ois_hpf1_byp

```
uint8_t ipreg_sys1_reg_172_t::gyro_ois_hpf1_byp
```

7.129.1.2 gyro_ui_lpfbw_sel

```
uint8_t ipreg_sys1_reg_172_t::gyro_ui_lpfbw_sel
```

7.129.1.3 resv_1

```
uint8_t ipreg_sys1_reg_172_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.130 ipreg_sys1_reg_173_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t gyro_ois_hpf2_byp: 1
- uint8_t resv_1: 7

7.130.1 Member Data Documentation

7.130.1.1 gyro_ois_hpf2_byp

```
uint8_t ipreg_sys1_reg_173_t::gyro_ois_hpf2_byp
```

7.130.1.2 resv_1

```
uint8_t ipreg_sys1_reg_173_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.131 ipreg_sys2_reg_123_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t accel_src_ctrl: 2
- uint8_t resv_1: 6

7.131.1 Member Data Documentation

7.131.1.1 accel_src_ctrl

```
uint8_t ipreg_sys2_reg_123_t::accel_src_ctrl
```

7.131.1.2 resv_1

```
uint8_t ipreg_sys2_reg_123_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.132 ipreg_sys2_reg_129_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t accel_lp_avg_sel: 4
- uint8_t accel_ois_hpfbw_sel: 3
- uint8_t resv_1: 1

7.132.1 Member Data Documentation

7.132.1.1 accel_lp_avg_sel

```
uint8_t ipreg_sys2_reg_129_t::accel_lp_avg_sel
```

7.132.1.2 accel_ois_hpfbw_sel

```
uint8_t ipreg_sys2_reg_129_t::accel_ois_hpfbw_sel
```

7.132.1.3 resv_1

```
uint8_t ipreg_sys2_reg_129_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.133 ipreg_sys2_reg_130_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t accel_ois_lpf1bw_sel: 3
- uint8_t accel_ois_lpf2bw_sel: 3
- uint8_t resv_1: 2

7.133.1 Member Data Documentation

7.133.1.1 accel_ois_lpf1bw_sel

```
uint8_t ipreg_sys2_reg_130_t::accel_ois_lpf1bw_sel
```

7.133.1.2 accel_ois_lpf2bw_sel

```
uint8_t ipreg_sys2_reg_130_t::accel_ois_lpf2bw_sel
```

7.133.1.3 resv_1

```
uint8_t ipreg_sys2_reg_130_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.134 ipreg_sys2_reg_131_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t accel_ui_lpfbw_sel: 3
- uint8_t resv_1: 5

7.134.1 Member Data Documentation

7.134.1.1 accel_ui_lpfbw_sel

```
uint8_t ipreg_sys2_reg_131_t::accel_ui_lpfbw_sel
```

7.134.1.2 resv_1

```
uint8_t ipreg_sys2_reg_131_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.135 ipreg_sys2_reg_132_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t accel_ois_hpf1_byp: 1
- uint8_t accel_ois_hpf2_byp: 1
- uint8_t accel_ois_m6_byp: 1
- uint8_t resv_1: 5

7.135.1 Member Data Documentation

7.135.1.1 accel_ois_hpf1_byp

```
uint8_t ipreg_sys2_reg_132_t::accel_ois_hpf1_byp
```

7.135.1.2 accel_ois_hpf2_byp

```
uint8_t ipreg_sys2_reg_132_t::accel_ois_hpf2_byp
```

7.135.1.3 accel_ois_m6_byp

```
uint8_t ipreg_sys2_reg_132_t::accel_ois_m6_byp
```

7.135.1.4 resv_1

```
uint8_t ipreg_sys2_reg_132_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.136 ireg_addr_15_8_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t ireg_addr_15_8: 8

7.136.1 Member Data Documentation

7.136.1.1 ireg_addr_15_8

```
uint8_t ireg_addr_15_8_t::ireg_addr_15_8
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.137 ireg_addr_7_0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t ireg_addr_7_0: 8

7.137.1 Member Data Documentation

7.137.1.1 ireg_addr_7_0

```
uint8_t ireg_addr_7_0_t::ireg_addr_7_0
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.138 ireg_data_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t ireg_data: 8

7.138.1 Member Data Documentation

7.138.1.1 ireg_data

```
uint8_t ireg_data_t::ireg_data
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.139 isr_0_7_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_status_accel_drdy_pin_0: 1
- uint8_t resv_1: 2
- uint8_t int_status_ext_odr_drdy_pin_0: 1
- uint8_t resv_2: 1
- uint8_t int_status_on_demand_pin_0: 1
- uint8_t resv_3: 2

7.139.1 Member Data Documentation

7.139.1.1 int_status_accel_drdy_pin_0

```
uint8_t isr_0_7_t::int_status_accel_drdy_pin_0
```

7.139.1.2 int_status_ext_odr_drdy_pin_0

```
uint8_t isr_0_7_t::int_status_ext_odr_drdy_pin_0
```

7.139.1.3 int_status_on_demand_pin_0

```
uint8_t isr_0_7_t::int_status_on_demand_pin_0
```

7.139.1.4 resv_1

```
uint8_t isr_0_7_t::resv_1
```

7.139.1.5 resv_2

```
uint8_t isr_0_7_t::resv_2
```

7.139.1.6 resv_3

```
uint8_t isr_0_7_t::resv_3
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.140 isr_16_23_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_status_accel_drdy_pin_2: 1
- uint8_t resv_1: 2
- uint8_t int_status_ext_odr_drdy_pin_2: 1
- uint8_t resv_2: 1
- uint8_t int_status_on_demand_pin_2: 1
- uint8_t resv_3: 2

7.140.1 Member Data Documentation

7.140.1.1 int_status_accel_drdy_pin_2

```
uint8_t isr_16_23_t::int_status_accel_drdy_pin_2
```

7.140.1.2 int_status_ext_odr_drdy_pin_2

```
uint8_t isr_16_23_t::int_status_ext_odr_drdy_pin_2
```

7.140.1.3 int_status_on_demand_pin_2

```
uint8_t isr_16_23_t::int_status_on_demand_pin_2
```

7.140.1.4 resv_1

```
uint8_t isr_16_23_t::resv_1
```

7.140.1.5 resv_2

```
uint8_t isr_16_23_t::resv_2
```

7.140.1.6 resv_3

```
uint8_t isr_16_23_t::resv_3
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.141 isr_8_15_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_status_accel_drdy_pin_1: 1
- uint8_t resv_1: 2
- uint8_t int_status_ext_odr_drdy_pin_1: 1
- uint8_t resv_2: 1
- uint8_t int_status_on_demand_pin_1: 1
- uint8_t resv_3: 2

7.141.1 Member Data Documentation

7.141.1.1 int_status_accel_drdy_pin_1

```
uint8_t isr_8_15_t::int_status_accel_drdy_pin_1
```

7.141.1.2 int_status_ext_odr_drdy_pin_1

```
uint8_t isr_8_15_t::int_status_ext_odr_drdy_pin_1
```

7.141.1.3 int_status_on_demand_pin_1

```
uint8_t isr_8_15_t::int_status_on_demand_pin_1
```

7.141.1.4 resv_1

```
uint8_t isr_8_15_t::resv_1
```

7.141.1.5 resv_2

```
uint8_t isr_8_15_t::resv_2
```

7.141.1.6 resv_3

```
uint8_t isr_8_15_t::resv_3
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.142 odr_decimate_config_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t accel_fifo_odr_dec: 4
- uint8_t gyro_fifo_odr_dec: 4

7.142.1 Member Data Documentation

7.142.1.1 accel_fifo_odr_dec

```
uint8_t odr_decimate_config_t::accel_fifo_odr_dec
```

7.142.1.2 gyro_fifo_odr_dec

```
uint8_t odr_decimate_config_t::gyro_fifo_odr_dec
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.143 pwr_mgmt0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t accel_mode: 2
- uint8_t gyro_mode: 2
- uint8_t resv_1: 4

7.143.1 Member Data Documentation

7.143.1.1 accel_mode

```
uint8_t pwr_mgmt0_t::accel_mode
```

7.143.1.2 gyro_mode

```
uint8_t pwr_mgmt0_t::gyro_mode
```

7.143.1.3 resv_1

```
uint8_t pwr_mgmt0_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.144 pwr_mgmt_aux1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t accel_aux1_en: 1
- uint8_t gyro_aux1_en: 1
- uint8_t resv_1: 6

7.144.1 Member Data Documentation

7.144.1.1 accel_aux1_en

```
uint8_t pwr_mgmt_aux1_t::accel_aux1_en
```

7.144.1.2 gyro_aux1_en

```
uint8_t pwr_mgmt_aux1_t::gyro_aux1_en
```

7.144.1.3 resv_1

```
uint8_t pwr_mgmt_aux1_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.145 pwr_mgmt_aux2_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t accel_aux2_en: 1
- uint8_t gyro_aux2_en: 1
- uint8_t resv_1: 6

7.145.1 Member Data Documentation

7.145.1.1 accel_aux2_en

```
uint8_t pwr_mgmt_aux2_t::accel_aux2_en
```

7.145.1.2 gyro_aux2_en

```
uint8_t pwr_mgmt_aux2_t::gyro_aux2_en
```

7.145.1.3 resv_1

```
uint8_t pwr_mgmt_aux2_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.146 reg_host_msg_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t testopenable: 1
- uint8_t resv_1: 4
- uint8_t edmp_on_demand_en: 1
- uint8_t resv_2: 2

7.146.1 Member Data Documentation

7.146.1.1 edmp_on_demand_en

```
uint8_t reg_host_msg_t::edmp_on_demand_en
```

7.146.1.2 resv_1

```
uint8_t reg_host_msg_t::resv_1
```

7.146.1.3 resv_2

```
uint8_t reg_host_msg_t::resv_2
```

7.146.1.4 testopenable

```
uint8_t reg_host_msg_t::testopenable
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.147 reg_misc1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t osc_id_ovrd: 4
- uint8_t resv_1: 4

7.147.1 Member Data Documentation

7.147.1.1 osc_id_ovrd

```
uint8_t reg_misc1_t::osc_id_ovrd
```

7.147.1.2 resv_1

```
uint8_t reg_misc1_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.148 reg_misc2_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t ireg_done: 1
- uint8_t soft_rst: 1
- uint8_t resv_1: 6

7.148.1 Member Data Documentation

7.148.1.1 ireg_done

```
uint8_t reg_misc2_t::ireg_done
```

7.148.1.2 resv_1

```
uint8_t reg_misc2_t::resv_1
```

7.148.1.3 soft_rst

```
uint8_t reg_misc2_t::soft_rst
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.149 rtc_config_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t resv_1: 5
- uint8_t rtc_mode: 1
- uint8_t rtc_align: 1
- uint8_t resv_2: 1

7.149.1 Member Data Documentation

7.149.1.1 resv_1

```
uint8_t rtc_config_t::resv_1
```

7.149.1.2 resv_2

```
uint8_t rtc_config_t::resv_2
```

7.149.1.3 rtc_align

```
uint8_t rtc_config_t::rtc_align
```

7.149.1.4 rtc_mode

```
uint8_t rtc_config_t::rtc_mode
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.150 selftest_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t en_ax_st: 1
- uint8_t en_ay_st: 1
- uint8_t en_az_st: 1
- uint8_t en_gx_st: 1
- uint8_t en_gy_st: 1
- uint8_t en_gz_st: 1
- uint8_t resv_1: 2

7.150.1 Member Data Documentation

7.150.1.1 en_ax_st

```
uint8_t selftest_t::en_ax_st
```

7.150.1.2 en_ay_st

```
uint8_t selftest_t::en_ay_st
```

7.150.1.3 en_az_st

```
uint8_t selftest_t::en_az_st
```

7.150.1.4 en_gx_st

```
uint8_t selftest_t::en_gx_st
```

7.150.1.5 en_gy_st

```
uint8_t selftest_t::en_gy_st
```

7.150.1.6 en_gz_st

```
uint8_t selftest_t::en_gz_st
```

7.150.1.7 resv_1

```
uint8_t selftest_t::resv_1
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.151 sifs_i3c_stc_cfg_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t resv_1: 2
- uint8_t i3c_stc_mode: 1
- uint8_t resv_2: 5

7.151.1 Member Data Documentation

7.151.1.1 i3c_stc_mode

```
uint8_t sifs_i3c_stc_cfg_t::i3c_stc_mode
```

7.151.1.2 resv_1

```
uint8_t sifs_i3c_stc_cfg_t::resv_1
```

7.151.1.3 resv_2

```
uint8_t sifs_i3c_stc_cfg_t::resv_2
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.152 sifs_ixc_error_status_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t sifs_ixc_timeout_err: 1
- uint8_t aux1_sifs_ixc_timeout_err: 1
- uint8_t resv_1: 6

7.152.1 Member Data Documentation

7.152.1.1 aux1_sifs_ixc_timeout_err

```
uint8_t sifs_ixc_error_status_t::aux1_sifs_ixc_timeout_err
```

7.152.1.2 resv_1

```
uint8_t sifs_ixc_error_status_t::resv_1
```

7.152.1.3 sifs_ixc_timeout_err

```
uint8_t sifs_ixc_error_status_t::sifs_ixc_timeout_err
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.153 smc_control_0_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t tmst_en: 1
- uint8_t tmst_fsync_en: 1
- uint8_t tmst_force_aux_fine_en: 1
- uint8_t temp_dis: 1
- uint8_t accel_lp_clk_sel: 1
- uint8_t resv_1: 3

7.153.1 Member Data Documentation

7.153.1.1 accel_lp_clk_sel

```
uint8_t smc_control_0_t::accel_lp_clk_sel
```

7.153.1.2 resv_1

```
uint8_t smc_control_0_t::resv_1
```

7.153.1.3 temp_dis

```
uint8_t smc_control_0_t::temp_dis
```

7.153.1.4 tmst_en

```
uint8_t smc_control_0_t::tmst_en
```

7.153.1.5 tmst_force_aux_fine_en

```
uint8_t smc_control_0_t::tmst_force_aux_fine_en
```

7.153.1.6 tmst_fsync_en

```
uint8_t smc_control_0_t::tmst_fsync_en
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.154 smc_control_1_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t resv_1: 3
- uint8_t sreg_aux_accel_only_en: 1
- uint8_t resv_2: 4

7.154.1 Member Data Documentation

7.154.1.1 resv_1

```
uint8_t smc_control_1_t::resv_1
```

7.154.1.2 resv_2

```
uint8_t smc_control_1_t::resv_2
```

7.154.1.3 sreg_aux_accel_only_en

```
uint8_t smc_control_1_t::sreg_aux_accel_only_en
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.155 sreg_ctrl_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t resv_1: 1
- uint8_t sreg_data_endian_sel: 1
- uint8_t resv_2: 6

7.155.1 Member Data Documentation

7.155.1.1 resv_1

```
uint8_t sreg_ctrl_t::resv_1
```

7.155.1.2 resv_2

```
uint8_t sreg_ctrl_t::resv_2
```

7.155.1.3 sreg_data_endian_sel

```
uint8_t sreg_ctrl_t::sreg_data_endian_sel
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.156 status_mask_pin_0_7_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_accel_drdy_pin_0_dis: 1
- uint8_t resv_1: 2
- uint8_t int_ext_odr_drdy_pin_0_dis: 1
- uint8_t resv_2: 1
- uint8_t int_on_demand_pin_0_dis: 1
- uint8_t resv_3: 2

7.156.1 Member Data Documentation

7.156.1.1 int_accel_drdy_pin_0_dis

```
uint8_t status_mask_pin_0_7_t::int_accel_drdy_pin_0_dis
```

7.156.1.2 int_ext_odr_drdy_pin_0_dis

```
uint8_t status_mask_pin_0_7_t::int_ext_odr_drdy_pin_0_dis
```

7.156.1.3 int_on_demand_pin_0_dis

```
uint8_t status_mask_pin_0_7_t::int_on_demand_pin_0_dis
```

7.156.1.4 resv_1

```
uint8_t status_mask_pin_0_7_t::resv_1
```

7.156.1.5 resv_2

```
uint8_t status_mask_pin_0_7_t::resv_2
```

7.156.1.6 resv_3

```
uint8_t status_mask_pin_0_7_t::resv_3
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.157 status_mask_pin_16_23_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_accel_drdy_pin_2_dis: 1
- uint8_t resv_1: 2
- uint8_t int_ext_odr_drdy_pin_2_dis: 1
- uint8_t resv_2: 1
- uint8_t int_on_demand_pin_2_dis: 1
- uint8_t resv_3: 2

7.157.1 Member Data Documentation

7.157.1.1 int_accel_drdy_pin_2_dis

```
uint8_t status_mask_pin_16_23_t::int_accel_drdy_pin_2_dis
```

7.157.1.2 int_ext_odr_drdy_pin_2_dis

```
uint8_t status_mask_pin_16_23_t::int_ext_odr_drdy_pin_2_dis
```

7.157.1.3 int_on_demand_pin_2_dis

```
uint8_t status_mask_pin_16_23_t::int_on_demand_pin_2_dis
```

7.157.1.4 resv_1

```
uint8_t status_mask_pin_16_23_t::resv_1
```

7.157.1.5 resv_2

```
uint8_t status_mask_pin_16_23_t::resv_2
```

7.157.1.6 resv_3

```
uint8_t status_mask_pin_16_23_t::resv_3
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.158 status_mask_pin_8_15_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t int_accel_drdy_pin_1_dis: 1
- uint8_t resv_1: 2
- uint8_t int_ext_odr_drdy_pin_1_dis: 1
- uint8_t resv_2: 1
- uint8_t int_on_demand_pin_1_dis: 1
- uint8_t resv_3: 2

7.158.1 Member Data Documentation

7.158.1.1 int_accel_drdy_pin_1_dis

```
uint8_t status_mask_pin_8_15_t::int_accel_drdy_pin_1_dis
```

7.158.1.2 int_ext_odr_drdy_pin_1_dis

```
uint8_t status_mask_pin_8_15_t::int_ext_odr_drdy_pin_1_dis
```

7.158.1.3 int_on_demand_pin_1_dis

```
uint8_t status_mask_pin_8_15_t::int_on_demand_pin_1_dis
```

7.158.1.4 resv_1

```
uint8_t status_mask_pin_8_15_t::resv_1
```

7.158.1.5 resv_2

```
uint8_t status_mask_pin_8_15_t::resv_2
```

7.158.1.6 resv_3

```
uint8_t status_mask_pin_8_15_t::resv_3
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.159 stc_config_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t resv_1: 2
- uint8_t stc_sensor_sel: 2
- uint8_t resv_2: 4

7.159.1 Member Data Documentation

7.159.1.1 resv_1

```
uint8_t stc_config_t::resv_1
```

7.159.1.2 resv_2

```
uint8_t stc_config_t::resv_2
```

7.159.1.3 stc_sensor_sel

```
uint8_t stc_config_t::stc_sensor_sel
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.160 sw_pll1_trim_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t sw_pll1_trim: 8

7.160.1 Member Data Documentation

7.160.1.1 sw_pll1_trim

```
uint8_t sw_pll1_trim_t::sw_pll1_trim
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.161 tmst_wom_config_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t wom_int_dur: 2
- uint8_t wom_int_mode: 1
- uint8_t wom_mode: 1
- uint8_t wom_en: 1
- uint8_t tmst_resol: 1
- uint8_t tmst_delta_en: 1
- uint8_t resv_1: 1

7.161.1 Member Data Documentation

7.161.1.1 resv_1

```
uint8_t tmst_wom_config_t::resv_1
```

7.161.1.2 tmst_delta_en

```
uint8_t tmst_wom_config_t::tmst_delta_en
```

7.161.1.3 tmst_resol

```
uint8_t tmst_wom_config_t::tmst_resol
```

7.161.1.4 wom_en

```
uint8_t tmst_wom_config_t::wom_en
```

7.161.1.5 wom_int_dur

```
uint8_t tmst_wom_config_t::wom_int_dur
```

7.161.1.6 wom_int_mode

```
uint8_t tmst_wom_config_t::wom_int_mode
```

7.161.1.7 wom_mode

```
uint8_t tmst_wom_config_t::wom_mode
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

7.162 who_am_i_t Struct Reference

```
#include <inv_imu_regmap_le.h>
```

Public Attributes

- uint8_t who_am_i: 8

7.162.1 Member Data Documentation

7.162.1.1 who_am_i

```
uint8_t who_am_i_t::who_am_i
```

The documentation for this struct was generated from the following file:

- inv_imu_regmap_le.h

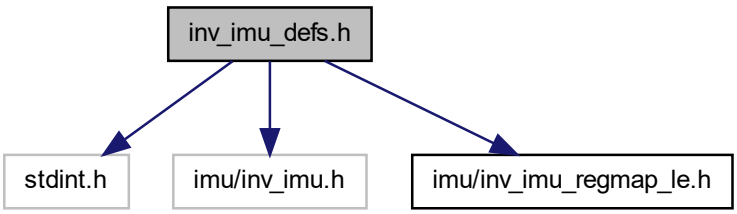
Chapter 8

File Documentation

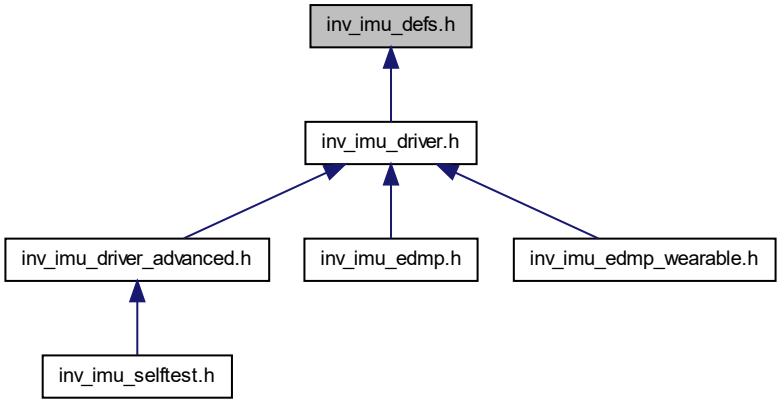
8.1 inv_imu_defs.h File Reference

```
#include <stdint.h>
#include "imu/inv_imu.h"
#include "imu/inv_imu_regmap_le.h"
```

Include dependency graph for inv_imu_defs.h:



This graph shows which files directly or indirectly include this file:



Classes

- struct inv_imu_sensor_data_t

  Sensor data from registers.
- union fifo_header_t

  Describe the content of the FIFO header.
- union fifo_comp_header_t

  Describe the content of the FIFO header for compressed packets.
- union fifo_header2_t

  Describe the content of the second FIFO header.
- union fifo_comp_decode_t

  Describe the content of the FIFO Compression Decoding Tag.
- struct fifo_configx_t

  Required registers to configure FIFO.
- struct intx_configx_t

  Required registers to configure interrupts.
- struct intx_statusx_t

  Registers to retrieve interrupts status.
- struct inv_imu_int_pin_config_t

  Interrupts pin configuration.

Macros

- #define INV_IMU_OK 0

  Success.
- #define INV_IMU_ERROR -1

  Unspecified error.
- #define INV_IMU_ERROR_TRANSPORT -3

  Error occurred at transport level.
- #define INV_IMU_ERROR_TIMEOUT -4

Action did not complete in the expected time window.

- #define INV_IMU_ERROR_BAD_ARG -11

  Invalid argument provided.

- #define INV_IMU_ERROR_EDMP_ODR -126

  EDMP ODR decimator reconfiguration is needed.

- #define INV_IMU_ERROR_EDMP_BUF_EMPTY -127

  EDMP buffer is empty.

- #define INV_IMU_DISABLE (0U)
- #define INV_IMU_ENABLE (1U)
- #define ACC_STARTUP_TIME_US 10000
- #define GYR_STARTUP_TIME_US 70000
- #define ACCEL_DATA_SIZE 6
- #define GYRO_DATA_SIZE 6
- #define TEMP_DATA_SIZE 2
- #define FIFO_HEADER_SIZE 1
- #define FIFO_TEMP_DATA_SIZE 1
- #define FIFO_TS_FSYNC_SIZE 2
- #define FIFO_TEMP_HIGH_RES_SIZE 1
- #define FIFO_ACCEL_GYRO_HIGH_RES_SIZE 3
- #define FIFO_ES0_6B_DATA_SIZE 6
- #define FIFO_ES0_9B_DATA_SIZE 9
- #define FIFO_ES1_DATA_SIZE 6
- #define INVALID_VALUE_FIFO ((int16_t)0x8000)
- #define INVALID_VALUE_FIFO_1B ((int8_t)0x80)
- #define OUT_OF_BOUND_TEMP_NEG_FIFO_1B ((int8_t)0x81)
- #define OUT_OF_BOUND_TEMP_POS_FIFO_1B ((int8_t)0x7F)
- #define FIFO_COMP_X2_COMPRESSION 0
- #define FIFO_COMP_X3_COMPRESSION 1
- #define FIFO_COMP_X4_COMPRESSION 2
- #define FIFO_COMP_1_SAMPLE_IN_FRAME 0
- #define FIFO_COMP_2_SAMPLES_IN_FRAME 1
- #define FIFO_COMP_3_SAMPLES_IN_FRAME 2
- #define FIFO_COMP_4_SAMPLES_IN_FRAME 3
- #define INT5_TO_INT8(in) (((in) < 16) ? ((int8_t)(in)) : ((int8_t)(in)-32))

  Converts an integer from a 5-bits signed to a 8-bits signed.

- #define INT4_TO_INT8(in) (((in) < 8) ? ((int8_t)(in)) : ((int8_t)(in)-16))

  Converts an integer from a 4-bits signed to a 8-bits signed.

- #define EDMP_INT_SRC_ACCEL_DRDY_MASK 0x01
- #define EDMP_INT_SRC_GYRO_DRDY_MASK 0x02
- #define EDMP_INT_SRC_EXT_INT_DRDY_MASK 0x04
- #define EDMP_INT_SRC_EXT_ODR_DRDY_MASK 0x08
- #define EDMP_INT_SRC_WOM_DRDY_MASK 0x10
- #define EDMP_INT_SRC_ON_DEMAND_MASK 0x20
- #define TAP_TMAX_400HZ 198
- #define TAP_TMAX_800HZ 396
- #define TAP_TMIN_400HZ 66
- #define TAP_TMIN_800HZ 132
- #define TAP_SMUDGE_REJECT_THR_400HZ 34
- #define TAP_SMUDGE_REJECT_THR_800HZ 68
- #define STC_RESULTS_ACCEL_X_MASK 0x0001
- #define STC_RESULTS_ACCEL_Y_MASK 0x0002
- #define STC_RESULTS_ACCEL_Z_MASK 0x0004
- #define STC_RESULTS_GYRO_X_MASK 0x0008
- #define STC_RESULTS_GYRO_Y_MASK 0x0010

- #define STC_RESULTS_GYRO_Z_MASK 0x0020
- #define STC_RESULTS_ST_STATUS_MASK 0x00C0
- #define STC_RESULTS_ACCEL_SC_MASK 0x0300
- #define STC_RESULTS_GYRO_SC_MASK 0x0C00
- #define SELFTESTCAL_INIT_EN_MASK 0x0001
- #define SELFTESTCAL_INIT_EN 0x0001
- #define SELFTESTCAL_INIT_DIS 0x0000
- #define SELFTEST_ACCEL_EN_MASK 0x0002
- #define SELFTEST_ACCEL_EN 0x0002
- #define SELFTEST_ACCEL_DIS 0x0000
- #define SELFTEST_GYRO_EN_MASK 0x0004
- #define SELFTEST_GYRO_EN 0x0004
- #define SELFTEST_GYRO_DIS 0x0000
- #define SELFTEST_AVERAGE_TIME_MASK 0x0380
- #define SELFTEST_ACCEL_THRESH_MASK 0x1C00
- #define SELFTEST_GYRO_THRESH_MASK 0xE000

Enumerations

- enum inv_imu_int_num_t { INV_IMU_INT1 , INV_IMU_INT2 }

  Interrupt number.
- enum pwr_mgmt0_gyro_mode_t { PWR_MGMT0_GYRO_MODE_LN = 0x03 , PWR_MGMT0_GYRO_MODE_LP = 0x02 , PWR_MGMT0_GYRO_MODE_STANDBY = 0x01 , PWR_MGMT0_GYRO_MODE_OFF = 0x00 }
- enum pwr_mgmt0_accel_mode_t { PWR_MGMT0_ACCEL_MODE_LN = 0x03 , PWR_MGMT0_ACCEL_MODE_LP = 0x02 , PWR_MGMT0_ACCEL_MODE_OFF = 0x00 }
- enum intx_config2_intx_drive_t { INTX_CONFIG2_INTX_DRIVE_PP = 0x00 , INTX_CONFIG2_INTX_DRIVE_OD = 0x01 }
- enum intx_config2_intx_mode_t { INTX_CONFIG2_INTX_MODE_PULSE = 0x00 , INTX_CONFIG2_INTX_MODE_LATCH = 0x01 }
- enum intx_config2_intx_polarity_t { INTX_CONFIG2_INTX_POLARITY_LOW = 0x00 , INTX_CONFIG2_INTX_POLARITY_HIG = 0x01 }
- enum accel_config0_accel_ui_fs_sel_t { ACCEL_CONFIG0_ACCEL_UI_FS_SEL_2_G = 0x4 , ACCEL_CONFIG0_ACCEL_UI = 0x3 , ACCEL_CONFIG0_ACCEL_UI_FS_SEL_8_G = 0x2 , ACCEL_CONFIG0_ACCEL_UI_FS_SEL_16_G = 0x1 }
- enum accel_config0_accel_odr_t { ACCEL_CONFIG0_ACCEL_ODR_1_5625_HZ = 0xF , ACCEL_CONFIG0_ACCEL_ODR_3_125_HZ = 0xE , ACCEL_CONFIG0_ACCEL_ODR_6_25_HZ = 0xD , ACCEL_CONFIG0_ACCEL_ODR_12_5_HZ = 0xC , ACCEL_CONFIG0_ACCEL_ODR_25_HZ = 0xB , ACCEL_CONFIG0_ACCEL_ODR_50_HZ = 0xA , ACCEL_CONFIG0_ACCEL_ODR_100_HZ = 0x9 , ACCEL_CONFIG0_ACCEL_ODR_200_HZ = 0x8 , ACCEL_CONFIG0_ACCEL_ODR_400_HZ = 0x7 , ACCEL_CONFIG0_ACCEL_ODR_800_HZ = 0x6 , ACCEL_CONFIG0_ACCEL_ODR_1600_HZ = 0x5 , ACCEL_CONFIG0_ACCEL_ODR_3200_HZ = 0x4 , ACCEL_CONFIG0_ACCEL_ODR_6400_HZ = 0x3 }
- enum gyro_config0_gyro_ui_fs_sel_t { GYRO_CONFIG0_GYRO_UI_FS_SEL_15_625_DPS = 8 , GYRO_CONFIG0_GYRO_UI_FS_SEL_31_25_DPS = 7 , GYRO_CONFIG0_GYRO_UI_FS_SEL_62_5_DPS = 6 , GYRO_CONFIG0_GYRO_UI_FS_SEL_125_DPS = 5 , GYRO_CONFIG0_GYRO_UI_FS_SEL_250_DPS = 4 , GYRO_CONFIG0_GYRO_UI_FS_SEL_500_DPS = 3 , GYRO_CONFIG0_GYRO_UI_FS_SEL_1000_DPS = 2 , GYRO_CONFIG0_GYRO_UI_FS_SEL_2000_DPS = 1 }
- enum gyro_config0_gyro_odr_t { GYRO_CONFIG0_GYRO_ODR_1_5625_HZ = 0xF , GYRO_CONFIG0_GYRO_ODR_3_125_HZ = 0xE , GYRO_CONFIG0_GYRO_ODR_6_25_HZ = 0xD , GYRO_CONFIG0_GYRO_ODR_12_5_HZ = 0xC , GYRO_CONFIG0_GYRO_ODR_25_HZ = 0xB , GYRO_CONFIG0_GYRO_ODR_50_HZ = 0xA , GYRO_CONFIG0_GYRO_ODR_100_HZ = 0x9 , GYRO_CONFIG0_GYRO_ODR_200_HZ = 0x8 , GYRO_CONFIG0_GYRO_ODR_400_HZ = 0x7 , GYRO_CONFIG0_GYRO_ODR_800_HZ = 0x6 , GYRO_CONFIG0_GYRO_ODR_1600_HZ = 0x5 , GYRO_CONFIG0_GYRO_ODR_3200_HZ = 0x4 , GYRO_CONFIG0_GYRO_ODR_6400_HZ = 0x3 }

- enum fifo_config0_fifo_mode_t { FIFO_CONFIG0_FIFO_MODE_SNAPSHOT = 0x02 , FIFO_CONFIG0_FIFO_MODE_STREAM = 0x01 , FIFO_CONFIG0_FIFO_MODE_BYPASS = 0x00 }
- enum fifo_config0_fifo_depth_t { FIFO_CONFIG0_FIFO_DEPTH_MAX = 0x1E , FIFO_CONFIG0_FIFO_DEPTH_APEX = 0x07 , FIFO_CONFIG0_FIFO_DEPTH_GAF = 0x04 }
- enum fifo_config2_fifo_wr_wm_gt_th_t { FIFO_CONFIG2_FIFO_WR_WM_EQ_OR_GT_TH = 0x1 , FIFO_CONFIG2_FIFO_WR_WM_EQ_TH = 0x0 }
- enum fifo_config4_fifo_comp_nc_flow_cfg_t { FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_EVERY_128_FR = 0x5 , FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_E = 0x4 , FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_EVERY_32_FR = 0x3 , FIFO_CONFIG4_FIFO_COMP_NC_FLOW_C = 0x2 , FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_EVERY_8_FR = 0x1 , FIFO_CONFIG4_FIFO_COMP_NC_FLOW_CFG_DIS = 0x0 }
- enum fifo_config4_fifo_es0_6b_9b_t { FIFO_CONFIG4_FIFO_ES0_9B = 0x1 , FIFO_CONFIG4_FIFO_ES0_6B = 0x0 }
- enum tmst_wom_config_tmst_resol_t { TMST_WOM_CONFIG_TMST_RESOL_16_US = 0x01 , TMST_WOM_CONFIG_TMST = 0x00 }
- enum tmst_wom_config_wom_mode_t { TMST_WOM_CONFIG_WOM_MODE_CMP_PREV = 0x01 , TMST_WOM_CONFIG_WOM_MODE_CMP_INIT = 0x00 }
- enum tmst_wom_config_wom_int_mode_t { TMST_WOM_CONFIG_WOM_INT_MODE_ANDED = 0x01 , TMST_WOM_CONFIG_WOM_INT_MODE_ORED = 0x00 }
- enum tmst_wom_config_wom_int_dur_t { TMST_WOM_CONFIG_WOM_INT_DUR_1_SMPL = 0x00 , TMST_WOM_CONFIG_WOM_INT_DUR_2_SMPL = 0x01 , TMST_WOM_CONFIG_WOM_INT_DUR_3_SMPL = 0x02 , TMST_WOM_CONFIG_WOM_INT_DUR_4_SMPL = 0x03 }
- enum fsync_config0_ap_fsync_sel_t { FSYNC_CONFIG0_AP_FSYNC_NO = 0x0 , FSYNC_CONFIG0_AP_FSYNC_TEMP = 0x1 , FSYNC_CONFIG0_AP_FSYNC_G = 0x2 , FSYNC_CONFIG0_AP_FSYNC_GYRO_Y = 0x3 , FSYNC_CONFIG0_AP_FSYNC_GYRO_Z = 0x4 , FSYNC_CONFIG0_AP_FSYNC_ACCEL_X = 0x5 , FSYNC_CONFIG0_AP_FSYNC_ACCEL_Y = 0x6 , FSYNC_CONFIG0_AP_FSYNC_ACCEL_Z = 0x7 }
- enum dmp_ext_sen_odr_cfg_ext_odr_t { DMP_EXT_SEN_ODR_CFG_EXT_ODR_3_25_HZ = 0x00 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_6_25_HZ = 0x01 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_12_5_HZ = 0x02 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_25_HZ = 0x03 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_50_HZ = 0x04 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_100_HZ = 0x05 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_200_HZ = 0x06 , DMP_EXT_SEN_ODR_CFG_EXT_ODR_400_HZ = 0x07 }
- enum dmp_ext_sen_odr_cfg_apex_odr_t { DMP_EXT_SEN_ODR_CFG_APEX_ODR_25_HZ = 0x00 , DMP_EXT_SEN_ODR_CFG_APEX_ODR_50_HZ = 0x01 , DMP_EXT_SEN_ODR_CFG_APEX_ODR_100_HZ = 0x02 , DMP_EXT_SEN_ODR_CFG_APEX_ODR_200_HZ = 0x03 , DMP_EXT_SEN_ODR_CFG_APEX_ODR_400_HZ = 0x04 , DMP_EXT_SEN_ODR_CFG_APEX_ODR_800_HZ = 0x05 }
- enum odr_decimate_config_gyro_fifo_odr_dec_t { ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_1 = 0x0 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_2 = 0x1 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_4 = 0x2 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC = 0x3 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_16 = 0x4 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_32 = 0x5 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_64 = 0x6 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC = 0x7 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_256 = 0x8 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_512 = 0x9 , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_1024 = 0xA , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_D = 0xB , ODR_DECIMATE_CONFIG_GYRO_FIFO_ODR_DEC_4096 = 0xC }
- enum odr_decimate_config_accel_fifo_odr_dec_t { ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_1 = 0x0 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_2 = 0x1 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_4 = 0x2 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DE = 0x3 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_16 = 0x4 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_32 = 0x5 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_64 = 0x6 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DE

= 0x7 ,
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_256 = 0x8 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_5
= 0x9 , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_1024 = 0xA , ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_
= 0xB ,
ODR_DECIMATE_CONFIG_ACCEL_FIFO_ODR_DEC_4096 = 0xC }

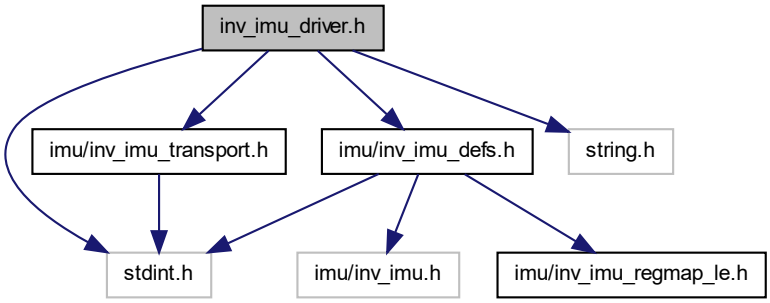
- enum intf_config1_ovrd_ap_spi_34_mode_ovrd_val_t { INTF_CONFIG1_OVRD_AP_SPI_34_MODE_OVRD_VAL_3_WIRE = 0x0 , INTF_CONFIG1_OVRD_AP_SPI_34_MODE_OVRD_VAL_4_WIRE = 0x1 }
- enum intf_config1_ovrd_ap_spi_mode_ovrd_val_t { INTF_CONFIG1_OVRD_AP_SPI_MODE_OVRD_VAL_0_OR_3 = 0x0 , INTF_CONFIG1_OVRD_AP_SPI_MODE_OVRD_VAL_1_OR_2 = 0x1 }
- enum drive_config0_pads_i2c_slew_t { DRIVE_CONFIG0_PADS_I2C_SLEW_TYP_20NS = 0x0 , DRIVE_CONFIG0_PADS_I2C_SLEW_TYP_7NS = 0x2 }
- enum drive_config0_pads_spi_slew_t {
DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_38NS = 0x0 , DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_14NS
= 0x1 , DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_10NS = 0x2 , DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_7NS
= 0x3 ,
DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_5NS = 0x4 , DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_4NS
= 0x5 , DRIVE_CONFIG0_PADS_SPI_SLEW_TYP_0_5NS = 0x6 }
- enum ioc_pad_scenario_ovrd_pads_int2_cfg_ovrd_val_t { IOC_PAD_SCENARIO_OVRD_INT2_CFG_OVRD_VAL_INT2 = 0 , IOC_PAD_SCENARIO_OVRD_INT2_CFG_OVRD_VAL_DRDY_INTR = 3 }
- enum reg_misc1_osc_id_ovrd_t {
REG_MISC1_OSC_ID_OVRD_OFF = 0x0 , REG_MISC1_OSC_ID_OVRD_EDOSC = 0x1 , REG_MISC1_OSC_ID_OVRD_RC
= 0x2 , REG_MISC1_OSC_ID_OVRD_PLL = 0x4 ,
REG_MISC1_OSC_ID_OVRD_EXT_CLK = 0x8 }
- enum fs_sel_aux_gyro_fs_sel_t {
FS_SEL_AUX_GYRO_FS_SEL_15_625_DPS = 8 , FS_SEL_AUX_GYRO_FS_SEL_31_25_DPS = 7 ,
FS_SEL_AUX_GYRO_FS_SEL_62_5_DPS = 6 , FS_SEL_AUX_GYRO_FS_SEL_125_DPS = 5 ,
FS_SEL_AUX_GYRO_FS_SEL_250_DPS = 4 , FS_SEL_AUX_GYRO_FS_SEL_500_DPS = 3 ,
FS_SEL_AUX_GYRO_FS_SEL_1000_DPS = 2 , FS_SEL_AUX_GYRO_FS_SEL_2000_DPS = 1 }
- enum fs_sel_aux_accel_fs_sel_t { FS_SEL_AUX_ACCEL_FS_SEL_2_G = 0x4 , FS_SEL_AUX_ACCEL_FS_SEL_4_G = 0x3 , FS_SEL_AUX_ACCEL_FS_SEL_8_G = 0x2 , FS_SEL_AUX_ACCEL_FS_SEL_16_G = 0x1 }
- enum smc_control_0_accel_lp_clk_sel_t { SMC_CONTROL_0_ACCEL_LP_CLK_RCOSC = 0x01 , SMC_CONTROL_0_ACCEL_LP_CLK_WUOSC = 0x00 }
- enum sreg_ctrl_sreg_data_endian_sel_t { SREG_CTRL_SREG_DATA_BIG_ENDIAN = 0x01 , SREG_CTRL_SREG_DATA_LIT = 0x00 }
- enum ipreg_sys1_reg_166_gyro_src_ctrl_sel_t { IPREG_SYS1_REG_166_GYRO_SRC_CTRL_INTERPOLATOR_ON_FIR_O = 0x2 , IPREG_SYS1_REG_166_GYRO_SRC_CTRL_INTERPOLATOR_OFF_FIR_ON = 0x1 , IPREG_SYS1_REG_166_GYR = 0x0 }
- enum ipreg_sys1_reg_170_gyro_lp_avg_sel_t {
IPREG_SYS1_REG_170_GYRO_LP_AVG_64 = 0xC , IPREG_SYS1_REG_170_GYRO_LP_AVG_32 = 0xB
, IPREG_SYS1_REG_170_GYRO_LP_AVG_20 = 0xA , IPREG_SYS1_REG_170_GYRO_LP_AVG_18 =
0x9 ,
IPREG_SYS1_REG_170_GYRO_LP_AVG_16 = 0x8 , IPREG_SYS1_REG_170_GYRO_LP_AVG_11 = 0x7
, IPREG_SYS1_REG_170_GYRO_LP_AVG_10 = 0x6 , IPREG_SYS1_REG_170_GYRO_LP_AVG_8 = 0x5
,
IPREG_SYS1_REG_170_GYRO_LP_AVG_7 = 0x4 , IPREG_SYS1_REG_170_GYRO_LP_AVG_5 = 0x3 ,
IPREG_SYS1_REG_170_GYRO_LP_AVG_4 = 0x2 , IPREG_SYS1_REG_170_GYRO_LP_AVG_2 = 0x1 ,
IPREG_SYS1_REG_170_GYRO_LP_AVG_1 = 0x0 }
- enum ipreg_sys1_reg_172_gyro_ui_lpfbw_sel_t {
IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_128 = 0x06 , IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_64
= 0x05 , IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_32 = 0x04 , IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_16
= 0x03 ,
IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_8 = 0x02 , IPREG_SYS1_REG_172_GYRO_UI_LPFBW_DIV_4
= 0x01 , IPREG_SYS1_REG_172_GYRO_UI_LPFBW_NO_FILTER = 0x00 }
- enum ipreg_sys2_reg_123_accel_src_ctrl_sel_t { IPREG_SYS2_REG_123_ACCEL_SRC_CTRL_INTERPOLATOR_ON_FIR_ = 0x2 , IPREG_SYS2_REG_123_ACCEL_SRC_CTRL_INTERPOLATOR_OFF_FIR_ON = 0x1 , IPREG_SYS2_REG_123_ACC = 0x0 }

- enum ipreg_sys2_reg_129_accel_lp_avg_sel_t {
  IPREG_SYS2_REG_129_ACCEL_LP_AVG_64 = 0xC , IPREG_SYS2_REG_129_ACCEL_LP_AVG_32 = 0xB , IPREG_SYS2_REG_129_ACCEL_LP_AVG_20 = 0xA , IPREG_SYS2_REG_129_ACCEL_LP_AVG_18 = 0x9 ,
  IPREG_SYS2_REG_129_ACCEL_LP_AVG_16 = 0x8 , IPREG_SYS2_REG_129_ACCEL_LP_AVG_11 = 0x7 , IPREG_SYS2_REG_129_ACCEL_LP_AVG_10 = 0x6 , IPREG_SYS2_REG_129_ACCEL_LP_AVG_8 = 0x5 ,
  IPREG_SYS2_REG_129_ACCEL_LP_AVG_7 = 0x4 , IPREG_SYS2_REG_129_ACCEL_LP_AVG_5 = 0x3 ,
  IPREG_SYS2_REG_129_ACCEL_LP_AVG_4 = 0x2 , IPREG_SYS2_REG_129_ACCEL_LP_AVG_2 = 0x1 ,
  IPREG_SYS2_REG_129_ACCEL_LP_AVG_1 = 0x0 }
- enum ipreg_sys2_reg_131_accel_ui_lpfbw_t {
  IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_128 = 0x06 , IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_64 = 0x05 , IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_32 = 0x04 , IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_1 = 0x03 ,
  IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_8 = 0x02 , IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_DIV_4 = 0x01 , IPREG_SYS2_REG_131_ACCEL_UI_LPFBW_NO_FILTER = 0x00 }
- enum selftest_average_time_t {
  SELFTEST_AVG_TIME_10_MS = 0x0000 , SELFTEST_AVG_TIME_20_MS = 0x0080 , SELFTEST_AVG_TIME_40_MS = 0x0100 , SELFTEST_AVG_TIME_80_MS = 0x0180 ,
  SELFTEST_AVG_TIME_160_MS = 0x0200 , SELFTEST_AVG_TIME_320_MS = 0x0280 }
- enum selftest_accel_threshold_t {
  SELFTEST_ACCEL_THRESHOLD_5_PERCENT = 0x0000 , SELFTEST_ACCEL_THRESHOLD_10_PERCENT = 0x0400 , SELFTEST_ACCEL_THRESHOLD_15_PERCENT = 0x0800 , SELFTEST_ACCEL_THRESHOLD_20_PERCENT = 0x0c00 ,
  SELFTEST_ACCEL_THRESHOLD_25_PERCENT = 0x1000 , SELFTEST_ACCEL_THRESHOLD_30_PERCENT = 0x1400 , SELFTEST_ACCEL_THRESHOLD_40_PERCENT = 0x1800 , SELFTEST_ACCEL_THRESHOLD_50_PERCENT = 0x1c00 }
- enum selftest_gyro_threshold_t {
  SELFTEST_GYRO_THRESHOLD_5_PERCENT = 0x0000 , SELFTEST_GYRO_THRESHOLD_10_PERCENT = 0x2000 , SELFTEST_GYRO_THRESHOLD_15_PERCENT = 0x4000 , SELFTEST_GYRO_THRESHOLD_20_PERCENT = 0x6000 ,
  SELFTEST_GYRO_THRESHOLD_25_PERCENT = 0x8000 , SELFTEST_GYRO_THRESHOLD_30_PERCENT = 0xa000 , SELFTEST_GYRO_THRESHOLD_40_PERCENT = 0xc000 , SELFTEST_GYRO_THRESHOLD_50_PERCENT = 0xe000 }
- enum stc_patch_params_t { SELFTEST_PATCH_EN_ACCEL_PHASE1 = 0x0001 , SELFTEST_PATCH_EN_ACCEL_PHASE2 = 0x0002 , SELFTEST_PATCH_EN_GYRO1_PHASE1 = 0x0004 , SELFTEST_PATCH_EN_GYRO1_PHASE2 = 0x0008 }

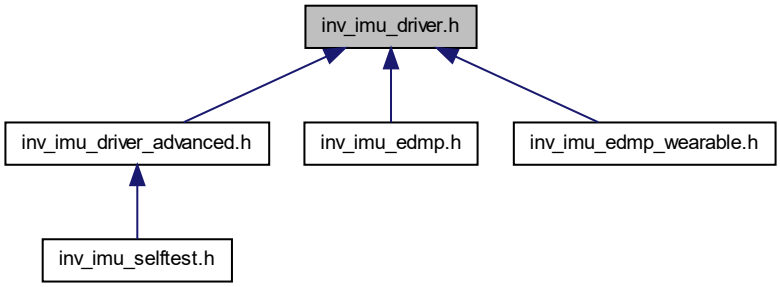
8.2 inv_imu_driver.h File Reference

```
#include "imu/inv_imu_defs.h"
#include "imu/inv_imu_transport.h"
#include <stdint.h>
#include <string.h>
```

Include dependency graph for inv_imu_driver.h:



This graph shows which files directly or indirectly include this file:



Classes

- struct inv_imu_device_t

  Basic driver configuration structure.
- union inv_imu_fifo_data_t

  One frame of FIFO header+data.
- struct inv_imu_int_state_t

  Interrupts definition.
- struct inv_imu_fifo_config_t

  Basic FIFO configuration.

Macros

- #define FORMAT_16_BITS_DATA(is_big_endian, pIn8, pOut16) *(pOut16) = ((is_big_endian) == 1) ? ((p↩ In8)[0] << 8) | (pIn8)[1] : ((pIn8)[1] << 8) | (pIn8)[0]

  Macro to convert 2 bytes in 1 half-word depending on IMU endianness.

Functions

- void inv_imu_sleep_us (inv_imu_device_t *s, uint32_t us)

  Sleep function.
- int inv_imu_soft_reset (inv_imu_device_t *s)

  Performs a soft reset of the device.
- int inv_imu_get_who_am_i (inv_imu_device_t *s, uint8_t *who_am_i)

  return WHOAMI value
- int inv_imu_set_accel_mode (inv_imu_device_t *s, pwr_mgmt0_accel_mode_t accel_mode)

  Configure accel mode.
- int inv_imu_set_gyro_mode (inv_imu_device_t *s, pwr_mgmt0_gyro_mode_t gyro_mode)

  Configure gyro mode.
- int inv_imu_set_accel_frequency (inv_imu_device_t *s, const accel_config0_accel_odr_t frequency)

  Configure accel Output Data Rate.
- int inv_imu_set_gyro_frequency (inv_imu_device_t *s, const gyro_config0_gyro_odr_t frequency)

  Configure gyro Output Data Rate.
- int inv_imu_set_accel_fsr (inv_imu_device_t *s, accel_config0_accel_ui_fs_sel_t accel_fsr)

  Set accel full scale range.
- int inv_imu_set_gyro_fsr (inv_imu_device_t *s, gyro_config0_gyro_ui_fs_sel_t gyro_fsr)

  Set gyro full scale range.
- int inv_imu_set_accel_lp_avg (inv_imu_device_t *s, ipreg_sys2_reg_129_accel_lp_avg_sel_t acc_avg)

  Set accel Low-Power averaging value.
- int inv_imu_set_gyro_lp_avg (inv_imu_device_t *s, ipreg_sys1_reg_170_gyro_lp_avg_sel_t gyr_avg)

  Set gyro Low-Power averaging value.
- int inv_imu_set_accel_ln_bw (inv_imu_device_t *s, ipreg_sys2_reg_131_accel_ui_lpfbw_t acc_bw)

  Set accel Low-Noise bandwidth value.
- int inv_imu_set_gyro_ln_bw (inv_imu_device_t *s, ipreg_sys1_reg_172_gyro_ui_lpfbw_sel_t gyr_bw)

  Set gyro Low-Noise bandwidth value.
- int inv_imu_get_register_data (inv_imu_device_t *s, inv_imu_sensor_data_t *data)

  Get current sensor data from the registers.
- int inv_imu_set_fifo_config (inv_imu_device_t *s, const inv_imu_fifo_config_t *fifo_config)

  Configures the FIFO to the specified state.
- int inv_imu_get_fifo_config (inv_imu_device_t *s, inv_imu_fifo_config_t *fifo_config)

  Gets the current FIFO configuration.
- int inv_imu_flush_fifo (inv_imu_device_t *s)

  Flush FIFO content.
- int inv_imu_get_frame_count (inv_imu_device_t *s, uint16_t *frame_count)

  Get FIFO frame count.
- int inv_imu_get_fifo_frame (inv_imu_device_t *s, inv_imu_fifo_data_t *data)

  Get one frame of FIFO data.
- int inv_imu_set_config_int (inv_imu_device_t *s, const inv_imu_int_num_t num, const inv_imu_int_state_t *it)

  Configure interrupts source.
- int inv_imu_get_config_int (inv_imu_device_t *s, const inv_imu_int_num_t num, inv_imu_int_state_t *it)

  Retrieve interrupts configuration.
- int inv_imu_set_pin_config_int (inv_imu_device_t *s, const inv_imu_int_num_t num, const inv_imu_int_pin_config_t *conf)

  Configure pin behavior.
- int inv_imu_get_int_status (inv_imu_device_t *s, const inv_imu_int_num_t num, inv_imu_int_state_t *it)

  Read interrupt 1 status.
- int inv_imu_get_endianness (inv_imu_device_t *s)

Read the UI endianness and set the inv_device endianness field.

- int inv_imu_select_accel_lp_clk (inv_imu_device_t *s, smc_control_0_accel_lp_clk_sel_t clk_sel)

  Select which clock to use when in Low Power mode.

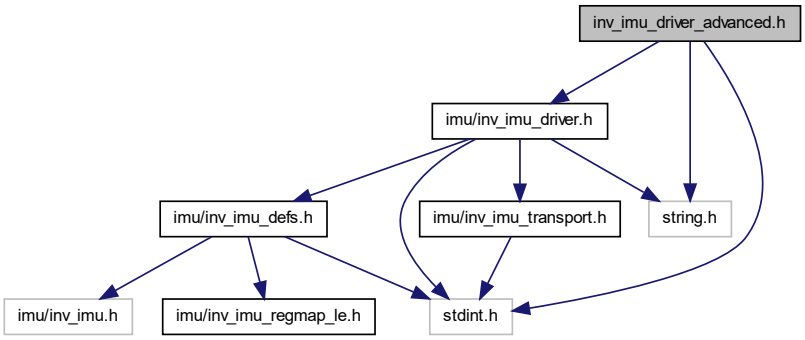
- const char * inv_imu_get_version (void)

  Return driver version x.y.z-suffix as a char array.

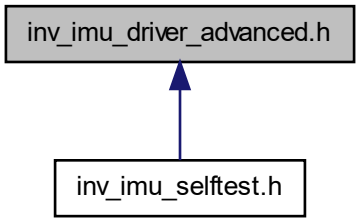
8.3 inv_imu_driver_advanced.h File Reference

```
#include "imu/inv_imu_driver.h"
#include <stdint.h>
#include <string.h>
```

Include dependency graph for inv_imu_driver_advanced.h:



This graph shows which files directly or indirectly include this file:



Classes

- struct inv_imu_sensor_event_t

  Sensor event structure definition.

- struct inv_imu_adv_var_t

  Definition of extended variables.

- struct inv_imu_adv_fifo_config_t

  FIFO configuration structure.

Macros

- #define FIFO_MIRRORING_SIZE 16 ∗ 258 /∗ packet size ∗ max_count = 4kB ∗/

  Maximum buffer size mirrored from FIFO.

Enumerations

- enum inv_imu_sensor_id_t {
  INV_SENSOR_ACCEL , INV_SENSOR_GYRO , INV_SENSOR_FSYNC_EVENT , INV_SENSOR_TEMPERATURE ,
  INV_SENSOR_EDMP_PEDOMETER_EVENT , INV_SENSOR_EDMP_PEDOMETER_COUNT , INV_SENSOR_EDMP_TILT , INV_SENSOR_EDMP_FF ,
  INV_SENSOR_EDMP_LOWG , INV_SENSOR_EDMP_HIGHG , INV_SENSOR_EDMP_SMD , INV_SENSOR_EDMP_TAP ,
  INV_SENSOR_EDMP_R2W_WAKE , INV_SENSOR_EDMP_R2W_SLEEP , INV_SENSOR_ES0 , INV_SENSOR_ES1 ,
  INV_SENSOR_MAX }

  Sensor identifier enumeration.

Functions

- int inv_imu_adv_init (inv_imu_device_t ∗s)

  Initializes device.
- int inv_imu_adv_device_reset (inv_imu_device_t ∗s)

  Performs a soft reset of the device.
- int inv_imu_adv_enable_accel_lp (inv_imu_device_t ∗s)

  Enable accel in low power mode.
- int inv_imu_adv_enable_accel_ln (inv_imu_device_t ∗s)

  Enable accel in low noise mode.
- int inv_imu_adv_disable_accel (inv_imu_device_t ∗s)

  Disable accel.
- int inv_imu_adv_enable_gyro_ln (inv_imu_device_t ∗s)

  Enable gyro in low noise mode.
- int inv_imu_adv_enable_gyro_lp (inv_imu_device_t ∗s)

  Enable gyro in low power mode.
- int inv_imu_adv_disable_gyro (inv_imu_device_t ∗s)

  Disable gyro.
- int inv_imu_adv_get_data_from_registers (inv_imu_device_t ∗s)

  Read all registers containing data (temperature, accelerometer and gyroscope).
- int inv_imu_adv_reset_fifo (inv_imu_device_t ∗s)

  reset IMU fifo
- int inv_imu_adv_get_fifo_config (inv_imu_device_t ∗s, inv_imu_adv_fifo_config_t ∗conf)

  Retrieve FIFO configuration.
- int inv_imu_adv_set_fifo_config (inv_imu_device_t ∗s, const inv_imu_adv_fifo_config_t ∗conf)

  Set FIFO configuration.
- int inv_imu_adv_get_data_from_fifo (inv_imu_device_t ∗s, uint8_t fifo_data[FIFO_MIRRORING_SIZE], uint16_t ∗fifo_count)

  Read all available packets from the FIFO.
- int inv_imu_adv_parse_fifo_data (inv_imu_device_t ∗s, const uint8_t fifo_data[FIFO_MIRRORING_SIZE], const uint16_t fifo_count)

  Parse packets from FIFO buffer.

- uint32_t inv_imu_adv_convert_odr_bitfield_to_us (uint32_t odr_bitfield)

  Converts accel_config0_accel_odr_t or gyro_config0_gyro_odr_t enums to period expressed in us.
- int inv_imu_adv_get_accel_fsr (inv_imu_device_t *s, accel_config0_accel_ui_fs_sel_t *accel_fsr)

  Access accel full scale range.
- int inv_imu_adv_get_gyro_fsr (inv_imu_device_t *s, gyro_config0_gyro_ui_fs_sel_t *gyro_fsr)

  Access gyro full scale range.
- int inv_imu_adv_set_timestamp_resolution (inv_imu_device_t *s, const tmst_wom_config_tmst_resol_t timestamp_resol)

  Set timestamp resolution.
- uint32_t inv_imu_adv_get_timestamp_resolution_us (inv_imu_device_t *s)

  Get timestamp resolution.
- int inv_imu_adv_configure_wom (inv_imu_device_t *s, const uint8_t wom_x_th, const uint8_t wom_y_th, const uint8_t wom_z_th, tmst_wom_config_wom_int_mode_t wom_int, tmst_wom_config_wom_int_dur_t wom_dur)

  Enable Wake On Motion.
- int inv_imu_adv_enable_wom (inv_imu_device_t *s)

  Enable Wake On Motion.
- int inv_imu_adv_disable_wom (inv_imu_device_t *s)

  Disable Wake On Motion.
- int inv_imu_adv_set_endianness (inv_imu_device_t *s, sreg_ctrl_sreg_data_endian_sel_t endianness)

  Set the UI endianness and set the inv_device endianness field.
- int inv_imu_adv_power_up_sram (inv_imu_device_t *s)

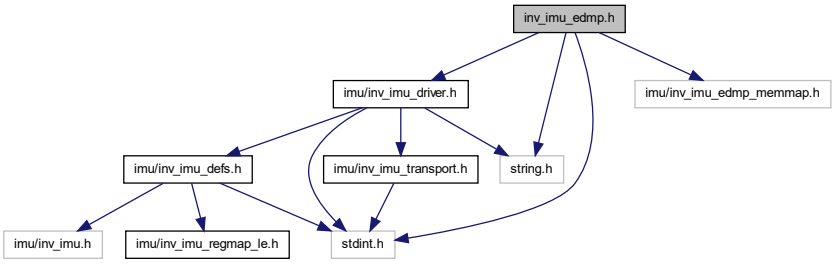
  Power-up the SRAM.
- int inv_imu_adv_power_down_sram (inv_imu_device_t *s)

  Power-down the SRAM.

8.4 inv_imu_edmp.h File Reference

```
#include "imu/inv_imu_driver.h"
#include "imu/inv_imu_edmp_memmap.h"
#include <stdint.h>
#include <string.h>
```

Include dependency graph for inv_imu_edmp.h:



Classes

- struct inv_imu_edmp_int_state_t

  APEX interrupts definition.
- struct int_apex_statusx_t

  Registers to retrieve interrupts status for APEX.
- struct int_apex_configx_t

  Registers to configure interrupts for APEX.
- struct edmp_apex_enx_t

  Registers to enable APEX features.
- struct inv_imu_edmp_apex_parameters_t

  IMU APEX inputs parameters definition.
- struct inv_imu_edmp_pedometer_data_t

  Pedometer outputs.
- struct inv_imu_edmp_tap_data_t

  Tap outputs.

Macros

- #define INV_IMU_WRITE_EDMP_SRAM(s, name, val) inv_imu_write_sram(s, (uint32_t)name, name##_↩ SIZE, val)

  Writes in EDMP SRAM.
- #define INV_IMU_READ_EDMP_SRAM(s, name, val) inv_imu_read_sram(s, (uint32_t)name, name##_↩ SIZE, val)

  Reads in EDMP SRAM.

Enumerations

- enum inv_imu_edmp_int_t { INV_IMU_EDMP_INT0 = 0 , INV_IMU_EDMP_INT1 , INV_IMU_EDMP_INT2 }

  EDMP input interrupt lines definition.
- enum inv_imu_edmp_activity_class_t { INV_IMU_EDMP_UNKNOWN = 0 , INV_IMU_EDMP_WALK = 1 , INV_IMU_EDMP_RUN = 2 }

  Pedometer activity class.
- enum inv_imu_edmp_tap_num_t { INV_IMU_EDMP_TAP_DOUBLE = 0x02 , INV_IMU_EDMP_TAP_SINGLE = 0x01 }

  Tap number definition.
- enum inv_imu_edmp_tap_axis_t { INV_IMU_EDMP_TAP_AXIS_Z = 0x02 , INV_IMU_EDMP_TAP_AXIS_Y = 0x01 , INV_IMU_EDMP_TAP_AXIS_X = 0x00 }

  Tap axis definition.
- enum inv_imu_edmp_tap_dir_t { INV_IMU_EDMP_TAP_DIR_POSITIVE = 0x01 , INV_IMU_EDMP_TAP_DIR_NEGATIVE = 0x00 }

  Tap direction definition.

Functions

- int inv_imu_edmp_set_frequency (inv_imu_device_t *s, const dmp_ext_sen_odr_cfg_apex_odr_t frequency)

  Configure EDMP Output Data Rate.
- int inv_imu_edmp_init_apex (inv_imu_device_t *s)

  Initialize EDMP APEX algorithms.
- int inv_imu_edmp_recompute_apex_decimation (inv_imu_device_t *s)

  Recompute EDMP APEX algorithms internal decimator based on new EDMP output Data Rate configured with `inv_imu_edmp_set_frequency`.
- int inv_imu_edmp_get_apex_parameters (inv_imu_device_t *s, inv_imu_edmp_apex_parameters_t *p)

  Returns current EDMP parameters for APEX algorithms.
- int inv_imu_edmp_set_apex_parameters (inv_imu_device_t *s, const inv_imu_edmp_apex_parameters_t *p)

  Configures EDMP parameters for APEX algorithms.
- int inv_imu_edmp_get_config_int_apex (inv_imu_device_t *s, inv_imu_edmp_int_state_t *it)

  Retrieve interrupts configuration.
- int inv_imu_edmp_set_config_int_apex (inv_imu_device_t *s, const inv_imu_edmp_int_state_t *it)

  Configure APEX interrupt.
- int inv_imu_edmp_enable (inv_imu_device_t *s)

  Enable EDMP.
- int inv_imu_edmp_disable (inv_imu_device_t *s)

  Disable EDMP.
- int inv_imu_edmp_enable_pedometer (inv_imu_device_t *s)

  Enable APEX algorithm Pedometer.
- int inv_imu_edmp_disable_pedometer (inv_imu_device_t *s)

  Disable APEX algorithm Pedometer.
- int inv_imu_edmp_enable_smd (inv_imu_device_t *s)

  Enable APEX algorithm Significant Motion Detection.
- int inv_imu_edmp_disable_smd (inv_imu_device_t *s)

  Disable APEX algorithm Significant Motion Detection.
- int inv_imu_edmp_enable_tilt (inv_imu_device_t *s)

  Enable APEX algorithm Tilt.
- int inv_imu_edmp_disable_tilt (inv_imu_device_t *s)

  Disable APEX algorithm Tilt.
- int inv_imu_edmp_enable_r2w (inv_imu_device_t *s)

  Enable APEX algorithm R2W.
- int inv_imu_edmp_disable_r2w (inv_imu_device_t *s)

  Disable APEX algorithm R2W.
- int inv_imu_edmp_enable_tap (inv_imu_device_t *s)

  Enable APEX algorithm Tap.
- int inv_imu_edmp_disable_tap (inv_imu_device_t *s)

  Disable APEX algorithm Tap.
- int inv_imu_edmp_enable_ff (inv_imu_device_t *s)

  Enable APEX algorithm Free Fall.
- int inv_imu_edmp_disable_ff (inv_imu_device_t *s)

  Disable APEX algorithm Free Fall.
- int inv_imu_edmp_get_int_apex_status (inv_imu_device_t *s, inv_imu_edmp_int_state_t *it)

  Read APEX interrupt status.
- int inv_imu_edmp_get_pedometer_data (inv_imu_device_t *s, inv_imu_edmp_pedometer_data_t *data)

  Retrieve pedometer outputs.
- int inv_imu_edmp_get_ff_data (inv_imu_device_t *s, uint16_t *freefall_duration)

  Retrieve APEX free fall outputs and format them.

- int inv_imu_edmp_get_tap_data (inv_imu_device_t *s, inv_imu_edmp_tap_data_t *data)

  Retrieve tap outputs.
- int inv_imu_edmp_mask_int_src (inv_imu_device_t *s, inv_imu_edmp_int_t edmp_int_nb, uint8_t int_mask)

  Mask requested interrupt sources for edmp interrupt line passed in parameter.
- int inv_imu_edmp_unmask_int_src (inv_imu_device_t *s, inv_imu_edmp_int_t edmp_int_nb, uint8_t int_mask)

  Unmask requested interrupt sources for edmp interrupt line passed in parameter.
- int inv_imu_edmp_configure (inv_imu_device_t *s)

  Setup EDMP to execute code in ROM.
- int inv_imu_edmp_run_ondemand (inv_imu_device_t *s, inv_imu_edmp_int_t edmp_int_nb)

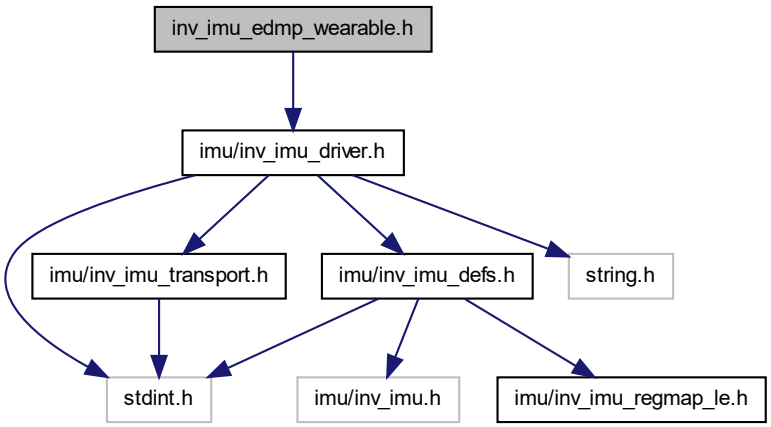
  Run EDMP using the on-demand mechanism.
- int inv_imu_edmp_wait_for_idle (inv_imu_device_t *s)

  Wait until EDMP idle bit is set (means EDMP execution is completed).

8.5 inv_imu_edmp_wearable.h File Reference

```
#include "imu/inv_imu_driver.h"
```

Include dependency graph for inv_imu_edmp_wearable.h:



Classes

- struct inv_imu_edmp_b2s_parameters_t

  IMU B2S parameters definition.

Functions

- int inv_imu_edmp_b2s_init (inv_imu_device_t *s)

  Initialize B2S algorithm.
- int inv_imu_edmp_b2s_get_parameters (inv_imu_device_t *s, inv_imu_edmp_b2s_parameters_t *b2s_params)

Get current B2S configuration settings.

- int inv_imu_edmp_b2s_set_parameters (inv_imu_device_t *s, const inv_imu_edmp_b2s_parameters_t *b2s_params)

  Set new B2S configuration settings.

- int inv_imu_edmp_b2s_enable (inv_imu_device_t *s)

  Enable APEX algorithm B2S.

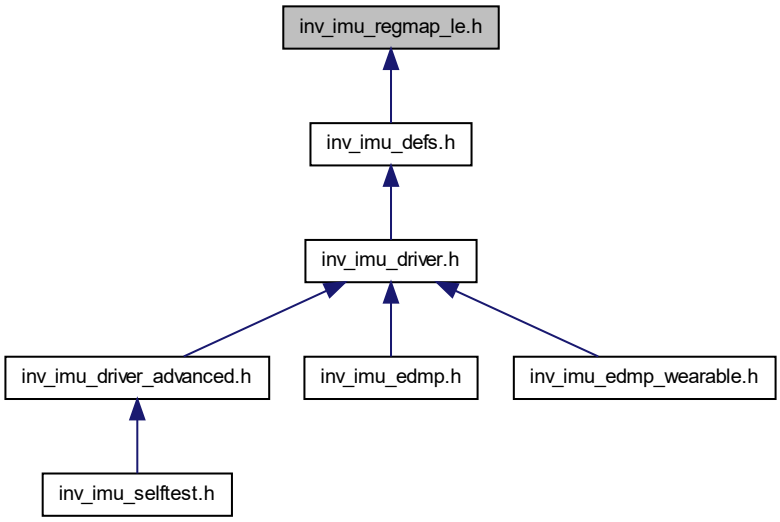
- int inv_imu_edmp_b2s_disable (inv_imu_device_t *s)

  Disable APEX algorithm B2S.

8.6 inv_imu_regmap_le.h File Reference

File exposing the device register map.

This graph shows which files directly or indirectly include this file:



Classes

- struct pwr_mgmt0_t
- struct fifo_data_t
- struct int1_config0_t
- struct int1_config1_t
- struct int1_config2_t
- struct int1_status0_t
- struct int1_status1_t
- struct accel_config0_t
- struct gyro_config0_t
- struct fifo_config0_t
- struct fifo_config2_t
- struct fifo_config3_t

- struct fifo_config4_t
- struct tmst_wom_config_t
- struct fsync_config0_t
- struct fsync_config1_t
- struct rtc_config_t
- struct dmp_ext_sen_odr_cfg_t
- struct odr_decimate_config_t
- struct edmp_apex_en0_t
- struct edmp_apex_en1_t
- struct apex_buffer_mgmt_t
- struct intf_config0_t
- struct intf_config1_ovrd_t
- struct intf_aux_config_t
- struct ioc_pad_scenario_t
- struct ioc_pad_scenario_aux_ovrd_t
- struct ioc_pad_scenario_ovrd_t
- struct drive_config0_t
- struct drive_config1_t
- struct drive_config2_t
- struct reg_misc1_t
- struct int_apex_config0_t
- struct int_apex_config1_t
- struct int_apex_status0_t
- struct int_apex_status1_t
- struct intf_config_ovrd_aux1_t
- struct pwr_mgmt_aux1_t
- struct fs_sel_aux1_t
- struct int2_config0_t
- struct int2_config1_t
- struct int2_config2_t
- struct int2_status0_t
- struct int2_status1_t
- struct intf_config_ovrd_aux2_t
- struct pwr_mgmt_aux2_t
- struct fs_sel_aux2_t
- struct int_aux2_config_t
- struct int_aux2_status_t
- struct who_am_i_t
- struct reg_host_msg_t
- struct ireg_addr_15_8_t
- struct ireg_addr_7_0_t
- struct ireg_data_t
- struct reg_misc2_t
- struct i2cm_command_0_t
- struct i2cm_command_1_t
- struct i2cm_command_2_t
- struct i2cm_command_3_t
- struct i2cm_dev_profile0_t
- struct i2cm_dev_profile1_t
- struct i2cm_dev_profile2_t
- struct i2cm_dev_profile3_t
- struct i2cm_control_t
- struct i2cm_status_t
- struct i2cm_ext_dev_status_t
- struct i2cm_rd_data0_t

- struct i2cm_rd_data1_t
- struct i2cm_rd_data2_t
- struct i2cm_rd_data3_t
- struct i2cm_rd_data4_t
- struct i2cm_rd_data5_t
- struct i2cm_rd_data6_t
- struct i2cm_rd_data7_t
- struct i2cm_rd_data8_t
- struct i2cm_rd_data9_t
- struct i2cm_rd_data10_t
- struct i2cm_rd_data11_t
- struct i2cm_rd_data12_t
- struct i2cm_rd_data13_t
- struct i2cm_rd_data14_t
- struct i2cm_rd_data15_t
- struct i2cm_rd_data16_t
- struct i2cm_rd_data17_t
- struct i2cm_rd_data18_t
- struct i2cm_rd_data19_t
- struct i2cm_rd_data20_t
- struct i2cm_wr_data0_t
- struct i2cm_wr_data1_t
- struct i2cm_wr_data2_t
- struct i2cm_wr_data3_t
- struct i2cm_wr_data4_t
- struct i2cm_wr_data5_t
- struct sifs_ixc_error_status_t
- struct edmp_sp_start_addr_t
- struct smc_control_0_t
- struct smc_control_1_t
- struct stc_config_t
- struct sreg_ctrl_t
- struct sifs_i3c_stc_cfg_t
- struct int_pulse_min_on_intf0_t
- struct int_pulse_min_on_intf1_t
- struct int_pulse_min_off_intf0_t
- struct int_pulse_min_off_intf1_t
- struct isr_0_7_t
- struct isr_8_15_t
- struct isr_16_23_t
- struct status_mask_pin_0_7_t
- struct status_mask_pin_8_15_t
- struct status_mask_pin_16_23_t
- struct int_i2cm_source_t
- struct accel_wom_x_thr_t
- struct accel_wom_y_thr_t
- struct accel_wom_z_thr_t
- struct selftest_t
- struct ipreg_misc_t
- struct sw_pll1_trim_t
- struct fifo_sram_sleep_t
- struct ipreg_sys1_reg_166_t
- struct ipreg_sys1_reg_168_t
- struct ipreg_sys1_reg_170_t
- struct ipreg_sys1_reg_171_t

- struct ipreg_sys1_reg_172_t
- struct ipreg_sys1_reg_173_t
- struct ipreg_sys2_reg_123_t
- struct ipreg_sys2_reg_129_t
- struct ipreg_sys2_reg_130_t
- struct ipreg_sys2_reg_131_t
- struct ipreg_sys2_reg_132_t
- struct ipreg_bar_reg_57_t
- struct ipreg_bar_reg_58_t
- struct ipreg_bar_reg_59_t
- struct ipreg_bar_reg_60_t
- struct ipreg_bar_reg_61_t
- struct ipreg_bar_reg_62_t

Macros

- #define ACCEL_DATA_X1_UI 0x00
- #define ACCEL_DATA_X0_UI 0x01
- #define ACCEL_DATA_Y1_UI 0x02
- #define ACCEL_DATA_Y0_UI 0x03
- #define ACCEL_DATA_Z1_UI 0x04
- #define ACCEL_DATA_Z0_UI 0x05
- #define GYRO_DATA_X1_UI 0x06
- #define GYRO_DATA_X0_UI 0x07
- #define GYRO_DATA_Y1_UI 0x08
- #define GYRO_DATA_Y0_UI 0x09
- #define GYRO_DATA_Z1_UI 0x0a
- #define GYRO_DATA_Z0_UI 0x0b
- #define TEMP_DATA1_UI 0x0c
- #define TEMP_DATA0_UI 0x0d
- #define TMST_FSYNCH 0x0e
- #define TMST_FSYNCL 0x0f
- #define PWR_MGMT0 0x10
- #define FIFO_COUNT_0 0x12
- #define FIFO_COUNT_1 0x13
- #define FIFO_DATA 0x14
- #define INT1_CONFIG0 0x16
- #define INT1_CONFIG1 0x17
- #define INT1_CONFIG2 0x18
- #define INT1_STATUS0 0x19
- #define INT1_STATUS1 0x1a
- #define ACCEL_CONFIG0 0x1b
- #define GYRO_CONFIG0 0x1c
- #define FIFO_CONFIG0 0x1d
- #define FIFO_CONFIG1_0 0x1e
- #define FIFO_CONFIG1_1 0x1f
- #define FIFO_CONFIG2 0x20
- #define FIFO_CONFIG3 0x21
- #define FIFO_CONFIG4 0x22
- #define TMST_WOM_CONFIG 0x23
- #define FSYNC_CONFIG0 0x24
- #define FSYNC_CONFIG1 0x25
- #define RTC_CONFIG 0x26
- #define DMP_EXT_SEN_ODR_CFG 0x27

- #define ODR_DECIMATE_CONFIG 0x28
- #define EDMP_APEX_EN0 0x29
- #define EDMP_APEX_EN1 0x2a
- #define APEX_BUFFER_MGMT 0x2b
- #define INTF_CONFIG0 0x2c
- #define INTF_CONFIG1_OVRD 0x2d
- #define INTF_AUX_CONFIG 0x2e
- #define IOC_PAD_SCENARIO 0x2f
- #define IOC_PAD_SCENARIO_AUX_OVRD 0x30
- #define IOC_PAD_SCENARIO_OVRD 0x31
- #define DRIVE_CONFIG0 0x32
- #define DRIVE_CONFIG1 0x33
- #define DRIVE_CONFIG2 0x34
- #define REG_MISC1 0x35
- #define INT_APEX_CONFIG0 0x39
- #define INT_APEX_CONFIG1 0x3a
- #define INT_APEX_STATUS0 0x3b
- #define INT_APEX_STATUS1 0x3c
- #define INTF_CONFIG_OVRD_AUX1 0x42
- #define ACCEL_DATA_X1_AUX1 0x44
- #define ACCEL_DATA_X0_AUX1 0x45
- #define ACCEL_DATA_Y1_AUX1 0x46
- #define ACCEL_DATA_Y0_AUX1 0x47
- #define ACCEL_DATA_Z1_AUX1 0x48
- #define ACCEL_DATA_Z0_AUX1 0x49
- #define GYRO_DATA_X1_AUX1 0x4a
- #define GYRO_DATA_X0_AUX1 0x4b
- #define GYRO_DATA_Y1_AUX1 0x4c
- #define GYRO_DATA_Y0_AUX1 0x4d
- #define GYRO_DATA_Z1_AUX1 0x4e
- #define GYRO_DATA_Z0_AUX1 0x4f
- #define TEMP_DATA1_AUX1 0x50
- #define TEMP_DATA0_AUX1 0x51
- #define TMST_FSYNCH_AUX1 0x52
- #define TMST_FSYNCL_AUX1 0x53
- #define PWR_MGMT_AUX1 0x54
- #define FS_SEL_AUX1 0x55
- #define INT2_CONFIG0 0x56
- #define INT2_CONFIG1 0x57
- #define INT2_CONFIG2 0x58
- #define INT2_STATUS0 0x59
- #define INT2_STATUS1 0x5a
- #define INTF_CONFIG_OVRD_AUX2 0x5c
- #define ACCEL_DATA_X1_AUX2 0x5e
- #define ACCEL_DATA_X0_AUX2 0x5f
- #define ACCEL_DATA_Y1_AUX2 0x60
- #define ACCEL_DATA_Y0_AUX2 0x61
- #define ACCEL_DATA_Z1_AUX2 0x62
- #define ACCEL_DATA_Z0_AUX2 0x63
- #define GYRO_DATA_X1_AUX2 0x64
- #define GYRO_DATA_X0_AUX2 0x65
- #define GYRO_DATA_Y1_AUX2 0x66
- #define GYRO_DATA_Y0_AUX2 0x67
- #define GYRO_DATA_Z1_AUX2 0x68
- #define GYRO_DATA_Z0_AUX2 0x69

- #define TEMP_DATA1_AUX2 0x6a
- #define TEMP_DATA0_AUX2 0x6b
- #define TMST_FSYNCH_AUX2 0x6c
- #define TMST_FSYNCL_AUX2 0x6d
- #define PWR_MGMT_AUX2 0x6e
- #define FS_SEL_AUX2 0x6f
- #define INT_AUX2_CONFIG 0x70
- #define INT_AUX2_STATUS 0x71
- #define WHO_AM_I 0x72
- #define REG_HOST_MSG 0x73
- #define IREG_ADDR_15_8 0x7c
- #define IREG_ADDR_7_0 0x7d
- #define IREG_DATA 0x7e
- #define REG_MISC2 0x7f
- #define I2CM_COMMAND_0 0xa206
- #define I2CM_COMMAND_1 0xa207
- #define I2CM_COMMAND_2 0xa208
- #define I2CM_COMMAND_3 0xa209
- #define I2CM_DEV_PROFILE0 0xa20e
- #define I2CM_DEV_PROFILE1 0xa20f
- #define I2CM_DEV_PROFILE2 0xa210
- #define I2CM_DEV_PROFILE3 0xa211
- #define I2CM_CONTROL 0xa216
- #define I2CM_STATUS 0xa218
- #define I2CM_EXT_DEV_STATUS 0xa21a
- #define I2CM_RD_DATA0 0xa21b
- #define I2CM_RD_DATA1 0xa21c
- #define I2CM_RD_DATA2 0xa21d
- #define I2CM_RD_DATA3 0xa21e
- #define I2CM_RD_DATA4 0xa21f
- #define I2CM_RD_DATA5 0xa220
- #define I2CM_RD_DATA6 0xa221
- #define I2CM_RD_DATA7 0xa222
- #define I2CM_RD_DATA8 0xa223
- #define I2CM_RD_DATA9 0xa224
- #define I2CM_RD_DATA10 0xa225
- #define I2CM_RD_DATA11 0xa226
- #define I2CM_RD_DATA12 0xa227
- #define I2CM_RD_DATA13 0xa228
- #define I2CM_RD_DATA14 0xa229
- #define I2CM_RD_DATA15 0xa22a
- #define I2CM_RD_DATA16 0xa22b
- #define I2CM_RD_DATA17 0xa22c
- #define I2CM_RD_DATA18 0xa22d
- #define I2CM_RD_DATA19 0xa22e
- #define I2CM_RD_DATA20 0xa22f
- #define I2CM_WR_DATA0 0xa233
- #define I2CM_WR_DATA1 0xa234
- #define I2CM_WR_DATA2 0xa235
- #define I2CM_WR_DATA3 0xa236
- #define I2CM_WR_DATA4 0xa237
- #define I2CM_WR_DATA5 0xa238
- #define SIFS_IXC_ERROR_STATUS 0xa24b
- #define EDMP_PRGRM_IRQ0_0 0xa24f
- #define EDMP_PRGRM_IRQ0_1 0xa250

- #define EDMP_PRGRM_IRQ1_0 0xa251
- #define EDMP_PRGRM_IRQ1_1 0xa252
- #define EDMP_PRGRM_IRQ2_0 0xa253
- #define EDMP_PRGRM_IRQ2_1 0xa254
- #define EDMP_SP_START_ADDR 0xa255
- #define SMC_CONTROL_0 0xa258
- #define SMC_CONTROL_1 0xa259
- #define STC_CONFIG 0xa263
- #define SREG_CTRL 0xa267
- #define SIFS_I3C_STC_CFG 0xa268
- #define INT_PULSE_MIN_ON_INTF0 0xa269
- #define INT_PULSE_MIN_ON_INTF1 0xa26a
- #define INT_PULSE_MIN_OFF_INTF0 0xa26b
- #define INT_PULSE_MIN_OFF_INTF1 0xa26c
- #define ISR_0_7 0xa26e
- #define ISR_8_15 0xa26f
- #define ISR_16_23 0xa270
- #define STATUS_MASK_PIN_0_7 0xa271
- #define STATUS_MASK_PIN_8_15 0xa272
- #define STATUS_MASK_PIN_16_23 0xa273
- #define INT_I2CM_SOURCE 0xa274
- #define ACCEL_WOM_X_THR 0xa27e
- #define ACCEL_WOM_Y_THR 0xa27f
- #define ACCEL_WOM_Z_THR 0xa280
- #define SELFTEST 0xa290
- #define IPREG_MISC 0xa297
- #define SW_PLL1_TRIM 0xa2a2
- #define FIFO_SRAM_SLEEP 0xa2a7
- #define IPREG_SYS1_REG_42 0xa42a
- #define IPREG_SYS1_REG_43 0xa42b
- #define IPREG_SYS1_REG_56 0xa438
- #define IPREG_SYS1_REG_57 0xa439
- #define IPREG_SYS1_REG_70 0xa446
- #define IPREG_SYS1_REG_71 0xa447
- #define IPREG_SYS1_REG_166 0xa4a6
- #define IPREG_SYS1_REG_168 0xa4a8
- #define IPREG_SYS1_REG_170 0xa4aa
- #define IPREG_SYS1_REG_171 0xa4ab
- #define IPREG_SYS1_REG_172 0xa4ac
- #define IPREG_SYS1_REG_173 0xa4ad
- #define IPREG_SYS2_REG_24 0xa518
- #define IPREG_SYS2_REG_25 0xa519
- #define IPREG_SYS2_REG_32 0xa520
- #define IPREG_SYS2_REG_33 0xa521
- #define IPREG_SYS2_REG_40 0xa528
- #define IPREG_SYS2_REG_41 0xa529
- #define IPREG_SYS2_REG_123 0xa57b
- #define IPREG_SYS2_REG_129 0xa581
- #define IPREG_SYS2_REG_130 0xa582
- #define IPREG_SYS2_REG_131 0xa583
- #define IPREG_SYS2_REG_132 0xa584
- #define IPREG_BAR_REG_57 0xa039
- #define IPREG_BAR_REG_58 0xa03a
- #define IPREG_BAR_REG_59 0xa03b
- #define IPREG_BAR_REG_60 0xa03c
- #define IPREG_BAR_REG_61 0xa03d
- #define IPREG_BAR_REG_62 0xa03e

8.6.1 Detailed Description

File exposing the device register map.

8.6.2 Macro Definition Documentation

8.6.2.1 ACCEL_CONFIG0

```
#define ACCEL_CONFIG0 0x1b
```

8.6.2.2 ACCEL_DATA_X0_AUX1

```
#define ACCEL_DATA_X0_AUX1 0x45
```

8.6.2.3 ACCEL_DATA_X0_AUX2

```
#define ACCEL_DATA_X0_AUX2 0x5f
```

8.6.2.4 ACCEL_DATA_X0_UI

```
#define ACCEL_DATA_X0_UI 0x01
```

8.6.2.5 ACCEL_DATA_X1_AUX1

```
#define ACCEL_DATA_X1_AUX1 0x44
```

8.6.2.6 ACCEL_DATA_X1_AUX2

```
#define ACCEL_DATA_X1_AUX2 0x5e
```

8.6.2.7 ACCEL_DATA_X1_UI

```
#define ACCEL_DATA_X1_UI 0x00
```

8.6.2.8 ACCEL_DATA_Y0_AUX1

```
#define ACCEL_DATA_Y0_AUX1 0x47
```

8.6.2.9 ACCEL_DATA_Y0_AUX2

```
#define ACCEL_DATA_Y0_AUX2 0x61
```

8.6.2.10 ACCEL_DATA_Y0_UI

```
#define ACCEL_DATA_Y0_UI 0x03
```

8.6.2.11 ACCEL_DATA_Y1_AUX1

```
#define ACCEL_DATA_Y1_AUX1 0x46
```

8.6.2.12 ACCEL_DATA_Y1_AUX2

```
#define ACCEL_DATA_Y1_AUX2 0x60
```

8.6.2.13 ACCEL_DATA_Y1_UI

```
#define ACCEL_DATA_Y1_UI 0x02
```

8.6.2.14 ACCEL_DATA_Z0_AUX1

```
#define ACCEL_DATA_Z0_AUX1 0x49
```

8.6.2.15 ACCEL_DATA_Z0_AUX2

```
#define ACCEL_DATA_Z0_AUX2 0x63
```

8.6.2.16 ACCEL_DATA_Z0_UI

```
#define ACCEL_DATA_Z0_UI 0x05
```

8.6.2.17 ACCEL_DATA_Z1_AUX1

```
#define ACCEL_DATA_Z1_AUX1 0x48
```

8.6.2.18 ACCEL_DATA_Z1_AUX2

```
#define ACCEL_DATA_Z1_AUX2 0x62
```

8.6.2.19 ACCEL_DATA_Z1_UI

```
#define ACCEL_DATA_Z1_UI 0x04
```

8.6.2.20 ACCEL_WOM_X_THR

```
#define ACCEL_WOM_X_THR 0xa27e
```

8.6.2.21 ACCEL_WOM_Y_THR

```
#define ACCEL_WOM_Y_THR 0xa27f
```

8.6.2.22 ACCEL_WOM_Z_THR

```
#define ACCEL_WOM_Z_THR 0xa280
```

8.6.2.23 APEX_BUFFER_MGMT

```
#define APEX_BUFFER_MGMT 0x2b
```

8.6.2.24 DMP_EXT_SEN_ODR_CFG

```
#define DMP_EXT_SEN_ODR_CFG 0x27
```

8.6.2.25 DRIVE_CONFIG0

```
#define DRIVE_CONFIG0 0x32
```

8.6.2.26 DRIVE_CONFIG1

```
#define DRIVE_CONFIG1 0x33
```

8.6.2.27 DRIVE_CONFIG2

```
#define DRIVE_CONFIG2 0x34
```

8.6.2.28 EDMP_APEX_EN0

```
#define EDMP_APEX_EN0 0x29
```

8.6.2.29 EDMP_APEX_EN1

```
#define EDMP_APEX_EN1 0x2a
```

8.6.2.30 EDMP_PRGRM_IRQ0_0

```
#define EDMP_PRGRM_IRQ0_0 0xa24f
```

8.6.2.31 EDMP_PRGRM_IRQ0_1

```
#define EDMP_PRGRM_IRQ0_1 0xa250
```

8.6.2.32 EDMP_PRGRM_IRQ1_0

```
#define EDMP_PRGRM_IRQ1_0 0xa251
```

8.6.2.33 EDMP_PRGRM_IRQ1_1

```
#define EDMP_PRGRM_IRQ1_1 0xa252
```

8.6.2.34 EDMP_PRGRM_IRQ2_0

```
#define EDMP_PRGRM_IRQ2_0 0xa253
```

8.6.2.35 EDMP_PRGRM_IRQ2_1

```
#define EDMP_PRGRM_IRQ2_1 0xa254
```

8.6.2.36 EDMP_SP_START_ADDR

```
#define EDMP_SP_START_ADDR 0xa255
```

8.6.2.37 FIFO_CONFIG0

```
#define FIFO_CONFIG0 0x1d
```

8.6.2.38 FIFO_CONFIG1_0

```
#define FIFO_CONFIG1_0 0x1e
```

8.6.2.39 FIFO_CONFIG1_1

```
#define FIFO_CONFIG1_1 0x1f
```

8.6.2.40 FIFO_CONFIG2

```
#define FIFO_CONFIG2 0x20
```

8.6.2.41 FIFO_CONFIG3

```
#define FIFO_CONFIG3 0x21
```

8.6.2.42 FIFO_CONFIG4

```
#define FIFO_CONFIG4 0x22
```

8.6.2.43 FIFO_COUNT_0

```
#define FIFO_COUNT_0 0x12
```

8.6.2.44 FIFO_COUNT_1

```
#define FIFO_COUNT_1 0x13
```

8.6.2.45 FIFO_DATA

```
#define FIFO_DATA 0x14
```

8.6.2.46 FIFO_SRAM_SLEEP

```
#define FIFO_SRAM_SLEEP 0xa2a7
```

8.6.2.47 FS_SEL_AUX1

```
#define FS_SEL_AUX1 0x55
```

8.6.2.48 FS_SEL_AUX2

```
#define FS_SEL_AUX2 0x6f
```

8.6.2.49 FSYNC_CONFIG0

```
#define FSYNC_CONFIG0 0x24
```

8.6.2.50 FSYNC_CONFIG1

```
#define FSYNC_CONFIG1 0x25
```

8.6.2.51 GYRO_CONFIG0

```
#define GYRO_CONFIG0 0x1c
```

8.6.2.52 GYRO_DATA_X0_AUX1

```
#define GYRO_DATA_X0_AUX1 0x4b
```

8.6.2.53 GYRO_DATA_X0_AUX2

```
#define GYRO_DATA_X0_AUX2 0x65
```

8.6.2.54 GYRO_DATA_X0_UI

```
#define GYRO_DATA_X0_UI 0x07
```

8.6.2.55 GYRO_DATA_X1_AUX1

```
#define GYRO_DATA_X1_AUX1 0x4a
```

8.6.2.56 GYRO_DATA_X1_AUX2

```
#define GYRO_DATA_X1_AUX2 0x64
```

8.6.2.57 GYRO_DATA_X1_UI

```
#define GYRO_DATA_X1_UI 0x06
```

8.6.2.58 GYRO_DATA_Y0_AUX1

```
#define GYRO_DATA_Y0_AUX1 0x4d
```

8.6.2.59 GYRO_DATA_Y0_AUX2

```
#define GYRO_DATA_Y0_AUX2 0x67
```

8.6.2.60 GYRO_DATA_Y0_UI

```
#define GYRO_DATA_Y0_UI 0x09
```

8.6.2.61 GYRO_DATA_Y1_AUX1

```
#define GYRO_DATA_Y1_AUX1 0x4c
```

8.6.2.62 GYRO_DATA_Y1_AUX2

```
#define GYRO_DATA_Y1_AUX2 0x66
```

8.6.2.63 GYRO_DATA_Y1_UI

```
#define GYRO_DATA_Y1_UI 0x08
```

8.6.2.64 GYRO_DATA_Z0_AUX1

```
#define GYRO_DATA_Z0_AUX1 0x4f
```

8.6.2.65 GYRO_DATA_Z0_AUX2

```
#define GYRO_DATA_Z0_AUX2 0x69
```

8.6.2.66 GYRO_DATA_Z0_UI

```
#define GYRO_DATA_Z0_UI 0x0b
```

8.6.2.67 GYRO_DATA_Z1_AUX1

```
#define GYRO_DATA_Z1_AUX1 0x4e
```

8.6.2.68 GYRO_DATA_Z1_AUX2

```
#define GYRO_DATA_Z1_AUX2 0x68
```

8.6.2.69 GYRO_DATA_Z1_UI

```
#define GYRO_DATA_Z1_UI 0x0a
```

8.6.2.70 I2CM_COMMAND_0

```
#define I2CM_COMMAND_0 0xa206
```

8.6.2.71 I2CM_COMMAND_1

```
#define I2CM_COMMAND_1 0xa207
```

8.6.2.72 I2CM_COMMAND_2

```
#define I2CM_COMMAND_2 0xa208
```

8.6.2.73 I2CM_COMMAND_3

```
#define I2CM_COMMAND_3 0xa209
```

8.6.2.74 I2CM_CONTROL

```
#define I2CM_CONTROL 0xa216
```

8.6.2.75 I2CM_DEV_PROFILE0

```
#define I2CM_DEV_PROFILE0 0xa20e
```

8.6.2.76 I2CM_DEV_PROFILE1

```
#define I2CM_DEV_PROFILE1 0xa20f
```

8.6.2.77 I2CM_DEV_PROFILE2

```
#define I2CM_DEV_PROFILE2 0xa210
```

8.6.2.78 I2CM_DEV_PROFILE3

```
#define I2CM_DEV_PROFILE3 0xa211
```

8.6.2.79 I2CM_EXT_DEV_STATUS

```
#define I2CM_EXT_DEV_STATUS 0xa21a
```

8.6.2.80 I2CM_RD_DATA0

```
#define I2CM_RD_DATA0 0xa21b
```

8.6.2.81 I2CM_RD_DATA1

```
#define I2CM_RD_DATA1 0xa21c
```

8.6.2.82 I2CM_RD_DATA10

```
#define I2CM_RD_DATA10 0xa225
```

8.6.2.83 I2CM_RD_DATA11

```
#define I2CM_RD_DATA11 0xa226
```

8.6.2.84 I2CM_RD_DATA12

```
#define I2CM_RD_DATA12 0xa227
```

8.6.2.85 I2CM_RD_DATA13

```
#define I2CM_RD_DATA13 0xa228
```

8.6.2.86 I2CM_RD_DATA14

```
#define I2CM_RD_DATA14 0xa229
```

8.6.2.87 I2CM_RD_DATA15

```
#define I2CM_RD_DATA15 0xa22a
```

8.6.2.88 I2CM_RD_DATA16

```
#define I2CM_RD_DATA16 0xa22b
```

8.6.2.89 I2CM_RD_DATA17

```
#define I2CM_RD_DATA17 0xa22c
```

8.6.2.90 I2CM_RD_DATA18

```
#define I2CM_RD_DATA18 0xa22d
```

8.6.2.91 I2CM_RD_DATA19

```
#define I2CM_RD_DATA19 0xa22e
```

8.6.2.92 I2CM_RD_DATA2

```
#define I2CM_RD_DATA2 0xa21d
```

8.6.2.93 I2CM_RD_DATA20

```
#define I2CM_RD_DATA20 0xa22f
```

8.6.2.94 I2CM_RD_DATA3

```
#define I2CM_RD_DATA3 0xa21e
```

8.6.2.95 I2CM_RD_DATA4

```
#define I2CM_RD_DATA4 0xa21f
```

8.6.2.96 I2CM_RD_DATA5

```
#define I2CM_RD_DATA5 0xa220
```

8.6.2.97 I2CM_RD_DATA6

```
#define I2CM_RD_DATA6 0xa221
```

8.6.2.98 I2CM_RD_DATA7

```
#define I2CM_RD_DATA7 0xa222
```

8.6.2.99 I2CM_RD_DATA8

```
#define I2CM_RD_DATA8 0xa223
```

8.6.2.100 I2CM_RD_DATA9

```
#define I2CM_RD_DATA9 0xa224
```

8.6.2.101 I2CM_STATUS

```
#define I2CM_STATUS 0xa218
```

8.6.2.102 I2CM_WR_DATA0

```
#define I2CM_WR_DATA0 0xa233
```

8.6.2.103 I2CM_WR_DATA1

```
#define I2CM_WR_DATA1 0xa234
```

8.6.2.104 I2CM_WR_DATA2

```
#define I2CM_WR_DATA2 0xa235
```

8.6.2.105 I2CM_WR_DATA3

```
#define I2CM_WR_DATA3 0xa236
```

8.6.2.106 I2CM_WR_DATA4

```
#define I2CM_WR_DATA4 0xa237
```

8.6.2.107 I2CM_WR_DATA5

```
#define I2CM_WR_DATA5 0xa238
```

8.6.2.108 INT1_CONFIG0

```
#define INT1_CONFIG0 0x16
```

8.6.2.109 INT1_CONFIG1

```
#define INT1_CONFIG1 0x17
```

8.6.2.110 INT1_CONFIG2

```
#define INT1_CONFIG2 0x18
```

8.6.2.111 INT1_STATUS0

```
#define INT1_STATUS0 0x19
```

8.6.2.112 INT1_STATUS1

```
#define INT1_STATUS1 0x1a
```

8.6.2.113 INT2_CONFIG0

```
#define INT2_CONFIG0 0x56
```

8.6.2.114 INT2_CONFIG1

```
#define INT2_CONFIG1 0x57
```

8.6.2.115 INT2_CONFIG2

```
#define INT2_CONFIG2 0x58
```

8.6.2.116 INT2_STATUS0

```
#define INT2_STATUS0 0x59
```

8.6.2.117 INT2_STATUS1

```
#define INT2_STATUS1 0x5a
```

8.6.2.118 INT_APEX_CONFIG0

```
#define INT_APEX_CONFIG0 0x39
```

8.6.2.119 INT_APEX_CONFIG1

```
#define INT_APEX_CONFIG1 0x3a
```

8.6.2.120 INT_APEX_STATUS0

```
#define INT_APEX_STATUS0 0x3b
```

8.6.2.121 INT_APEX_STATUS1

```
#define INT_APEX_STATUS1 0x3c
```

8.6.2.122 INT_AUX2_CONFIG

```
#define INT_AUX2_CONFIG 0x70
```

8.6.2.123 INT_AUX2_STATUS

```
#define INT_AUX2_STATUS 0x71
```

8.6.2.124 INT_I2CM_SOURCE

```
#define INT_I2CM_SOURCE 0xa274
```

8.6.2.125 INT_PULSE_MIN_OFF_INTF0

```
#define INT_PULSE_MIN_OFF_INTF0 0xa26b
```

8.6.2.126 INT_PULSE_MIN_OFF_INTF1

```
#define INT_PULSE_MIN_OFF_INTF1 0xa26c
```

8.6.2.127 INT_PULSE_MIN_ON_INTF0

```
#define INT_PULSE_MIN_ON_INTF0 0xa269
```

8.6.2.128 INT_PULSE_MIN_ON_INTF1

```
#define INT_PULSE_MIN_ON_INTF1 0xa26a
```

8.6.2.129 INTF_AUX_CONFIG

```
#define INTF_AUX_CONFIG 0x2e
```

8.6.2.130 INTF_CONFIG0

```
#define INTF_CONFIG0 0x2c
```

8.6.2.131 INTF_CONFIG1_OVRD

```
#define INTF_CONFIG1_OVRD 0x2d
```

8.6.2.132 INTF_CONFIG_OVRD_AUX1

```
#define INTF_CONFIG_OVRD_AUX1 0x42
```

8.6.2.133 INTF_CONFIG_OVRD_AUX2

```
#define INTF_CONFIG_OVRD_AUX2 0x5c
```

8.6.2.134 IOC_PAD_SCENARIO

```
#define IOC_PAD_SCENARIO 0x2f
```

8.6.2.135 IOC_PAD_SCENARIO_AUX_OVRD

```
#define IOC_PAD_SCENARIO_AUX_OVRD 0x30
```

8.6.2.136 IOC_PAD_SCENARIO_OVRD

```
#define IOC_PAD_SCENARIO_OVRD 0x31
```

8.6.2.137 IPREG_BAR_REG_57

```
#define IPREG_BAR_REG_57 0xa039
```

8.6.2.138 IPREG_BAR_REG_58

```
#define IPREG_BAR_REG_58 0xa03a
```

8.6.2.139 IPREG_BAR_REG_59

```
#define IPREG_BAR_REG_59 0xa03b
```

8.6.2.140 IPREG_BAR_REG_60

```
#define IPREG_BAR_REG_60 0xa03c
```

8.6.2.141 IPREG_BAR_REG_61

```
#define IPREG_BAR_REG_61 0xa03d
```

8.6.2.142 IPREG_BAR_REG_62

```
#define IPREG_BAR_REG_62 0xa03e
```

8.6.2.143 IPREG_MISC

```
#define IPREG_MISC 0xa297
```

8.6.2.144 IPREG_SYS1_REG_166

```
#define IPREG_SYS1_REG_166 0xa4a6
```

8.6.2.145 IPREG_SYS1_REG_168

```
#define IPREG_SYS1_REG_168 0xa4a8
```

8.6.2.146 IPREG_SYS1_REG_170

```
#define IPREG_SYS1_REG_170 0xa4aa
```

8.6.2.147 IPREG_SYS1_REG_171

```
#define IPREG_SYS1_REG_171 0xa4ab
```

8.6.2.148 IPREG_SYS1_REG_172

```
#define IPREG_SYS1_REG_172 0xa4ac
```

8.6.2.149 IPREG_SYS1_REG_173

```
#define IPREG_SYS1_REG_173 0xa4ad
```

8.6.2.150 IPREG_SYS1_REG_42

```
#define IPREG_SYS1_REG_42 0xa42a
```

8.6.2.151 IPREG_SYS1_REG_43

```
#define IPREG_SYS1_REG_43 0xa42b
```

8.6.2.152 IPREG_SYS1_REG_56

```
#define IPREG_SYS1_REG_56 0xa438
```

8.6.2.153 IPREG_SYS1_REG_57

```
#define IPREG_SYS1_REG_57 0xa439
```

8.6.2.154 IPREG_SYS1_REG_70

```
#define IPREG_SYS1_REG_70 0xa446
```

8.6.2.155 IPREG_SYS1_REG_71

```
#define IPREG_SYS1_REG_71 0xa447
```

8.6.2.156 IPREG_SYS2_REG_123

```
#define IPREG_SYS2_REG_123 0xa57b
```

8.6.2.157 IPREG_SYS2_REG_129

```
#define IPREG_SYS2_REG_129 0xa581
```

8.6.2.158 IPREG_SYS2_REG_130

```
#define IPREG_SYS2_REG_130 0xa582
```

8.6.2.159 IPREG_SYS2_REG_131

```
#define IPREG_SYS2_REG_131 0xa583
```

8.6.2.160 IPREG_SYS2_REG_132

```
#define IPREG_SYS2_REG_132 0xa584
```

8.6.2.161 IPREG_SYS2_REG_24

```
#define IPREG_SYS2_REG_24 0xa518
```

8.6.2.162 IPREG_SYS2_REG_25

```
#define IPREG_SYS2_REG_25 0xa519
```

8.6.2.163 IPREG_SYS2_REG_32

```
#define IPREG_SYS2_REG_32 0xa520
```

8.6.2.164 IPREG_SYS2_REG_33

```
#define IPREG_SYS2_REG_33 0xa521
```

8.6.2.165 IPREG_SYS2_REG_40

```
#define IPREG_SYS2_REG_40 0xa528
```

8.6.2.166 IPREG_SYS2_REG_41

```
#define IPREG_SYS2_REG_41 0xa529
```

8.6.2.167 IREG_ADDR_15_8

```
#define IREG_ADDR_15_8 0x7c
```

8.6.2.168 IREG_ADDR_7_0

```
#define IREG_ADDR_7_0 0x7d
```

8.6.2.169 IREG_DATA

```
#define IREG_DATA 0x7e
```

8.6.2.170 ISR_0_7

```
#define ISR_0_7 0xa26e
```

8.6.2.171 ISR_16_23

```
#define ISR_16_23 0xa270
```

8.6.2.172 ISR_8_15

```
#define ISR_8_15 0xa26f
```

8.6.2.173 ODR_DECIMATE_CONFIG

```
#define ODR_DECIMATE_CONFIG 0x28
```

8.6.2.174 PWR_MGMT0

```
#define PWR_MGMT0 0x10
```

8.6.2.175 PWR_MGMT_AUX1

```
#define PWR_MGMT_AUX1 0x54
```

8.6.2.176 PWR_MGMT_AUX2

```
#define PWR_MGMT_AUX2 0x6e
```

8.6.2.177 REG_HOST_MSG

```
#define REG_HOST_MSG 0x73
```

8.6.2.178 REG_MISC1

```
#define REG_MISC1 0x35
```

8.6.2.179 REG_MISC2

```
#define REG_MISC2 0x7f
```

8.6.2.180 RTC_CONFIG

```
#define RTC_CONFIG 0x26
```

8.6.2.181 SELFTEST

```
#define SELFTEST 0xa290
```

8.6.2.182 SIFS_I3C_STC_CFG

```
#define SIFS_I3C_STC_CFG 0xa268
```

8.6.2.183 SIFS_IXC_ERROR_STATUS

```
#define SIFS_IXC_ERROR_STATUS 0xa24b
```

8.6.2.184 SMC_CONTROL_0

```
#define SMC_CONTROL_0 0xa258
```

8.6.2.185 SMC_CONTROL_1

```
#define SMC_CONTROL_1 0xa259
```

8.6.2.186 SREG_CTRL

```
#define SREG_CTRL 0xa267
```

8.6.2.187 STATUS_MASK_PIN_0_7

```
#define STATUS_MASK_PIN_0_7 0xa271
```

8.6.2.188 STATUS_MASK_PIN_16_23

```
#define STATUS_MASK_PIN_16_23 0xa273
```

8.6.2.189 STATUS_MASK_PIN_8_15

```
#define STATUS_MASK_PIN_8_15 0xa272
```

8.6.2.190 STC_CONFIG

```
#define STC_CONFIG 0xa263
```

8.6.2.191 SW_PLL1_TRIM

```
#define SW_PLL1_TRIM 0xa2a2
```

8.6.2.192 TEMP_DATA0_AUX1

```
#define TEMP_DATA0_AUX1 0x51
```

8.6.2.193 TEMP_DATA0_AUX2

```
#define TEMP_DATA0_AUX2 0x6b
```

8.6.2.194 TEMP_DATA0_UI

```
#define TEMP_DATA0_UI 0x0d
```

8.6.2.195 TEMP_DATA1_AUX1

```
#define TEMP_DATA1_AUX1 0x50
```

8.6.2.196 TEMP_DATA1_AUX2

```
#define TEMP_DATA1_AUX2 0x6a
```

8.6.2.197 TEMP_DATA1_UI

```
#define TEMP_DATA1_UI 0x0c
```

8.6.2.198 TMST_FSYNCH

```
#define TMST_FSYNCH 0x0e
```

8.6.2.199 TMST_FSYNCH_AUX1

```
#define TMST_FSYNCH_AUX1 0x52
```

8.6.2.200 TMST_FSYNCH_AUX2

```
#define TMST_FSYNCH_AUX2 0x6c
```

8.6.2.201 TMST_FSYNCL

```
#define TMST_FSYNCL 0x0f
```

8.6.2.202 TMST_FSYNCL_AUX1

```
#define TMST_FSYNCL_AUX1 0x53
```

8.6.2.203 TMST_FSYNCL_AUX2

```
#define TMST_FSYNCL_AUX2 0x6d
```

8.6.2.204 TMST_WOM_CONFIG

```
#define TMST_WOM_CONFIG 0x23
```

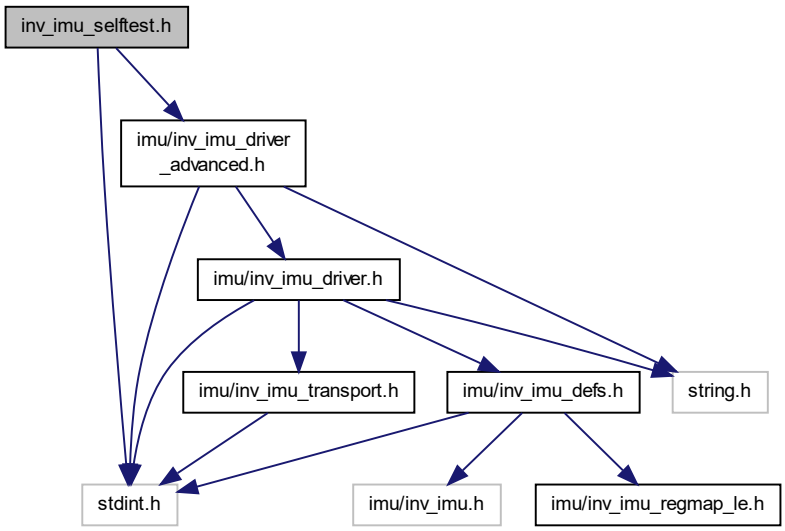
8.6.2.205 WHO_AM_I

```
#define WHO_AM_I 0x72
```

8.7 inv_imu_selftest.h File Reference

```
#include <stdint.h>
#include "imu/inv_imu_driver_advanced.h"
```

Include dependency graph for inv_imu_selftest.h:



Classes

- struct inv_imu_selftest_parameters_t

  Self-Test parameters.
- struct inv_imu_selftest_output_t

  Self-test outputs.

Macros

- #define INV_IMU_ST_STATUS_SUCCESS 1

  Indicates test is successful.
- #define INV_IMU_ST_STATUS_FAIL -1

  Indicates test is failing.
- #define INV_IMU_ST_STATUS_NOT_RUN 0

  Indicates test has not run.

Functions

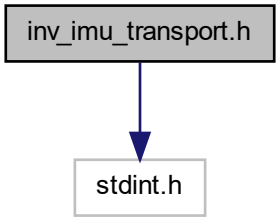
- int inv_imu_selftest_init_params (inv_imu_device_t *s, inv_imu_selftest_parameters_t *st_params)

  Provide recommended parameters to execute self-test.
- int inv_imu_selftest (inv_imu_device_t *s, const inv_imu_selftest_parameters_t *st_params, inv_imu_selftest_output_t *st_output)

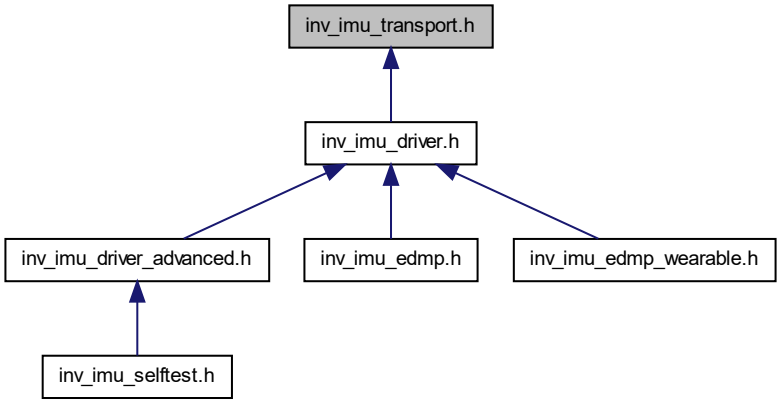
  Perform hardware self-test for Accel and/or Gyro.

8.8 inv_imu_transport.h File Reference

`#include <stdint.h>`
Include dependency graph for inv_imu_transport.h:



This graph shows which files directly or indirectly include this file:



Classes

- struct inv_imu_transport_t

  Structure dedicated to transport layer transport interface.

Macros

- #define UI_I2C 0

  identifies I2C interface.
- #define UI_SPI4 1

  identifies 4-wire SPI interface.
- #define UI_SPI3 2

  identifies 3-wire SPI interface.

Typedefs

- typedef int(∗ inv_imu_read_reg_t) (uint8_t reg, uint8_t ∗buf, uint32_t len)

  Function pointer to read register(s).
- typedef int(∗ inv_imu_write_reg_t) (uint8_t reg, const uint8_t ∗buf, uint32_t len)

  Function pointer to write register(s).
- typedef uint32_t inv_imu_serif_type_t

  Serif type definition.

Functions

- int inv_imu_read_reg (void ∗t, uint32_t reg, uint32_t len, uint8_t ∗buf)

  Reads data from a register on IMU.
- int inv_imu_write_reg (void ∗t, uint32_t reg, uint32_t len, const uint8_t ∗buf)

  Writes data to a register on IMU.
- int inv_imu_read_sram (void ∗t, uint32_t addr, uint32_t len, uint8_t ∗buf)

  Reads data from SRAM on IMU.
- int inv_imu_write_sram (void ∗t, uint32_t addr, uint32_t len, const uint8_t ∗buf)

  Writes data to SRAM on IMU.

8.9 mainpage.dox File Reference

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