SAM D11 Series Family Silicon Errata and Data Sheet Clarification

The SAM D11 Series family of devices that you have received conform functionally to the current Device Data Sheet (Atmel-42363H-SAM-D11-Datasheet_09/2016), except for the anomalies described in this document.

New Silicon Errata Issues

Note:	This document provides information on new errata issues for the SAM D11 Series of devices. Please refer to the current device data sheet for all pre-existing silicon errata issues.

1. Module: BOD12

On External Reset, the BOD12 reset cause can also be triggered.

Work around

Ignore BOD12 reset cause if External reset cause is set.

Affected Silicon Revisions

A	B						
X							

2. Module: SERCOM I^2C STATUS.CLKHOLD bit

The SERCOM I^2C STATUS.CLKHOLD bit can be written, whereas it is a read-only status bit in both Host and Client modes.

Work around

Do not clear the STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

A	B						
X	X						

3. Module: Device Standby Wakeup

Upon wakeup from standby with the Arm® Core register PRIMASK = 1, the first instruction fetched by the CPU in Flash memory will be the first instruction following the Wait For Interrupt (WFI) instruction. This instruction may be returned corrupted and lead to unpredictable behavior.

If PRIMASK = 0, the first instruction fetched by the CPU will be the first instruction of the interrupt handler. This one will be correctly returned to the CPU.

Work around

The following two possible workarounds can be used independently:

1. Disable Flash sleep in Standby Sleep mode (SLEEPPRM=DISABLED).
2. Place the standby sleep function in SRAM and make sure that at least one dummy Flash fetch is completed before exiting the function. This can be achieved by reading 2 data in memory, with addresses separated by at least the cache size. Because the first read could be a cache hit, the second one will be a cache miss and will generate a real read in memory.

The following code examples may be used:

```
__attribute__((noinline,
section(".ramfunc")))
void ram_sleep(void)
{
__DSB();
__WFI();
//
```

The following sequence ensures that the Flash is ready before returning from the RAM code:

```
#define CACHE_SIZE_IN_BYTES 64
((volatile unsigned int
*)FLASH_ADDR)[CACHE_SIZE_IN_BYTES/
sizeof(unsigned int)];
//will read a word at FLASH_ADDR +
0x40 in this case
```

```
((volatile        unsigned        int
*)FLASH_ADDR)[(CACHE_SIZE_IN_BYTES*2
)/sizeof(unsigned int)];
//will read a word at FLASH_ADDR +
0x80 in this case
}
```

Affected Silicon Revisions

A	B						
X	X						

Data Sheet Clarifications

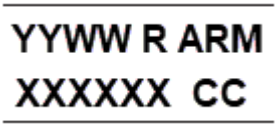
The following typographic corrections and clarifications are to be noted for the latest version of the Device Data Sheet (Atmel-42363H-SAM-D11-Datasheet_09/2016).

Note: Corrections in tables and paragraphs are shown in **BOLD.** Where possible, the original bold text formatting has been removed for clarity.

1. Module: Package Marking Information

In the current device data sheet, the SAM D11 Package Marking Information is missing. The information is as follows:

All devices are marked with the Atmel logo, a shortened ordering code and additional marking (the two last lines).



Where:

- "Y" or "YY": Manufacturing Year (last OR two last digit(s))
- "WW": Manufacturing Week
- "R": Revision
- "XXXXXX": Lot number
- "CC": Internal Code

2. Module: OSC32K and XOSC32K EN1K bit

The OSC32K and XOSC32K EN1K bits and the associated 1.024 kHz clock outputs are referenced several times in the device data sheet. The OSC32K and XOSC32K EN1K bits and the associated 1.024 kHz clock outputs are not implemented for this device.

3. Module: OSCULP32K Characteristics

The value for the minimum output frequency is incorrect. The corrected information is shown in **BOLD** below:

TABLE 35-45: ULTRA LOW POWER INTERNAL 32KHZ RC OSCILLATOR CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{OUT}	Output frequency	Calibrated against a 32.768 kHz reference at 25°C, over [-40, +85]C, over [1.62, 3.63]V	27.8	32.768	37.8	kHz
		Calibrated against a 32.768 kHz reference at 25°C, at V_{DD}=3.3V	**32.5**	32.768	32.8	
		Calibrated against a 32.768 kHz reference at 25°C, over [1.62, 3.63]V	31.9	32.768	33.1	
Duty	Duty Cycle			50		%

4. Module: Brown-Out Detectors (BOD) Characteristics

Figures 35-2, 35-3, 35-4, 40-2, 40-3, and 40-4 have an incorrect reset Polarity value. The corrected figures are as shown below:

FIGURE 35-2 and 40-2: POR OPERATING PRINCIPLE:

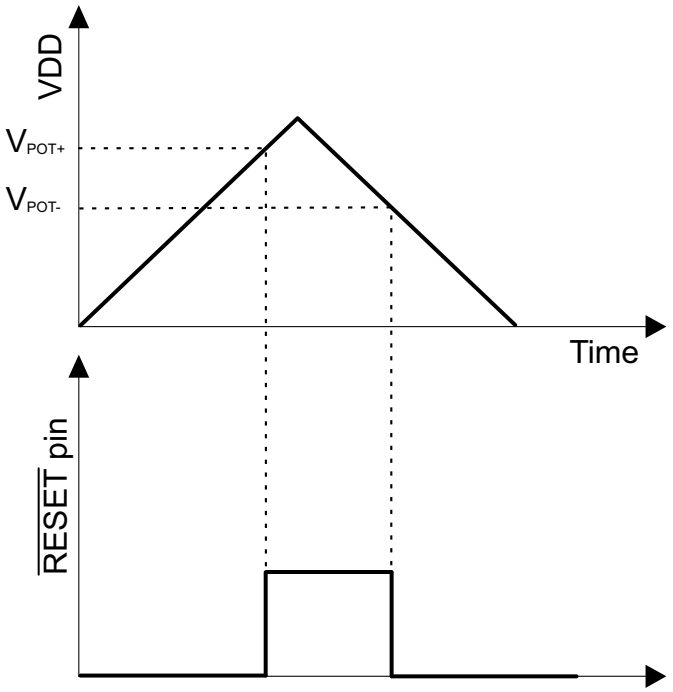


FIGURE 35-3 AND 40-3: BOD33 HYSTERESIS OFF

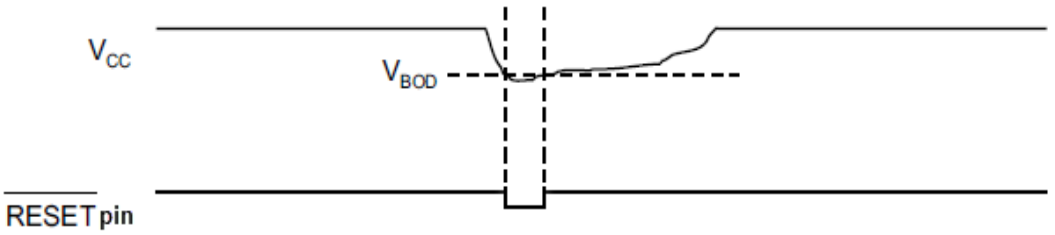
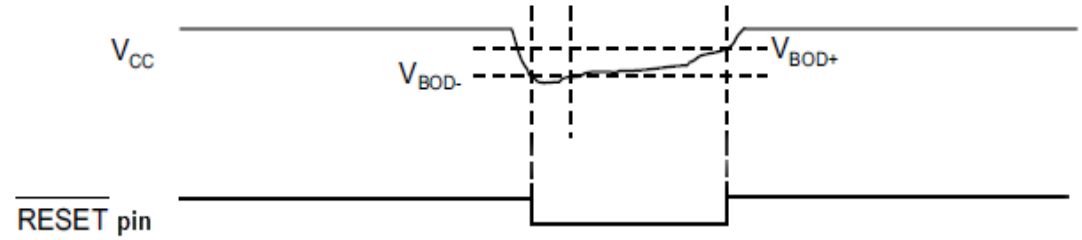


FIGURE 35-4 AND 40-4: BOD33 LEVEL VALUE



5. Module: ADC Power Management

Section 31.5.2 has new information added, and is shown in **BOLD** below:

The ADC will continue to operate in any sleep modes where the selected source clock is running. The ADC's interrupts can be used to wake up the device from sleep modes (**Except the OVERRUN interrupt)**. The events can trigger other operations in the system without exiting the sleep modes. Refer to "PM – Power Manager" on page 110 for details on the different sleep modes.

Section 31.6.12 has new information added, and is shown in **BOLD** below:

When RUNSTDBY is one, any enabled ADC interrupt source can wake up the CPU **(except the OVERRUN interrupt)**. While the CPU is sleeping, ADC conversion can only be triggered by events.

6. Module: EVSYS USER Register Summary

The USER register is displayed incorrectly in the Register Summary. The correct USER register summary section is displayed as follows:

0x0120	USER0	7:0					CHANNEL[3:0]				
...											
0x0136	USER22	7:0					CHANNEL [3:0]				

7. Module: EVSYS Principle of Operation

Section 23.6.1 has incorrect information in the second part, the corrected information is shown in **BOLD**.

The EVSYS allows for communication between peripherals through events. Peripherals that respond to events (event users) are connected to multiplexers which have all event channels as input. **Each peripheral emitting events (Event Generator) can be connected to one or multiple event users, using one or multiple channels of the Event System.**

8. Module: NVMCTRL - CTRLA Register

Table 21-6 for the Command bit displays Write Lock bits as a feature. The Write Lock bits are not supported on this device.

9. Module: NVMCTRL - NVM User Configuration

Tables 21-2 and 21-3 show incorrect values on the last row of each table. These values are not possible per the device memory density.

10. Module: RTC - Overview

The overview section for the RTC had a new verbiage, which has been highlighted in **BOLD**.

The Real-Time Counter (RTC) is a 32-bit counter with a 10-bit programmable prescaler that typically runs continuously to keep track of time. The RTC can wake up the device from sleep modes using the alarm/compare wake up, periodic wake up or overflow wake up mechanisms.

The RTC is clocked by any clock sources selectable through the Generic Clock module (GCLK), providing the signal GCLK_RTC.

The RTC can generate periodic peripheral events from outputs of the prescaler, as well as alarm/compare interrupts and peripheral events, which can trigger at any counter value. Additionally, the timer can trigger an overflow interrupt and peripheral event, and be reset on the occurrence of an alarm/compare match. This allows periodic interrupts and peripheral events at very long and accurate intervals.

The 10-bit programmable prescaler can scale down the clock source, hence a wide range of resolutions and time-out periods can be configured. With a 32.768 kHz clock source, the minimum counter tick interval is 30.5 µs, and time-out periods can range up to 36 hours. With the counter tick interval configured to 1s, the maximum time-out period is more than 136 years.

11. Module: SYSCTRL - XOSC Register

The register description for the GAIN bit has been updated. The newly added text is shown in **BOLD**.

These bits select the gain for the oscillator. The listed maximum frequencies are recommendations, and might vary based on capacitive load and crystal characteristics. **These bits must be configured even when the Automatic Amplitude Gain Control is active.**

12. Module: SYSCTRL - XOSC Register

The AMPGC bit has been updated with a new note, as shown below in **BOLD**.

Note: The configuration of the oscillator gain is mandatory even if AMPGC feature is enabled at startup.

13. Module: Debug Operation - DCFGn Register

The register is erroneously listed as Read-Write. This register is Read Only.

14. Module: USB - STATUS.SPEED

The USB STATUS.SPEED bit field description in table 30-9 is wrong. The correct description is given below:

SPEED[1:0]	SPEED STATUS
0x0	**Full-speed mode**
0x1	**Low-speed mode**
0x2	Reserved
0x3	Reserved

15. Module: SERCOM I^2C INTFLAG.DRDY bit

The description of the SERCOM I^2C INTFLAG.DRDY bit is not complete. The **BOLD** part below must be added:

This flag is set when a I^2C client byte transmission **or reception** is successfully completed.

16. Module: NVMCTRL AUX1 Device Configuration Register

Contrary to what is stated in the data sheet, the DCFG0/1 registers located in the AUX1 Area 2 are internal **read-only** registers and must not be written.

17. Module: DMAC SRCADDR and DSTADDR Registers' Descriptions

The description for the DMAC SRCADDR register is replaced by the following:

Bits 31:0 – SRCADDR[31:0] Transfer Source Address
This bit field holds the block transfer source address.
When source address incrementation is disabled (BTCTRL.SRCINC=0), SRCADDR corresponds to the last beat transfer address in the block transfer.
When source address incrementation is enabled (BTCTRL.SRCINC=1), SRCADDR is calculated as follows:
If BTCTRL.STEPSEL=1:

$$SRCADDR = SRCADDR_{START} + BTCNT \cdot \left(BEATSIZE + 1\right) \cdot 2^{STEPSIZE}$$

If BTCTRL.STEPSEL=0:

$$SRCADDR = SRCADDR_{START} + BTCNT \cdot (BEATSIZE + 1)$$

- $SRCADDR_{START}$ is the source address of the first beat transfer in the block transfer
- BTCNT is the initial number of beats remaining in the block transfer
- BEATSIZE is the configured number of bytes in a beat
- STEPSIZE is the configured number of beats for each incrementation

The description for the DMAC DSTADDR register is replaced by the following:

Bits 31:0 – DSTADDR[31:0] Transfer Destination Address
This bit field holds the block transfer destination address.
When destination address incrementation is disabled (BTCTRL.DSTINC=0), DSTADDR corresponds to the last beat transfer address in the block transfer.
When destination address incrementation is enabled (BTCTRL.DSTINC=1), DSTADDR is calculated as follows:
If BTCTRL.STEPSEL=1:

$$DSTADDR = DSTADDR_{START} + BTCNT \bullet (BEATSIZE + 1)$$

If BTCTRL.STEPSEL=0:

$$DSTADDR = DSTADDR_{START} + BTCNT \bullet \left(BEATSIZE + 1\right) \bullet 2^{STEPSIZE}$$

- $DSTADDR_{START}$ is the destination address of the first beat transfer in the block transfer
- BTCNT is the initial number of beats remaining in the block transfer
- BEATSIZE is the configured number of bytes in a beat
- STEPSIZE is the configured number of beats for each incrementation

18. Module: RTC and TC READREQ.RCONT bit fields

A note is added to the RTC and TC READREQ.RCONT bit fields descriptions:

For the RTC:

Note: Once the continuous synchronization is enabled, the first write in the COUNT/CLOCK register will be stalled for a maximum of 6 APB + 6 RTC clock cycles (the time for the on-going read synchronization to complete).

For the TC:

Note: Once the continuous synchronization is enabled, the first write in the COUNT/CCx register will be stalled for a maximum of 6 APB + 6 TC clock cycles (the time for the on-going read synchronization to complete).

19. Module: DMAC BASEADDR, WRBADDR and DESCADDR registers alignment

The description for the 3 DMAC BASEADDR, WRBADDR and DESCADDR registers erroneously states that these registers must be 128-bit aligned. These registers must actually be **64-bit aligned.**

20. Module: DAC Maximum Input Clock Frequency

The Electrical Characteristics table 35-6 erroneously defines the DAC maximum input clock as 350 kHz. This value is corrected to 48 MHz.

21. Module: DAC Start Conversion Event

A note has been added to the start conversion paragraph in chapter 33.6.4.3:

Note: When a DAC Start Conversion event is enabled, only DATABUF must be written (not DATA).

The description of the EVTCTRL.STARTEI bit has been updated to:

0: A new conversion will not be triggered on an incoming event. **Only DATA must be written (not DATABUF).**

1: A new conversion will be triggered on an incoming event. **Only DATABUF must be written (not DATA).**

22. Module: DAC Electrical Characteristics

The conversion rate of 350 ksps mentioned in Note 1 for the DAC Accuracy Characteristics tables 35-28 and 40-26 is incorrect. All values have been measured using a conversion rate of 35 ksps.

23. Module: ADC Electrical Characteristics at 85°C

The table 35-21 Operating Conditions is corrected as shown in **BOLD** as follows:

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
RES	Resolution	-	8	-	12	bits
F_{CLK_ADC}	ADC Clock frequency	-	30	-	2100	kHz
	Sample rate(1)	Single shot	5	-	300	ksps
		Free running	5	-	350(3)	
	Sampling time(1)	-	**250**	-	-	**ns**
	Sampling time with DAC as input(2)	-	**3**	-	-	**µs**
	Sampling time with Temp sens as input(2)	-	**10**	-	-	**µs**
	Sampling time with Bandgap as input(2)	-	**10**	-	-	**µs**
	Conversion time(1)	1x Gain	6	-	-	cycles
^{V}REF	Voltage reference range	-	1.0	-	V_{DDANA}-0.6	V
INT1V	Internal 1V reference (2, **4**)	-	-	1.0	-	V
INTVCC0	Internal ratiometric reference 0(2)	-	-	V_{DDANA}/1.48	-	V
INTVCC0 Voltage Error	Internal ratiometric reference 0(2) error	2.0V<V_{DDANA}<3.063 V	-1	-	1	%
INTVCC1	Internal ratiometric reference 1(2)	V_{DDANA}>2.0V	-	V_{DDANA}/2	-	V
INTVCC1 Voltage Error	Internal ratiometric reference 1(2) error	2.0V<V_{DDANA}<3.063 V	-1	-	1	%
	Conversion range(1)	Differential mode	-V_{REF}/GAIN	-	+V_{REF}/GAIN	V
		Single-ended mode	0.0	-	+V_{REF}/GAIN	V
C_{SAMPLE}	Sampling capacitance(2)	-	-	3.5	-	pF
R_{SAMPLE}	Input channel source resistance(2)	-	-	-	3.5	kΩ
I_{DD}	DC supply current(1)	f_{CLK_ADC} = 2.1MHzl(3)	-	3.8	4.5	mA

Note 1: These values are based on characterization. These values are not covered by test limits in production.

2: These values are based on simulation. These values are not covered by test limits in production or characterization.

3: In this condition and for a sample rate of 350ksps, a conversion takes 6 clock cycles of the ADC clock (conditions: 1X gain, 12-bit resolution, differential mode, free-running).

4: It is the buffered internal reference of 1.0V derived from the internal 1.1V bandgap reference.

Table 35-22 Differential Mode is corrected as shown in **BOLD** as follows:

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ENOB	Effective Number Of Bits	With gain compensation	-	10.5	10.7	bits
TUE	Total Unadjusted Error	1x Gain	3.1	4.3	20	LSB
INLI	Integral Non Linearity	1x Gain	1.0	1.3	6.3	LSB
DNL	Differential Non Linearity	1x Gain	+/-0.3	+/-0.5	+/-0.98	LSB
GE	Gain Error	Ext. Ref 1x	-25.0	2.5	+25.0	mV
		$V_{REF} = V_{DDANA}/1.48$	-30.0	-1.5	+30.0	mV
		VREF = INT1V	-15.0	-5.0	+10.0	mV
	Gain Accuracy(4)	Ext. Ref. 0.5x	+/-0.04	+/-0.2	+/-1.5	%
		Ext. Ref. 2x to 16x	+/-0.1	+/-0.4	+/-2.0	%
OE	Offset Error	Ext. Ref. 1x	-10.0	-1.5	+10.0	mV
		$V_{REF} = V_{DDANA}/1.48$	-10.0	0.5	+10.0	mV
		VREF = INT1V	-10.0	3.0	+10.0	mV
SFDR	Spurious Free Dynamic Range	1x Gain F_{CLK_ADC} = 2.1 MHz F_{IN} = 40 kHz A_{IN} = 95% FSR	62.7	70.4	75.8	dB
SINAD	Signal-to-Noise and Distortion		54.1	61.4	62.7	dB
SNR	Signal-to-Noise Ratio		54.5	63.6	65.6	dB
THD	Total Harmonic Distortion		-74	-70.2	-63	dB
	Noise RMS	T = 25°C	0.6	1.0	2	mV

Note 1: Maximum numbers are based on characterization and not tested in production, and valid for 5% to 95% of the input voltage range.

2: Dynamic parameter numbers are based on characterization and not tested in production.

3: Respect the input common mode voltage through the following equations (where VCM_IN is the Input channel common mode voltage):

- If $|V_{IN}| > V_{REF}/4$
  - $V_{CM\_IN} < 0.95*V_{DDANA} + V_{REF}/4 - 0.75V$
  - $V_{CM\_IN} > V_{REF}/4 - 0.05*V_{DDANA} - 0.1V$
- If $|V_{IN}| < V_{REF}/4$
  - $V_{CM\_IN} < 1.2*V_{DDANA} - 0.75V$
  - $V_{CM\_IN} > 0.2*V_{DDANA} - 0.1V$

4: The gain accuracy represents the gain error expressed in percent. Gain accuracy (%) = (Gain Error in V x 100) / (2*Vref/GAIN)

24. Module: Bandgap Electrical Characteristics at 85°C

The “Bandgap Reference Characteristics” chapter and its table 35-30 “Internal 1.1V Bandgap Reference Characteristics" are both renamed to "**Bandgap and Internal 1.0V Reference Characteristics**".

Table 35-30 is updated as follows with corrections in **BOLD**:

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Bandgap	Internal 1.1V Bandgap reference	Over voltage and [-40°C, +85°C]	1.08	1.10	1.12	V
		Over voltage at 25°C	1.07	1.10	1.11	
INT1V	**Internal 1.0V reference voltage (1)**	**Over voltage and [-40°C, +85°C]**	**0.98**	**1.00**	**1.02**	
		Over voltage at 25°C	**0.97**	**1.00**	**1.01**	
Note 1: These values are simulation based and are not covered by production test limits.						

25. Module: ADC Electrical Characteristics at 105°C

Table 40-19 Operating Conditions is corrected as shown in **BOLD** as follows:

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
RES	Resolution		8	-	12	bits
F_{CLK_ADC}	ADC Clock frequency		30	-	2100	kHz
	Sample rate(1)	Single shot	5	-	300	ksps
		Free running	5	-	350(3)	
	Sampling time(1)		**250**	-	-	**ns**
	Sampling time with DAC as input(2)		**3**			**µs**
	Sampling time with Temp sens as input(2))		**10**			**µs**
	Sampling time with Bandgap as input(2))		**10**			**µs**
	Conversion time(1)	1x Gain	6	-	-	cycles
V_{DDANA}	Power supply voltage	T > 85°C	2.7		3.6	V
V_{REF}	Voltage reference range		1.0	-	V_{DDANA}-0.6	V
INT1V	Internal 1V reference (2, 4)		-	1.0	-	V
INTVCC0	Internal ratiometric reference 0(2)		-	V_{DDANA}/1.48	-	V
INTVCC0 Voltage Error	Internal ratiometric reference 0(2) error	2.0V<V_{DDANA}<3.063 V	-1	-	1	%
INTVCC1	Internal ratiometric reference 1(2)	V_{DDANA}>2.0V	-	V_{DDANA}/2	-	V
INTVCC1 Voltage Error	Internal ratiometric reference 1(2) error	2.0V<V_{DDANA}<3.063 V	-1	-	1	%
	Conversion range(1)	Differential mode	-V_{REF}/GAIN	-	+V_{REF}/GAIN	V
		Single-ended mode	0.0	-	+V_{REF}/GAIN	V
C_{SAMPLE}	Sampling capacitance(2)		-	3.5	-	pF
R_{SAMPLE}	Input channel source resistance(2)		-	-	3.5	kΩ
I_{DD}	DC supply current(1)	f_{CLK_ADC} = 2.1 MHzl(3)	-	3.8	4.5	mA

Note 1: These values are based on characterization. These values are not covered by test limits in production.

2: These values are based on simulation. These values are not covered by test limits in production or characterization.

3: In this condition and for a sample rate of 350ksps, a conversion takes 6 clock cycles of the ADC clock (conditions: 1X gain, 12-bit resolution, differential mode, free-running).

4: It is the buffered internal reference of 1.0V derived from the internal 1.1V bandgap reference.

Table 40-20 Differential Mode is corrected as shown in **BOLD** as follows:

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ENOB	Effective Number Of Bits	With gain compensation	-	10.0	10.4	bits
TUE	Total Unadjusted Error	1x Gain	3.1	4.3	16	LSB
INLI	Integral Non Linearity	1x Gain	1.0	1.3	5.0	LSB
DNL	Differential Non Linearity	1x Gain	+/-0.3	+/-0.5	+/-0.98	LSB
GE	Gain Error	Ext. Ref 1x	-25.0	2.5	+25.0	mV
		$V_{REF} = V_{DDANA}/1.48$	-30.0	-1.5	+30.0	mV
		VREF = INT1V	-15.0	-5.0	+10.0	mV
	Gain Accuracy(4)	Ext. Ref. 0.5x	+/-0.04	+/-0.2	+/-1.0	%
		Ext. Ref. 2x to 16x	+/-0.1	+/-0.4	+/-1.5	%
OE	Offset Error	Ext. Ref. 1x	-10.0	-1.5	+10.0	mV
		$V_{REF}=V_{DDANA}/1.48$	-10.0	0.5	+10.0	mV
		VREF = INT1V	-10.0	3.0	+10.0	mV
SFDR	Spurious Free Dynamic Range	1x Gain F_{CLK_ADC} = 2.1 MHz F_{IN} = 40 kHz A_{IN} = 95% FSR	63.0	70.4	74.8	dB
SINAD	Signal-to-Noise and Distortion		57.0	61.4	64.3	dB
SNR	Signal-to-Noise Ratio		57.9	63.6	65.5	dB
THD	Total Harmonic Distortion		-74.5	-70.2	-64.5	dB
	Noise RMS	T = 25°C	0.6	1.0	2	mV

Note 1: Maximum numbers are based on characterization and not tested in production, and valid for 5% to 95% of the input voltage range.

2: Dynamic parameter numbers are based on characterization and not tested in production.

3: Respect the input common mode voltage through the following equations (where VCM_IN is the Input channel common mode voltage):

- If $|V_{IN}| > V_{REF}/4$
  - $V_{CM\_IN} < 0.95*V_{DDANA} + V_{REF}/4 - 0.75V$
  - $V_{CM\_IN} > V_{REF}/4 - 0.05*V_{DDANA} - 0.1V$
- If $|V_{IN}| < V_{REF}/4$
  - $V_{CM\_IN} < 1.2*V_{DDANA} - 0.75V$
  - $V_{CM\_IN} > 0.2*V_{DDANA} - 0.1V$

4: The ADC channels on pins PA08, PA09, PA10, PA11 are powered from the VDDIO power supply. The ADC performance of these pins will not be the same as all the other ADC channels on pins powered from the VDDANA power supply..

5: The gain accuracy represents the gain error expressed in percent. Gain accuracy (%) = (Gain Error in V x 100) / (2*Vref/GAIN).

26. Module: Bandgap Electrical Characteristics at 105°C

The “Bandgap Reference Characteristics” chapter and its table 40-28 “Internal 1.1V Bandgap Reference Characteristics" are both renamed to "**Bandgap and Internal 1.0V Reference Characteristics**". The table 40-28 is updated as follows with corrections in **BOLD**:

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Bandgap	Internal 1.1V Bandgap reference	Over voltage and [-40°C, +105°C]	1.08	1.10	1.12	V
		Over voltage at 25°C	1.07	1.10	1.11	
INT1V	**Internal 1.0V reference voltage (1)**	**Over voltage and [-40°C, +85°C]**	**0.98**	**1.00**	**1.02**	
		Over voltage at 25°C	**0.97**	**1.00**	**1.01**	
Note 1: These values are simulation based and are not covered by production test limits.						

APPENDIX A: REVISION HISTORY

Revision A Document (07/2019)

This is the initial released version of this document.

Revision B Document (03/2021)

This revision includes numerous typographical updates, along with the following new information:

The I^2C standard uses the terminology "master" and "slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively.

The following Errata were added:

- **2. Module: “SERCOM I^2C STATUS.CLKHOLD bit”**
- **3. Module: “Device Standby Wakeup”**

Updated the following Data Sheet Clarifications with new images and descriptions:

- **2. Module: “OSC32K and XOSC32K EN1K bit”**
- **4. Module: “Brown-Out Detectors (BOD) Characteristics”**
- **5. Module: “ADC Power Management”**
- **9. Module: “NVMCTRL - NVM User Configuration”**
- **11. Module: “SYSCTRL - XOSC Register”**

The following Data Sheet Clarifications were added:

- **14. Module: “USB - STATUS.SPEED”**
- **15. Module: “SERCOM I^2C INTFLAG.DRDY bit”**
- **16. Module: “NVMCTRL AUX1 Device Configuration Register”**
- **17. Module: “DMAC SRCADDR and DSTADDR Registers' Descriptions”**
- **18. Module: “RTC and TC READREQ.RCONT bit fields”**
- **19. Module: “DMAC BASEADDR, WRBADDR and DESCADDR registers alignment”**
- **20. Module: “DAC Maximum Input Clock Frequency”**
- **21. Module: “DAC Start Conversion Event”**
- **22. Module: “DAC Electrical Characteristics”**
- **23. Module: “ADC Electrical Characteristics at 85°C”**
- **24. Module: “Bandgap Electrical Characteristics at 85°C”**
- **25. Module: “ADC Electrical Characteristics at 105°C”**
- **26. Module: “Bandgap Electrical Characteristics at 105°C”**

The following Data Sheet Clarifications were removed:

- Module: 32 kHz Ultra-Low Power Internal Oscillator (OSCULP32K) Operation

NOTES:

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