Xcelium Tutorial

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Before going to next steps, please note that those lines that start with '#' are explanation, lines that follow with '$' are commands and you need to copy and then paste in your terminal and press enter.

0. Log in Wilkinson Lab

This tutorial should be run on a Wilkinson lab machine. For remote access, we recommend using the FastX remote desktop through a browser. Please refer to the instructions at http://it.eecs.northwestern.edu/info/2020/09/14/info-labs-fastx.html.

You may also log in through other methods that support graphical applications.

1. RTL simulation

In this part, you only need the verilog code (RTL) "alu_conv.v" and its testbench "alu_conv_test.v"

1) # Create a directory for the assignment. In this tutorial we call that directory Lab1.
Go into the directory "Lab1" and copy all Verilog files (in this case alu_conv.v and alu_conv_test.v) from the class folder located at **/vol/ece303/genus_tutorial** into Lab1.

```
$ cd ./Lab1
$ cp /vol/ece303/genus_tutorial/alu_conv.v .
$ cp /vol/ece303/genus_tutorial/alu_conv_test.v .
```

Lab1 folder should contain: alu_conv.v , alu_conv_test.v. You could type "ls" to see files in the directory.

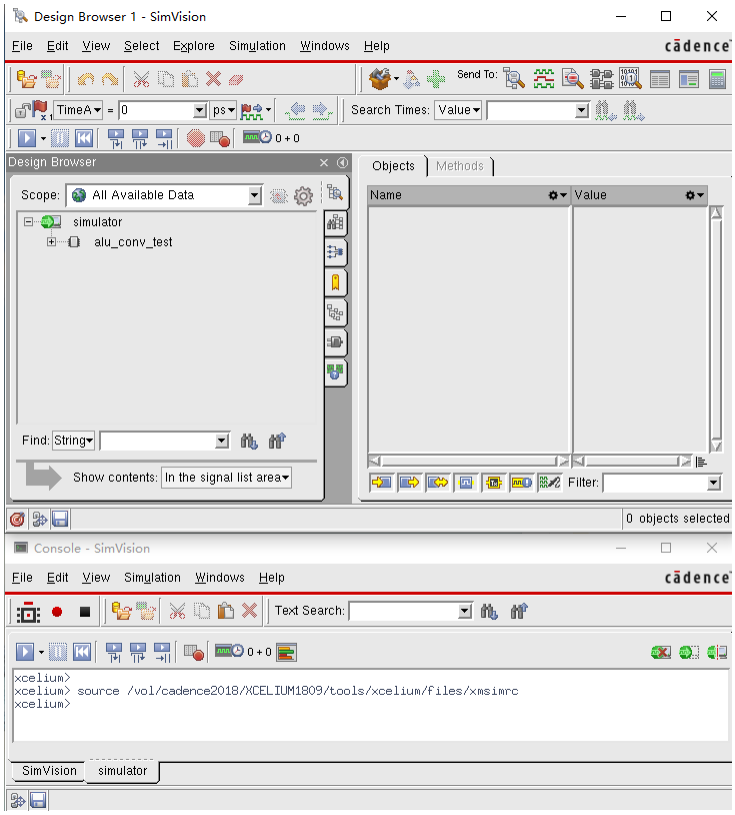
2) # Enter the following commands to source the cadence environment

```
$ source /vol/ece303/genus_tutorial/cadence.env
```

```
[qcb2982@ras ~/Lab1]$ source /vol/ece303/genus_tutorial/cadence.env
```

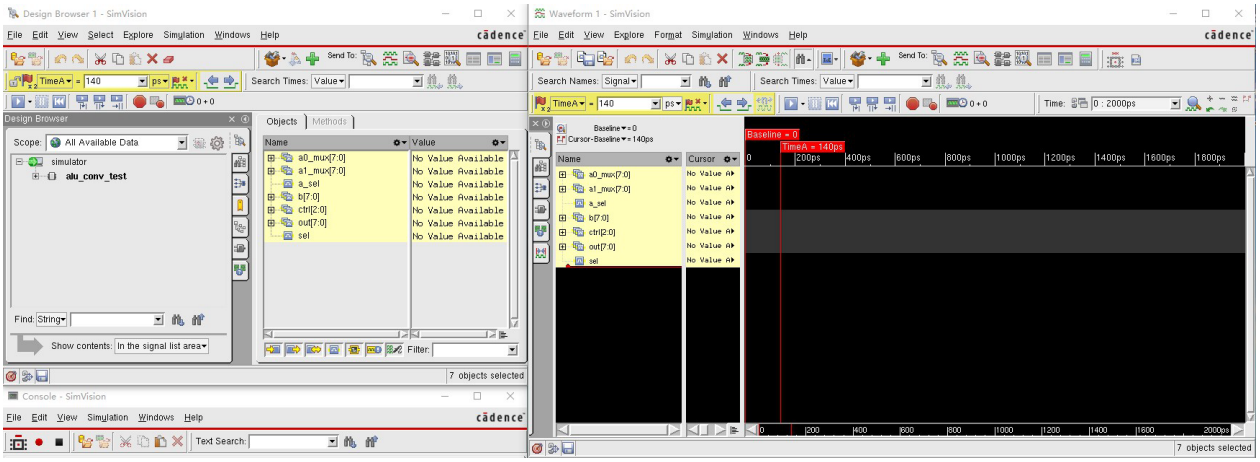
3) # Type the following command to run the cadence tool. In this case you will see a new open window like this:

```
$ xrun -64bit -gui -access r alu_conv.v alu_conv_test.v
```



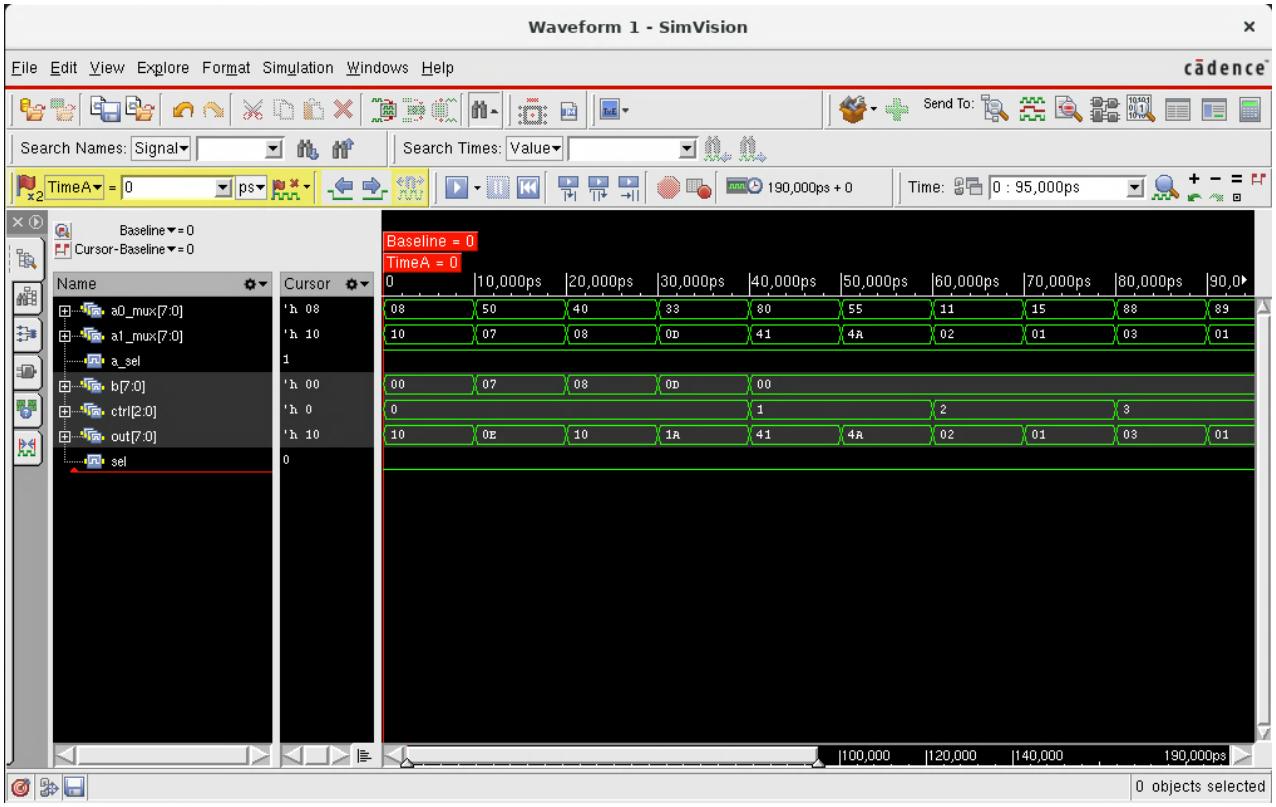
Important: the terminal should show no error, or the new window will not pop-up.

4) # In this window you can select the signal you want to send to the **Waveform Window** (right click a signal -> Send to Waveform Window)



5) # In the Waveform SimVison window you can simulate your design. Simulation->Run.

Note: You need to use zoom in/out function to pick the expected observation time period.



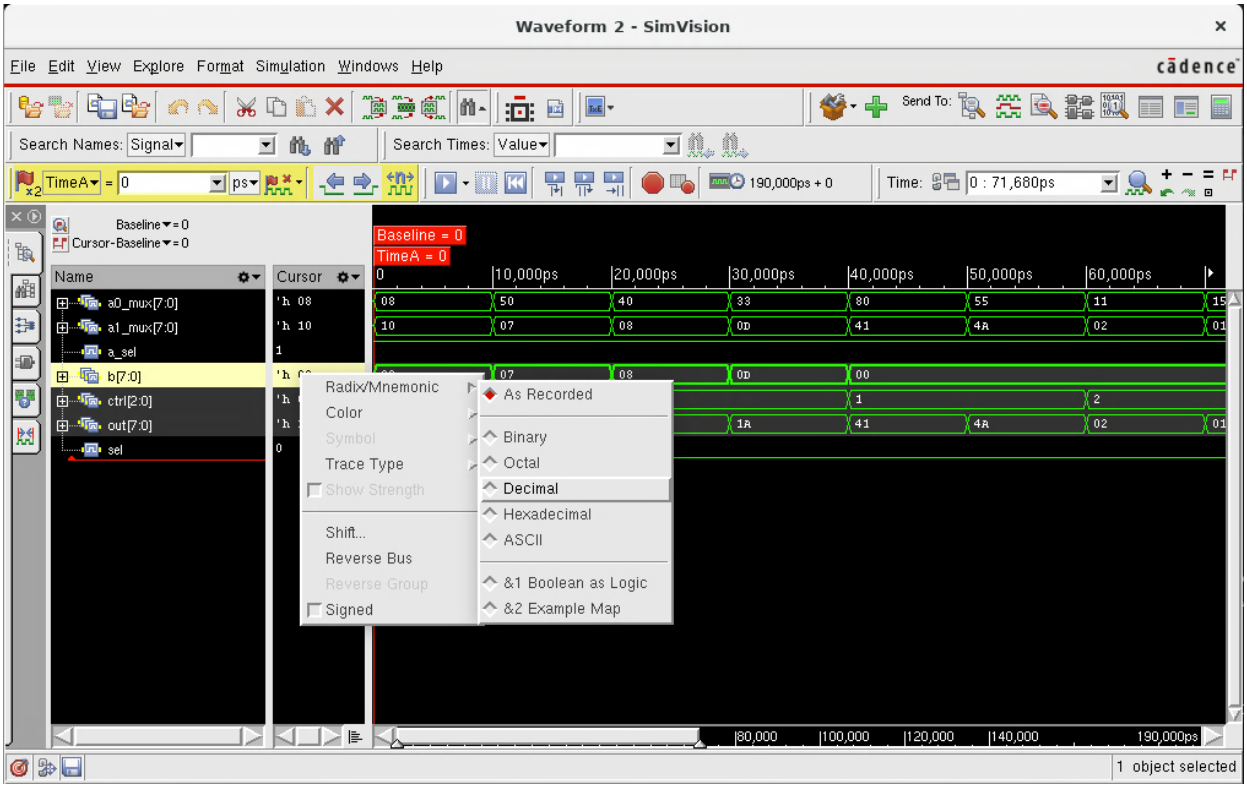
Important: if you see error bellow, click “Reset the simulation back to time 0”. Then run simulation again.

```
Simulation complete via $finish(1) at time 290 NS + 0
./alu_conv_test.v:233                #20 $finish;\r
xcelium> run
xmsim: *E,RNFNSH: Cannot continue simulation due to a previous $finish.
xcelium>
```

6) # Verify the result of RTL code

Based on the observation, you can confirm whether the function is correct of your RTL code.

Right click column of Cursor to change value from Hex to Decimal or Binary, so that you can check whether the result is correct.


Waveform 2 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Search Names: Signal
Search Times: Value
TimeA = 0 ps
Time: 0 : 71,680ps
Baseline = 0
Cursor-Baseline = 0
Name
Cursor
a0_mux[7:0]
a1_mux[7:0]
a_sel
b[7:0]
ctrl[2:0]
out[7:0]
sel
Baseline = 0
TimeA = 0
10,000ps
20,000ps
30,000ps
40,000ps
50,000ps
60,000ps
Radix/Mnemonic
Color
Symbol
Trace Type
Show Strength
Shift...
Reverse Bus
Reverse Group
Signed
As Recorded
Binary
Octal
Decimal
Hexadecimal
ASCII
&1 Boolean as Logic
&2 Example Map
80,000
100,000
120,000
140,000
190,000ps
1 object selected