Problem 1:
Module:

```
`timescale 1ps/1ps

module p1(A0,A1,EN,Y0,Y1,Y2,Y3);
  input A0,A1,EN;
  output Y0,Y1,Y2,Y3;

  assign Y0 = ~A0&~A1&EN;
  assign Y1 = A0&~A1&EN;
  assign Y2 = ~A0&A1&EN;
  assign Y3 = A0&A1&EN;
endmodule
```

Test bench:

```
`timescale 1ps/1ps

module p1_tb;
  reg A0,A1,EN;
  wire Y0,Y1,Y2,Y3;

  p1 test(A0,A1,EN,Y0,Y1,Y2,Y3);

  always
  begin
    $dumpfile("p1.vcd");
    $dumpvars(0,p1_tb);

    A0 = 0;
    A1 = 0;
    EN = 0;
    #10
    A0 = 0;
    A1 = 0;
    EN = 1;
    #10
    A0 = 0;
    A1 = 1;
    EN = 0;
    #10
    A0 = 0;
    A1 = 1;
```

```
    EN = 1;
    #10
    A0 = 1;
    A1 = 0;
    EN = 0;
    #10
    A0 = 1;
    A1 = 0;
    EN = 1;
    #10
    A0 = 1;
    A1 = 1;
    EN = 0;
    #10
    A0 = 1;
    A1 = 1;
    EN = 1;
    #10
    $finish;
  end
endmodule
```

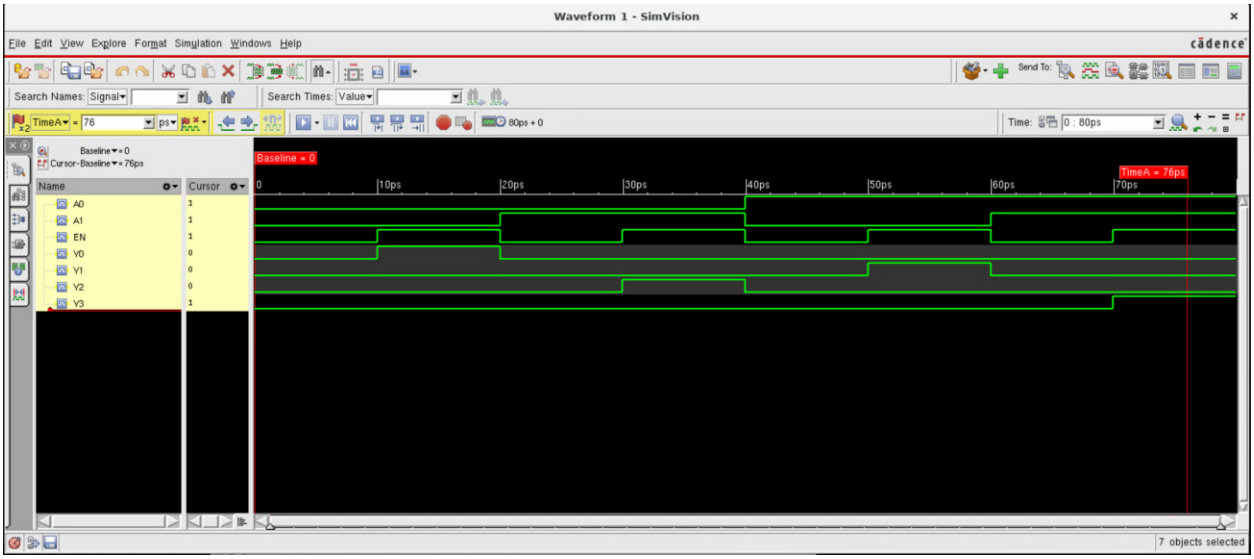

Fig 1: Problem 1 showing all possible inputs/outputs

Problem 2:
Module:

```
`timescale 1ps/1ps

module p2(A,B,CIN,S,COUT);
  input A,B,CIN;
  output S,COUT;

  assign S = (A^B)^CIN;
  assign COUT = (A&CIN)|(B&CIN)|(A&B);
endmodule
```

Test bench:

```
`timescale 1ps/1ps

module p2_tb;
  reg C0,A0,B0,A1,B1,A2,B2,A3,B3;
  wire S0,C1,S1,C2,S2,C3,S3,C4;

  p2 ADD0(A0,B0,C0,S0,C1);
  p2 ADD1(A1,B1,C1,S1,C2);
  p2 ADD2(A2,B2,C2,S2,C3);
  p2 ADD3(A3,B3,C3,S3,C4);

  always
  begin
    $dumpfile("p2.vcd");
    $dumpvars(0,p2_tb);

    A0 = 0;
    A1 = 1;
    A2 = 0;
    A3 = 1;

    B0 = 1;
    B1 = 1;
    B2 = 0;
    B3 = 1;

    C0 = 0;
    #10
    A0 = 0;
```

```
    A1 = 1;
    A2 = 0;
    A3 = 1;

    B0 = 1;
    B1 = 1;
    B2 = 0;
    B3 = 1;

    C0 = 1;
    #10
    A0 = 0;
    A1 = 1;
    A2 = 0;
    A3 = 1;

    B0 = 1;
    B1 = 1;
    B2 = 0;
    B3 = 0;

    C0 = 1;
    #10
    A0 = 0;
    A1 = 0;
    A2 = 0;
    A3 = 1;

    B0 = 1;
    B1 = 1;
    B2 = 0;
    B3 = 0;

    C0 = 1;
    #10
    $finish;
  end
endmodule
```

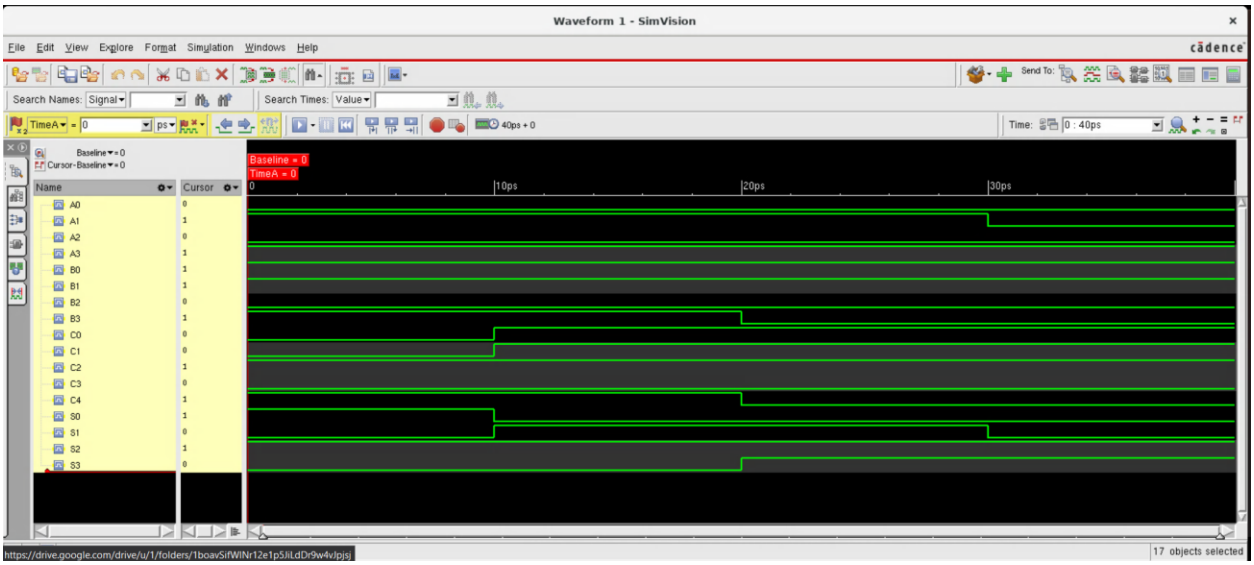

Figure 2: Problem 2 showing 4 possible inputs/outputs

Problem 5
Module:

```
`timescale 1ps/1ps

module p5(
   input [2:0] a,
   input [2:0] b,
   output [5:0] f
);

   wire [2:0] s1;
   wire [2:0] s2;
   wire [3:0] p1;

   wire [2:0] s3;
   wire [3:0] p2;

   assign s1 = {a[2]&b[0], a[1]&b[0], a[0]&b[0]};
   assign s2 = {a[2]&b[1], a[1]&b[1], a[0]&b[1]};
   assign p1 = s2+s1[2:1];

   assign s3 = {a[2]&b[2], a[1]&b[2], a[0]&b[2]};
   assign p2 = s3+p1[3:1];

   assign f = {p2,p1[0],s1[0]};

endmodule
```

Test bench:

```
`timescale 1ps/1ps

module p5_tb;
   reg [2:0] a;
   reg [2:0] b;
   wire [5:0] f;

   p5 mult(a,b,f);

   initial begin
      $dumpfile("p5.vcd");
      $dumpvars(0,p5_tb);
```

```
      a = 0;
      b = 0;
      repeat(8) begin
        repeat(7) begin
          #10
          b = b+1;
        end
        #10
        a = a+1;
        b = 0;
      end
    end
endmodule
```

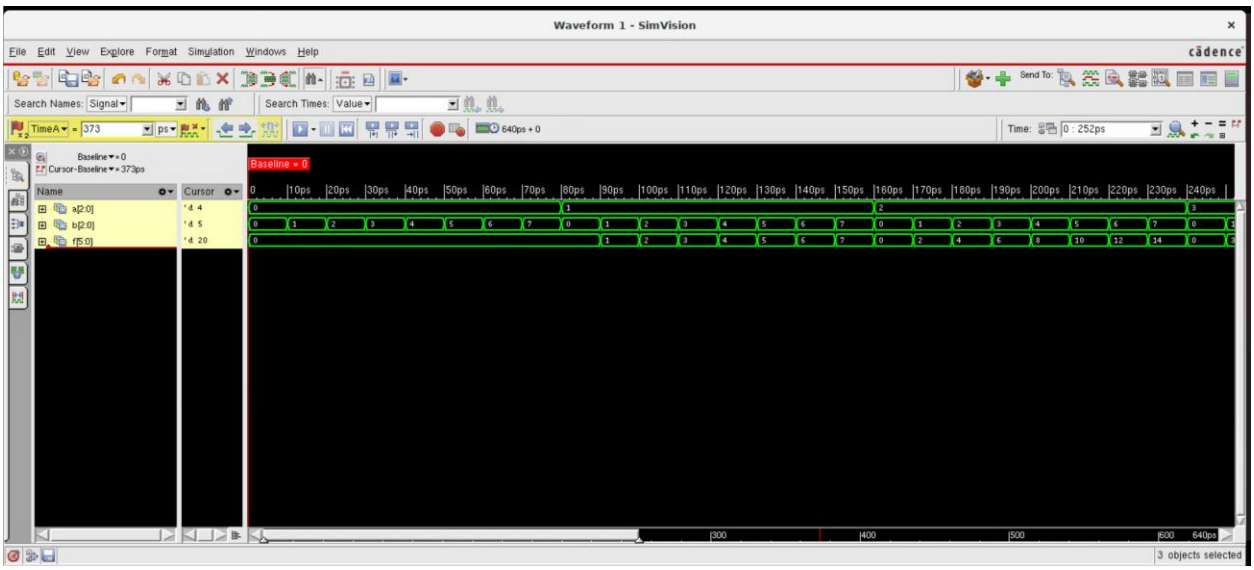

Figure 3: Problem 5 view 1

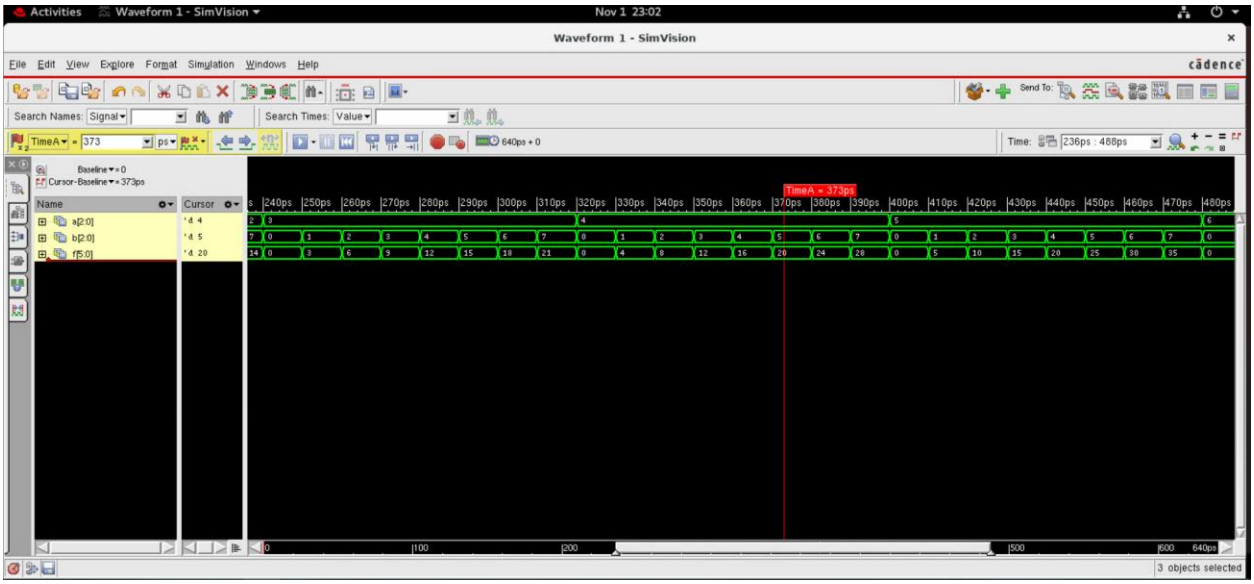

Figure 4: Problem 5 view 2

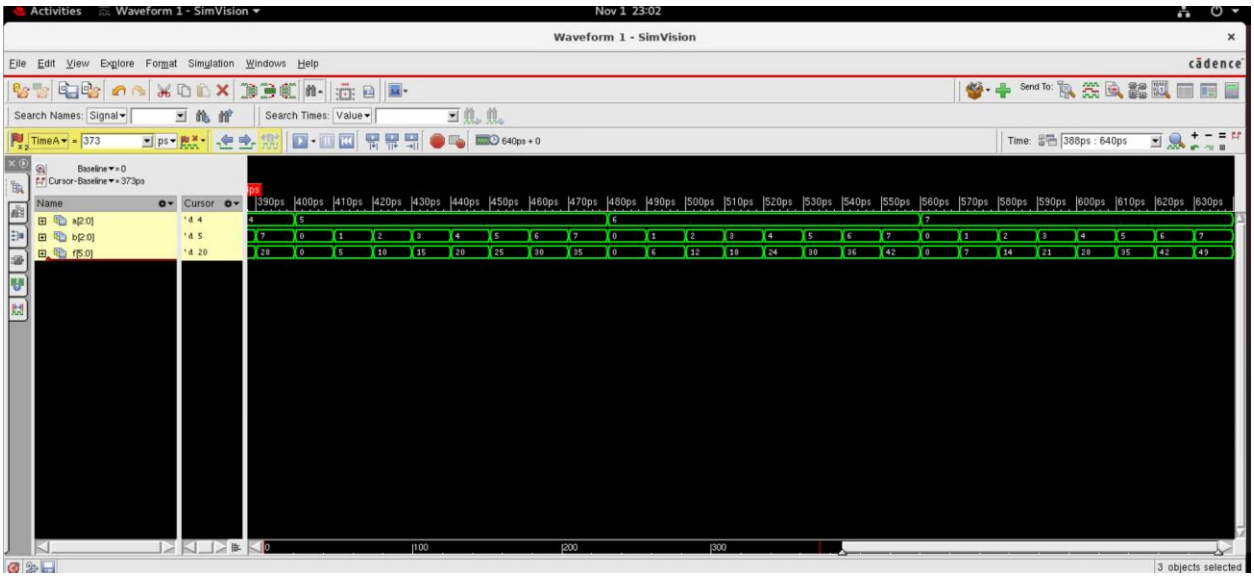

Figure 5: Problem 5 view 3