Assignment #2
EECS 303: Advanced Digital Logic Design

Problem 0. Following the "Xcelium Tutorial" complete the RTL simulation of the example design of the conventional Arithmetic Logic Unit (alu_conv.v) provided in the Assignment folder, using the testbench file (alu_conv_test.v) also provided in the Assignment folder.

Problem 1. Unate Covering: (20 points)

Solve the following covering problem.

NOTE: If Branch and Bound is needed at any point, use the following rules: (i) The next pivoting column should be selected as the one that covers the most rows. (ii) If there are no two independent rows in the cyclic core, the lower bound should be assumed to be equal to 2. **Clearly identify the initial Upper and Lower Bounds and the partial solutions costs and any updates made to the best solution found in your steps.**

	Col1	Col2	Col3	Col4	Col5
Row1	1	1	0	1	0
row2	1	0	1	0	1
row3	1	0	0	1	0
row4	0	1	1	1	0
row5	0	1	0	1	1
row6	1	0	1	1	0

Problem 2. Minimizing Two-level Logic Functions Using the QM Method (30 Points):

Simplify the following Boolean functions using the Quine-McCluskey algorithm. You need to (1) find out all the prime implicants (2) find out a minimum cover using techniques from the class (first attempt to reduce the covering table using by trying to identify essential columns and using row/column elimination rules) If a cyclic core is obtained, then use branch and bound)

(1) f (a, b, c, d) = S (0, 5, 6, 10, 11, 13)+d(4, 8, 14)

(2) f (a, b, c) = S (0, 2, 3, 4, 5, 7)

Problem 3. Value Representations: (20 Points) For each of the following fill the table with the corresponding information:

	Signed Or Unsigned	Width	Base: Decimal, Binary, Octal, Hexadecimal, etc.	Equivalent Integer Value
8’b00001000				
16’hABCD				
4’sb1110				
4’d12				
4’b1100				
8’shFF				
8’sb00011100				
12’h2A8				
6’sb111101				
12’o3456				

Problem 4 Module Statements (30 Points):

Write a structural Verilog module for the combinational circuit in the Figure shown below

Write a testbench and simulate the Verilog code using Excelium for ONLY 4 input cases of your choice (2 of which should result in ALARM=1 and the other 2 should result in ALARM=0). Include screenshots of the simulation output.

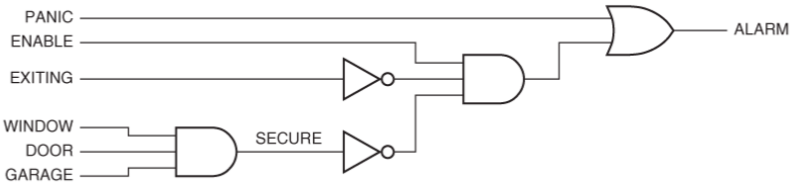

Figure 3-16 Alarm circuit derived from logic expression.