CE303 HW#3

P3: a) To get from inputs A_0, B_0, C_0 to S_3 we use 2 XOR per adder, meaning 2×4×3 = 24 time units (by the critical path; in series)

To get from inputs A_0, B_0, C_0 to C_4 we use 2 XOR per adder for the first 3 adders & then 1 AND & 1 OR, meaning 2×3×3+2 = 20 time units (by the critical path; in series)

b) Given Sum delay is 2 times Carry delay:

↳ worst case goes through 20 FA, 13 carries & 7 sums

↳ $D_s = 2$ $D_c = 1$ → 13×1 + 7×2 = 27

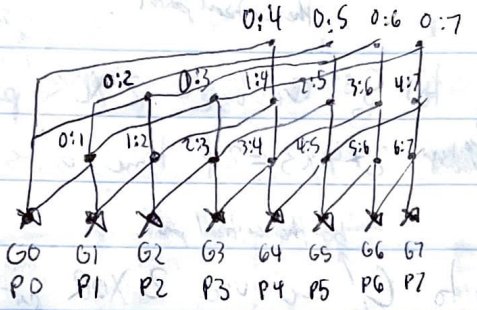
Given Carry delay is 2 times Sum delay:

↳ worst case goes through 20 FA, 14 carries & 6 sums

↳ $D_s = 1$ $D_c = 2$ → 14×2 + 6 = 34

↳ I would favor having faster carries

P4:



The critical path involves 3 dot products, and at each dot product the critical path goes through 1 AND gate and 1 OR gate and at the beginning G_0 & P_0 are created by a single gate each in parallel → 3+2+1 = 7 gates

↳ Critical Path:

$A_0B_0 = G_0$ → $P_1G_0 + G_1 = G_{0:1}$ → $P_{2:3}G_{0:1} + G_{2:3} = G_{0:3}$

A_0B_0: 1st gate; P_1G_0: 2nd gate; $+G_1$: 3rd gate; $P_{2:3}G_{0:1}$: 4th gate; $+G_{2:3}$: 5th gate

↳ $G_{0:3}$ → $P_{4:7}G_{0:3} + G_{4:7} = G_{0:7}$

$P_{4:7}G_{0:3}$: 6th gate; $+G_{4:7}$: 7th gate