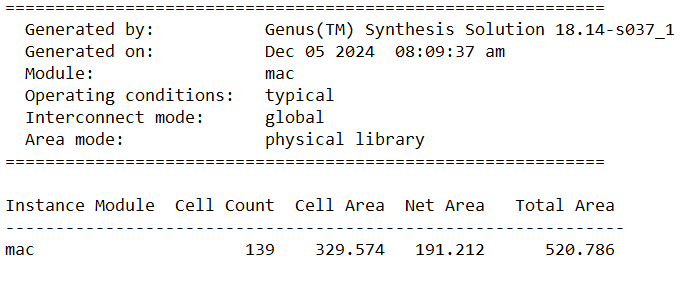
Problem 1:

A computer screen shot of a keyboard

Description automatically generated

|  |  |  |
| --- | --- | --- |
| Area: | Cell Counts: | Timing Slack: |

Report Area:  


Report Timing:  
A screenshot of a computer program

Description automatically generated

A screenshot of a computer

Description automatically generated  
  
RTL:  
`timescale 1ns/1ps

module mac(

    input signed [3:0] IN,W, //should be signed

    input clk, rstb,

    output reg signed [11:0] OUT //should be signed

);

reg signed [6:0] A; //should be signed

reg signed [10:0] B; //should be signed

reg [3:0] counter;

always @(posedge clk or negedge rstb) begin

    if(~rstb) begin

        counter = 0;

        OUT = 0;

        B = 0;

        A = 0;

    end else if(counter == 9) begin

        counter = 0;

        OUT = B;

        B = 0;

        A = IN\*W;

    end else if(counter < 9) begin

        counter = counter + 1;

        A = IN\*W;

        B = A+B;

    end else begin

        counter = 0;

        OUT = 0;

        B = 0;

        A = 0;

    end

end

endmodule

Testbench:  
`timescale 1ns/1ps

module mac\_tb;

    reg signed [3:0] IN,W; //should be signed

    reg clk, rstb;

    wire signed [11:0] OUT; //should be signed

    mac mymac(IN,W,clk,rstb,OUT);

    always begin

        $dumpfile("mac.vcd");

        $dumpvars(0,mac\_tb);

        IN = 0;

        W = 0;

        rstb = 1;

        clk = 1;

        repeat(21) begin

            #0.5

            clk = 0;

            #0.5

            clk = 1;

            IN = IN + 1;

            W = W + 2;

        end

        $finish;

    end

endmodule

SDC:

create\_clock -name clk -period 1.0 -waveform { 0 0.5 } [get\_ports clk]

set\_input\_delay -max 0.5 -clock clk [get\_ports {IN W}]

set\_input\_delay -min -0.2 -clock clk [get\_ports {IN W rstb}]

set\_output\_delay -max 0.5 -clock clk [get\_ports {OUT}]

set\_output\_delay -min -0.2 -clock clk [get\_ports {OUT}]