Everything i know

The AVM System for Various Intelligent Manufacturing Applications

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VM Definition

Virtual Metrology

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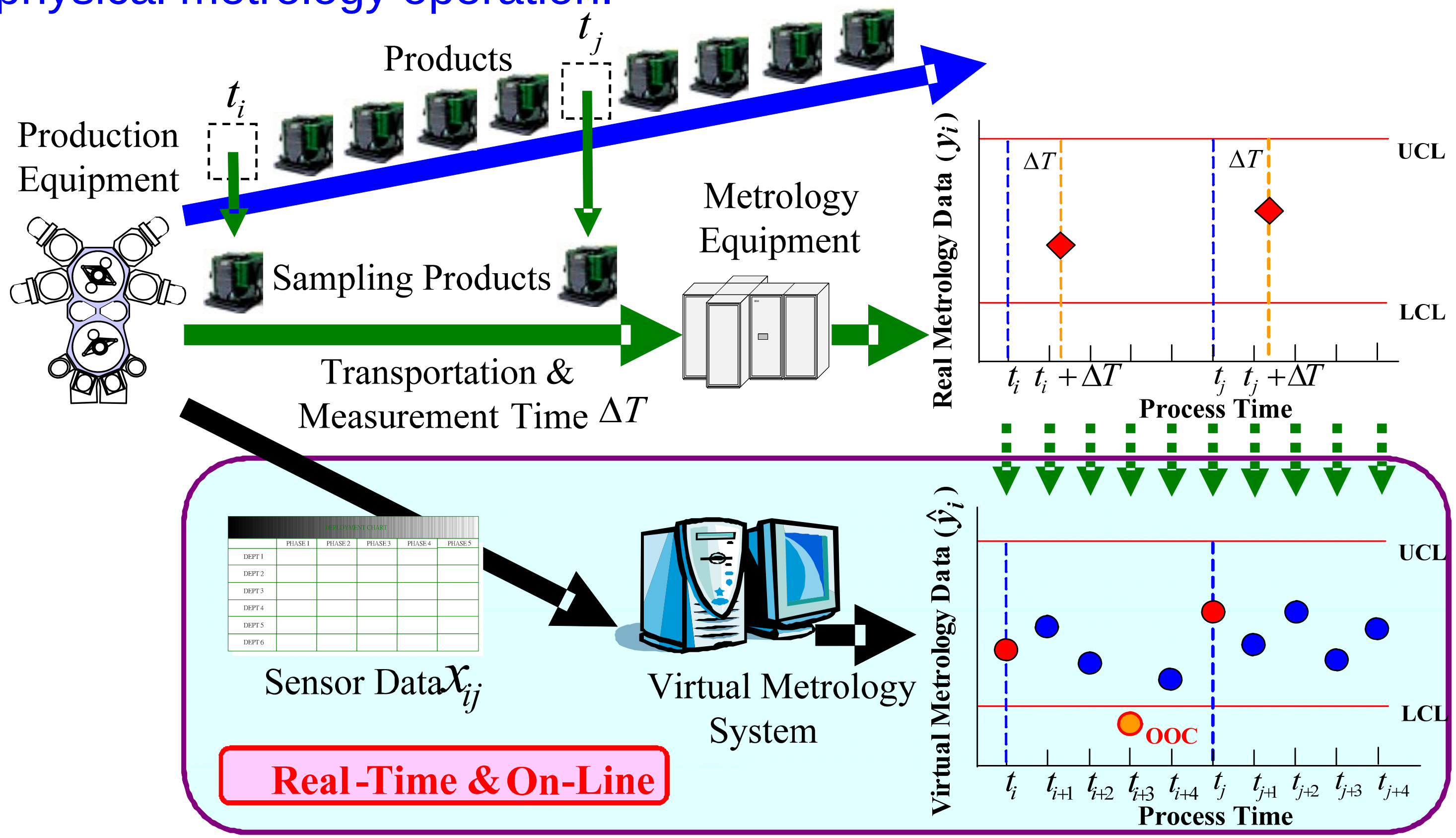
- Virtual Metrology (VM) is a method to conjecture manufacturing quality of a process tool based on data sensed from the process tool and without physical metrology operation.



- VM can convert sampling inspections with metrology delay into real-time and on-line total inspection.

Live Demo of the AVM System for CNC Precision Machining

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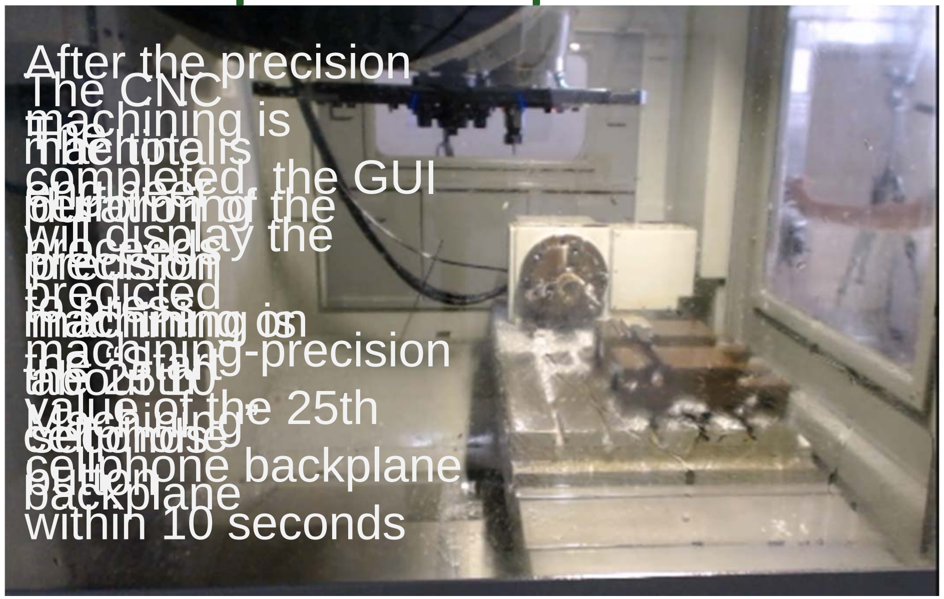
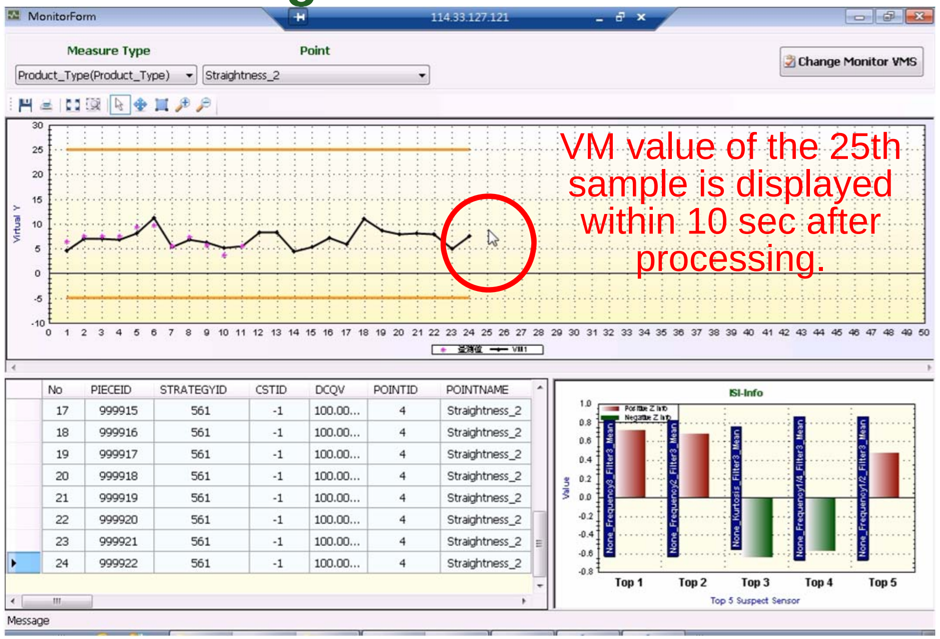
(At the 2012 Taiwan International Machine Tool Exhibition)

- Video showing the precision machining on cellphone backplanes.



(The CNC tool was located in a machine tool factory in Taiwan)

- GUI displaying real-time and online VM values of straightness 2.



(The GUI was shown at the Exhibition Hall in Taipei, Taiwan)

Benefit of Virtual Metrology

Why Develop & Implement VM

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Why develop and implement VM?

INTERNATIONAL SEMATECH ISMI MANUFACTURING INITIATIVE

- Cost and productivity impacts to device maker
  - Cycle Time
    - VM allows product to skip metrology sampling steps in the process flow
  - Cost
    - Savings = Fewer metrology tools required
    - Cost = develop and maintain each VM solution implemented

ISMI DRAM Fab Model (1/2)

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Why develop and implement VM?

INTERNATIONAL SEMATECH ISMI MANUFACTURING INITIATIVE

	# steps	sum of PTIME	VM success ratio	post VM # steps	Cost basis for metro tool	metro tool	# tools in baseline	CAPEX redux	PTIME reduc	CT redux	Total CT red
GREEN	74	98.78	50%	37	1000000	film thk	28	$ 14,000,000	49	370	419
YELLOW	64	58.54	20%	51	2000000	cd sem	16	$ 6,400,000	12	128	140
RED	130	189.39	2%	127	1000000	PLY defect	43	$ 860,000	4	26	30
		total min/lot baseline					**Reduction in capital cost**	**$ 21,260,000**			589
		6887.54									9.81
		days cycle time		post VM CT	**8.55%**	**reduction in cycle time**					0.41
		4.78		4.37							
				cost to set up and maintain VM			per year	#applications	cost per year		
					per Green application		$150000	12	$ 1,800,000		WIP movem
					per yellow application		$200000	3	$ 600,000		5
					per red application		$300000	1	$ 300,000		5
Factory Capacity								total	$ 2,700,000		5
30k wafer starts per month, + 4.5K NPWs											
Inspect PLY 43											
Measure CD 16											
Measure Film 28											
Measure Overlay 9											

ISMI DRAM Fab Model (2/2)

- A DRAM 300mm fab model example with capacity of 30K wafer starts plus 4.5K non production wafers (i.e., test wafers) per month is utilized by ISMI.
- This model is applied with ISMI's 45nm generic logic process flow metrology steps mapped as easy/medium/difficult for VM implementation and optimistic/realistic/pessimistic scenarios are designed respectively for VM penetration.
- By applying fab-wide VM implementation and realistic scenario analysis, this model yields
  - 8.55% cycle time reduction
  - US$ 21M capex reduction; and
  - additional cost of US$ 2.7M per year to maintain VM

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Overall Benefit of VM [6] (1/2)

$$Benifit = W_O * \left[\frac{1}{1-(\Delta CT_P + \Delta CT_M)} - 1 \right] * (1+\Delta Y) * (P-C) + \Delta Cost_M + \Delta Cost_T - Cost_V$$

W_O = number of wafer output per year;

$\triangle CT_P$ = % cycle time reduction due to VM allowing production wafers to skip metrology sampling steps in the on-line process monitoring flow;

$\triangle CT_M$ = % cycle time reduction due to VM allowing less test wafers used in the off-line tool monitoring process and more intelligent dynamic metrology and process schemes;

$\triangle Y$ = % enhancement due to improvement on process capability (from VM supporting APC), reduction in scrap, and so forth;

P = average selling price per 300mm production wafer;

C = average production cost per 300mm production wafer;

$\triangle Cost_M$ = cost saving of test wafers per year when applying VM in all production lines;

$\triangle Cost_T$ = capex reduction per year when applying VM in all production lines;

$Cost_V$ = additional cost per year to maintain VM;

$Cost_Q$ = additional cost per year due to false alarms and missed detections caused by VM.

Overall Benefit of VM [6] (2/2)

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- Substituting all the parameter values mentioned above into (1), the benefit of VM yields US$ 63,458,792 per year for this fab model with capacity of 30K wafer starts plus 4.5K test wafers per month.

- In conclusion, given the assumptions noted above, VM fab-wide implementation is expected to gain extra $\left[\frac{1}{1-(\Delta CT_P + \Delta CT_M)}\right]$ (=10.56%) production volume output due to ($\triangle CT_P$ +$\triangle CT_M$ = 9.55%) cycle-time reduction. This extra production volume output contributes the major portion of VM total benefit.

Evaluation of Economic Effects as the Basis for Assessing VM Investment by Koitzsch and Honold*

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- Koitzsch and Honold’s study* indicated that the benefit per fab per year is greater than 30 million US dollars. The calculations were performed for a 200 mm wafer fab of the 0.13 um technology.

*M. Koitzsch, and A. Honold “Evaluation of Economic Effects as the Basis for Assessing Virtual Metrology Investment,” *Future Fab International*, issue 37, April 2011.

Difficulties and Challenges of Traditional VM

Difficulties and Challenges of Traditional VM

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- Traditional VM scheme has major drawbacks listed below and requires significant improvements for better accuracy and shorter deployment time to support production-Line operations:
  1. VM values are provided without the reliance indexes (RIs) so users don't know whether VM values are reliable or not
  2. Promptness and accuracy may not be achieved simultaneously
  3. Not able to perform on-line and real-time quality evaluation of process-and-metrology data collected
  4. Creating VM models one by one with a lot of historical data, huge labor expenses and model-creation time is prohibitively expensive

- **The AVM system can solve the above difficulties since the AVM system has the following merits/novelties that traditional VM lacks.**

VM Architecture

Traditional Virtual Metrology System

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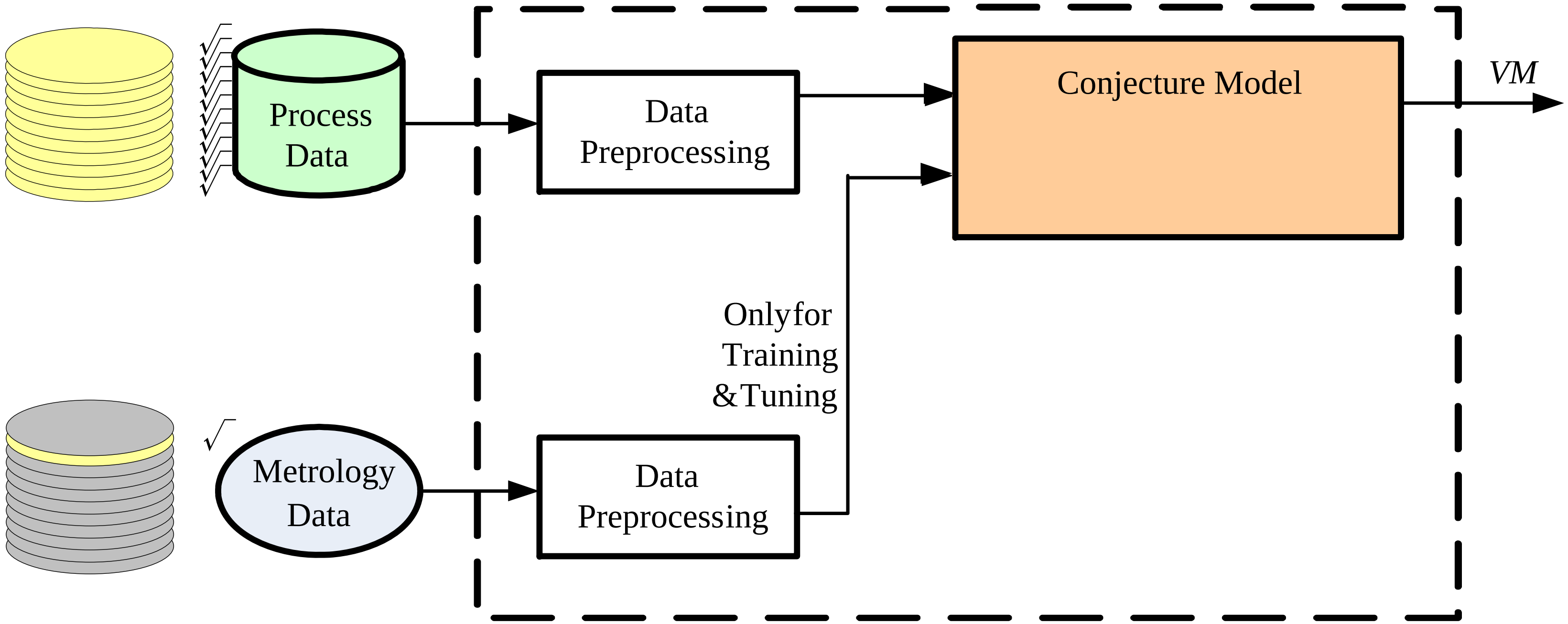
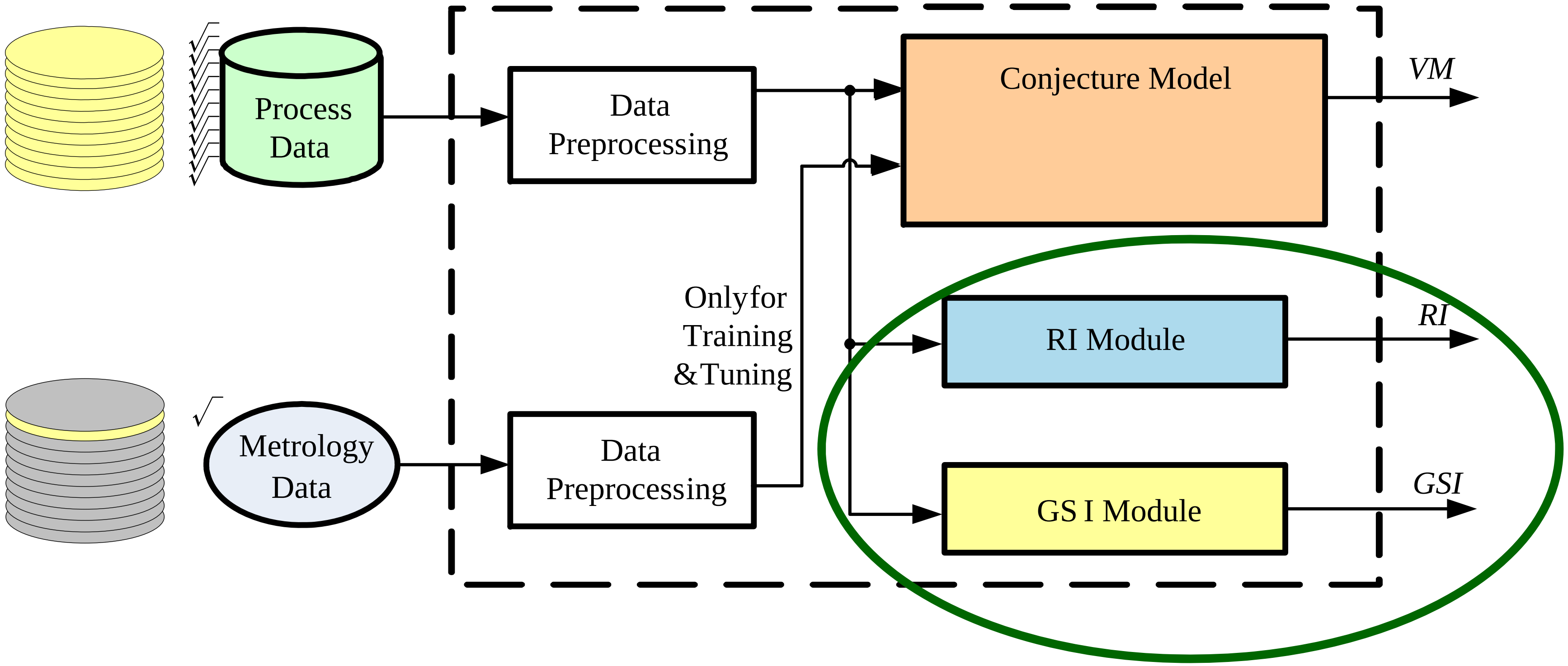


Advanced VMS with *RI* & *GSI* *



*: ROC Patent No.: I315054
US Patent No.: 7,593,912 B2

Dual Phase VMS** with *RI* & *GSI*

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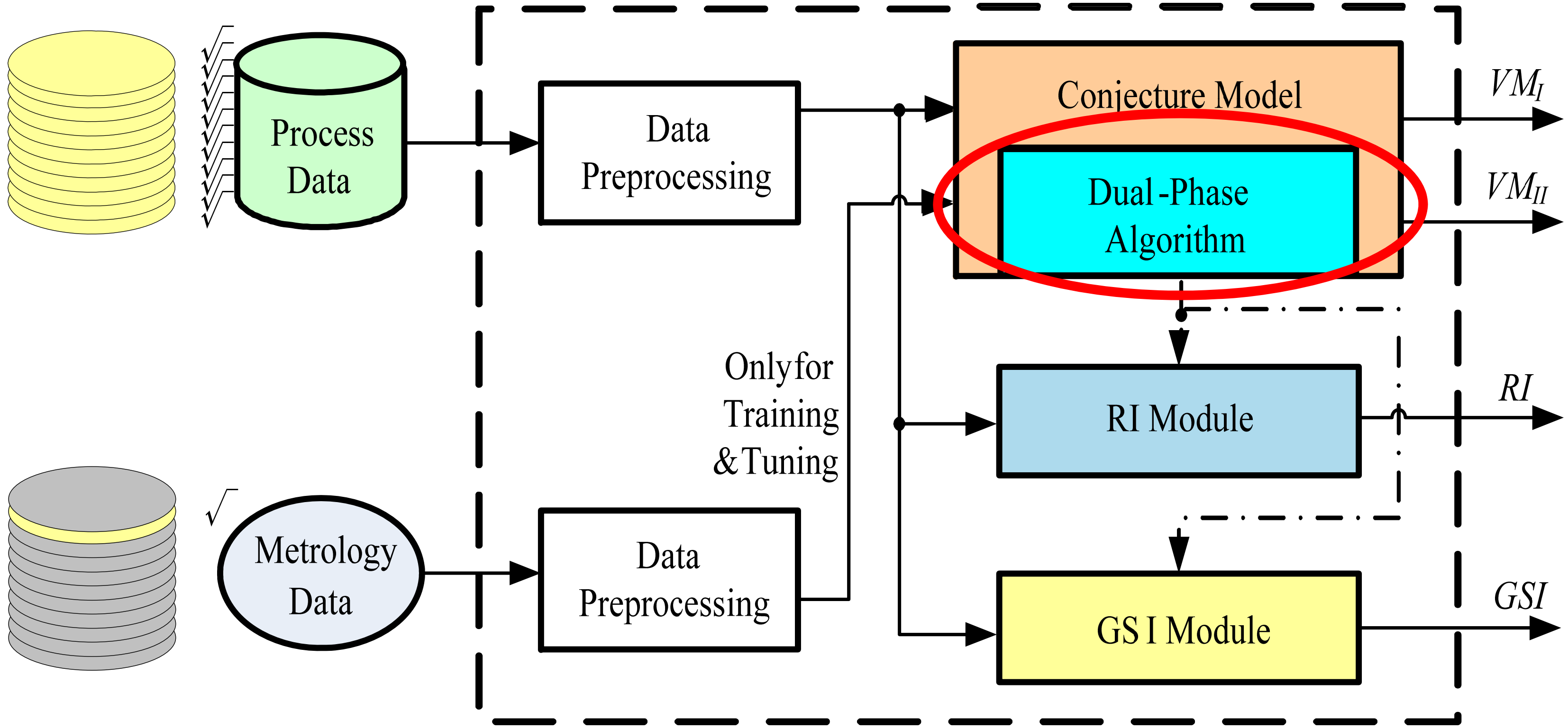
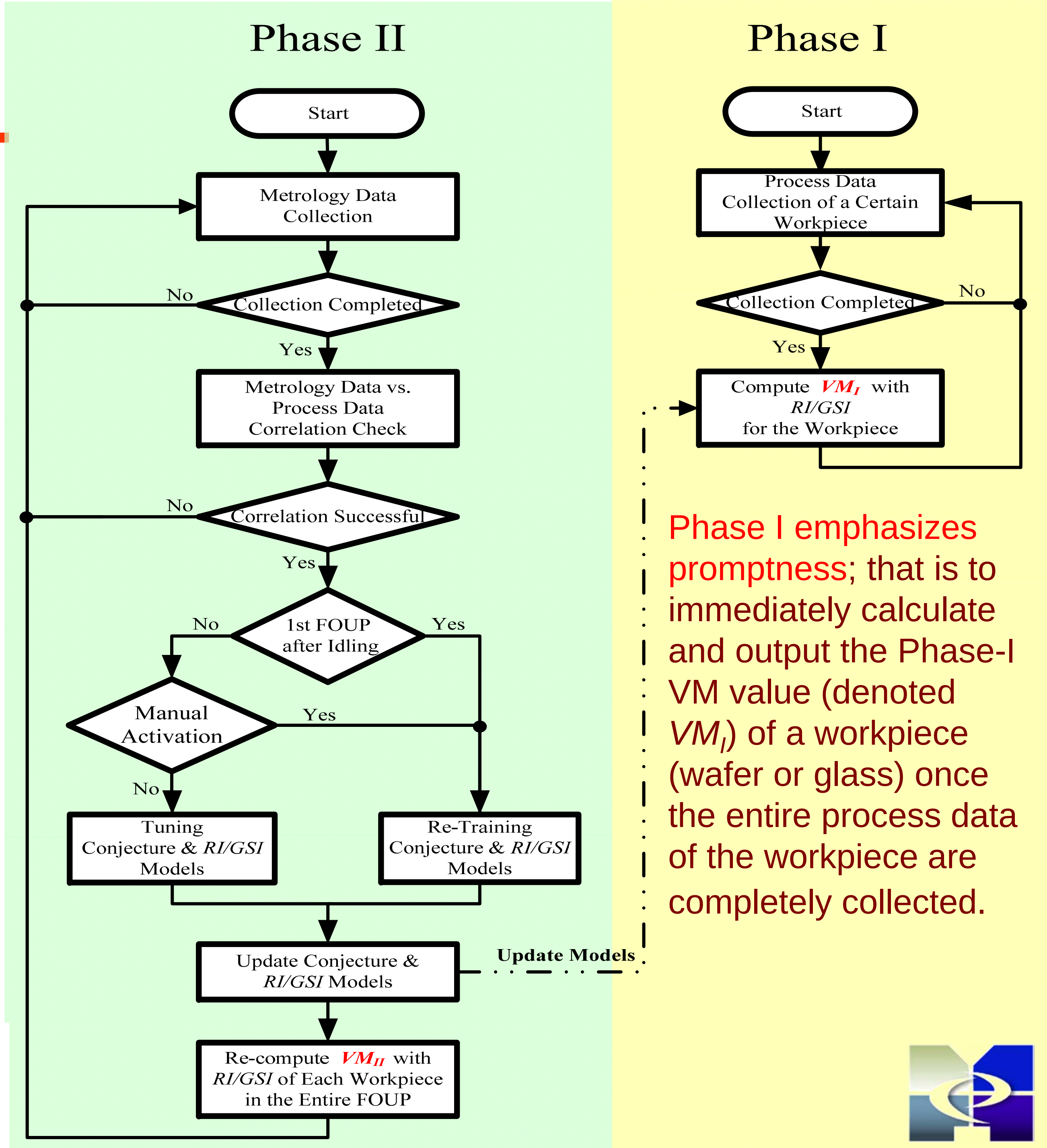


**: ROC Patent No.: I338916;
US Patent No.: 7,603,328 B2;
Korea Patent No.: 10-0915339;
Japan Patent No.:4584295;
China Patent No.: 823284

Dual-Phase VM Conjecture Algorithm



Phase II improves accuracy; that is not to re-calculate and output the Phase-II VM values (denoted VM_{II}) of all the workpieces in the cassette (also called FOUP) until an actual metrology value (required for tuning or re-training purposes) of a workpiece in the same cassette is collected.

Phase I emphasizes promptness; that is to immediately calculate and output the Phase-I VM value (denoted VM_I) of a workpiece (wafer or glass) once the entire process data of the workpiece are completely collected.

DQI_X and DQI_y for Data Preprocessing

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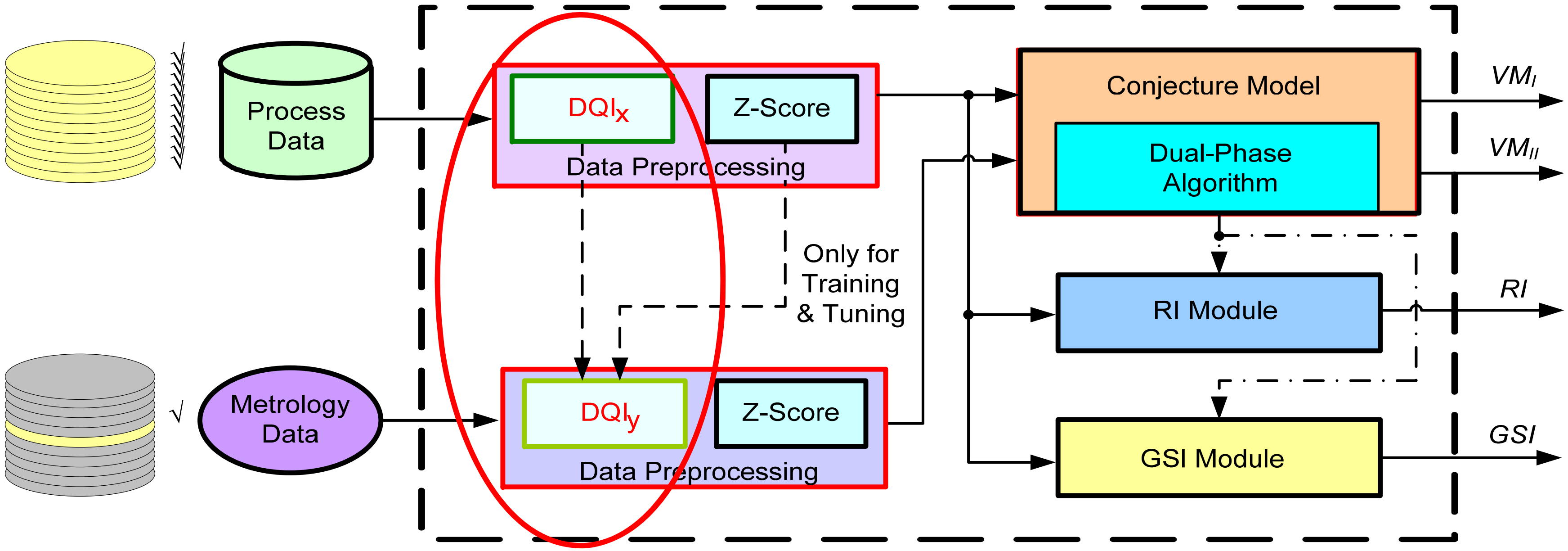
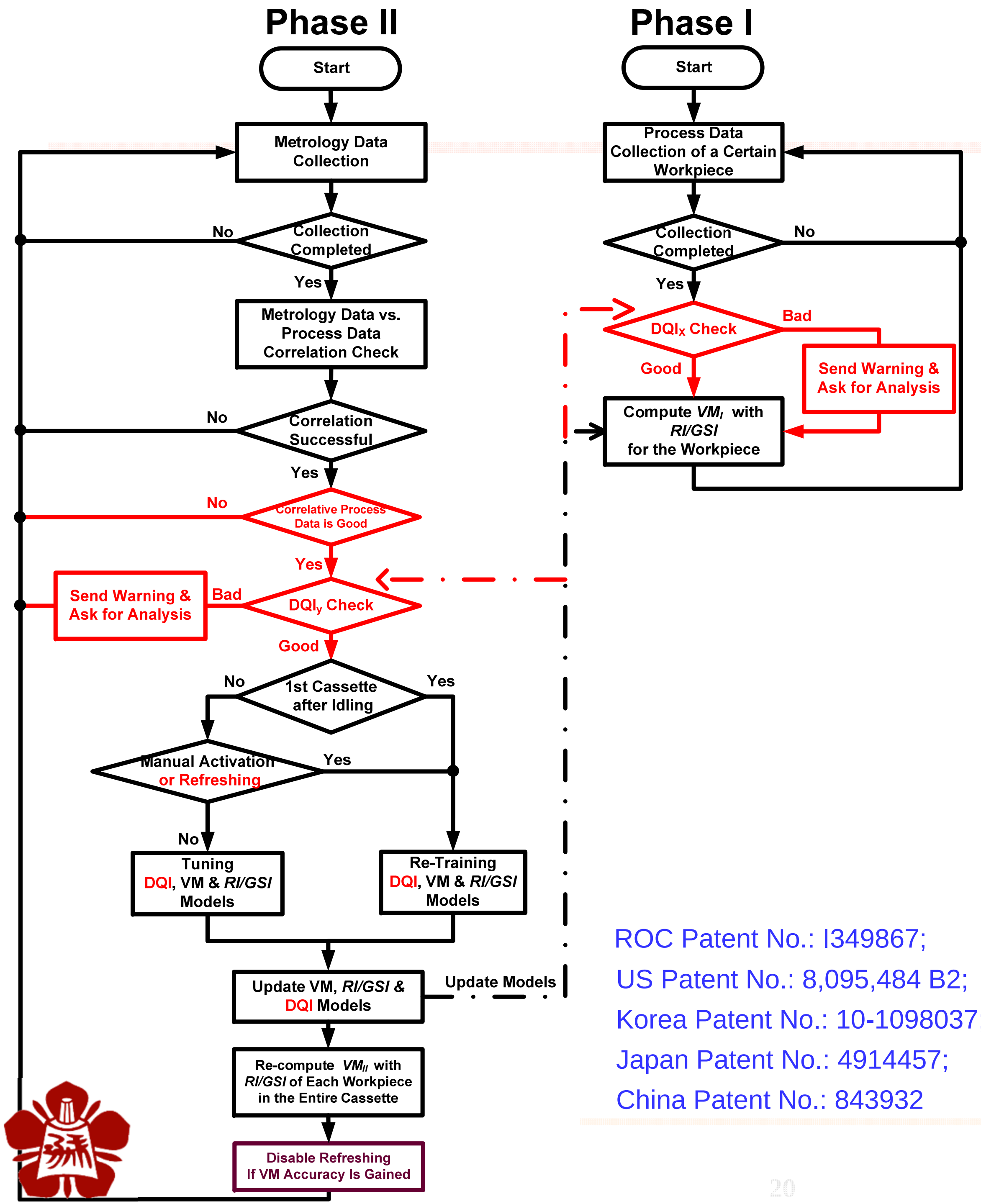


ROC Patent No.: I349867;
US Patent No.: 8,095,484 B2;
Korea Patent No.: 10-1098037;
Japan Patent No.: 4914457;
China Patent No.: 843932

Advanced Dual-Phase VM Algorithm



- The DQI_X and DQI_y models are added into the algorithm to perform automatic data quality evaluation.
- A model refreshing mechanism is added into the algorithm for automatic model-refreshing control.
- When VM accuracy is gained, the refreshing procedure will stop automatically and the system will enter the normal operation state.

ROC Patent No.: I349867;
US Patent No.: 8,095,484 B2;
Korea Patent No.: 10-1098037;
Japan Patent No.: 4914457;
China Patent No.: 843932

The AVM System

The Features of AVM

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Feature	Description
Production-Line Support	1. VM values are provided with their accompanying Reliance Indexes (RIs) & Global Similarity Indexes (GSIs) so users know whether VM values are reliable or not (p23) 2. On-line refreshing of VM models is performed whenever an actual metrology value is available by applying the Dual-Phase Algorithm (p24) 3. The AVM System is able to perform on-line and real-time quality evaluation of process-and-metrology data collected / DQI_X & DQI_y (p25) 4. The AVM System possesses Automatic Fanning-Out and Model-Refreshing capabilities so as to facilitate fab-wide VM implementation possible (p26)
Generic Framework	1. Generic framework design that is different from one-off solution, which needs re-design on every different technology or process application (p28) 2. Integration with MES such that extension of VM applications is relatively easy (p29) 3. Supporting W2W APC by utilizes AVM with RI/GSI in the feedback loop to prevent adopting an unreliable VM value for control (p30)
Feasibility	1. Strong theoretical foundation and Novelty (AVM related papers &patents) (p90) 2. Well-experienced on the industry-university projects: The AVM System has been technology-transferred to tsmc/CMI/Motech/UMC and gained successful & satisfied results after on-line implementations (p36) 3. Feasible, Generic, & Complete system architecture that is superior to other-venders' VM systems (p28 & 35)

AVM Novelty 1: RI & GSI [2] [A]

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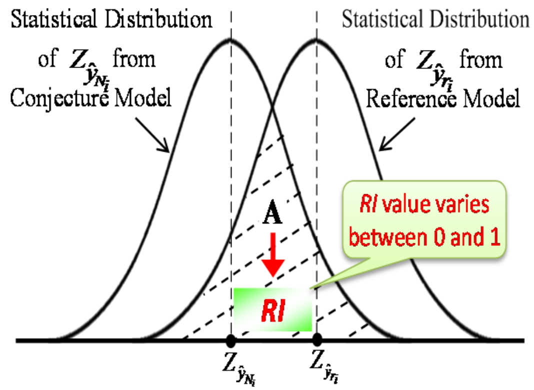
- **RI --** The AVM system generates the accompanying **Reliance Index (RI)** of each VM_I and VM_{II}. The AVM system has two different VM prediction models, and RI is defined as the percentage of intersection between the statistical normal distributions of those two normalized prediction values. Therefore, the RI value is between 0 and 1. If those two prediction values are exactly the same, the corresponding RI value is 1, and if those two values are far apart, the corresponding RI value is 0. Therefore, users can check the reliability of the VM prediction via its corresponding RI value.



- **GSI --** When deviations occur in the process data such that the similarity between this new set of process data and the model set of all historical process data is bad, then the accuracy of the VM value conjectured by NN and the reference prediction value predicted by MR would not be good. However, it is still possible that the conjectured VM value and the predicted reference value happen to be nearly the same such that the RI value is higher than RI_T. To compensate for this unavoidable substitution, the **Global Similarity Index (GSI)** is proposed to help the RI gauge the reliance level of VM.

AVM Novelty 2: Dual-Phase VM Method [1] [B]

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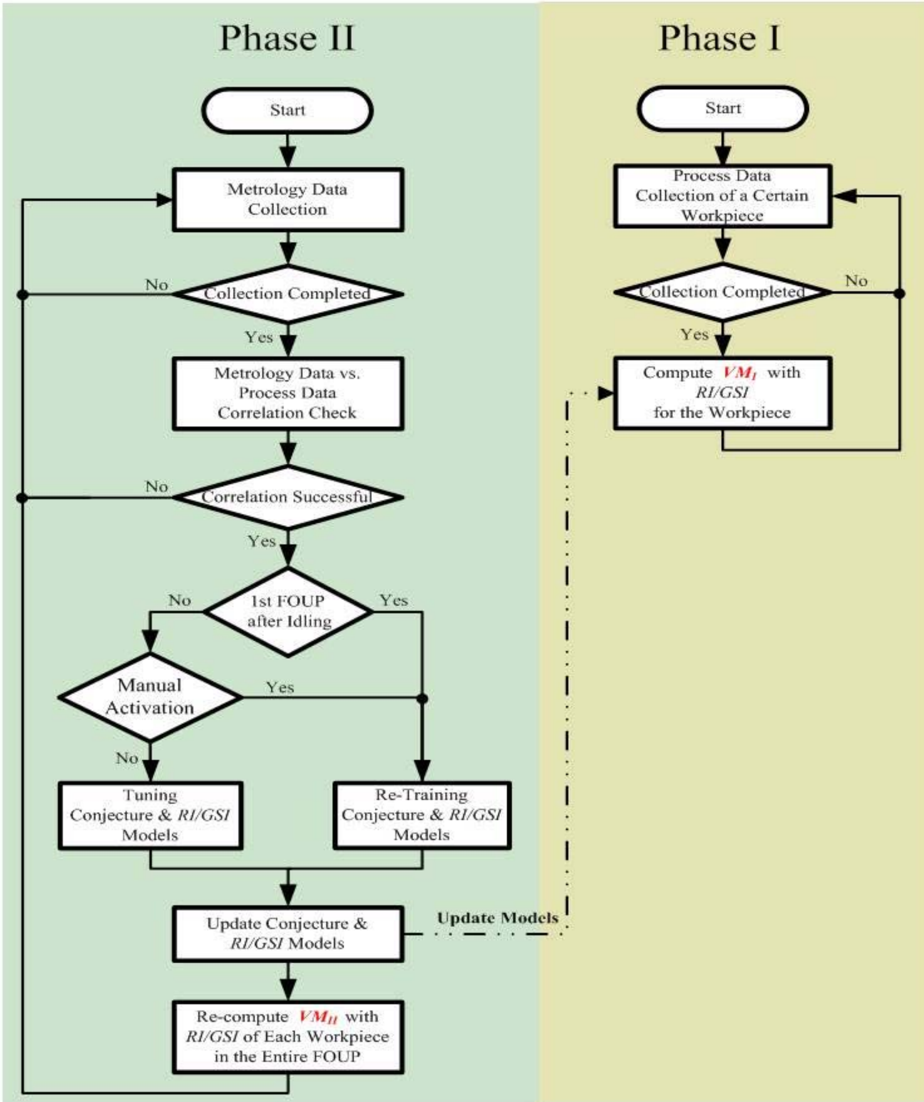
- The AVM system can generate dual-phase VM values.
- Phase I emphasizes promptness to immediately calculate and output the Phase-I VM value (denoted VM_I) of a workpiece (wafer or glass) once the entire process data of the workpiece are completely collected.
- Phase II improves accuracy to re-calculate (with the newly refreshed VM models) and output the Phase-II VM values (denoted VM_{II}) of all the workpieces in a cassette immediately after an actual metrology value of a workpiece in the cassette is collected (for refreshing the models).
- If promptness is the major concern, then VM_I is selected; and if accuracy is the first priority, then VM_{II} is chosen. As such, the outputs of the AVM system can meet the requirements of promptness and accuracy simultaneously.



Demo of the RI, GSI, & Dual-Phase Schemes

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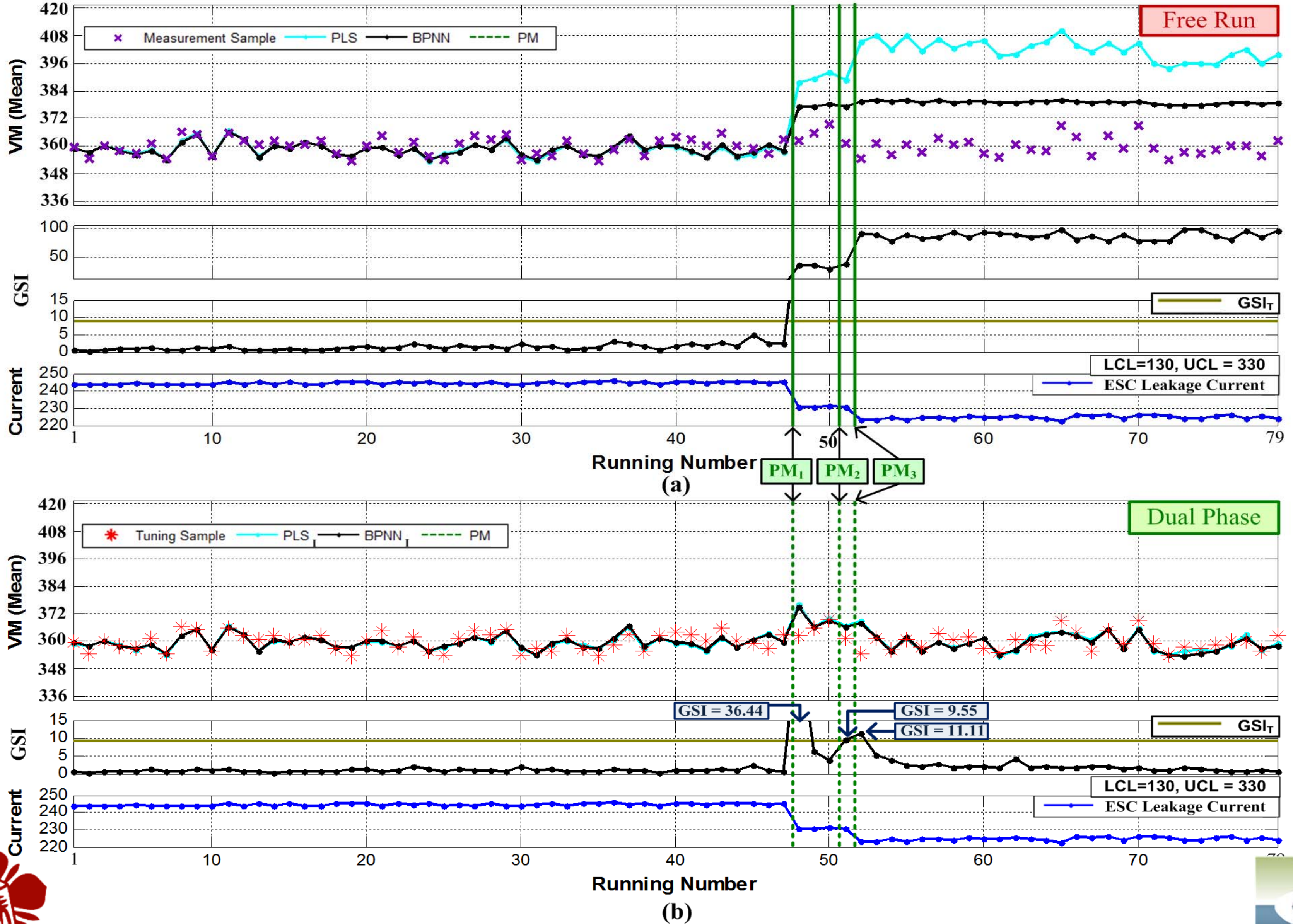

AVM Novelty 3: Automatic Data Quality Evaluation [7] [C]

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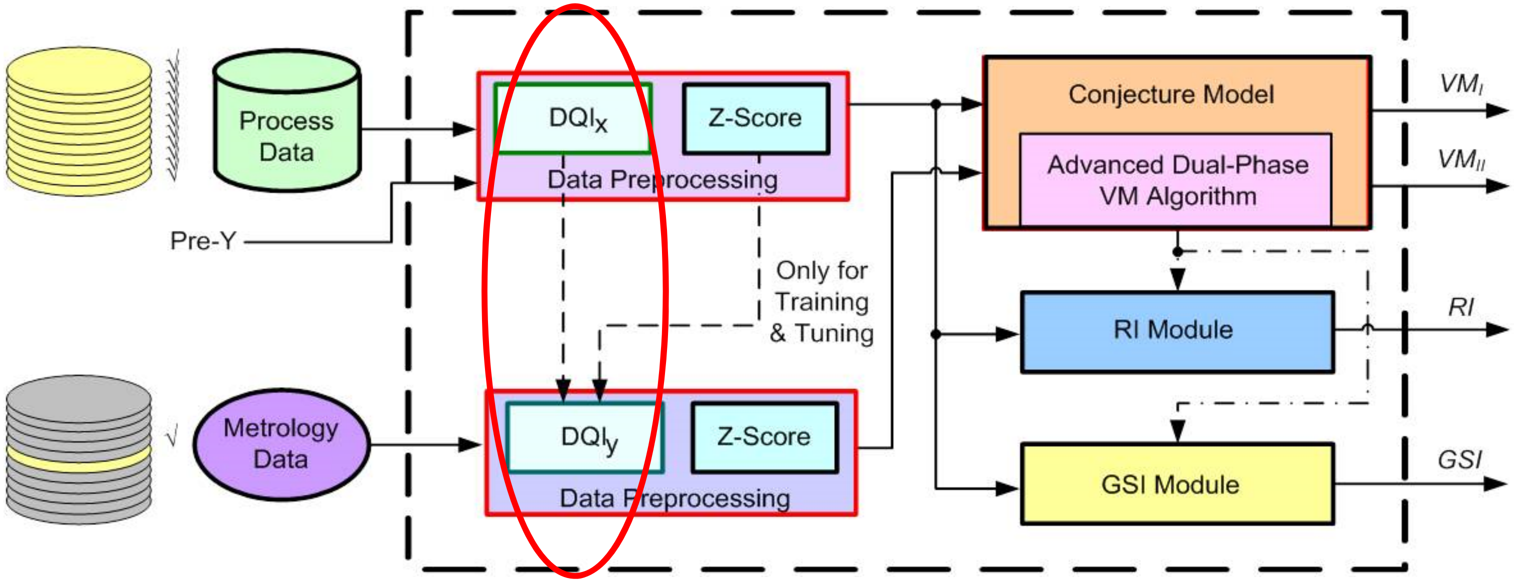
- The AVM system is equipped with the process data quality index (DQI_X) algorithm and the metrology data quality index (DQI_y) algorithm. Upon receiving a set of process data, the AVM system uses the DQI_X algorithm to perform on-line and real-time detection of a possible process-data abnormality. Whenever an actual metrology datum of a workpiece is obtained, the DQI_y algorithm is then used to perform on-line and real-time evaluation of a possible metrology-datum abnormality before this metrology datum can be considered for tuning or re-training the VM models. As a result, deterioration of VM accuracy due to model refreshing with bad-quality data is waived.



Demo of the DQI_y Algorithm [7]

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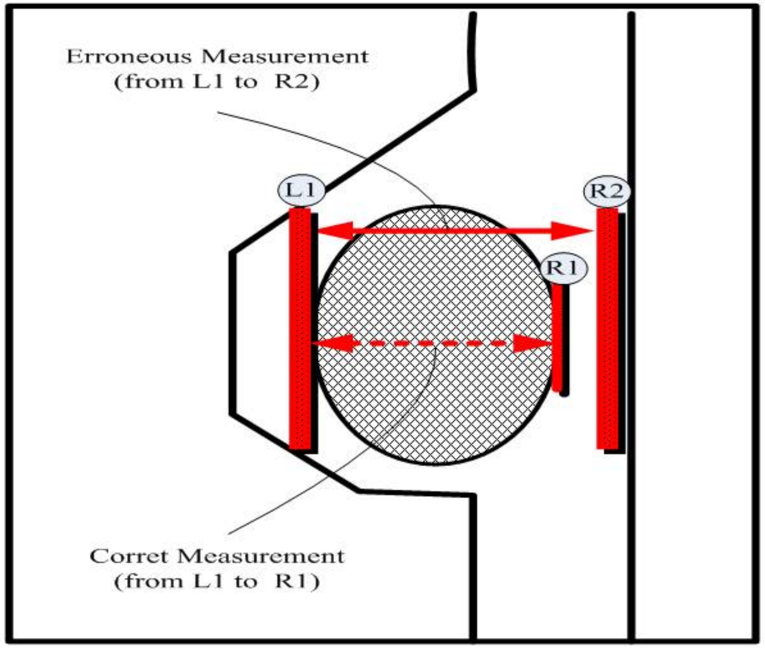
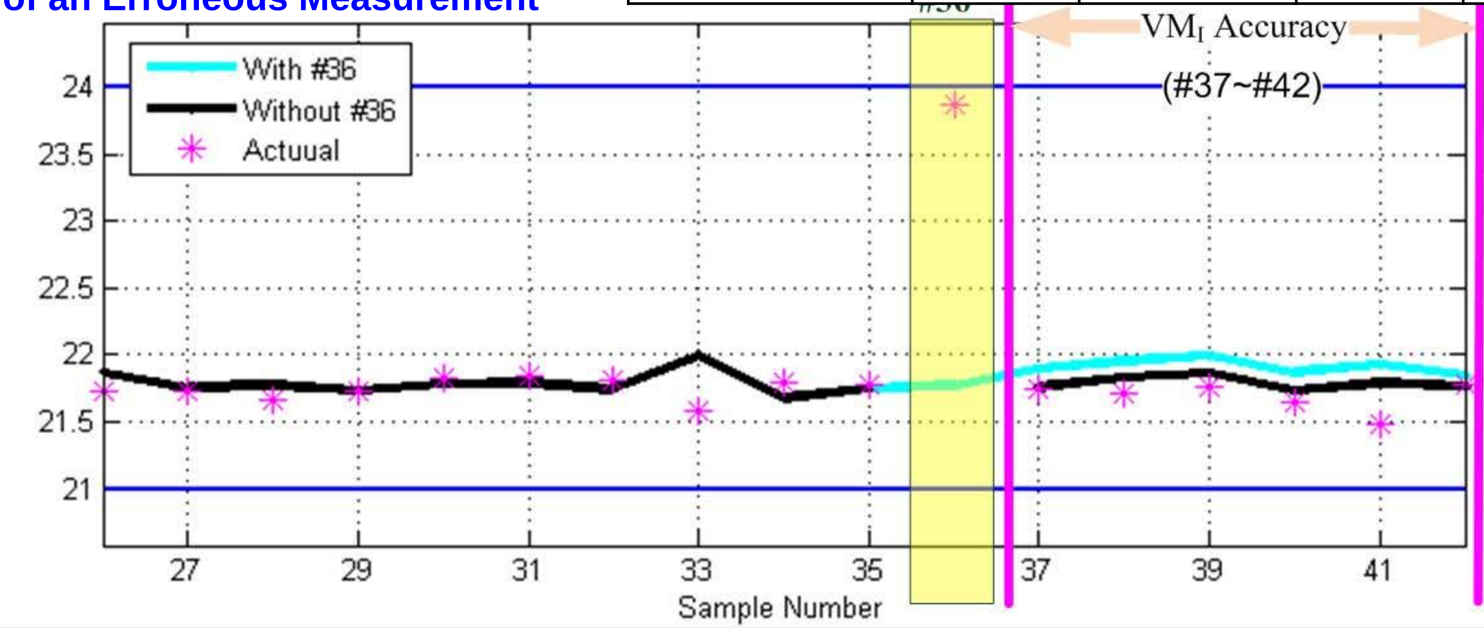


Example of an Erroneous Measurement

VM Accuracy with and without Metrology Abnormal Data

#37~#42 VM Accuracy (%)	BPNN			
	VM_I		VM_{II}	
	MAPE	Max Error	MAPE	Max Error
With #36	1.1108	2.1814	0.9695	1.8991
Without #36	0.7571	1.8009	0.6507	1.5321



Effects on VM Accuracy with and without Metrology Abnormal Data

AVM Novelty 4: Automatic Fanning Out and Model Refreshing [8][C]

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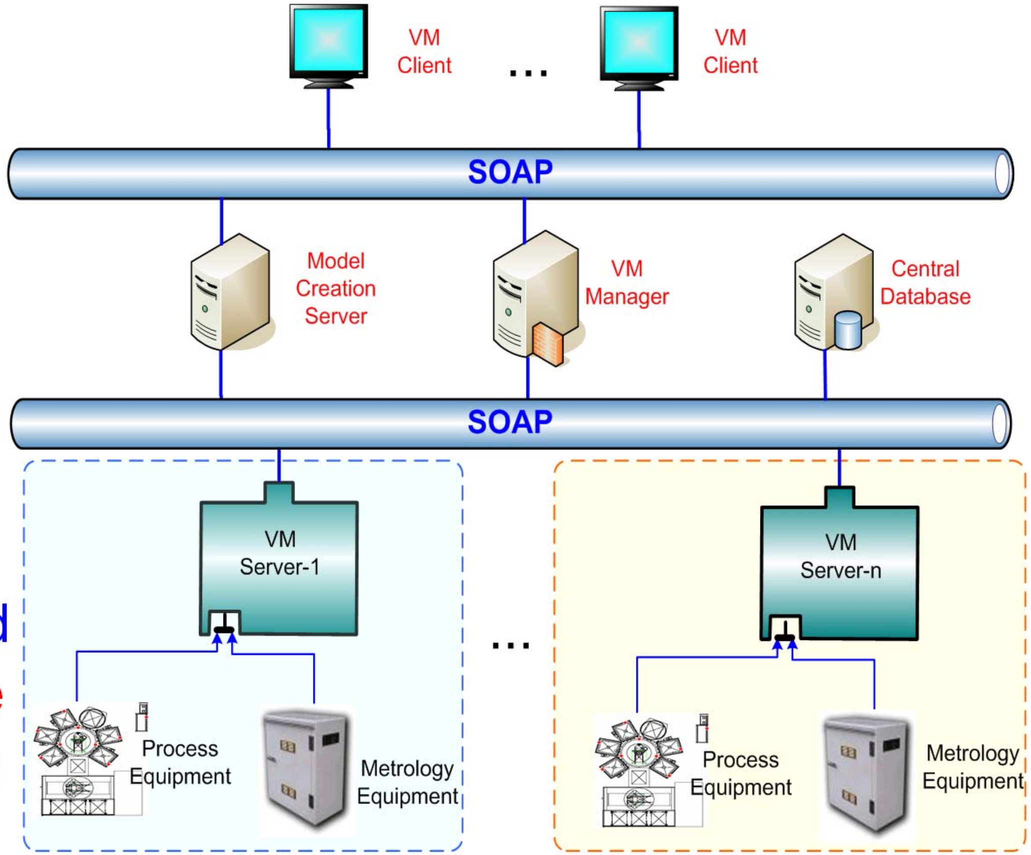
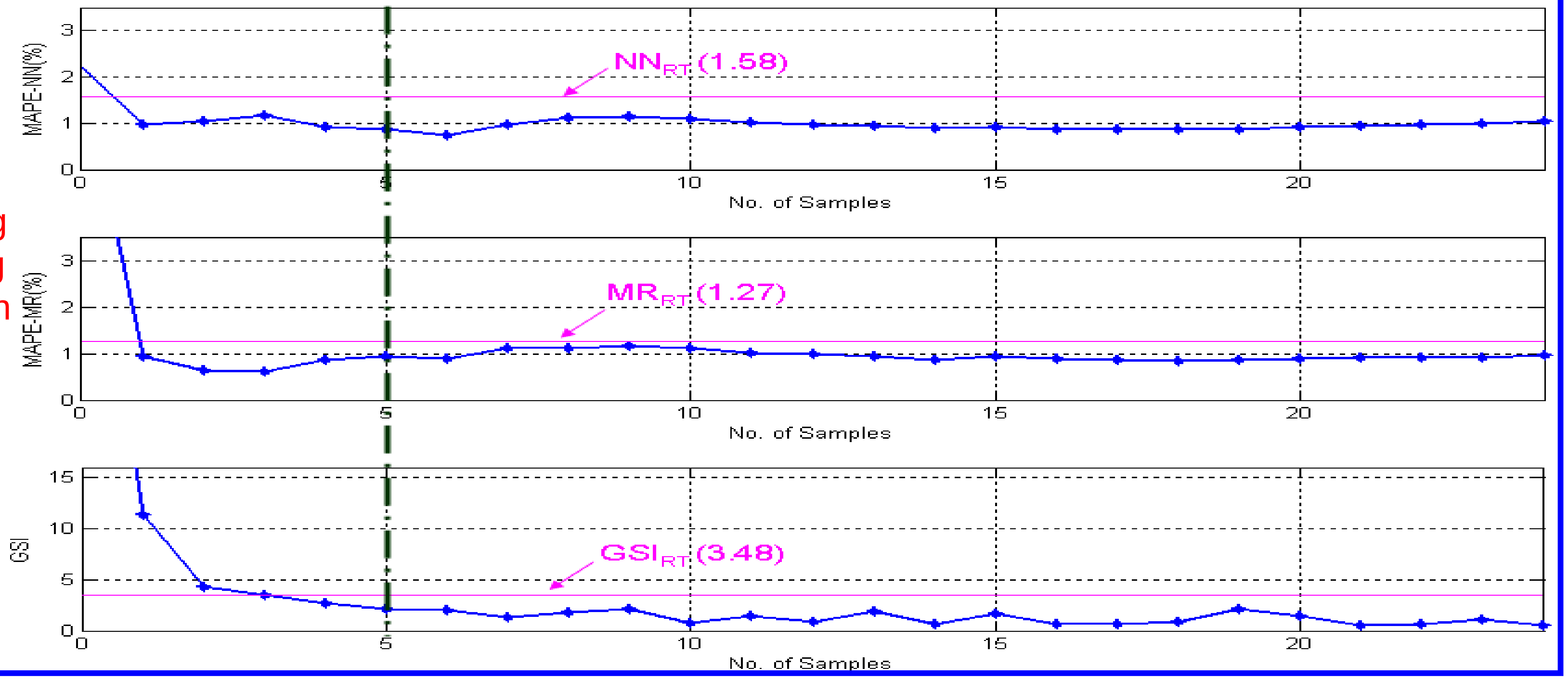
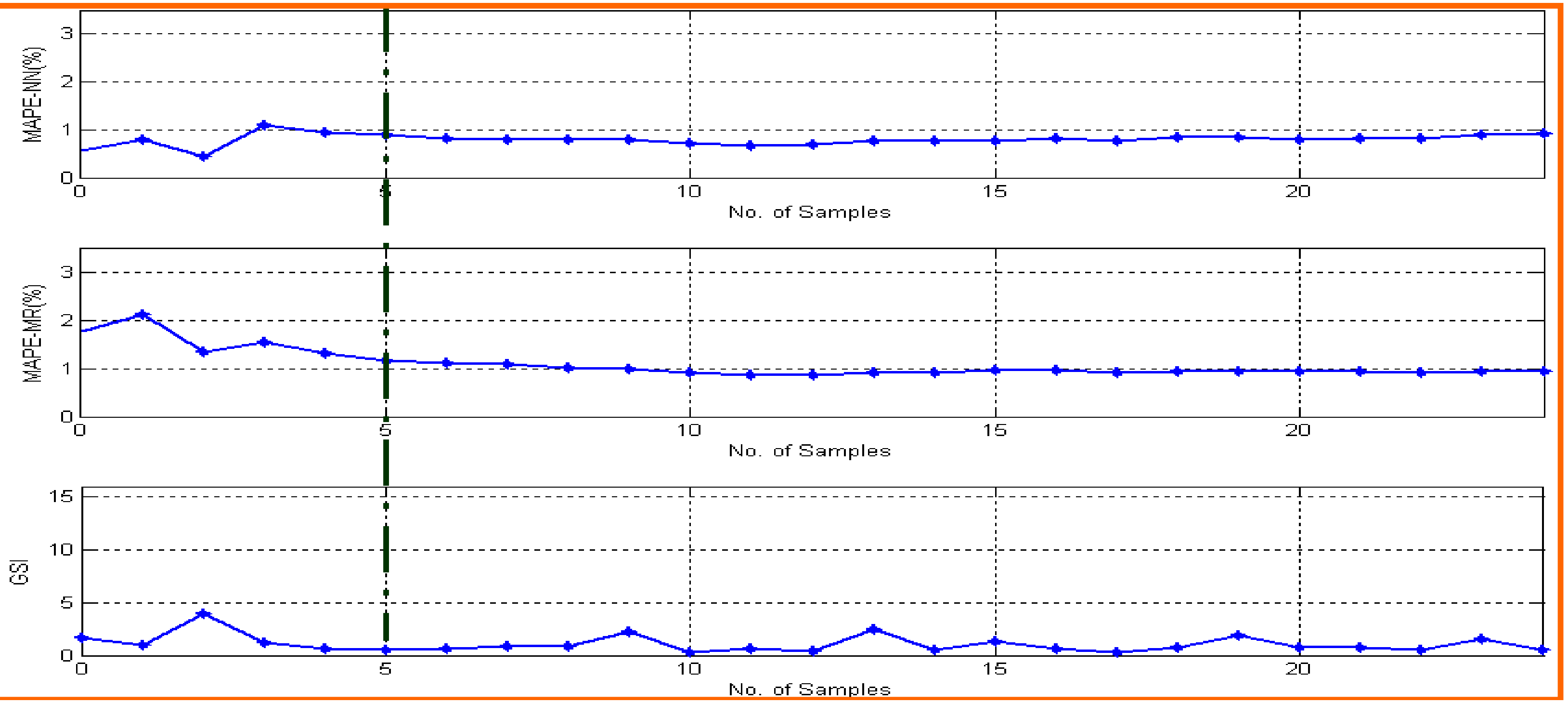
- The AVM system possesses automatic fanning out and model refreshing capabilities to enable VM models of a specific chamber to be propagated and refreshed to other chambers of the same type of tools for maintaining VM accuracy of all chambers while saving tremendous labor expenses and model-creation time. Hence, the AVM system facilitates fab-wide VM implementation possible.



Performing Refreshing Process on Ch F with Ch A's Models [8]



Ch F VM Results with the VM Models Built by Ch F Itself [8]



AVM Novelty 5: AVM System Integration Framework [10]

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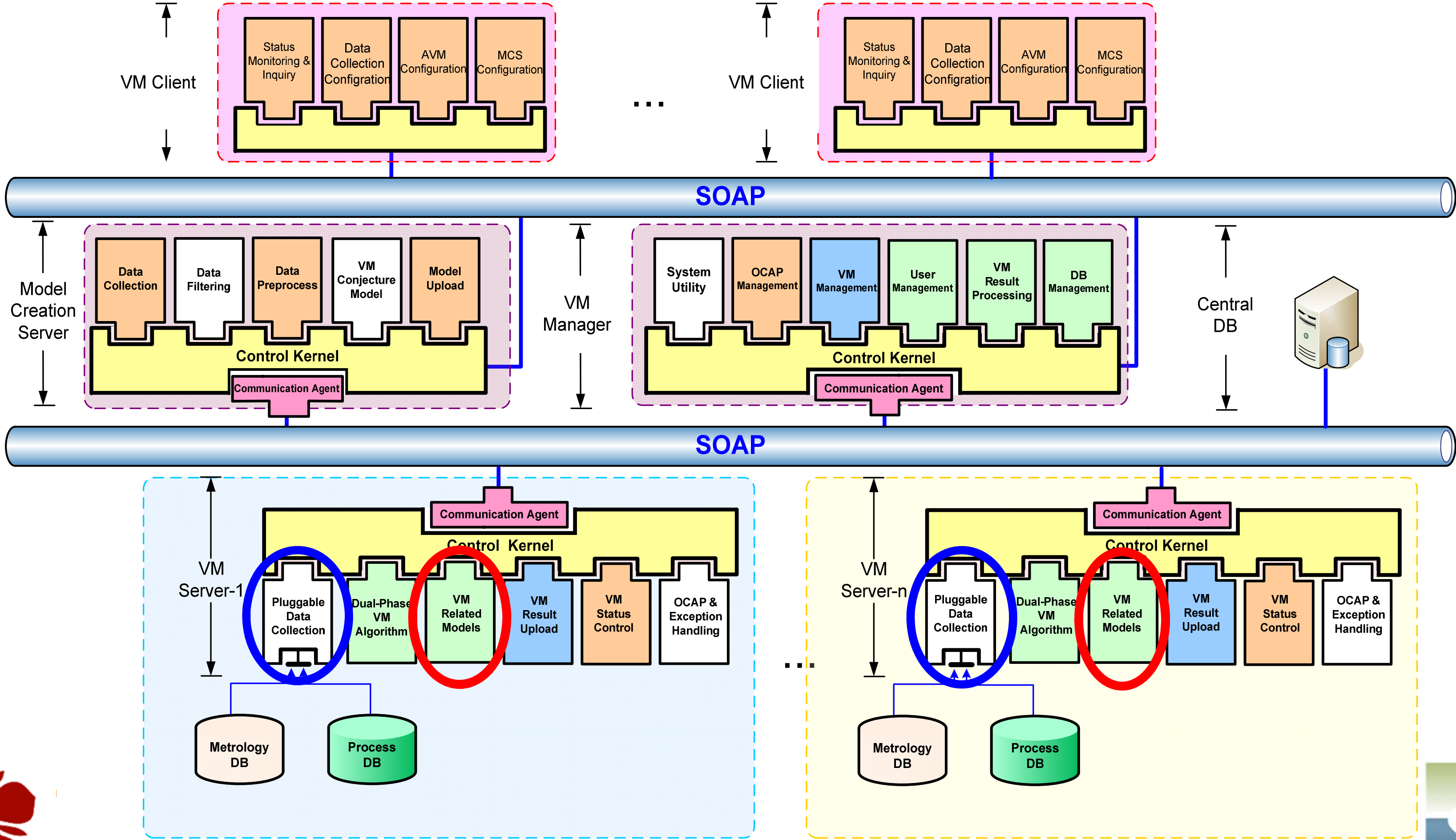
- The proposed AVMSIF can allow the complex AVM system to be created in a systematic and easy manner. Also, by adopting plug-and-play interfaces and desired functional modules, the AVMSIF can be applied to different types of equipment in the factory-wide VM deployment and can adopt best-of-breed VM-related models.



AVM Novelty 6: Integrating AVM into MES [6] [D]

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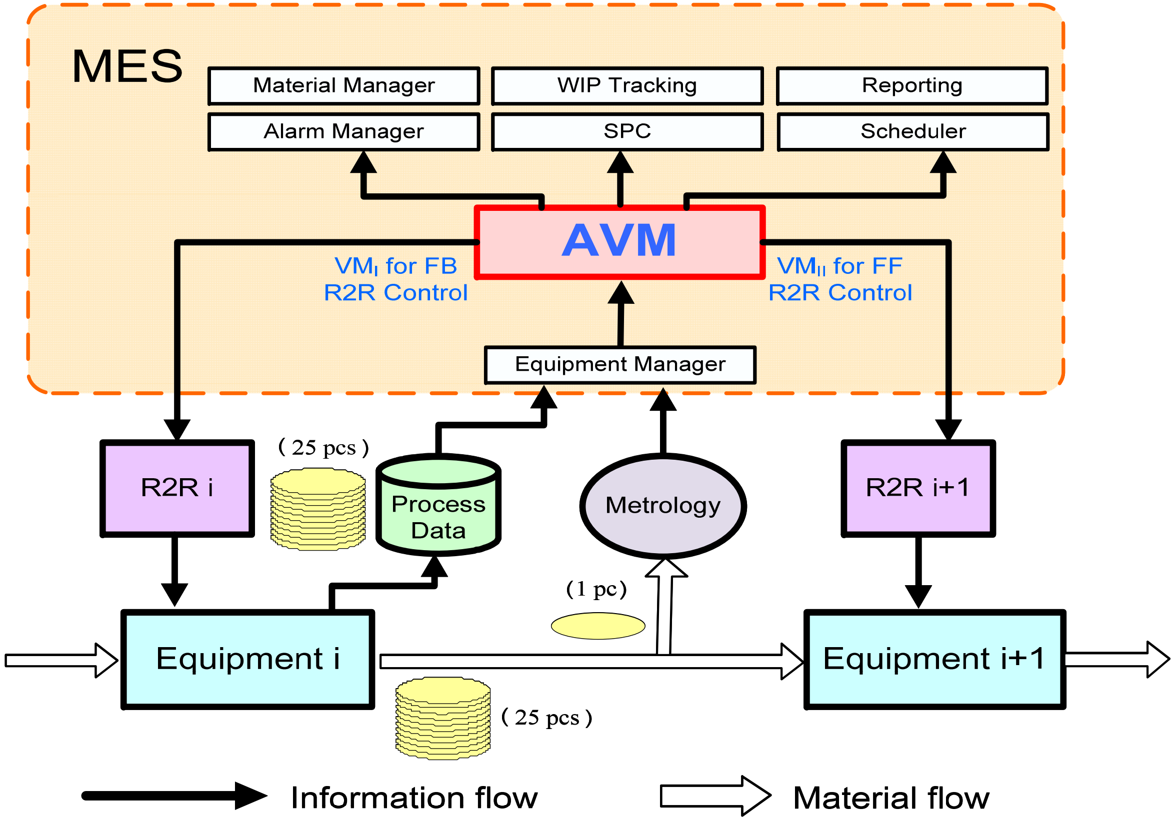
- The purpose is to integrate the functions of AVM with those of MES. The interfaces among AVM, other MES components, and R2R (run-to-run) modules in the novel manufacturing system are defined so that the total quality inspection system can be realized and the R2R capability can be migrated from lot-to-lot control to wafer-to-wafer control.



AVM Novelty 7: APC Utilizing AVM with RI/GSI [11] [13] [E]

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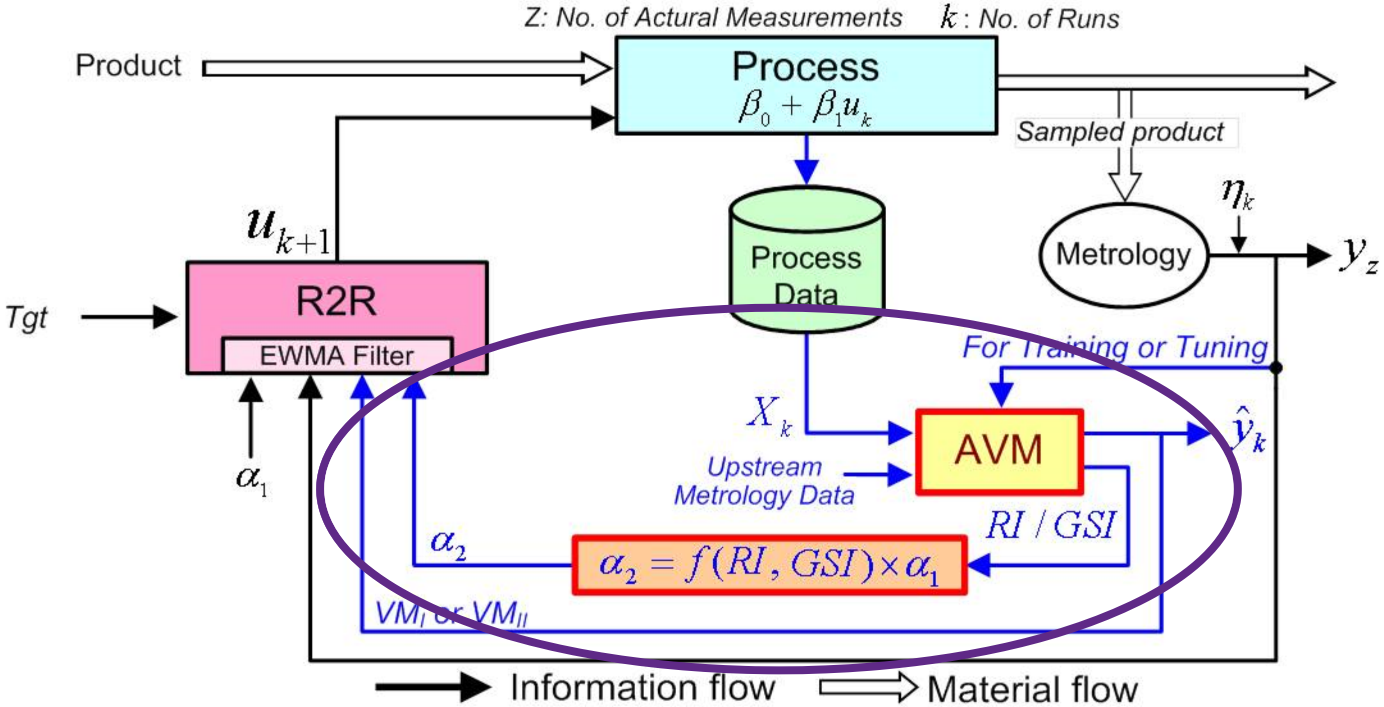
- A key challenge preventing effective utilization of VM in R2R control is the inability to take the reliance level in the VM feedback loop of R2R control into consideration. The reason is that adopting an unreliable VM value may be worse than if no VM is utilized. The AVM system possesses the RI of VM to gauge the reliability of VM results [2], [A]. Therefore, this novelty is to invent a novel scheme of R2R control that utilizes AVM with RI/GSI in the feedback loop. Successful results will appear in [11] & [13].



R2R Controller with $\alpha_2 = f(RI, GSI) \times \alpha_1$ [11] [E]

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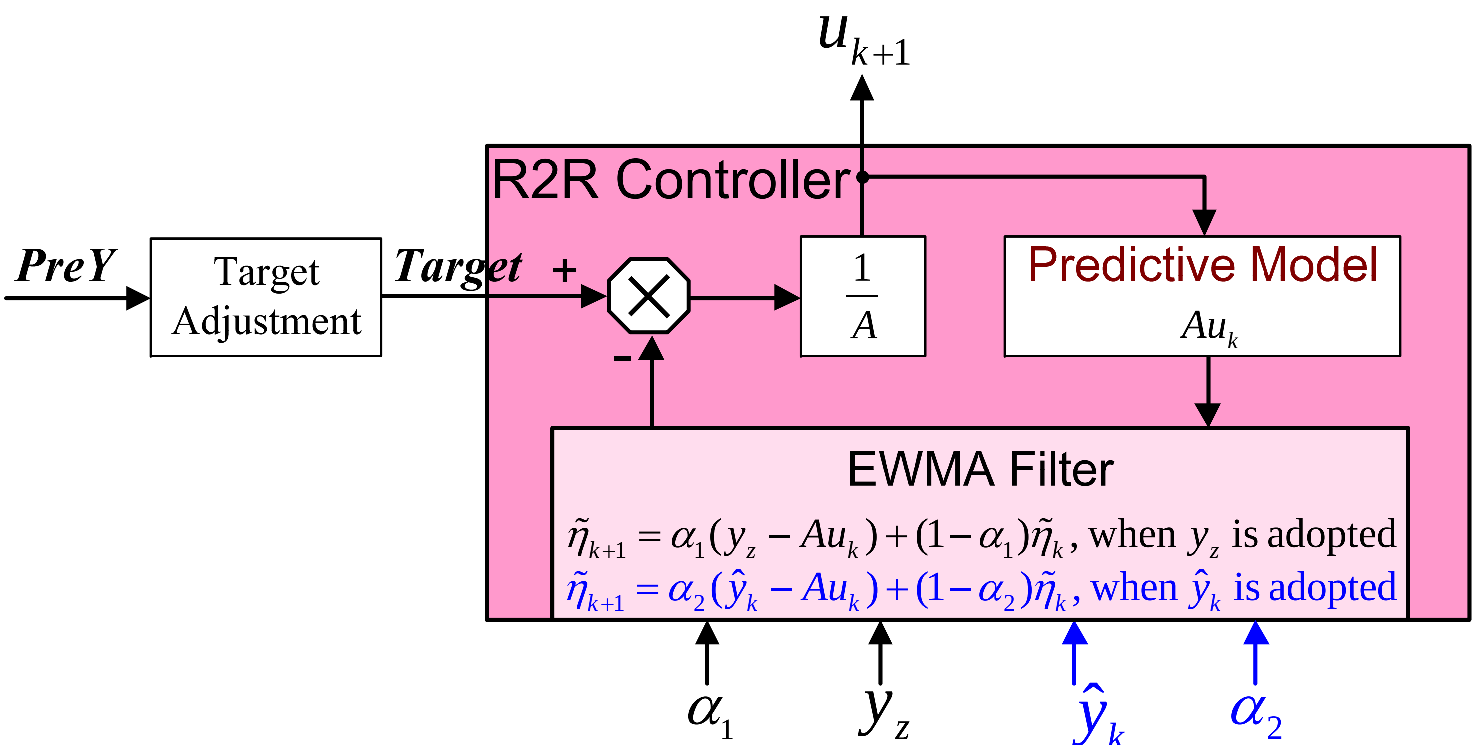
$$f(RI,\ GSI) = \begin{cases} 0, \text{ if } RI < RI_T \text{ or } GSI > GSI_T \\ RI, \text{ if } RI \geq RI_T \text{ and } GSI \leq GSI_T \text{ and for } k \leq C \\ 1\text{-}RI, \text{ if } RI \geq RI_T \text{ and } GSI \leq GSI_T \text{ and for } k > C \end{cases}$$



Mean $MAPE_P$ Curves as functions of α_1 of 5-Cases APC Methods [11] [E]

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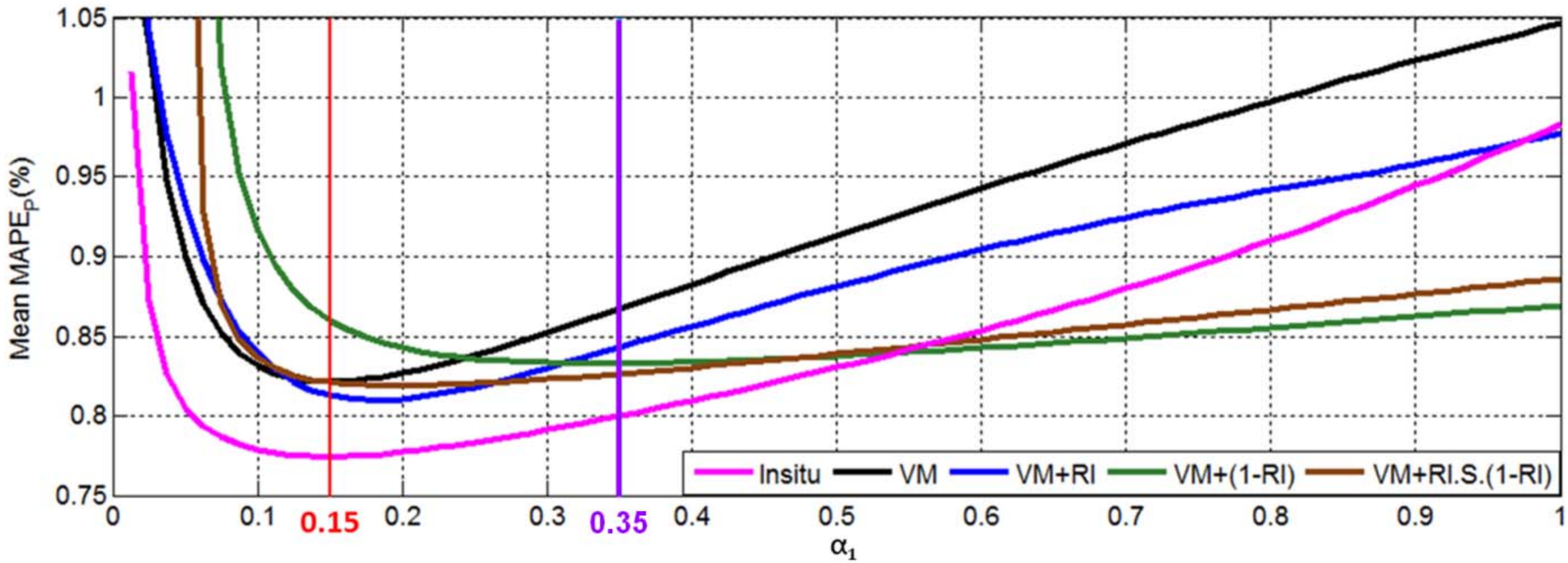
Case 1 (Insitu): R2R with in-situ metrology
Case 2 (VM): R2R+VM without RI
Case 3 (VM+RI): R2R+VM with RI
Case 4 (VM+1-RI) : R2R+VM with (1-RI)
Case 5 (VM+RI.S.(1-RI)): R2R+VM with RI.S.(1-RI)



The Verification Results of the NSC Project entitled:
"Developing APC with AVM for ARC Quality Improvement of Solar Cells"(1/2)

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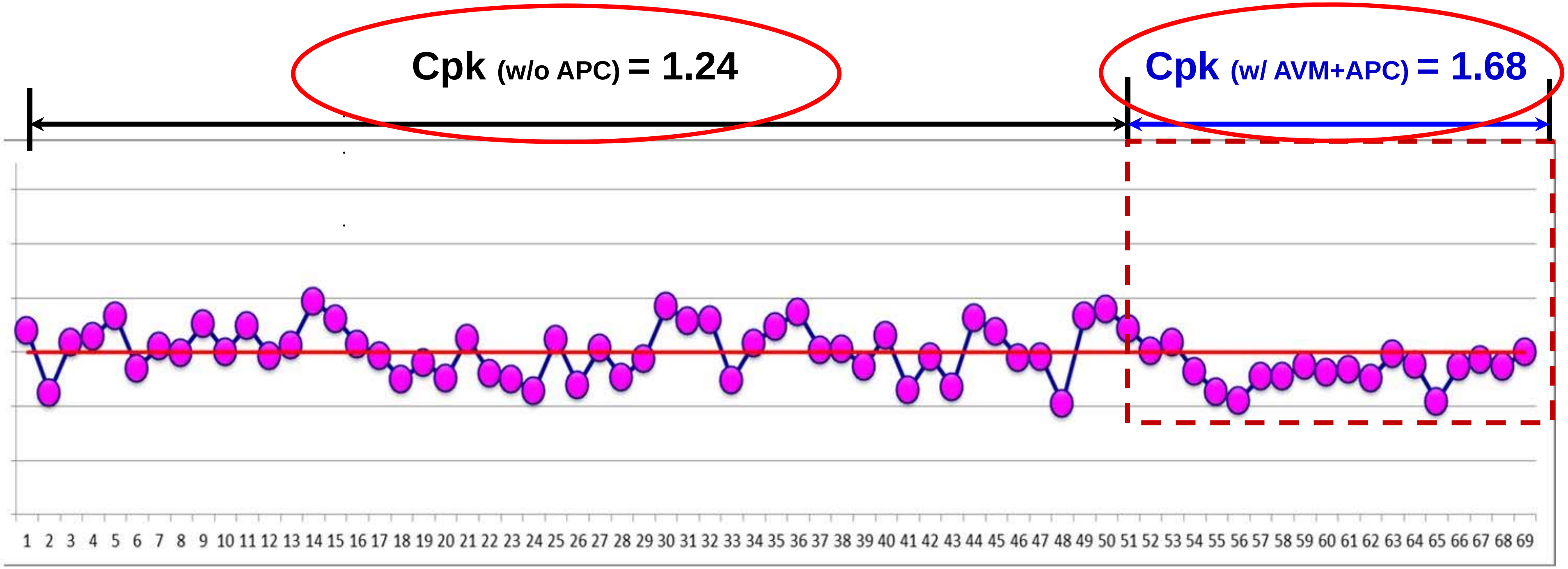

$$\mathrm{Cpk} = \min\{\frac{USL - \mu}{3\sigma}, \frac{\mu - LSL}{3\sigma}\}$$

The Verification Results of the NSC Project entitled:
"Developing APC with AVM for ARC Quality Improvement of Solar Cells"(2/2)

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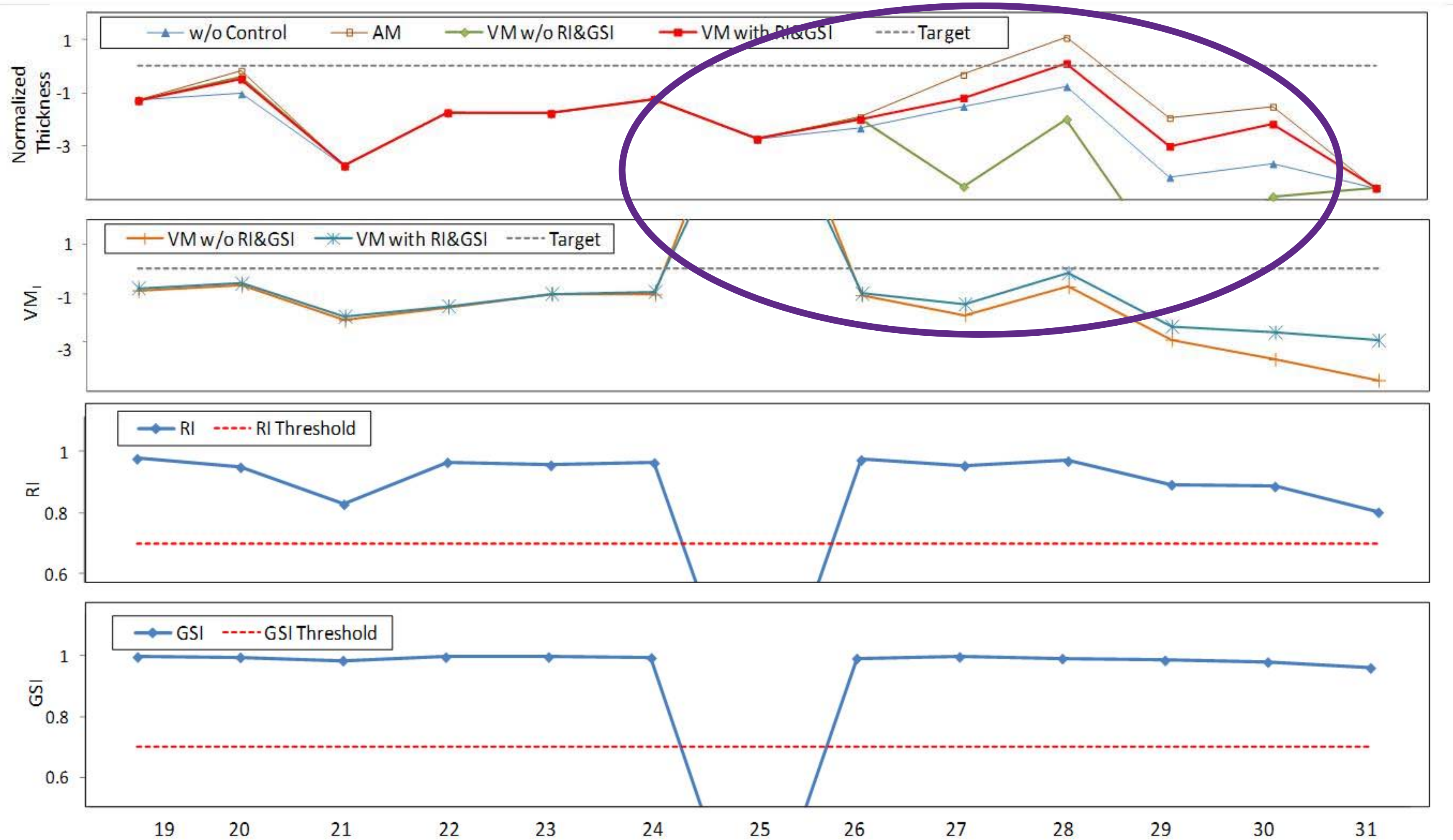

RI and GSI are lower than RI_T and GSI_T, Respectively at Sample 25 [13]

AVM – A Fully Automated VM Solution

- After surveying all VM systems available on the web and in the market, it was found that most of the VM systems can only reach Level 1 or Level 2; while the AVM system [A], [B], [C] has reached the highest level – Level 3. Therefore, only the AVM system possesses the fully automated and fab-wide implementation capability to meet the real production needs. Further, an AVM System Implementation Framework (AVMSIF) has also been developed and deployed in various high-tech factories [10].

Level of VM Deployment and Degree of Automation [8]

Level 3 – Full Automation (AVM)
Automatic Data Quality Evaluation, Automatic Fanning Out, & Model Refreshing; Supporting APC

The AVM System

Level 2 – Pluggability
Pluggable Designs for Models & Data Collections

Level 1 – On-Line Conjecturing
On-Line Data Collection, On-Line Learning, & Real-Time Conjecturing with Remote Monitoring

Level 0 – Off-Line Analysis and Modeling
Off-Line Data Collection, Data Analysis, Data Preprocessing, & Model Creation

Other Commercialized VM Systems

Verification and Implementation Results of the AVM System

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- Based on the AVMSIF framework, the AVM system has been physically implemented as a commercial product and has successfully been deployed in production lines of various companies [10]. The verification results are described below:
  - **Semiconductor**

    TSMC's Fab 14 via technology transfer (Contract No.: NSC-N-095-00037) in 2007. Portions of the verification results were published in [2], [3], and [4]. And, **UMC's Fab 12A** via technology transfer (Contract No.:NSC-N-102-00049) in 2013.
  - **TFT-LCD**

    CMO's 5th and 6th Fabs through two National Science Council (NSC) industry-university cooperation projects and technology transfers (Contract Nos.: NSC-N-095-00027, NSC-I-097-00015, NSC-N-098-00099, etc.) during 2006 to 2010. Portions of the verification results were published in [3], [5], [7], [8], and [9].
  - **Solar-Cell**

    Motech Inc. via technology transfer (Contract No.: NSC-N-099-00031) and the NSC projects entitled: "Applying AVM Technology for ARC Yield Improvement of Solar Cell" in 2010 and "Developing APC with AVM Technology for ARC Quality Improvement of Solar Cells" in 2011. The final on-line verification results show that the Cpk of the ARC process can improve at least 20 %. Preliminary results were presented at ISSM 2011; and the complete results are shown in [13].

Introducing the TFT-LCD Production Tools and Manufacturing Processes

- TFT Process
- CF Process
- LCD Process

Process Flow of TFT-LCD Manufacturing 1/2

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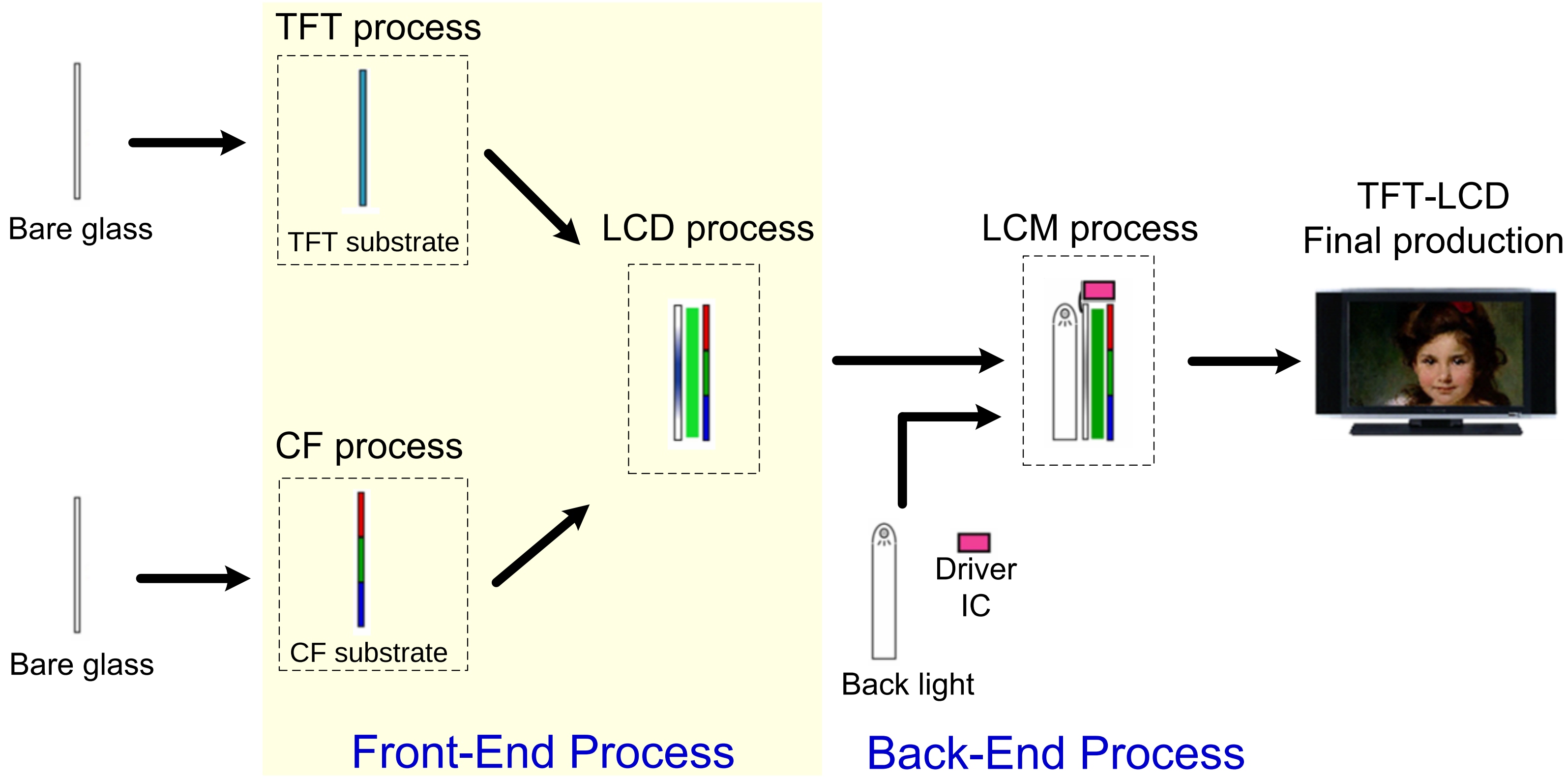
- The TFT-LCD manufacturing flow consists of four processes: TFT, CF (color filter), LCD, and LCM (liquid crystal module).



Process Flow of TFT-LCD Manufacturing 2/2

- TFT process： The transistors are fabricated on a piece of glass substrate.
- CF process ： Color sources including red, green, and blue are produced on a glass.
- LCD process ：TFT substrate is joined with a CF substrate.
- LCM process ： Additional components, such as driver integrated circuits and backlight units, are connected to comprise the final fabricated product.

TFT Process

Semiconductor Layer of the TFT Process Flow with Deployment of AVM Servers

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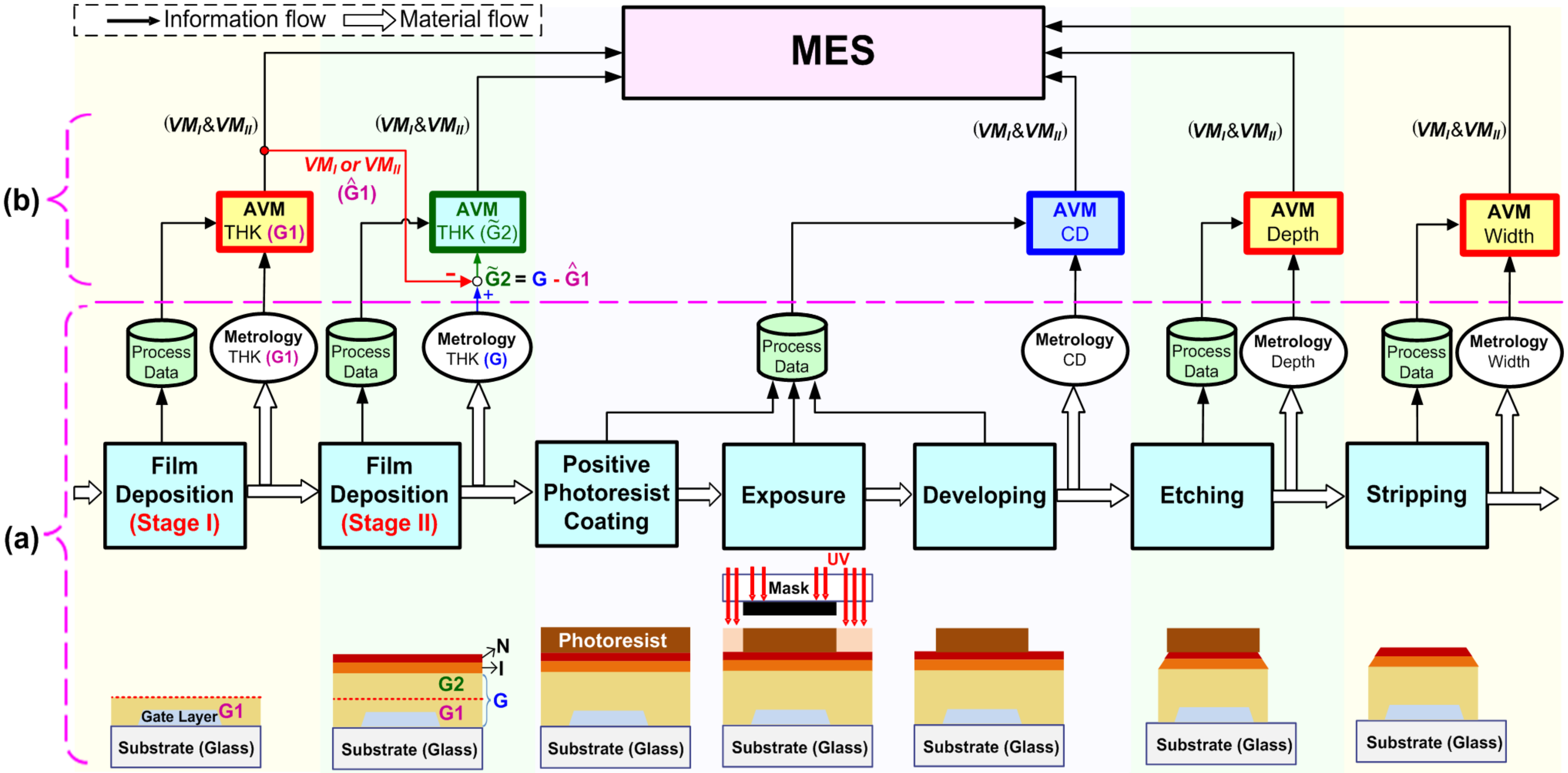

(a) Semiconductor Layer Process Flow. (b) Deployment of AVM Servers.

Thin-Film Structure in CVD Process

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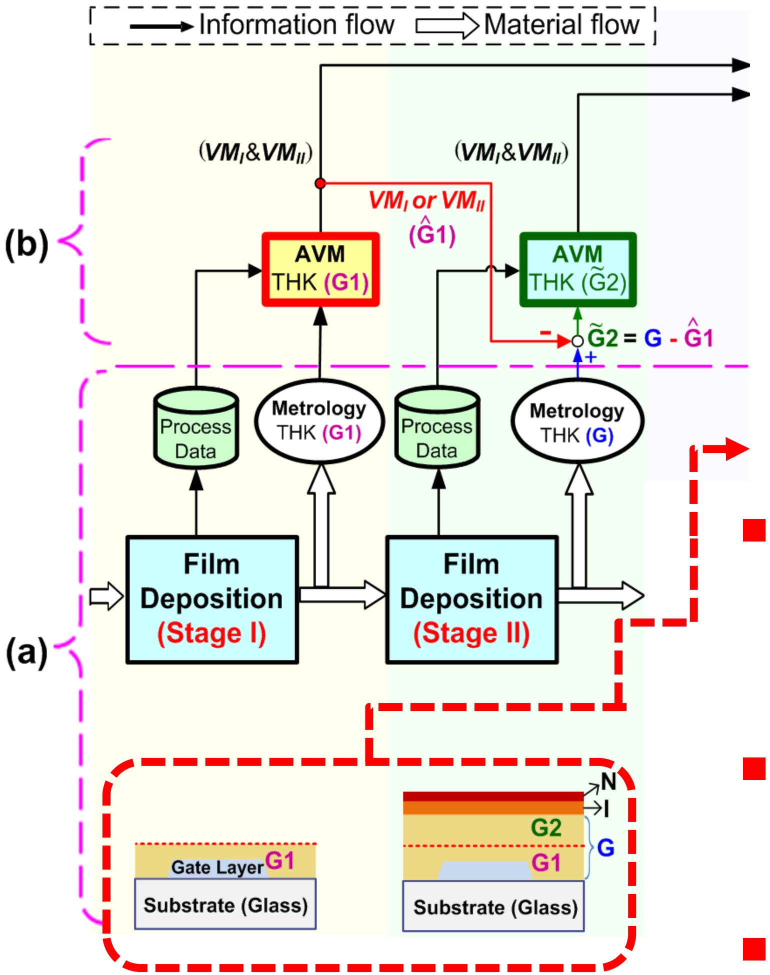

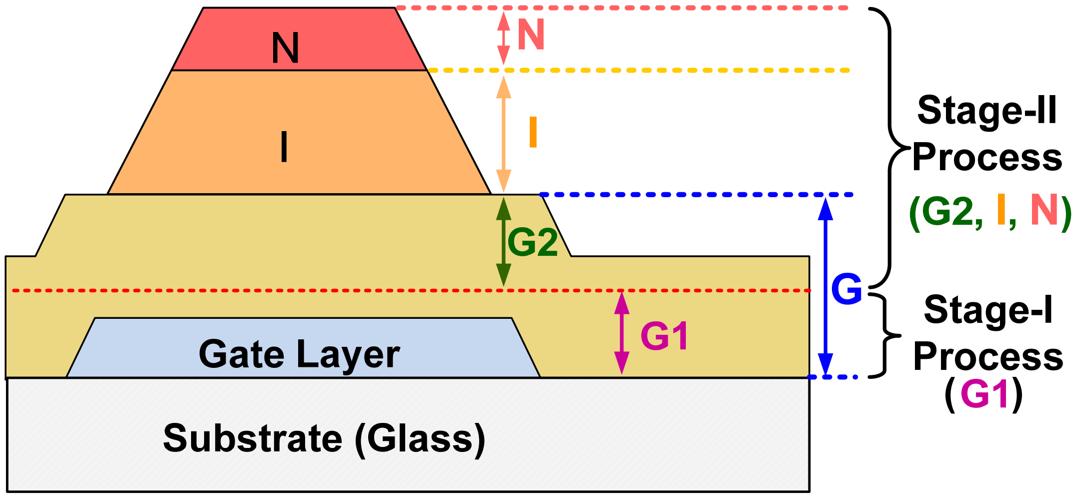

- G layer: Serves as a gate insulator that comprises silane, ammonia, and nitrogen. The G layer is further decomposed into two layers, G1 and G2, to enhance the production yield
- I layer: which contains intrinsic amorphous silicon, is formed via the CVD reaction between silane and hydrogen.
- N layer: which contains n-plus amorphous silicon, is deposited with silane, hydrogen, and phosphine.

Combination of TFT Photo Step

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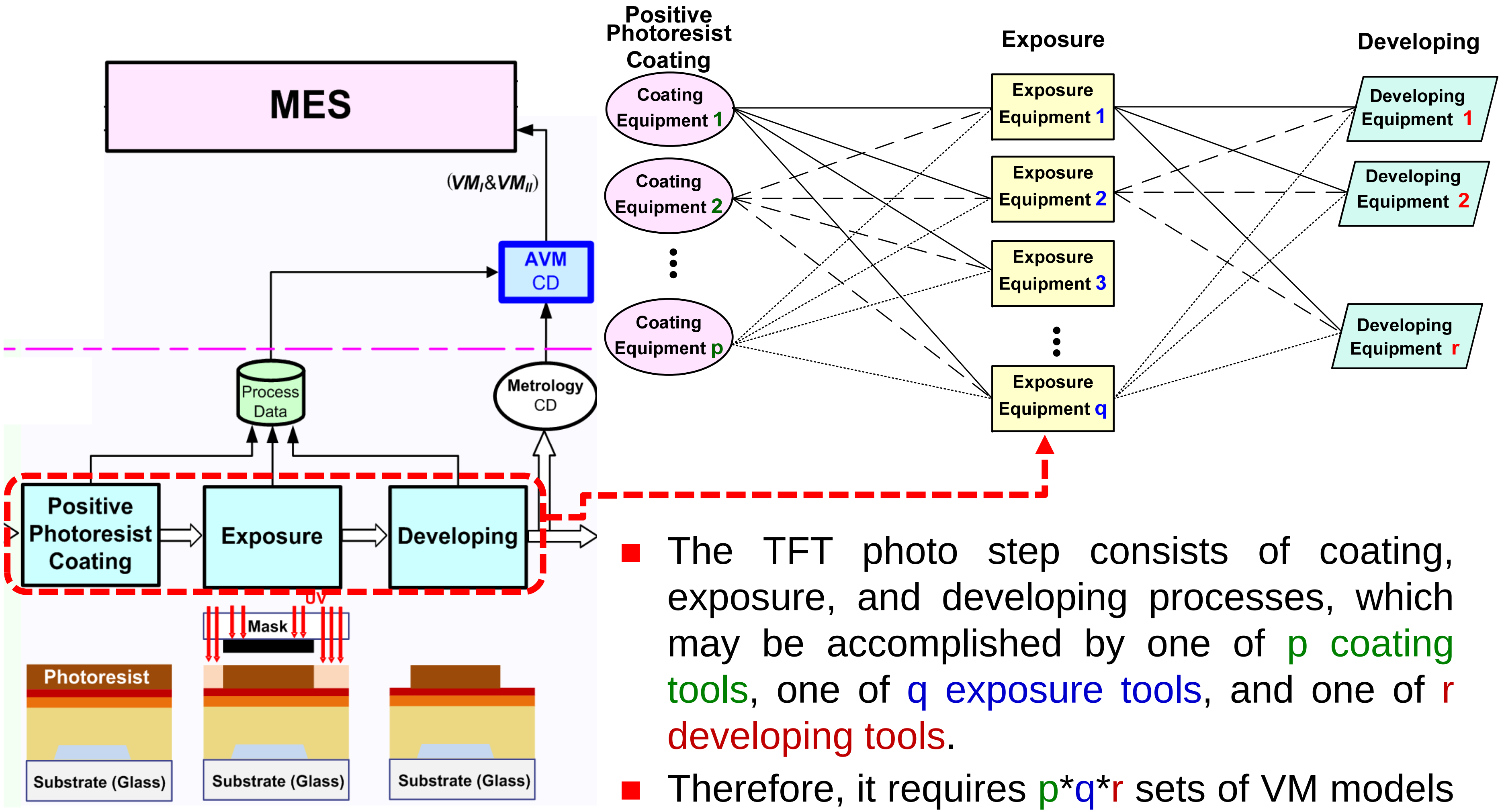

- The TFT photo step consists of coating, exposure, and developing processes, which may be accomplished by one of p coating tools, one of q exposure tools, and one of r developing tools.
- Therefore, it requires p*q*r sets of VM models to maintain the accuracy of VM conjecturing.

Semiconductor Layer of the TFT Process Flow with Deployment of AVM Servers

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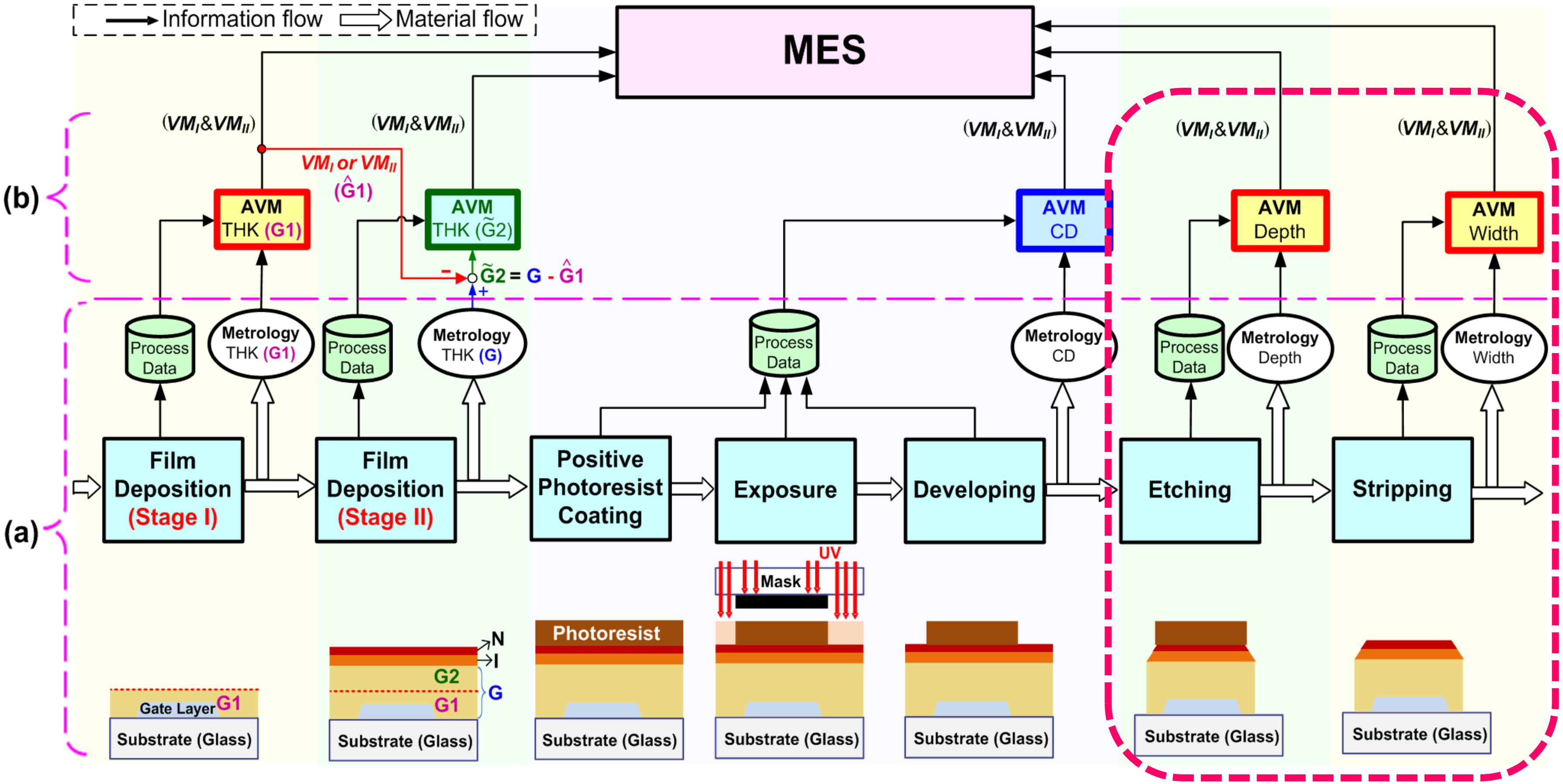

(a) Semiconductor Layer Process Flow. (b) Deployment of AVM Servers.

CF Process

CF Manufacturing Process Flow with Deployment of AVM Servers 1/2

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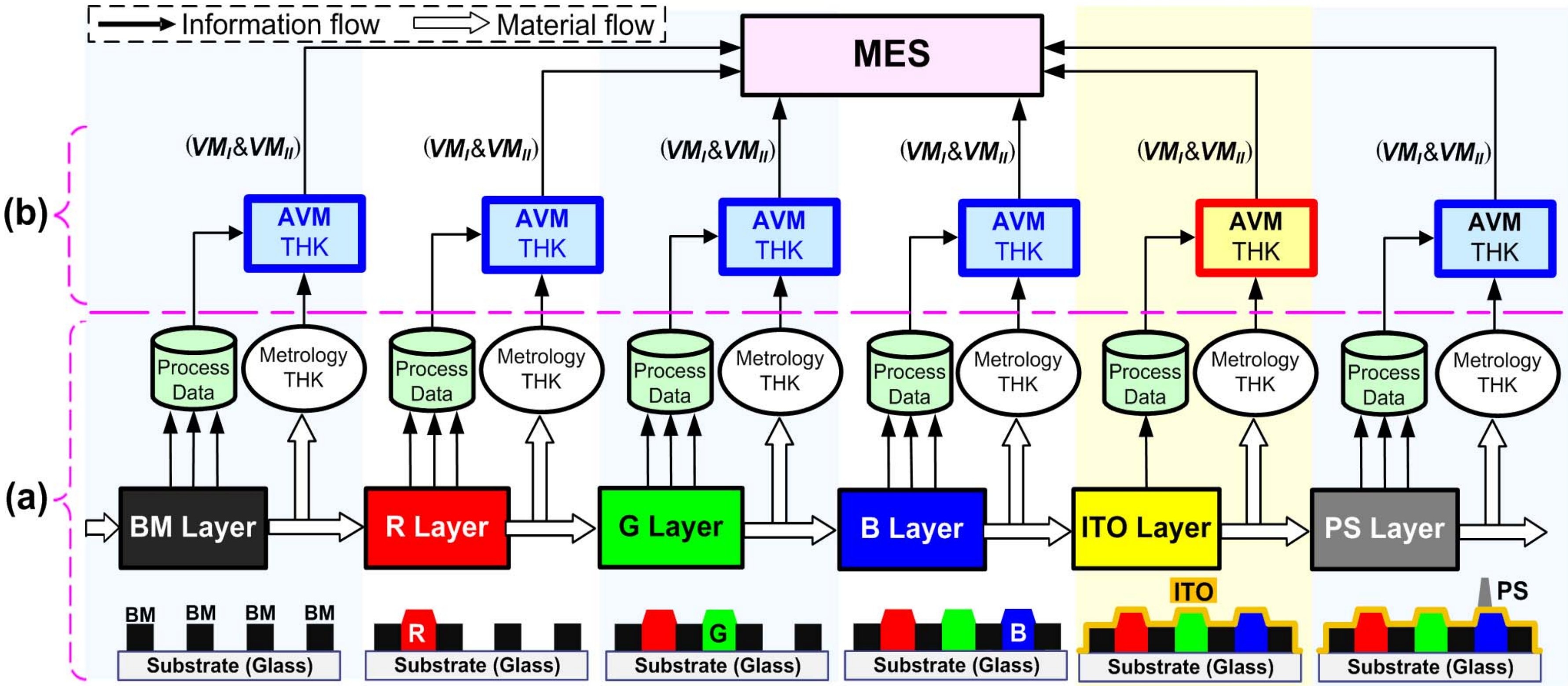
- The CF manufacturing process includes black matrix (BM), red (R), green (G), blue (B), indium tin oxide (ITO), and photo space (PS) layers.



(a) CF Manufacturing Process Flow. (b) Deployment of AVM Servers.

CF Manufacturing Process Flow with Deployment of AVM Servers 2/2

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- BM ： BM covers the light leak of TFT; R, G, and B generate colors
- ITO ： ITO controls the direction of crystal
- PS ：PS is the support between TFT and CF.
- Except for the ITO layer, the processes of the other ones are the same as those of the TFT photo step.

PS Layer Flow with Deployment of AVM Servers

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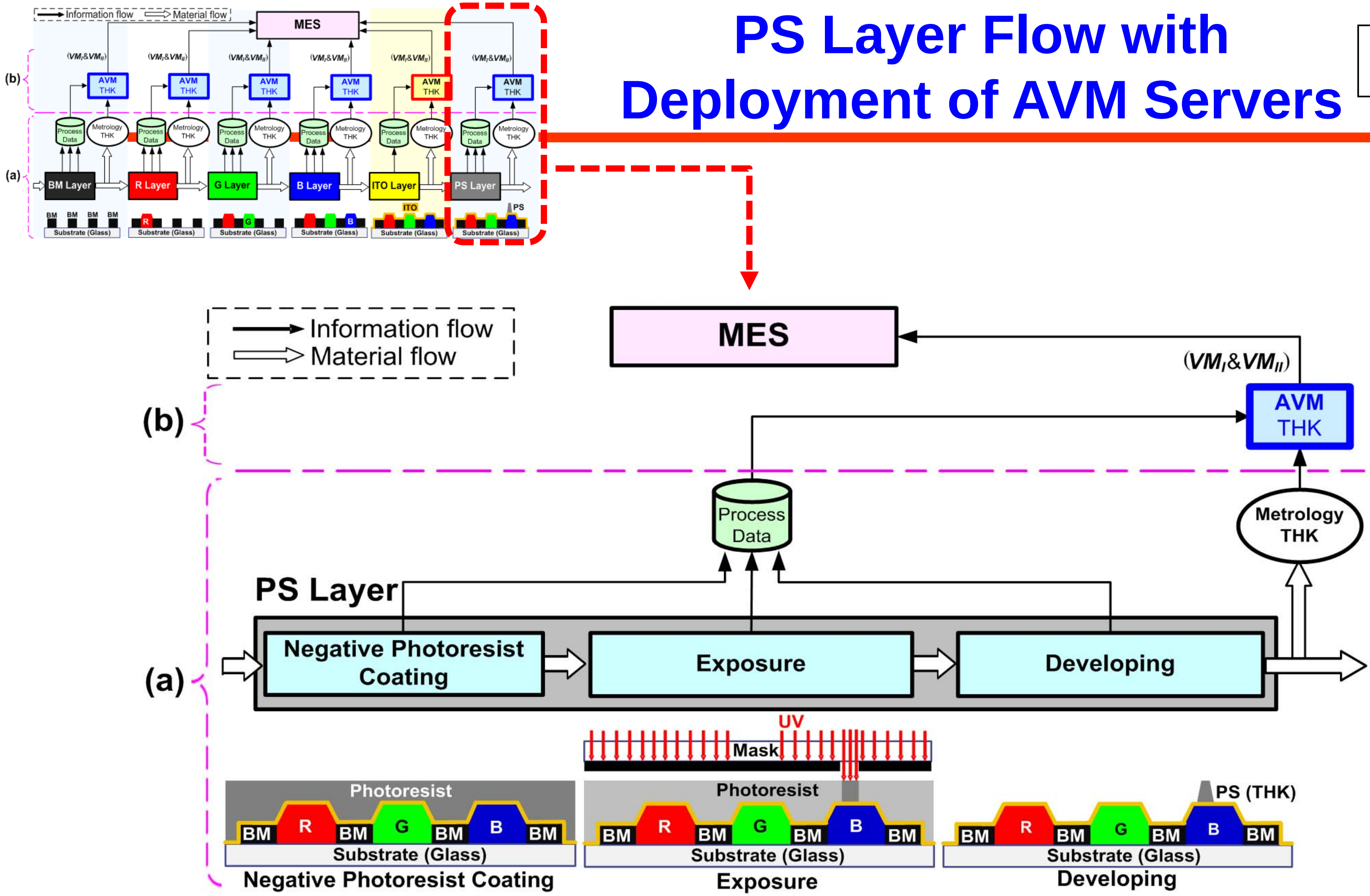

(a) CF Manufacturing Process Flow. (b) Deployment of AVM Servers.

LCD Process

LCD Manufacturing Process Flow with Deployment of AVM Servers

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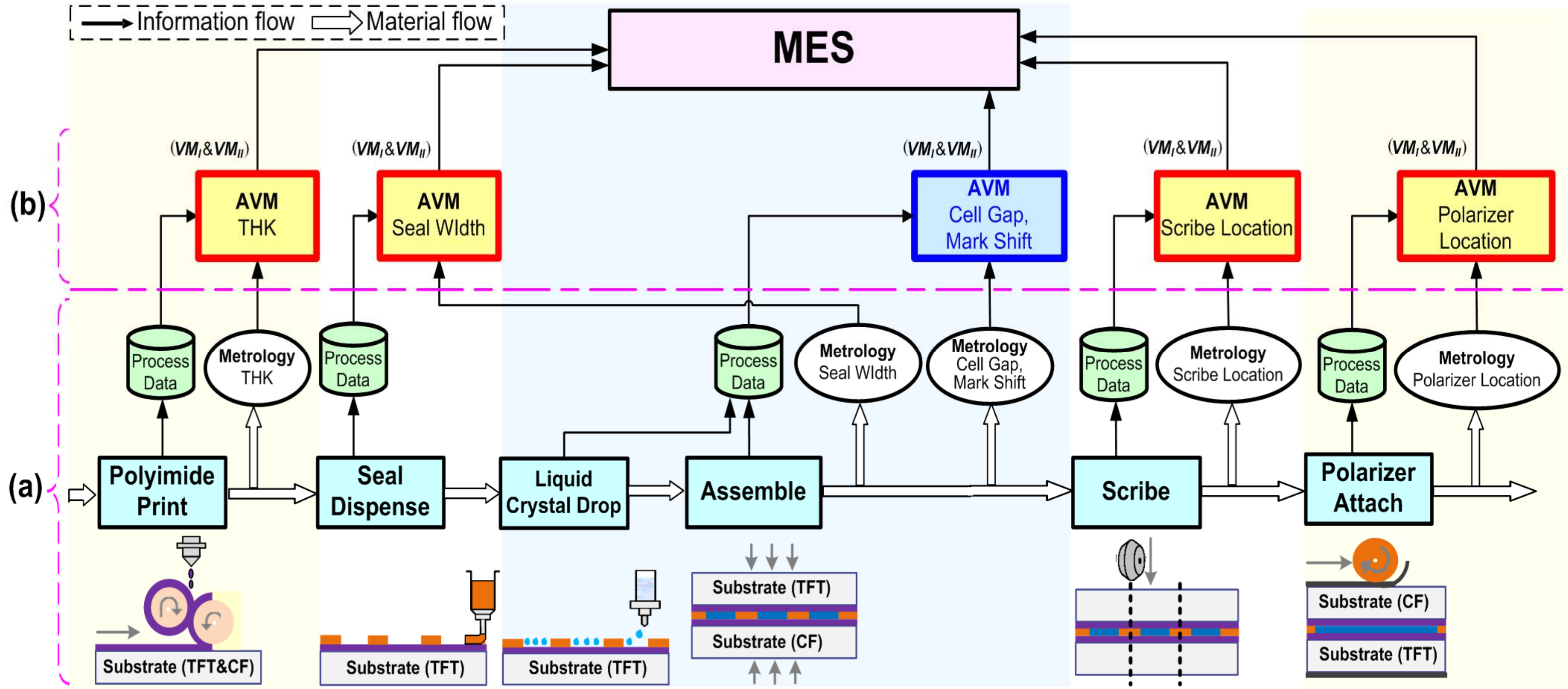

(a) LCD Manufacturing Process Flow. (b) Deployment of AVM Servers.

AVM Deployment Types for TFT-LCD Manufacturing

- Single-Stage VM Deployment
- Dual-Stage VM Deployment
- Cooperative-Tools VM Deployment
  - Combination
  - Inline
- Concept of a Virtual Cassette

Single-Stage VM Deployment

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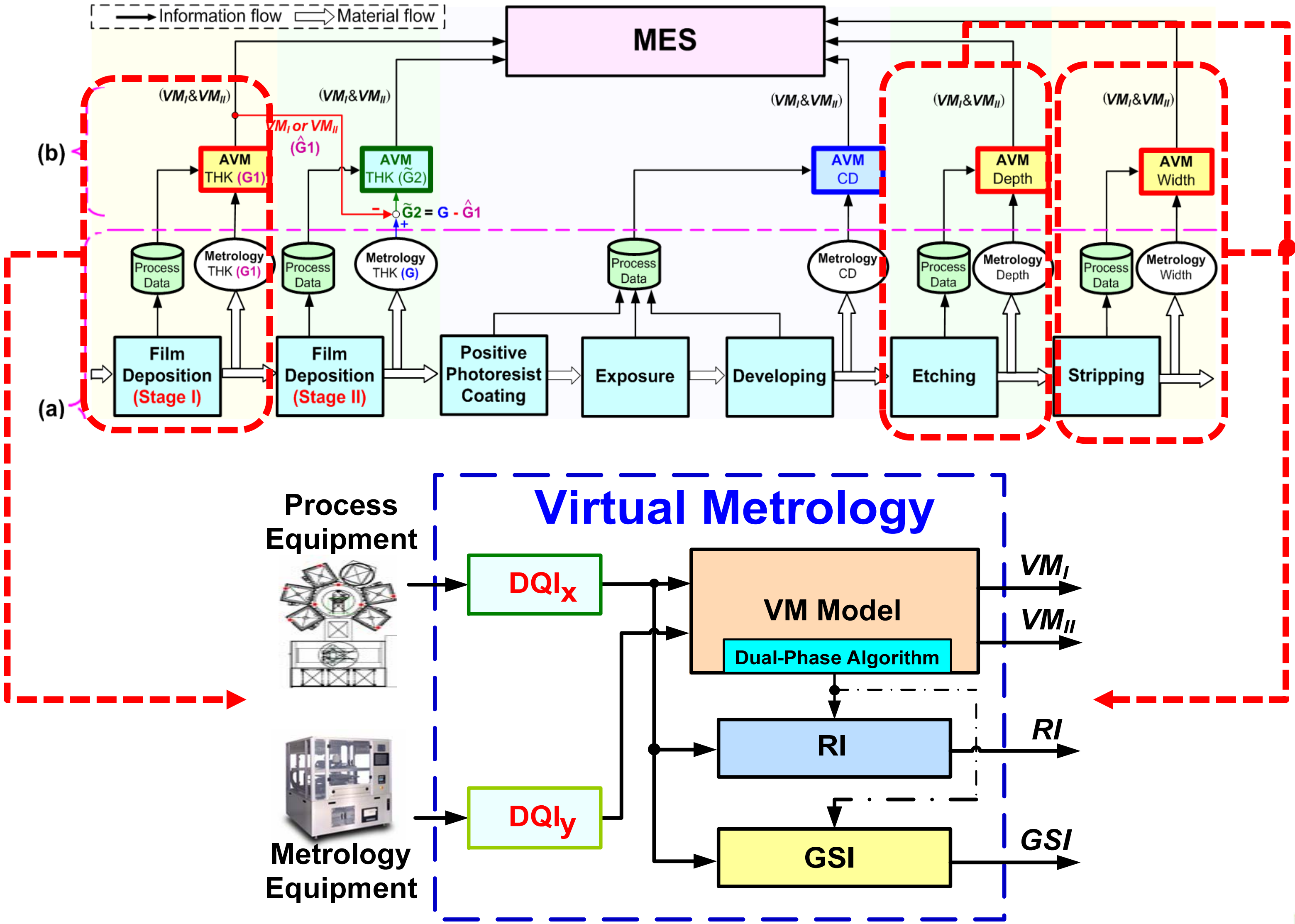
不可外流



Dual-Stage VM Deployment

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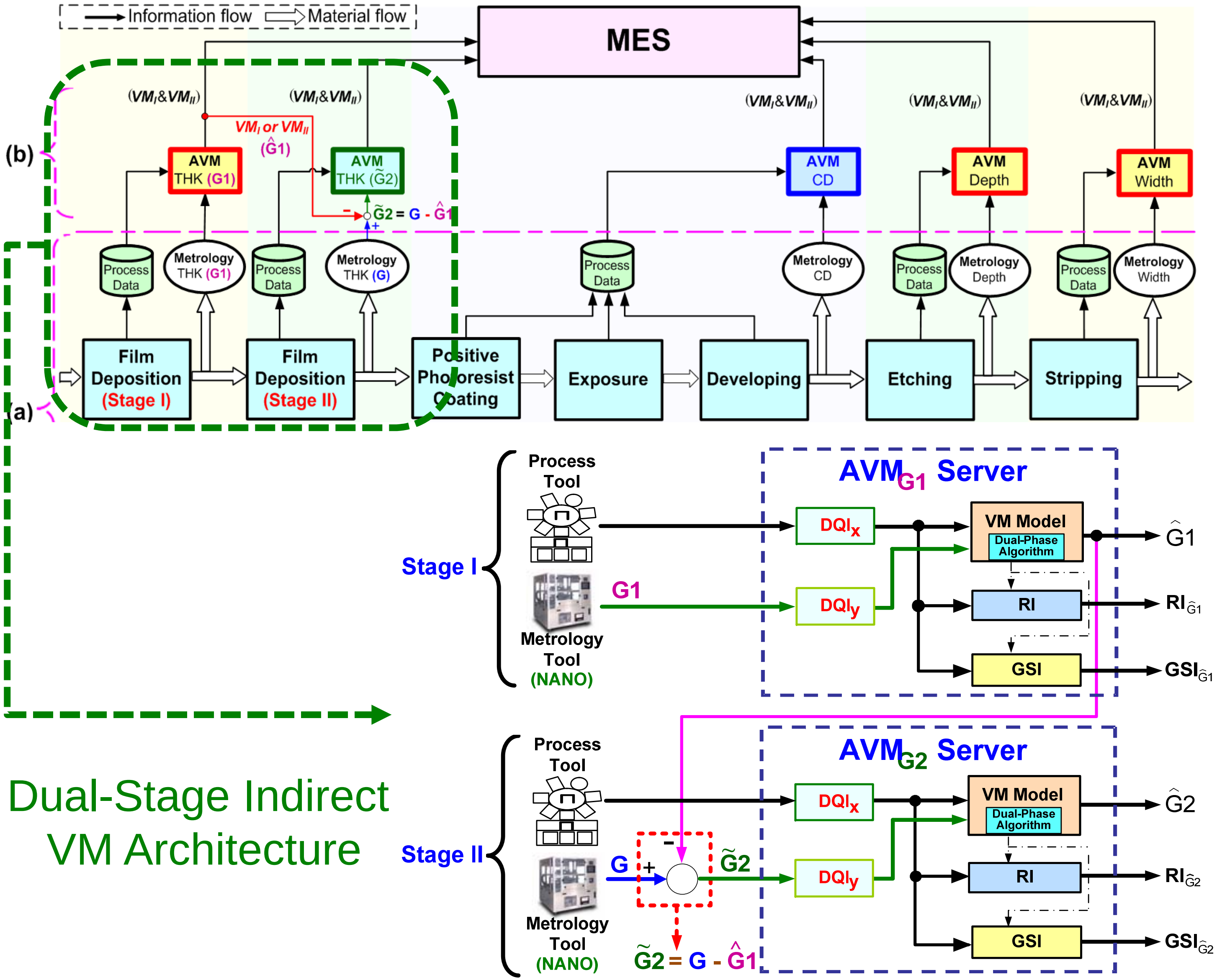

Dual-Stage Indirect VM Architecture

Cooperative-Tools VM Deployment

機密文件
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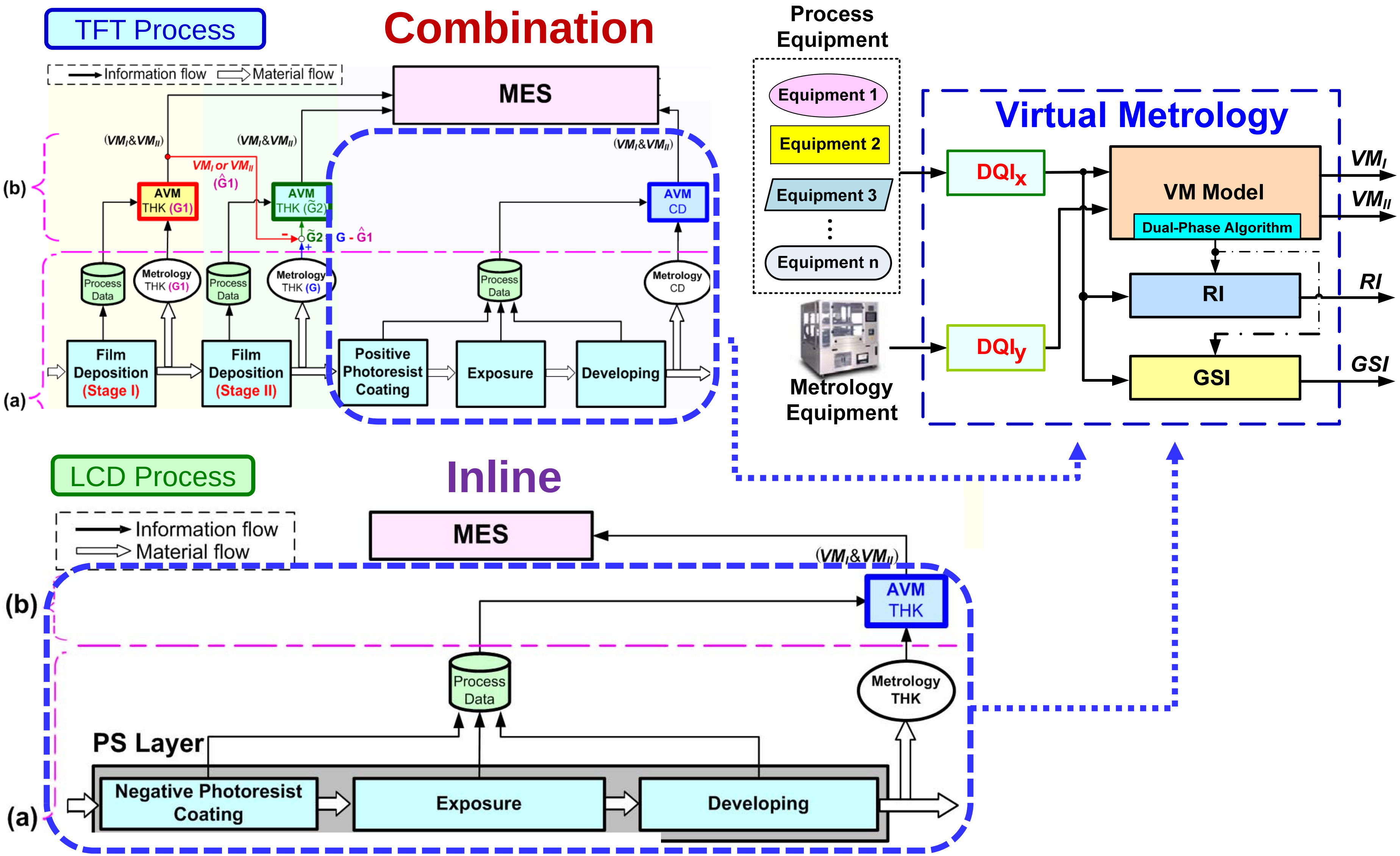

Concept of Virtual Cassette (VC)

Concept of Virtual Cassette (VC) 1/2

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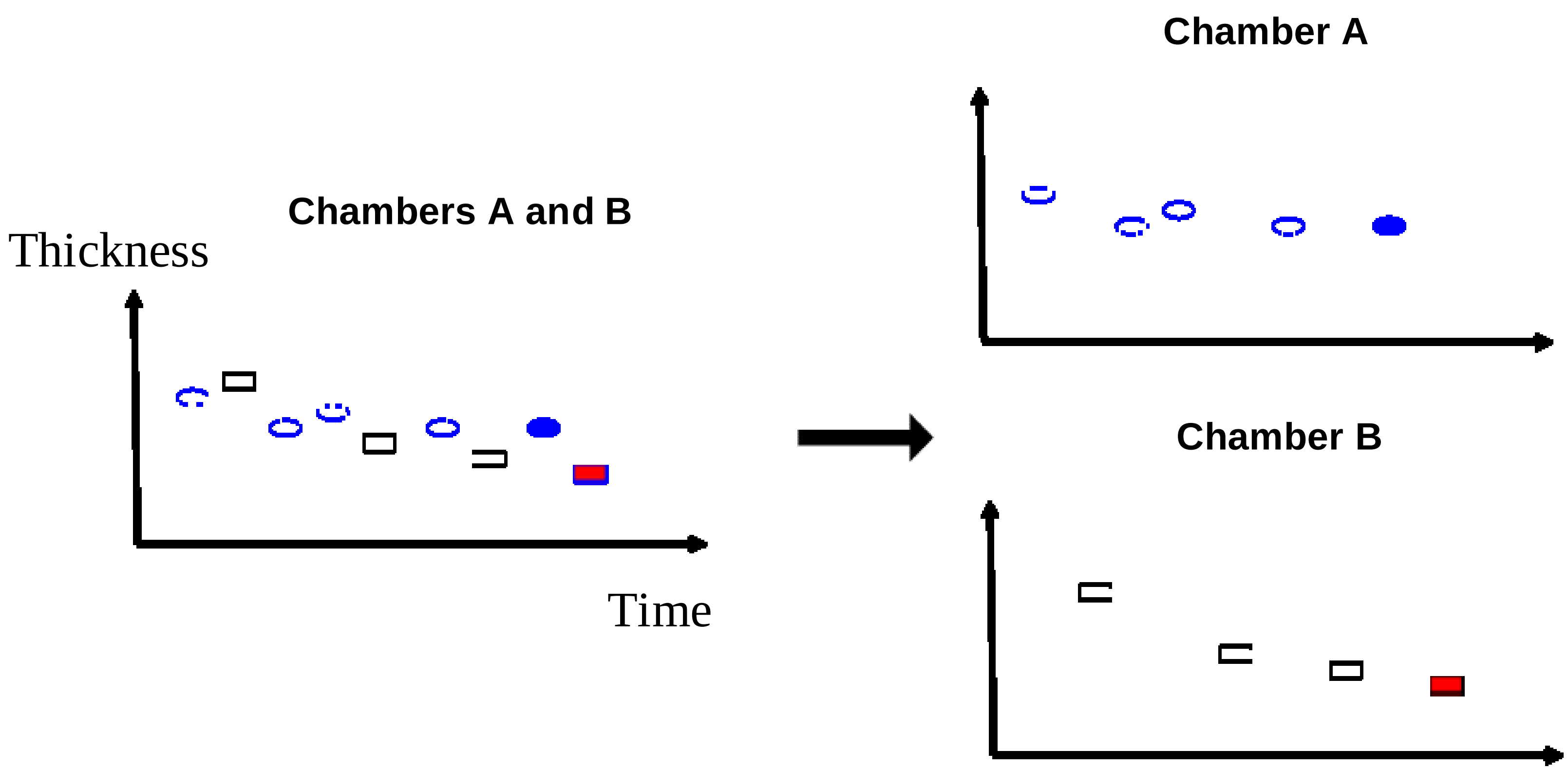

Concept of Virtual Cassette (VC) 2/2

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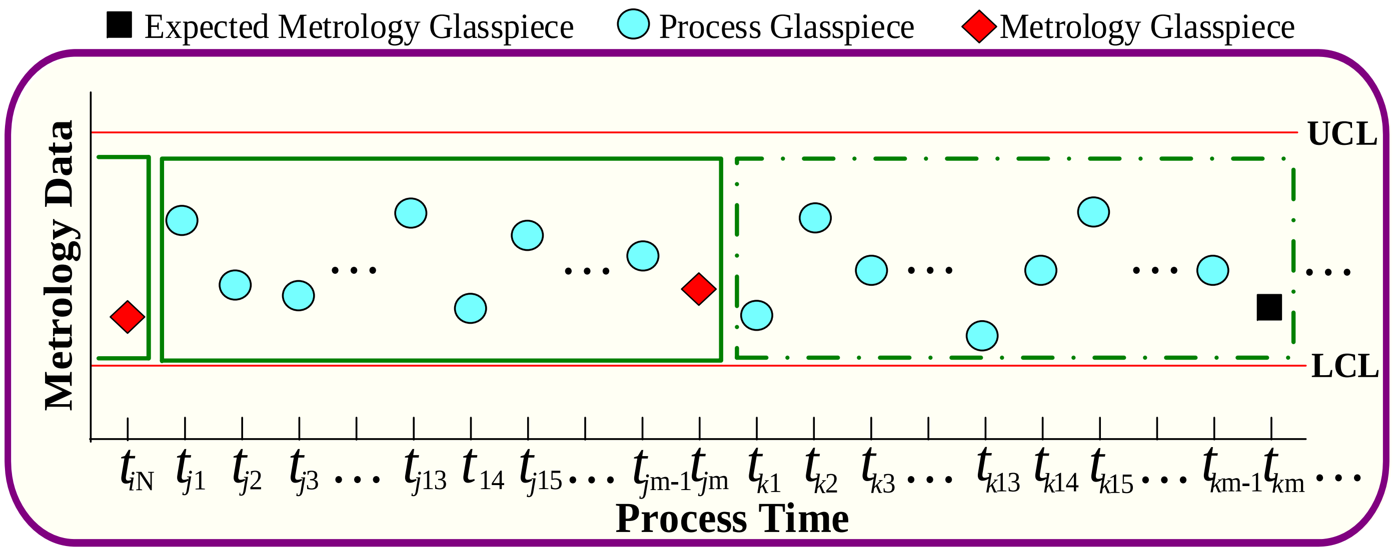
- A virtual cassette is defined to contain many process glasspieces and one metrology glasspiece.
- Moreover, a virtual cassette starts collecting process glasspieces that are processed by a specific chamber one by one and ends collecting until a metrology glasspiece of the same chamber has been obtained.



: The Confirmed VC, : The Expected VC.

Illustrative Examples of TFT-LCD Manufacturinfg

- Single-Stage
- Dual-Stage
- Cooperative-Tools Example
  - Combination
  - Inline

Illustrative Examples

- The **CVD process of TFT-LCD manufacturing** is selected for the **Single-Stage** & **Dual-Stage** cases.
- The **Photo process of TFT-LCD manufacturing** is selected for the **Combination Cooperative-Tools** case.
- The **Photo-Space (PS) process of CF manufacturing** is selected for the **Inline Cooperative-Tools** case.
- All the experimental data were collected from process tools that are practically operating in a **fifth generation TFT-LCD factory**.

Accuracy Evaluator

- The conjecture accuracy calculated from the test data is quantified by the mean absolute percentage error (MAPE) and maximum error (Max Error). Its formula is represented as follows.

$$MAPE = \frac{\sum_{i=1}^{n} \left| (\hat{y}_i - y_i) / y \right|}{n} \times 100\%$$

$$Max\ Error = \max \left\{ \frac{\left| (\hat{y}_i - y_i) \right|}{y} \times 100\% \quad , \quad i = 1,2,\ldots,n \right\}$$

Given the conjecture VM value $\hat{y}_i$, actual metrology value y_i, and the sample size *n.*

- The closer the MAPE and Max Error are to zero, the better the conjecture accuracy is achieved.

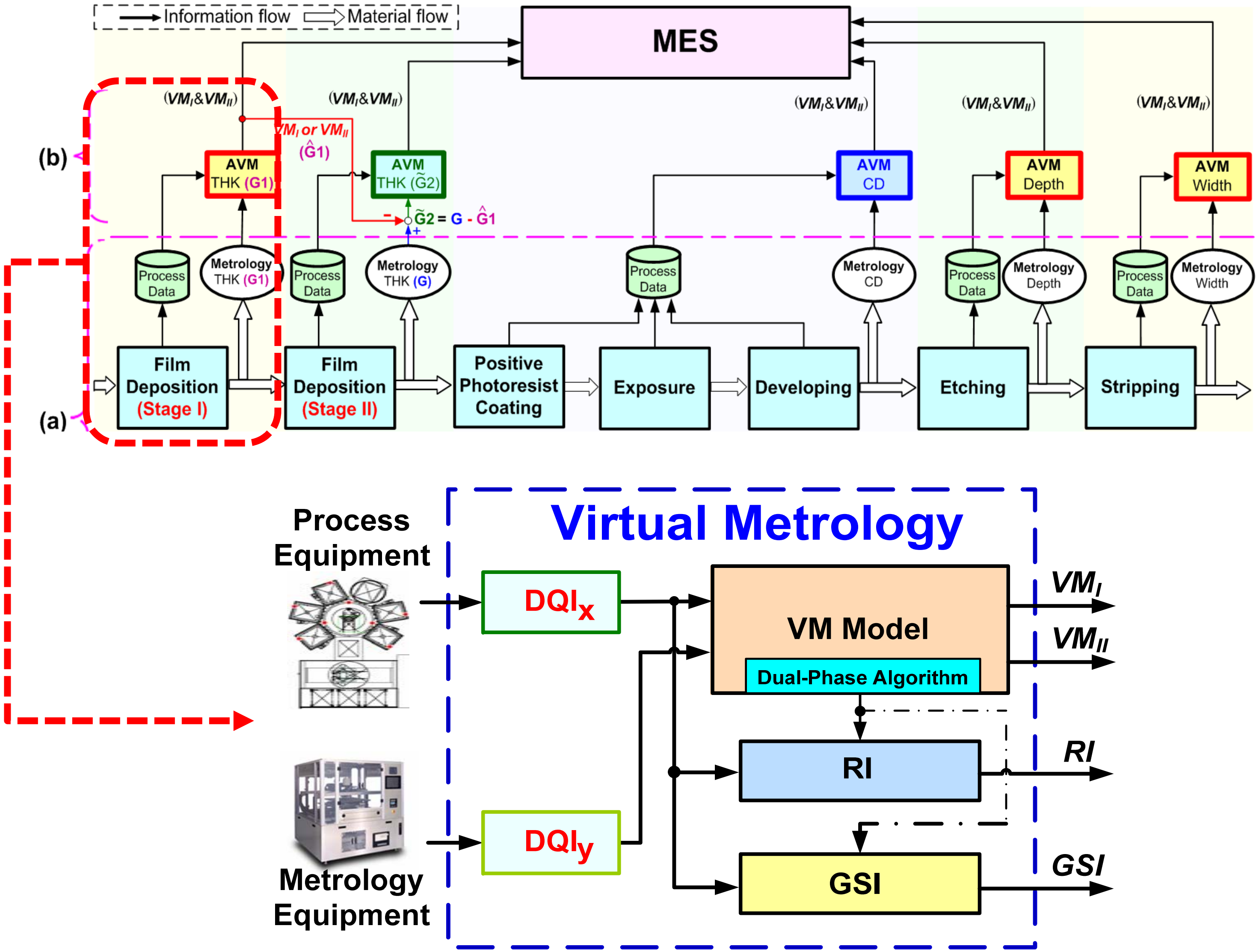
Single-Stage Example

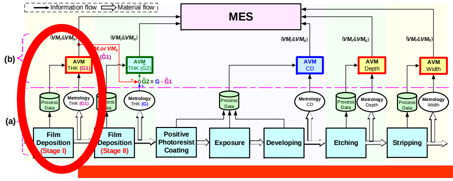
- CVD process of TFT-LCD Manufacturing

TFT Process

Single-Stage Example
Stage-I Film Deposition, G1 Layer

機密文件
不可外流

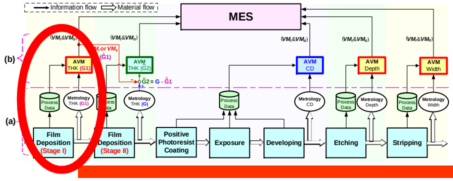




Single-Stage Example
Experiment Setup

機密文件
不可外流

Item	Content
Data Source	Fifth generation TFT-LCD factory
Process	**G1** in **CVD** of TFT Manufacturing
Glass Size	26”
Chambers	• Each CVD tool contains five chambers • Chamber A is chosen for demo
Metrology	Thickness (THK) of G1
Measurement Positions	• 19 positions are measured • Position 2 is chosen for demo
Process Parameters	Ten significant process parameters EX: gas flow, temperature, pressure, RF power, etc.
Data Sets	• 68 sets of real metrology data and corresponding process data • 44 for modeling; 24 for running test



Single-Stage Example

Measurement Positions

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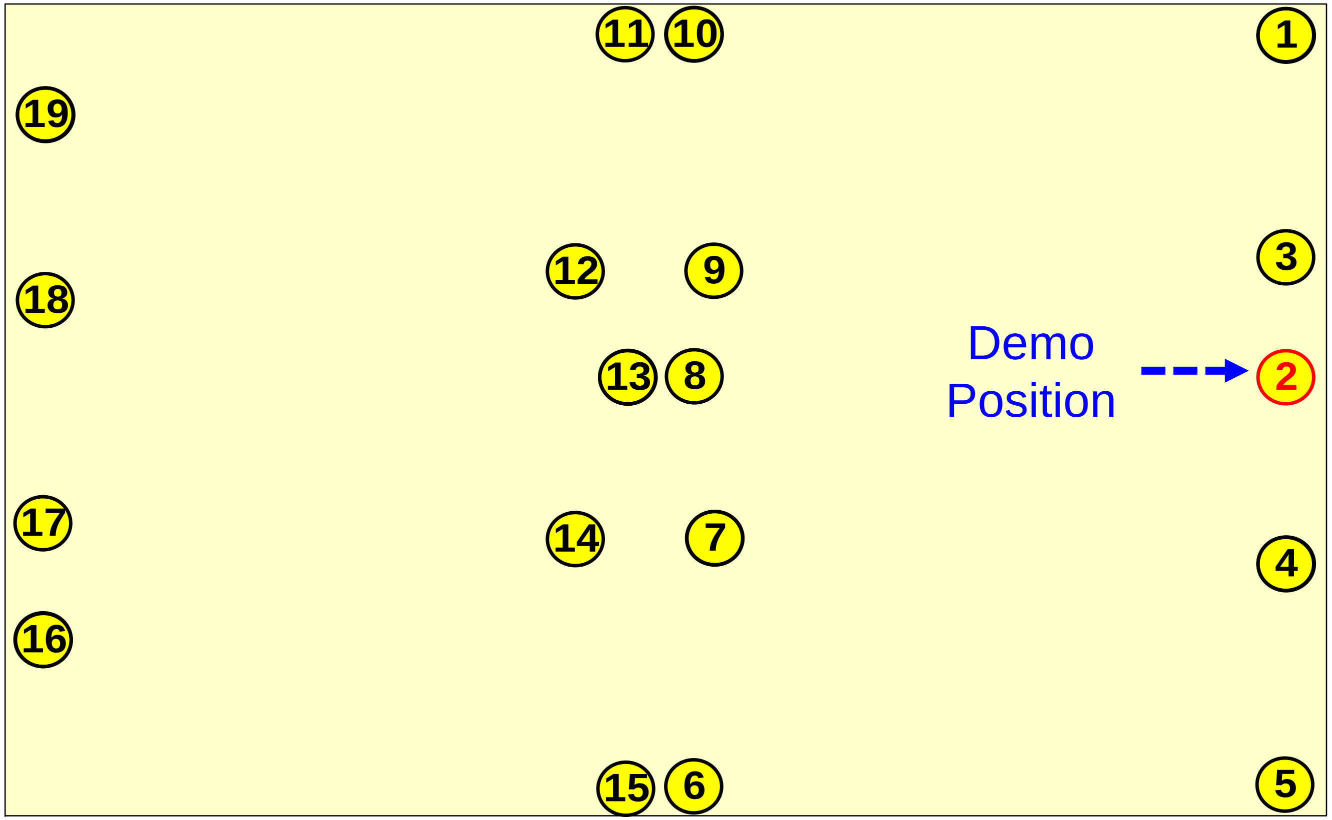

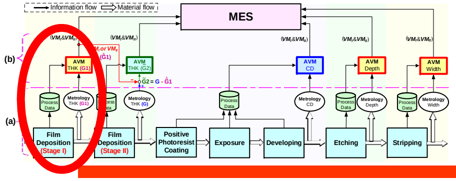

Single-Stage Example

Stage-I VM Results at Position 2

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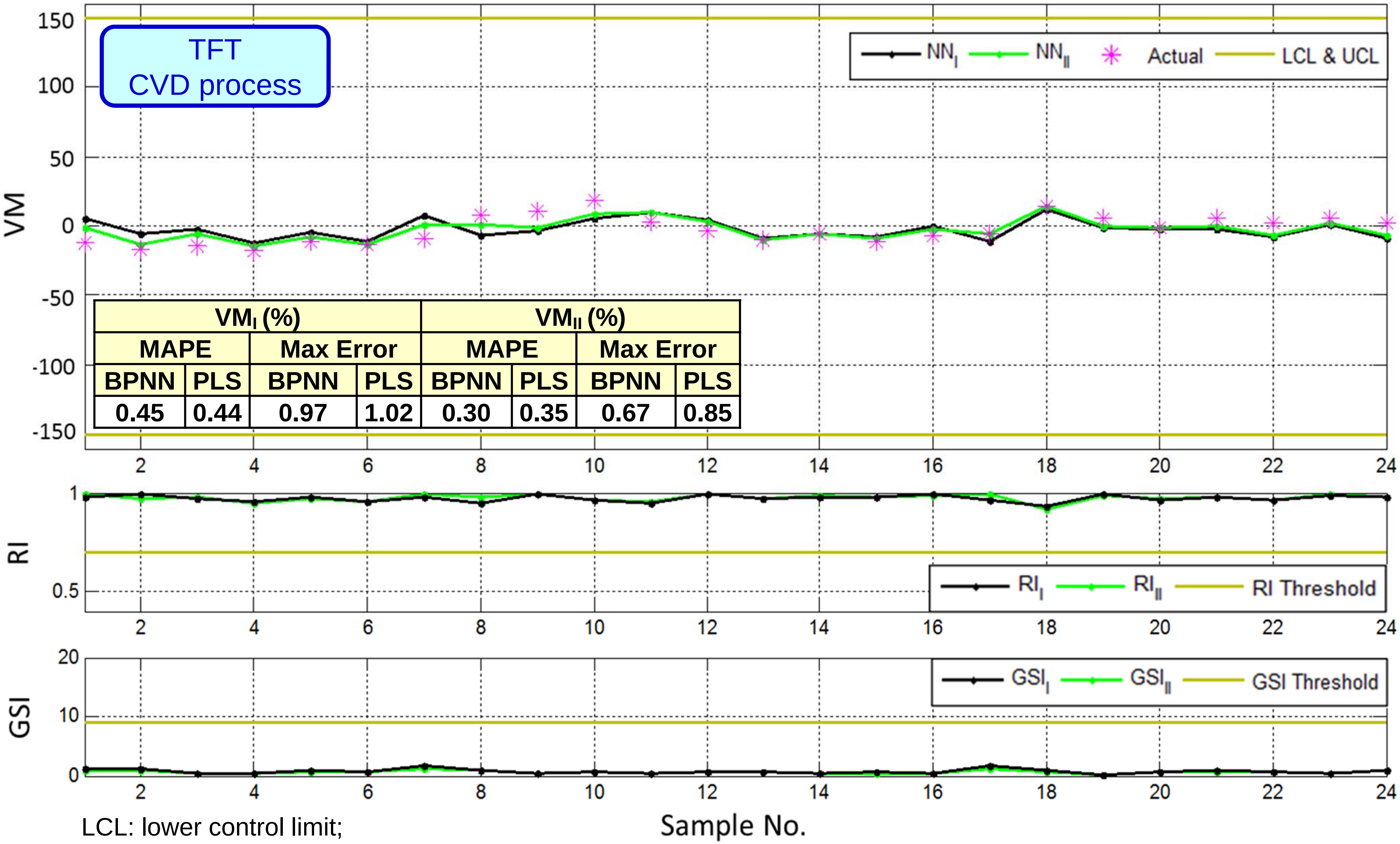
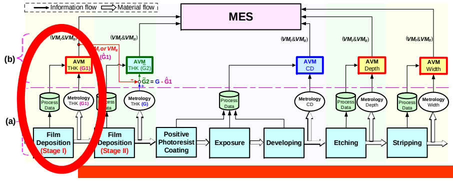


VM_I (%)				VM_{II} (%)			
MAPE		Max Error		MAPE		Max Error	
BPNN	PLS	BPNN	PLS	BPNN	PLS	BPNN	PLS
0.45	0.44	0.97	1.02	0.30	0.35	0.67	0.85

LCL: lower control limit;
UCL: upper control limit.



Single-Stage Example

VM Accuracy

機密文件
不可外流

Measured Pos.	VM$_{I}$ (%)				VM$_{II}$ (%)			
	MAPE		Max Error		MAPE		Max Error	
	BPNN	PLS	BPNN	PLS	BPNN	PLS	BPNN	PLS
1	0.48	0.44	0.92	1.17	0.30	0.37	0.68	0.94
2	0.45	0.44	0.97	1.02	0.30	0.35	0.67	0.85
3	0.51	0.51	1.25	1.30	0.37	0.41	0.92	1.01
4	0.46	0.44	0.90	0.95	0.33	0.35	0.70	0.78
5	0.41	0.39	0.76	0.88	0.31	0.33	0.69	0.84
6	0.57	0.58	1.13	1.22	0.43	0.48	0.98	1.10
7	0.57	0.54	1.44	1.45	0.45	0.45	1.31	1.25
8	0.66	0.63	1.33	1.22	0.54	0.52	1.22	0.99
9	0.63	0.61	1.61	1.30	0.53	0.51	1.47	1.03
10	0.63	0.60	1.24	1.28	0.46	0.49	1.05	1.07
11	0.64	0.62	1.30	1.35	0.48	0.51	1.12	1.12
12	0.67	0.67	1.45	1.30	0.55	0.50	1.33	0.91
13	0.68	0.66	1.32	1.48	0.55	0.55	1.15	1.06
14	0.60	0.57	1.34	1.44	0.49	0.47	1.22	1.26
15	0.61	0.62	1.18	1.29	0.46	0.51	1.04	1.16
16	0.56	0.60	1.42	1.54	0.40	0.50	1.08	1.31
17	0.64	0.63	1.65	1.76	0.49	0.53	1.24	1.55
18	0.62	0.60	1.54	1.30	0.47	0.50	1.06	1.13
19	0.54	0.56	1.66	1.41	0.46	0.51	1.30	1.20
Mean	0.58	0.57	1.30	1.33	0.44	0.47	1.08	1.09

Dual-Stage Example

- **CVD process of TFT-LCD Manufacturing**

TFT Process

Dual-Stage Example

Stage-II Film Deposition, G2 Layer

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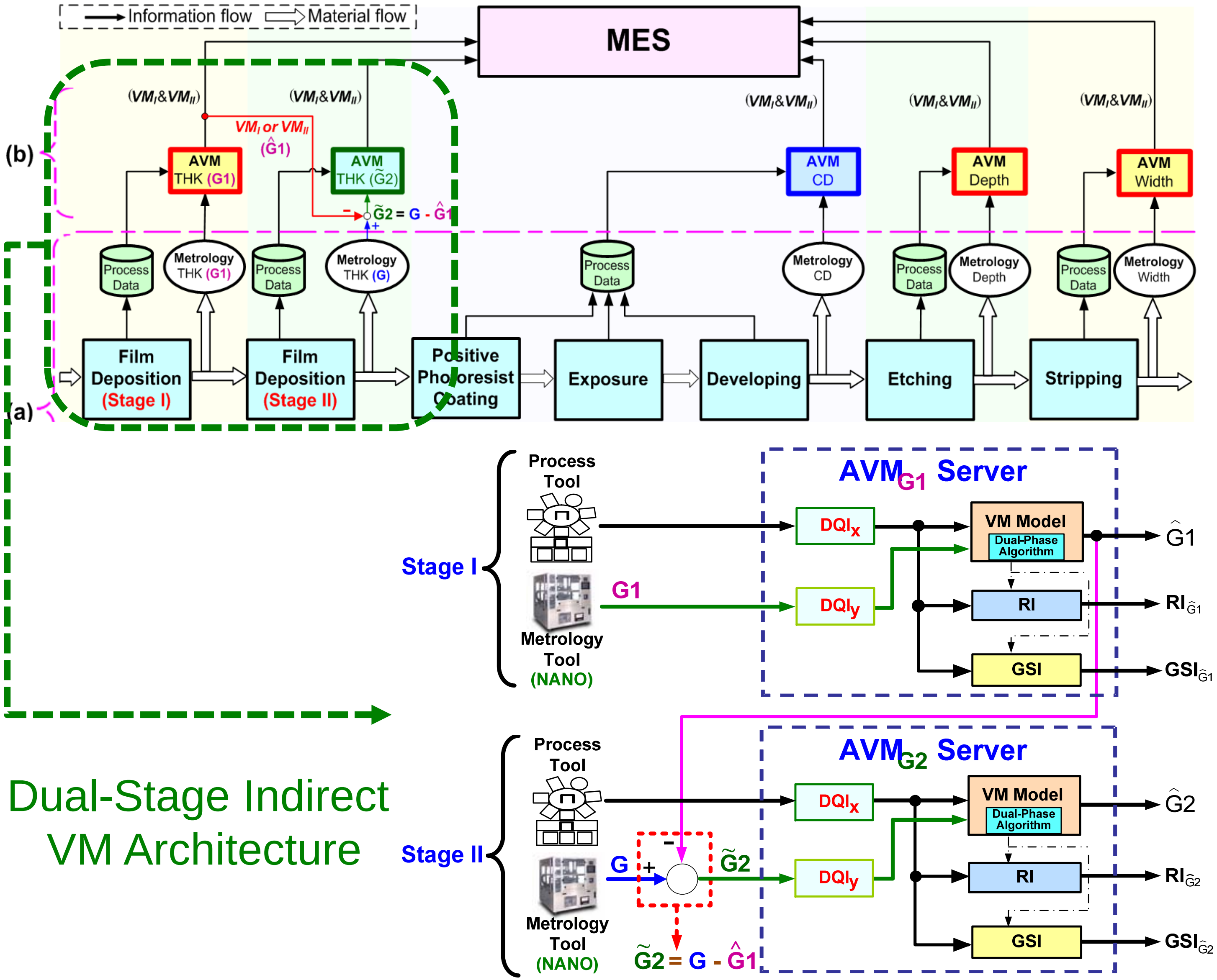

Dual-Stage Indirect
VM Architecture

TFT Process

Dual-Stage Example

Dual-Stage Indirect VM Architecture

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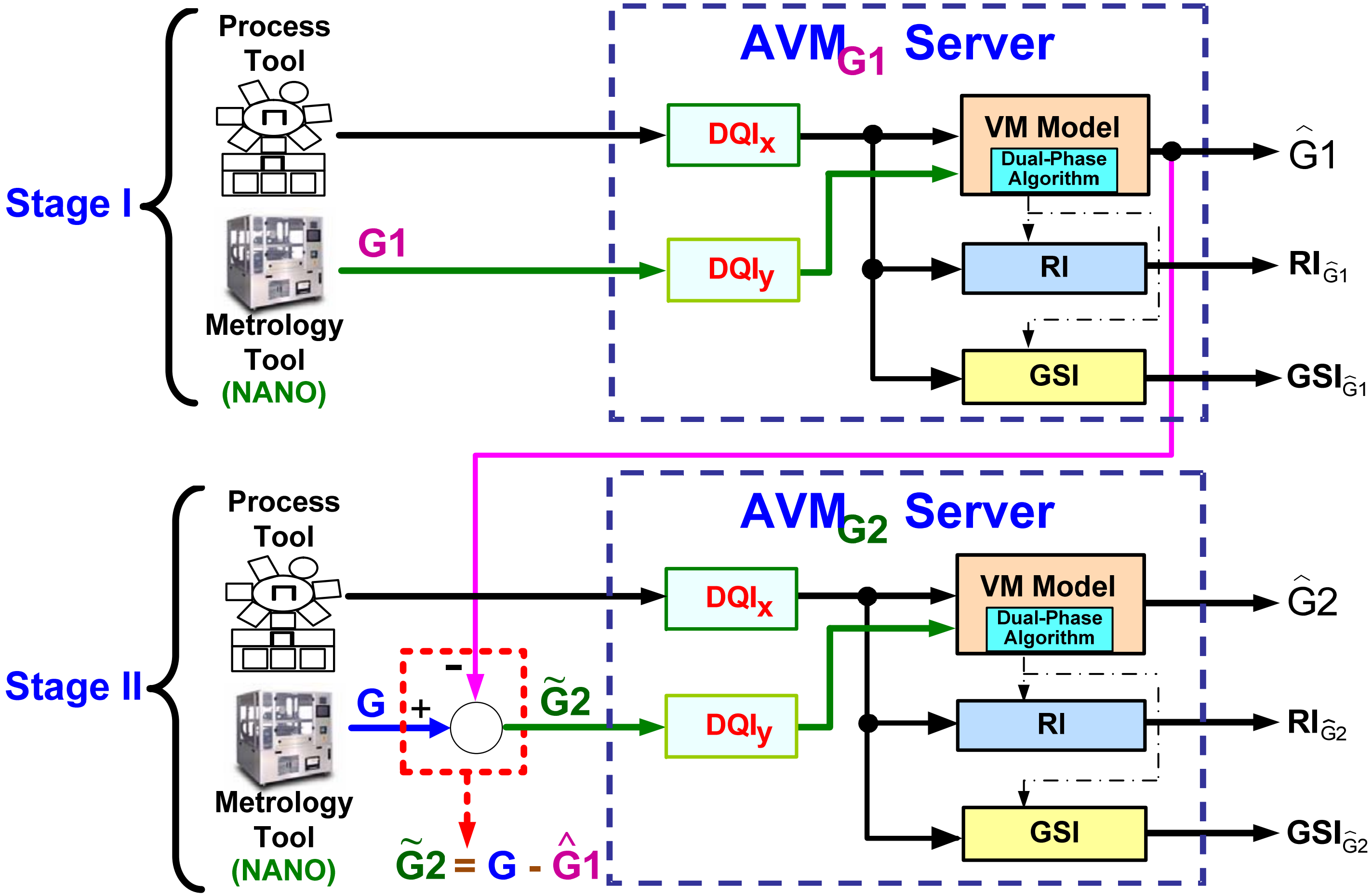

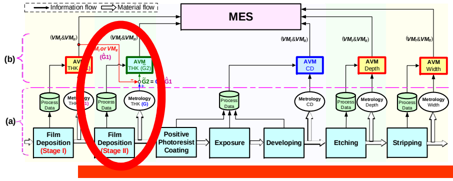

Dual-Stage Example
Experiment Setup

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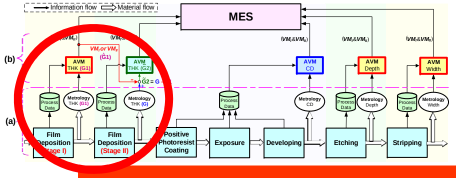
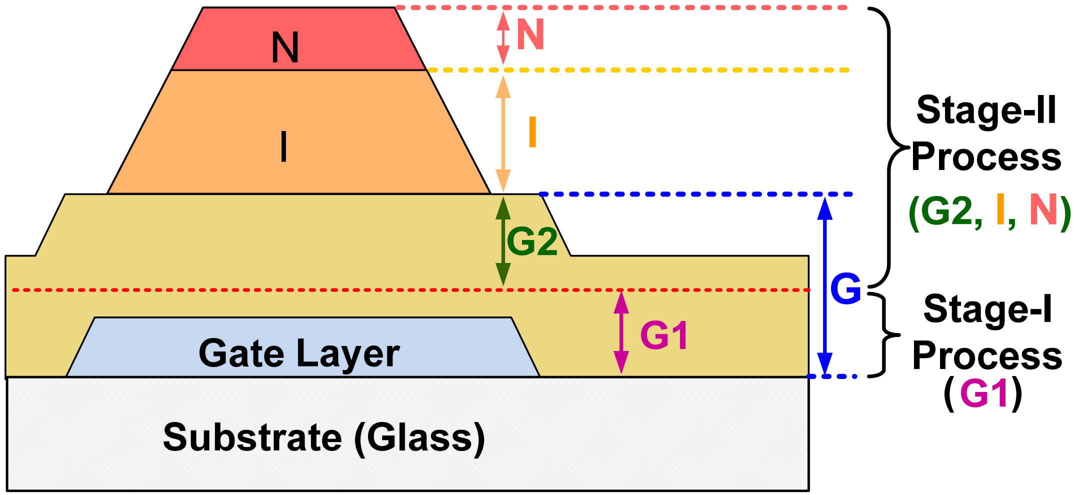
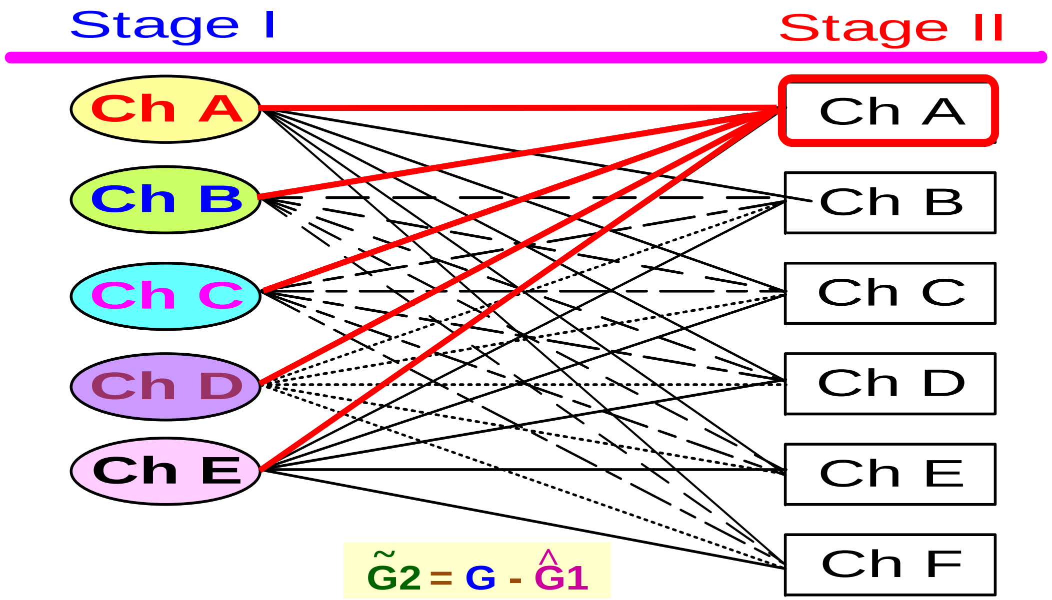
Item	Content
Data Source	Fifth generation TFT-LCD factory
Process	**G2** in **CVD** of TFT Manufacturing
Glass Size	26”
Chambers	• Each CVD tool contains six chambers • Chamber A is chosen for demo
Metrology	Thickness (THK) of **G (=G1+G2)**
Measurement Positions	• 19 positions are measured • Position 2 is chosen for demo
Process Parameters	Ten significant process parameters. EX: gas flow, temperature, pressure, RF power, etc.
Data Sets	• 47 sets of real metrology data and corresponding process data • 26 for modeling; 21 for running test



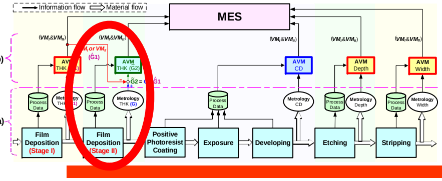
Dual-Stage Example

Metrology Setup





$$\tilde{G}2 = G - \hat{G}1$$



Dual-Stage Example

Stage-II VM Results at Position 2

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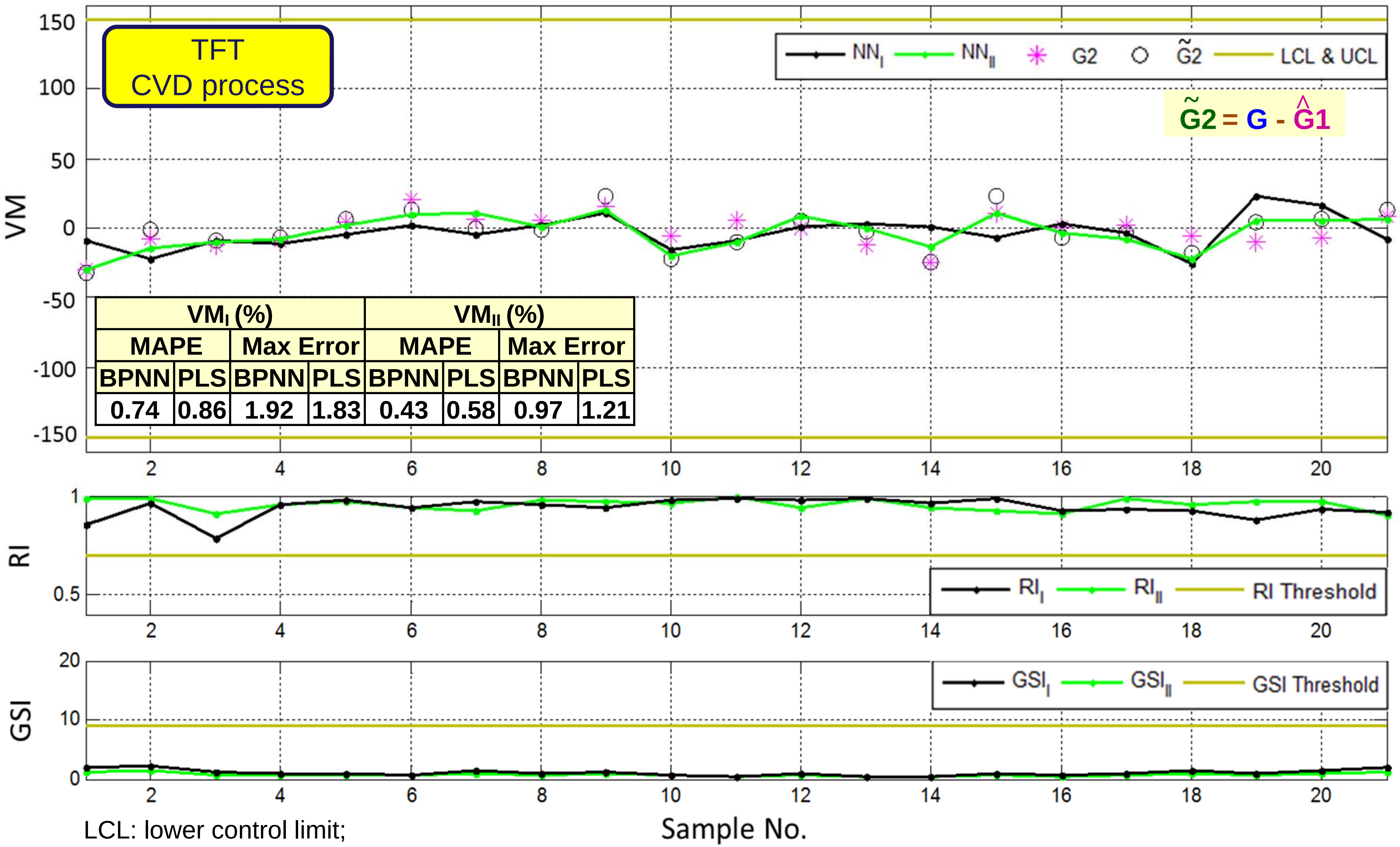
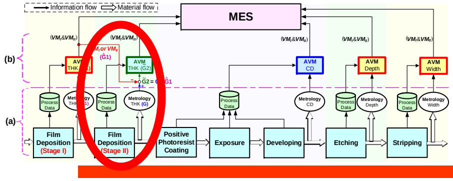


VM_I (%)				VM_{II} (%)			
MAPE		Max Error		MAPE		Max Error	
BPNN	PLS	BPNN	PLS	BPNN	PLS	BPNN	PLS
0.74	0.86	1.92	1.83	0.43	0.58	0.97	1.21

LCL: lower control limit;
UCL: upper control limit.



Dual-Stage Example
VM Accuracy

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不可外流

VM Accuracy								
Measured Pos.	VM_I (%)				VM_{II} (%)			
	MAPE		Max Error		MAPE		Max Error	
	BPNN	PLS	BPNN	PLS	BPNN	PLS	BPNN	PLS
1	1.18	1.12	4.51	3.59	0.57	0.76	1.53	2.34
2	0.74	0.86	1.92	1.83	0.43	0.58	0.97	1.21
3	0.80	0.84	1.84	2.01	0.45	0.61	1.04	1.20
4	0.76	0.82	1.87	1.93	0.49	0.56	1.13	1.24
5	1.26	1.21	3.96	3.53	0.73	0.86	2.14	2.69
6	0.71	0.83	2.38	2.09	0.43	0.57	1.44	1.78
7	0.75	0.84	2.18	2.15	0.56	0.63	1.37	1.80
8	0.76	0.72	1.86	1.85	0.47	0.50	1.29	1.55
9	0.79	0.81	1.98	1.83	0.45	0.54	1.27	1.27
10	0.60	0.65	2.20	1.81	0.39	0.44	1.17	1.31
11	0.53	0.47	1.48	0.88	0.33	0.33	0.80	0.76
12	0.82	0.79	1.89	1.69	0.54	0.56	1.17	1.46
13	0.75	0.77	1.81	1.69	0.49	0.57	1.12	1.45
14	0.65	0.67	1.48	1.55	0.45	0.52	1.08	1.35
15	0.69	0.71	2.10	1.62	0.42	0.51	1.02	1.25
16	0.69	0.83	2.06	1.76	0.46	0.57	1.40	1.30
17	0.78	0.84	2.13	1.71	0.47	0.60	1.38	1.19
18	0.78	0.85	2.08	2.05	0.49	0.61	1.21	1.28
19	0.64	0.71	1.64	1.63	0.44	0.50	1.25	1.24
Mean	0.77	0.81	2.18	1.96	0.48	0.57	1.25	1.46

Example of Combination Cooperative-Tools

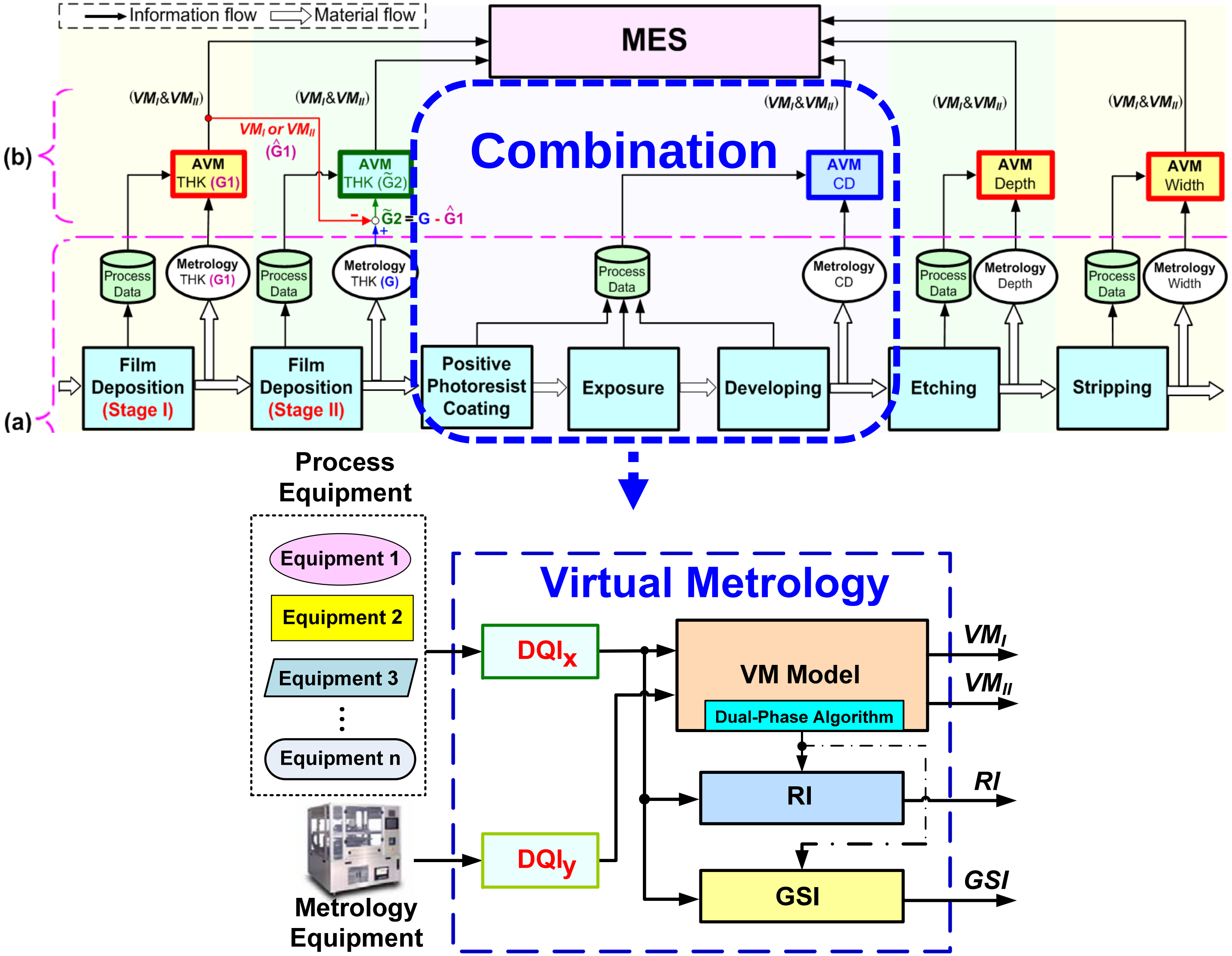
- **Photo process of TFT-LCD Manufacturing**

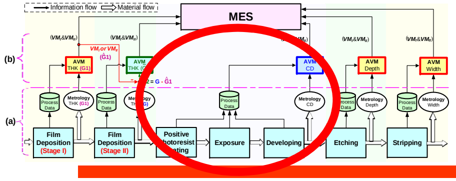
TFT Process

Combination Cooperative-Tools

Photo Process: Coating / Exposure / Developing

機密文件
不可外流



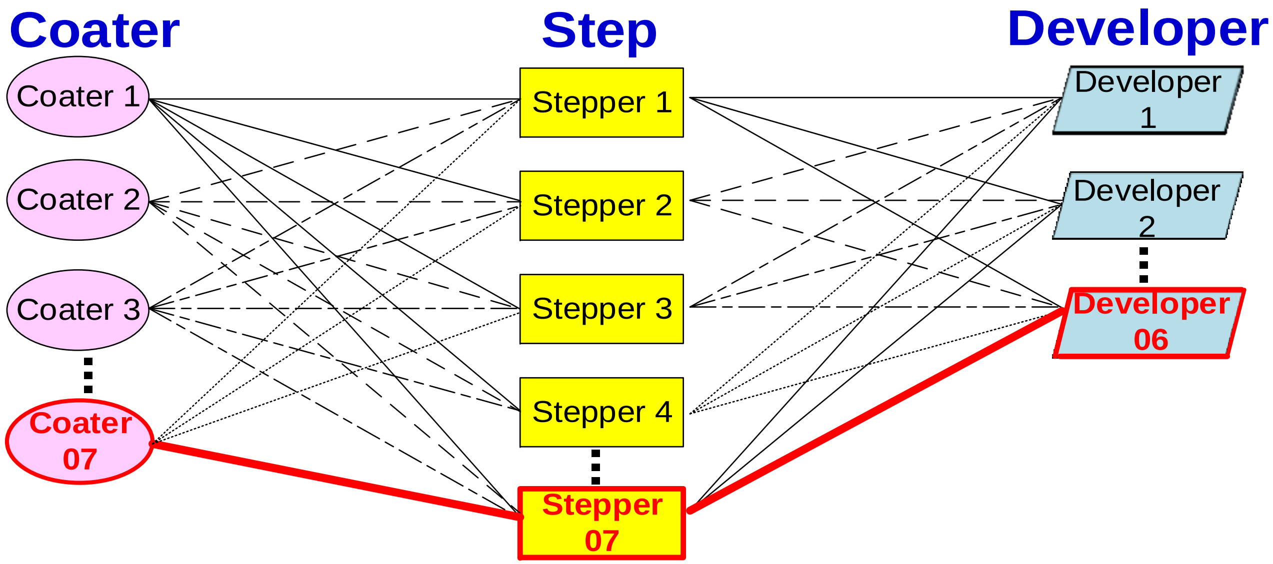


Combination Cooperative-Tools

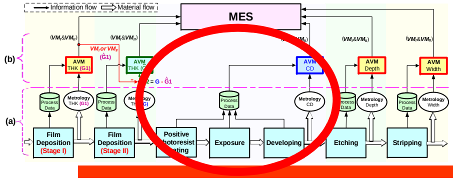
Combination Setup

Coating tools	Exposure tools	Developing tools	Max Combination	Demo Combination
8	7	10	560 (=8*7*10)	7-7-6

- The **7-7-6** combination is **the most frequent rout**; therefore, it has the **largest population of historical samples** and is selected for building the first VM models.



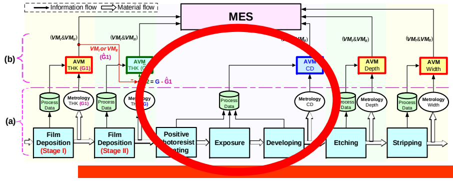
- The VM models of all the **other combinations** can then be constructed by the **automatic model-refreshing scheme**.



Combination Cooperative-Tools
Experiment Setup

機密文件
不可外流

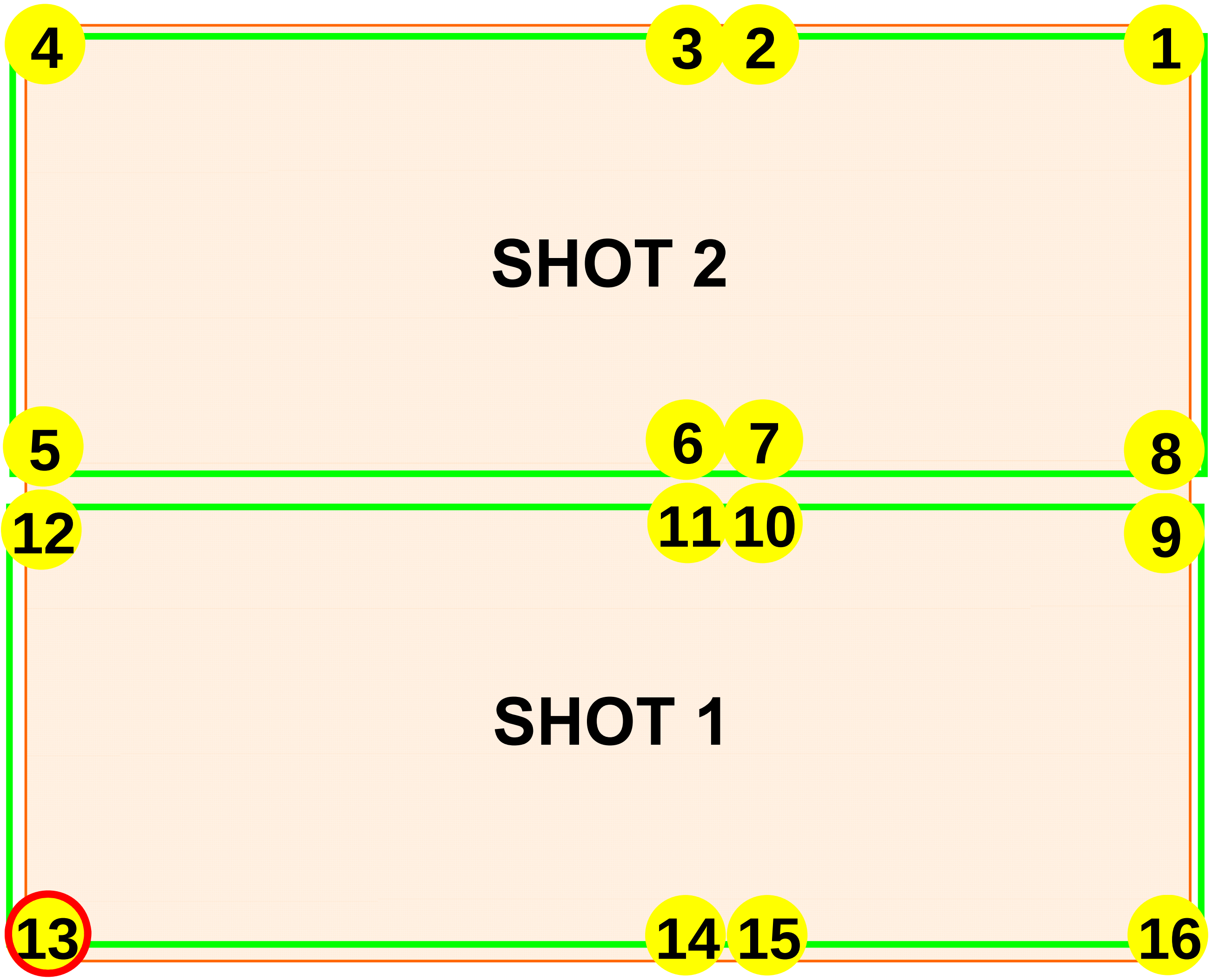
Item	Content
Data Source	Fifth generation TFT-LCD factory
Process	**Photo (Coating/Exposure/Developing)** of TFT Manufacturing
Glass Size	14.1”
Combination	• Coating tools: 8; Exposure tools: 7; Developing tools: 10 • Max Combination: 560 (=8*7*10) • Combination 7-7-6 is chosen for demo
Metrology	• Critical Dimension (CD)
Measurement Positions	• 16 positions are measured • Position 13 is chosen for demo
Process Parameters	• 21 key process parameters • Coating temperature, glass thickness, etc., for coating • Lamp illumination, exposure energy, etc., for exposure • Process time, spray temperature, etc., for developing
Data Sets	• 166 sets of real metrology data and corresponding process data • 110 for modeling; 56 for running test



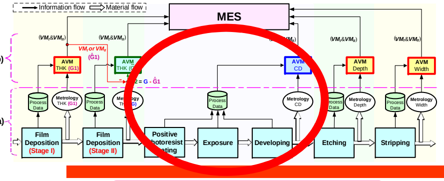
Combination Cooperative-Tools

Measurement Positions of a 14.1”-product Glass

機密文件
不可外流



Demo Position



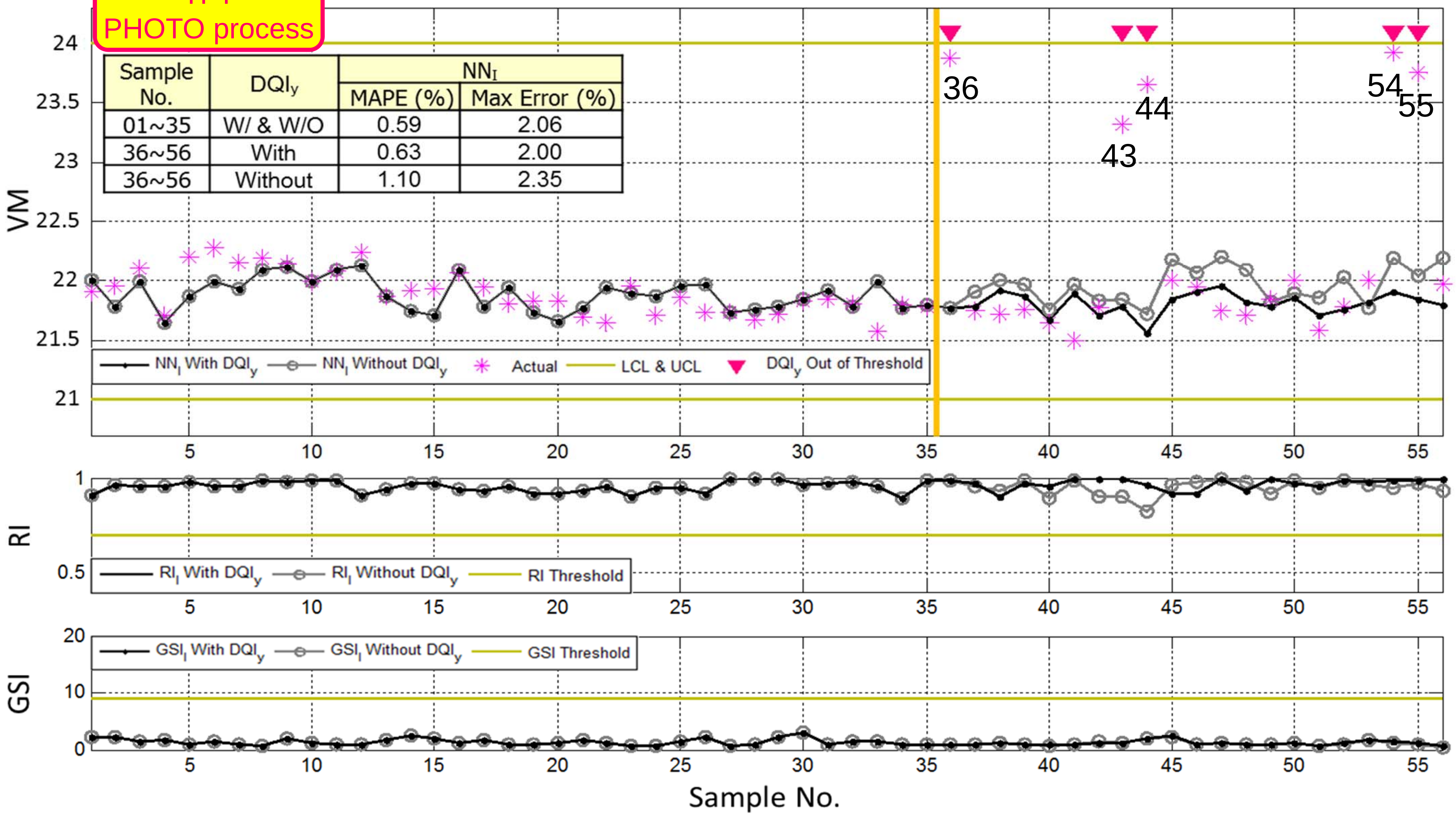
Combination Cooperative-Tools

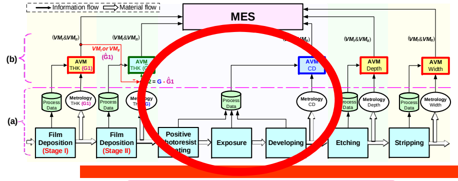
VM_I Result at Position 13

機密文件
不可外流

TFT
PHOTO process

Sample No.	DQI_y	NN_I MAPE (%)	NN_I Max Error (%)
01~35	W/ & W/O	0.59	2.06
36~56	With	0.63	2.00
36~56	Without	1.10	2.35





Combination Cooperative-Tools

Erroneous Measurements

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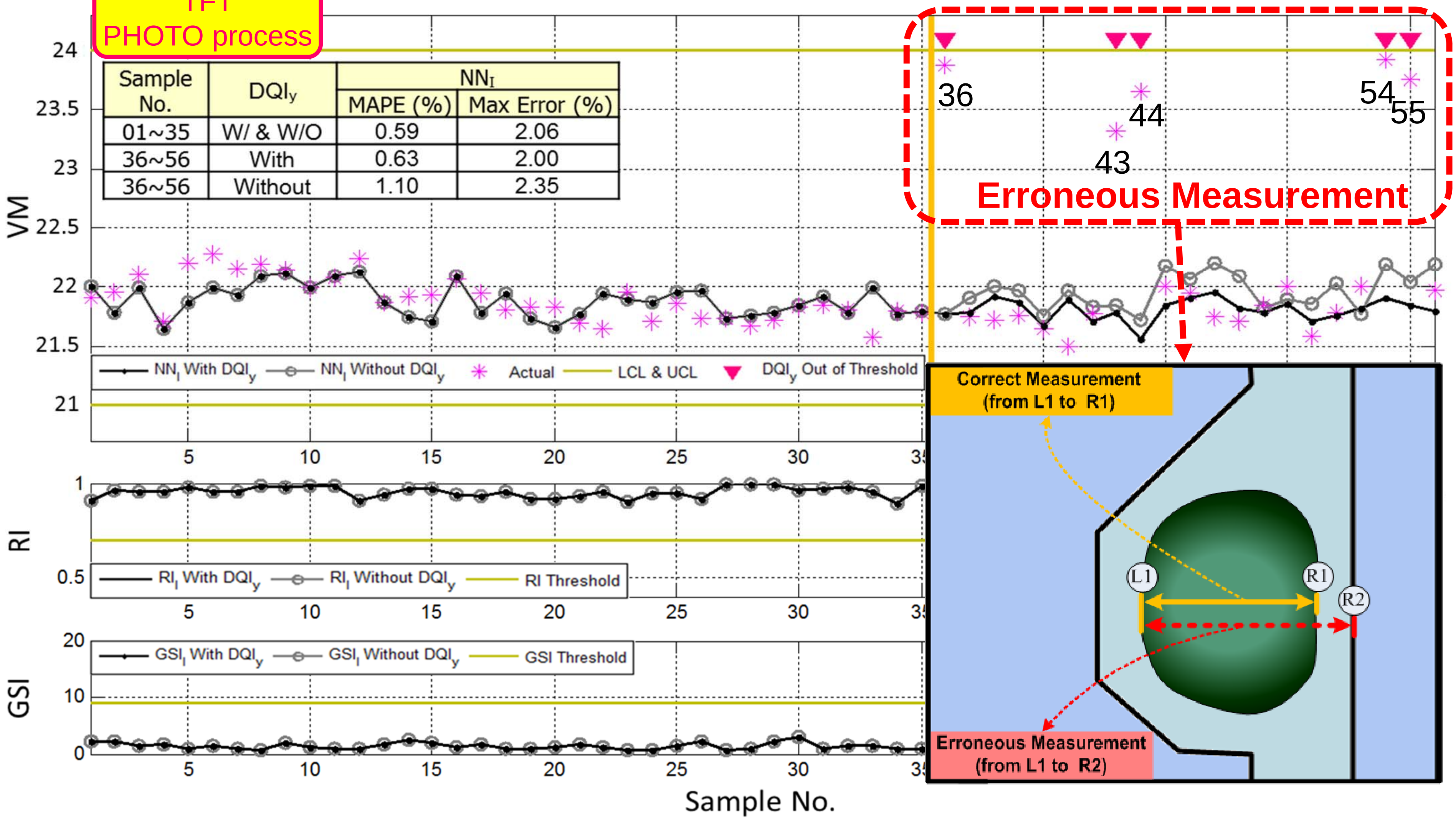
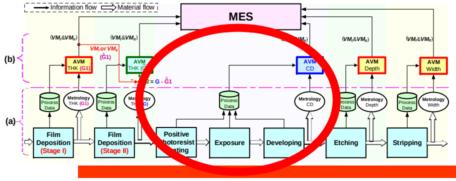
TFT
PHOTO process

Sample No.	DQI_y	NN_I MAPE (%)	NN_I Max Error (%)
01~35	W/ & W/O	0.59	2.06
36~56	With	0.63	2.00
36~56	Without	1.10	2.35





Combination Cooperative-Tools

Exclusion Tests (#57 ~ #68)

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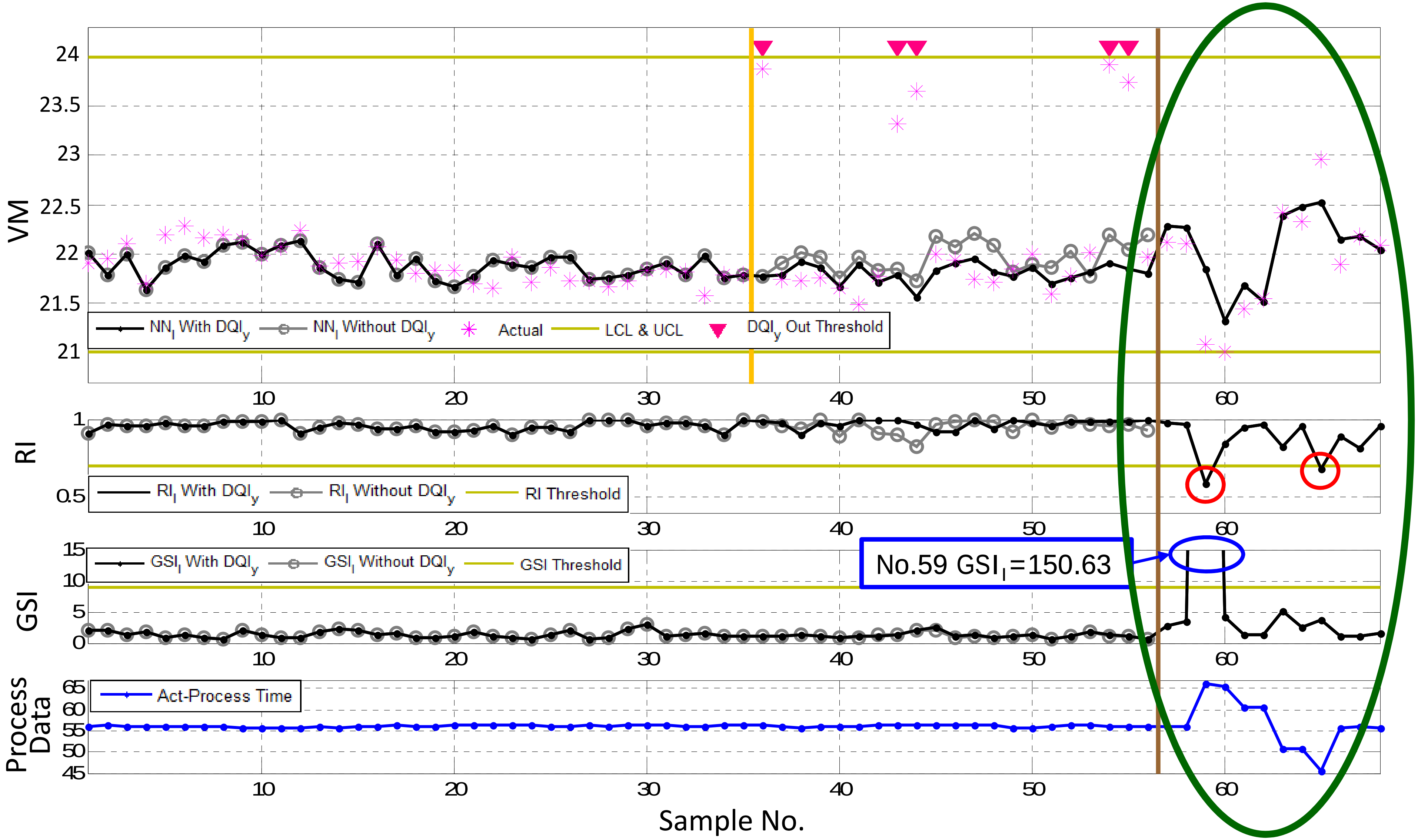

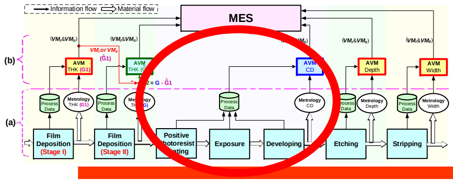

Combination Cooperative-Tools
VM Accuracy

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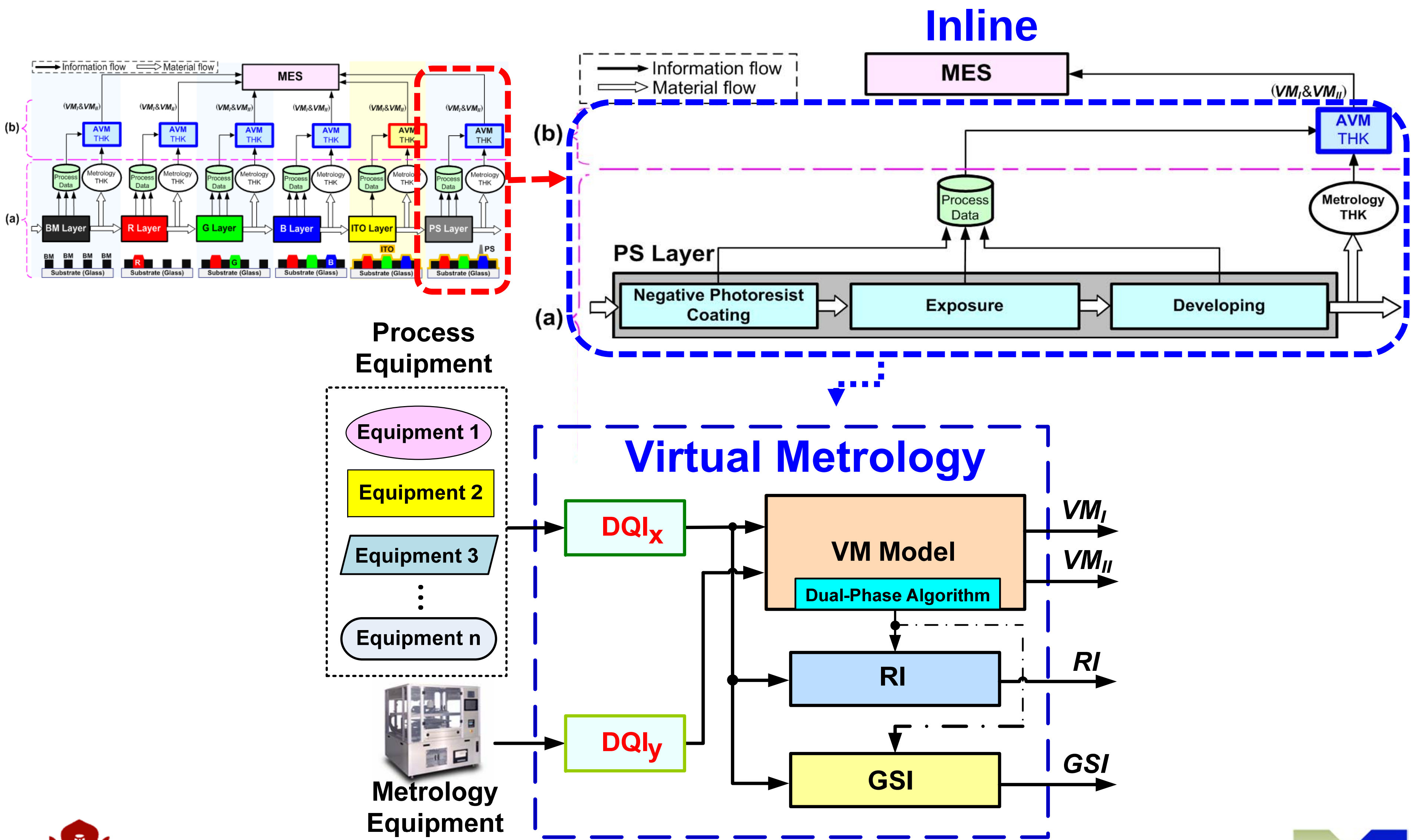
VM Accuracy (No.01~No.56 With DQI_y)								
Measured Pos.	VM_I (%)				VM_{II} (%)			
	MAPE		Max Error		MAPE		Max Error	
	BPNN	PLS	BPNN	PLS	BPNN	PLS	BPNN	PLS
1	0.89	0.90	2.42	2.34	0.74	0.82	1.97	2.20
2	0.68	0.68	1.99	2.27	0.53	0.60	1.60	2.02
3	0.63	0.56	1.85	1.97	0.47	0.47	1.43	1.77
4	0.75	0.74	2.02	2.03	0.53	0.64	1.66	1.66
5	0.63	0.63	1.69	1.90	0.41	0.52	1.22	1.52
6	0.43	0.40	1.21	1.29	0.28	0.35	0.70	1.17
7	0.45	0.44	1.48	1.46	0.30	0.37	0.91	1.33
8	0.73	0.67	1.96	1.97	0.52	0.55	1.66	1.39
9	0.76	0.78	1.99	2.14	0.50	0.62	1.57	1.72
10	0.39	0.45	1.39	1.24	0.25	0.35	0.61	1.06
11	0.56	0.54	1.56	1.61	0.38	0.47	0.98	1.50
12	0.53	0.59	1.77	1.66	0.34	0.46	1.16	1.56
13	0.61	0.64	2.06	2.02	0.42	0.50	1.39	1.46
14	0.83	0.84	3.03	2.56	0.59	0.70	1.93	2.34
15	0.78	0.73	2.89	3.12	0.55	0.65	2.30	2.51
16	0.75	0.76	2.65	2.48	0.53	0.63	1.79	2.05
Mean	0.65	0.65	2.00	2.00	0.46	0.54	1.43	1.70

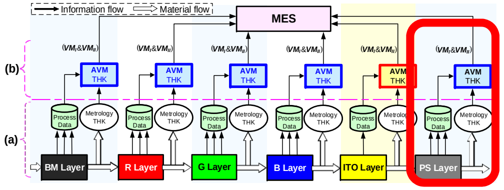
Example of Inline Cooperative-Tools

- **Photo-Space Process of CF Manufacturing**

Inline Cooperative-Tools

PS Layer Process: Coating / Exposure / Developing





Inline Cooperative-Tools

Experiment Setup

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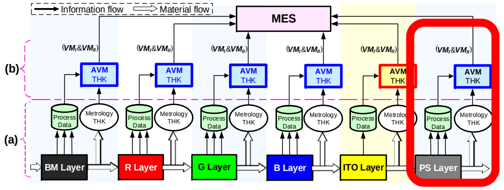
Item	Content
Data Source	Fifth generation TFT-LCD factory
Process	**PS Process (coating/exposure/developing)** of CF Manufacturing
Glass Size	31.5”
Inline	1 Coating tool + 1 Exposure tool + 1 Developing tool
Metrology	• PS-height (THK)
Measurement Positions	• 36 positions are measured • Position 1 is chosen for demo
Process Parameters	• Seven significant process parameters • EX: lamp identity, exposure accumulation, total discharge, pump rate, bake time, stage temperature, and mask count.
Data Sets	• 150 sets of real metrology data and corresponding process data • 100 for modeling; 50 for running test



Inline Cooperative-Tools

VM results at Position 1

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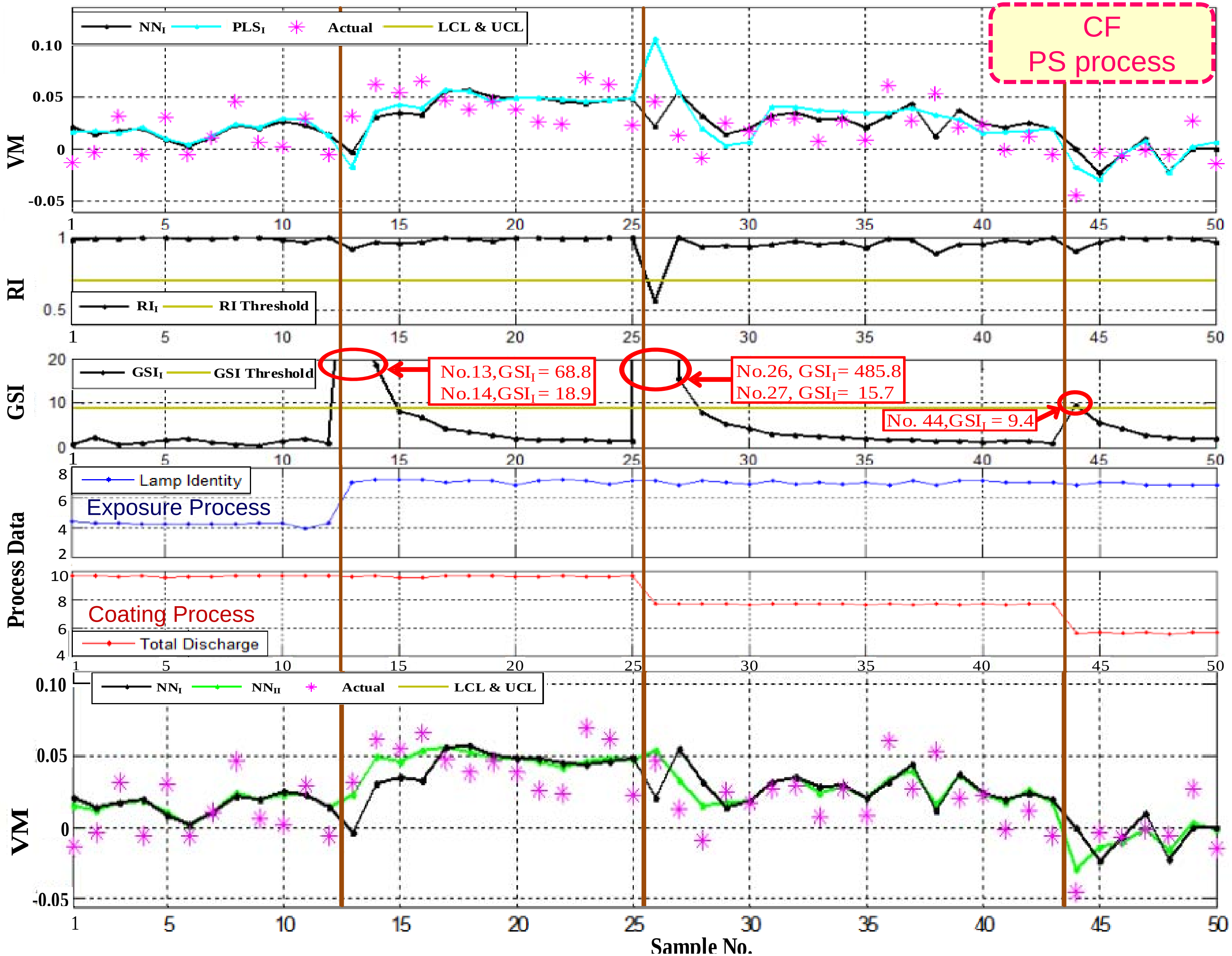

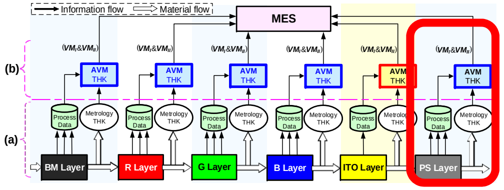

Inline Example of Cooperative-Tools

VM Accuracy

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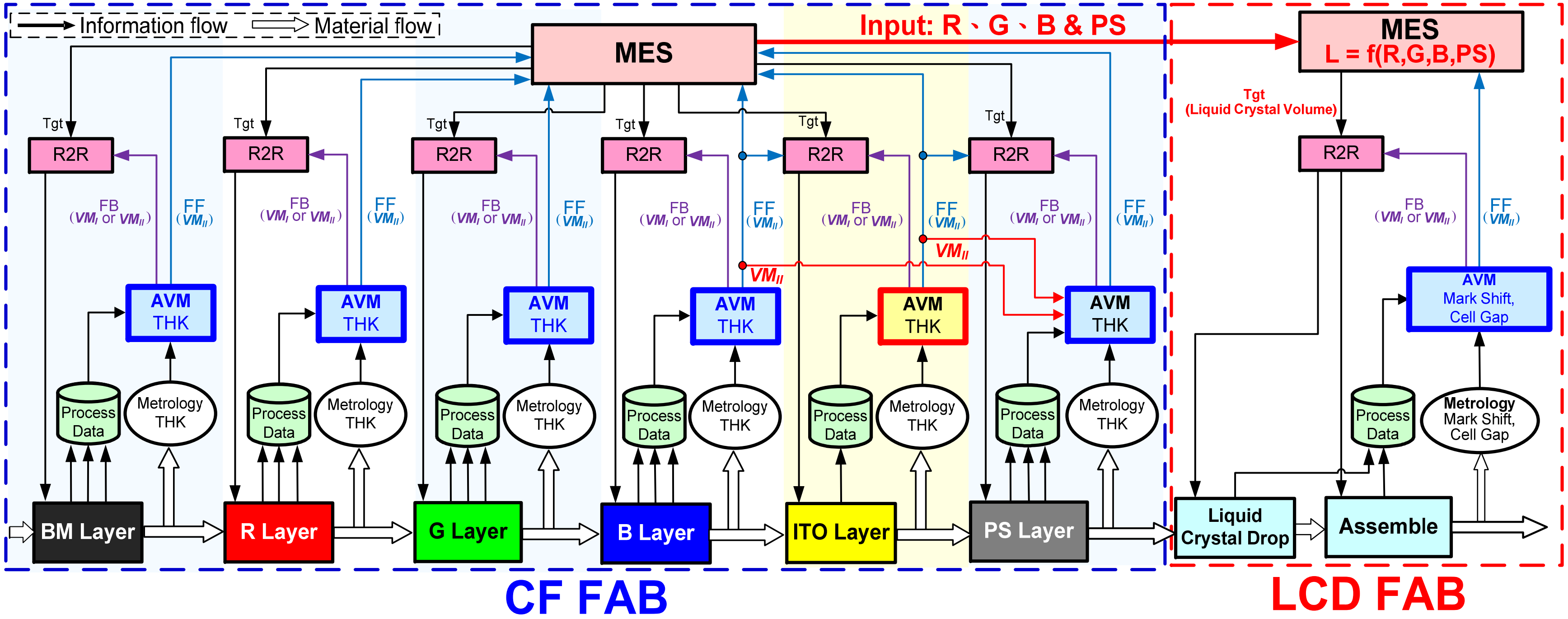
VM Accuracy																	
Pos.	VM_{I} (%)				VM_{II} (%)				Pos.	VM_{I} (%)				VM_{II} (%)			
	MAPE		Max Error		MAPE		Max Error			MAPE		Max Error		MAPE		Max Error	
	BPNN	PLS	BPNN	PLS	BPNN	PLS	BPNN	PLS		BPNN	PLS	BPNN	PLS	BPNN	PLS	BPNN	PLS
1	0.52	0.53	1.25	0.91	0.43	0.48	1.11	1.29	19	0.58	0.57	1.91	1.56	0.49	0.52	1.53	1.39
2	0.46	0.44	1.24	1.12	0.35	0.40	0.94	1.09	20	0.46	0.44	1.30	1.12	0.34	0.34	1.25	0.97
3	0.42	0.42	1.31	1.29	0.39	0.41	1.28	1.45	21	0.41	0.37	1.43	1.05	0.35	0.36	1.07	1.11
4	0.40	0.41	1.31	1.26	0.45	0.45	1.45	1.46	22	0.44	0.43	1.67	1.36	0.38	0.35	1.02	1.05
5	0.46	0.47	1.76	1.67	0.45	0.47	1.01	1.47	23	0.42	0.42	1.32	1.22	0.57	0.54	1.46	1.33
6	0.49	0.49	1.82	1.84	0.33	0.33	0.89	0.82	24	0.37	0.36	1.40	1.14	0.34	0.33	0.97	1.23
7	0.54	0.52	1.89	1.73	0.30	0.30	0.85	1.15	25	0.45	0.41	1.17	1.18	0.32	0.32	1.05	1.06
8	0.61	0.55	1.75	1.94	0.37	0.39	1.03	1.06	26	0.43	0.42	1.27	1.43	0.38	0.38	1.07	1.13
9	0.55	0.53	1.18	1.42	0.37	0.42	1.22	1.33	27	0.66	0.61	1.77	1.85	0.43	0.40	1.17	1.11
10	0.43	0.37	1.59	1.25	0.38	0.38	1.00	0.94	28	0.48	0.47	1.51	1.44	0.38	0.40	1.04	1.03
11	0.40	0.38	1.15	0.93	0.33	0.32	1.06	1.09	29	0.41	0.39	1.25	1.15	0.39	0.38	1.43	1.10
12	0.40	0.37	1.25	1.15	0.41	0.41	1.40	1.62	30	0.43	0.43	1.49	1.44	0.31	0.33	1.00	1.03
13	0.36	0.35	1.32	1.42	0.51	0.51	1.33	1.73	31	0.39	0.37	1.38	1.21	0.36	0.36	1.11	1.26
14	0.37	0.36	1.27	1.08	0.35	0.30	1.06	1.02	32	0.49	0.50	1.44	1.57	0.40	0.41	1.23	1.24
15	0.45	0.47	1.33	1.26	0.33	0.32	1.14	1.02	33	0.44	0.44	1.15	1.22	0.37	0.38	1.25	1.15
16	0.43	0.44	1.29	1.16	0.30	0.31	1.05	0.98	34	0.48	0.47	1.48	1.52	0.41	0.43	1.27	1.47
17	0.46	0.46	1.45	1.38	0.36	0.38	0.99	1.07	35	0.50	0.46	1.27	1.27	0.41	0.43	1.17	1.23
18	0.48	0.45	1.36	1.24	0.40	0.40	1.08	1.03	36	0.50	0.49	1.62	1.44	0.44	0.44	1.34	1.33
									Mean	0.46	0.44	1.43	1.34	0.39	0.39	1.15	1.19

Advanced Application of TFT-LCD Manufacturing

- An inter-fab AVM application that forwards the PS, R, G, and B VM values of each individual glass generated in the CF fab to the LCD fab for glass-to-glass liquid crystal volume control in the liquid-crystal-drop process may be proposed for the future work.



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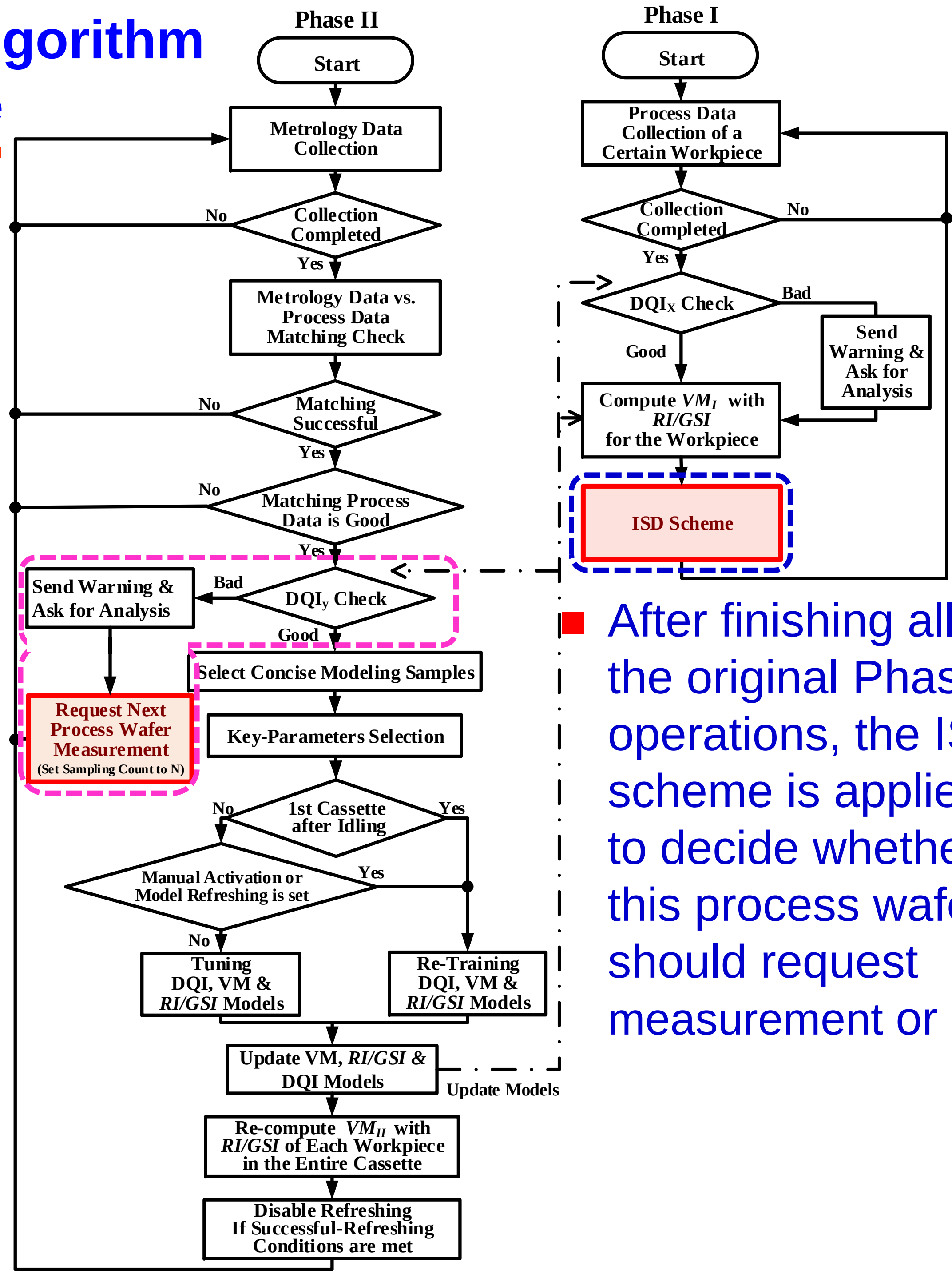
Illustrative Example of Semiconductor Manufacturinfg

- Applying the Intelligent Sampling Decision (ISD) Scheme to accomplish Sampling Rate Reduction of PECVD manufacturing process

Advanced Dual-Phase Algorithm with ISD Scheme



- When a DQI_y abnormality occurs, the Sampling Count is set to N.
- This action enforces the current process wafer in ISD to be measured for compensating the loss that the original DQI_y abnormal wafer cannot be utilized to update VM models.

- After finishing all the original Phase-I operations, the ISD scheme is applied to decide whether this process wafer should request measurement or not.

ISD Example (1/3)

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- An illustrated example of reducing the sampling rate to 1/2 and 1/4 of the original setting using paired data of process and metrology values of 180 wafers from a plasma-enhanced chemical vapor deposition (PECVD) process.
- However, due to the fact that only the metrology wafers have their corresponding real metrology data for checking VM accuracy.
- For concise presentation, M is set to be 1; and N in the ISD scheme should be set to 1, 2, and 4. The original sampling rates 2/25, 1/25, and 1/50 are converted to rates 1/1, 1/2, and 1/4 respectively in this example.

ISD Example (2/3)

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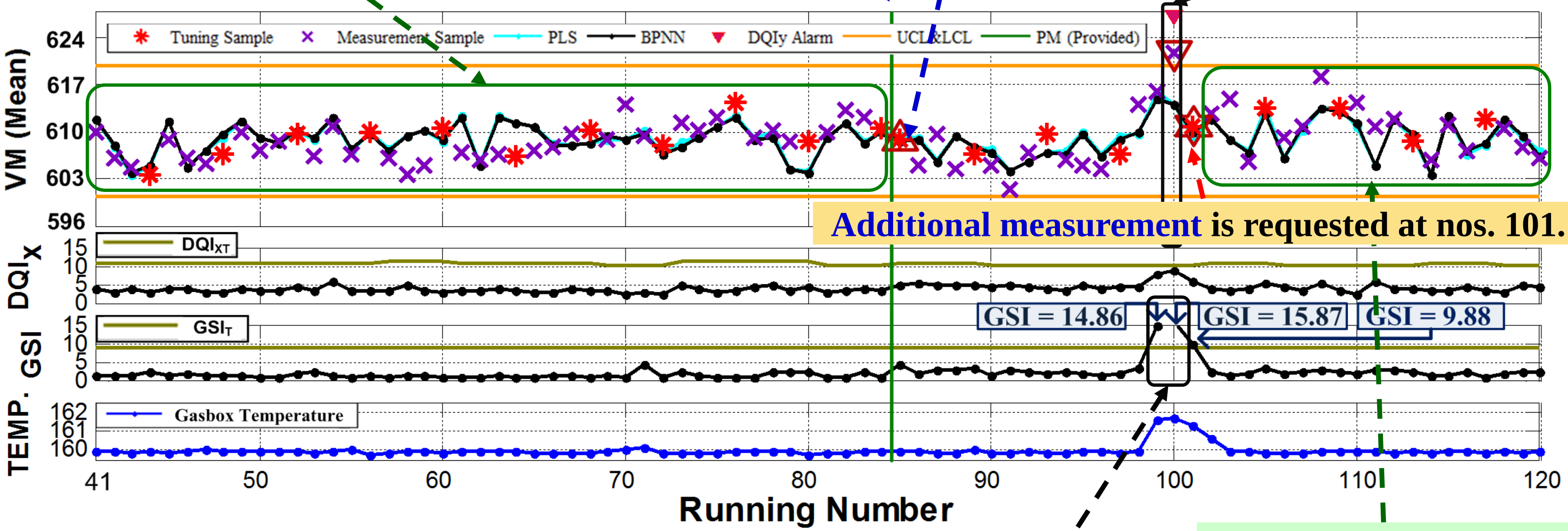
A PM operation causing status change appears in the time period between nos. 84 and 85.

ISD sends a measurement request at nos. 85 for updating the VM models.

Nos. 41-84 shows that only 1 out of 4 original samples is selected for updating the VM models because the manufacturing process is stable.

After obtaining the metrology value of nos. 100, the AVM system detects that it's DQI_y value is abnormal.



Additional measurement is requested at nos. 101.

Example of Sampling Rate Reduction to 1/4 using ISD Scheme

The stability of the manufacturing process is resumed

After the detection of two consecutive GSI alarms at nos.99 & 100, then the nos. 100 is requested to be measured.

PECVD process

ISD Example (3/3)

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- The accuracy comparison of sampling rate reduction from the original setting (1/1) to 1/2 and 1/4 with those 180 test wafers.

Sampling Rate Reduction using ISD Scheme

Sampling Rate		MAPE (%)		95% Max Error (%)	
		NN_I	PLS_I	NN_I	PLS_I
Original	1/1	0.41	0.42	0.86	0.81
ISD	1/2	0.40	0.40	0.87	0.90
ISD	1/4	0.40	0.41	0.88	0.91

- As a result, ISD can not only reduce sampling rate, but also keep VM accuracy at an acceptable level.

Remarks

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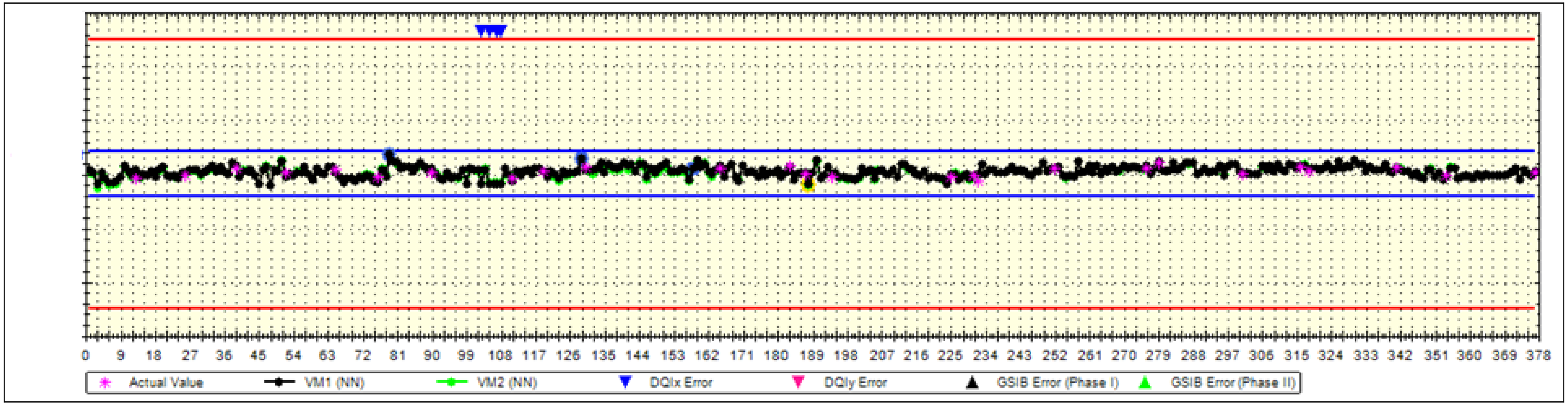
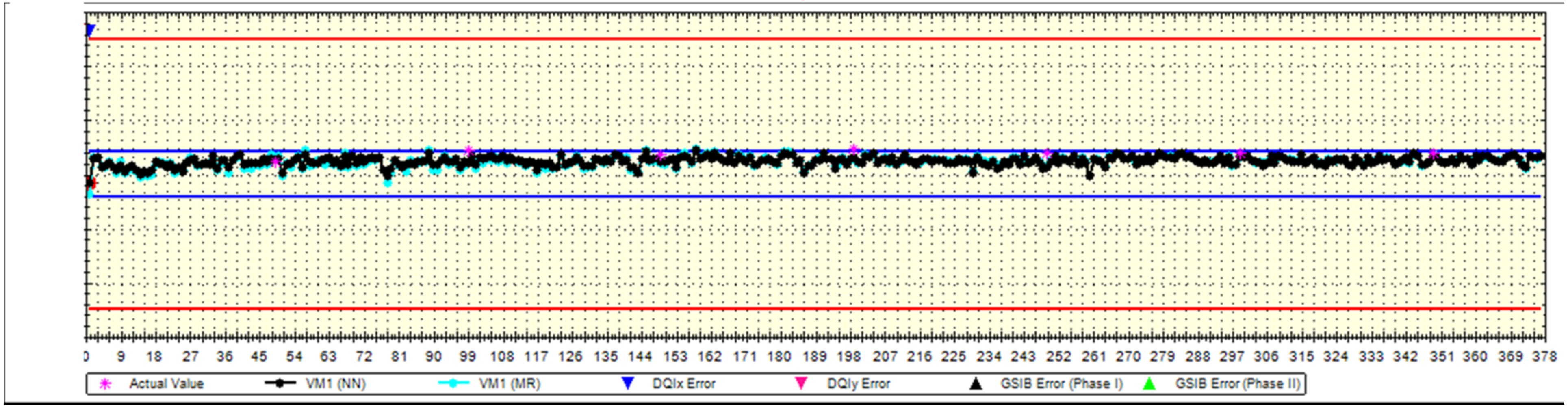
- The proposed ISD scheme can reduce sampling rate whenever a manufacturing process is stable.
- When the disruptions occurs, the ISD scheme will request additional measurements to update the VM models for maintaining the VM accuracy.
- Based on the example of a PECVD process in a foundry, the ISD scheme has been proven to be a powerful algorithm that can reduce the sampling rate to one fourth of the original setting and remain similar VM accuracy at the same time.
- By sampling rate reduction, the process cycle time of the metrology tools can be decreased such that the total production cost can be lowered.

Sampling Rates 2/25 vs. 1/50

Sampling Rate 2/25



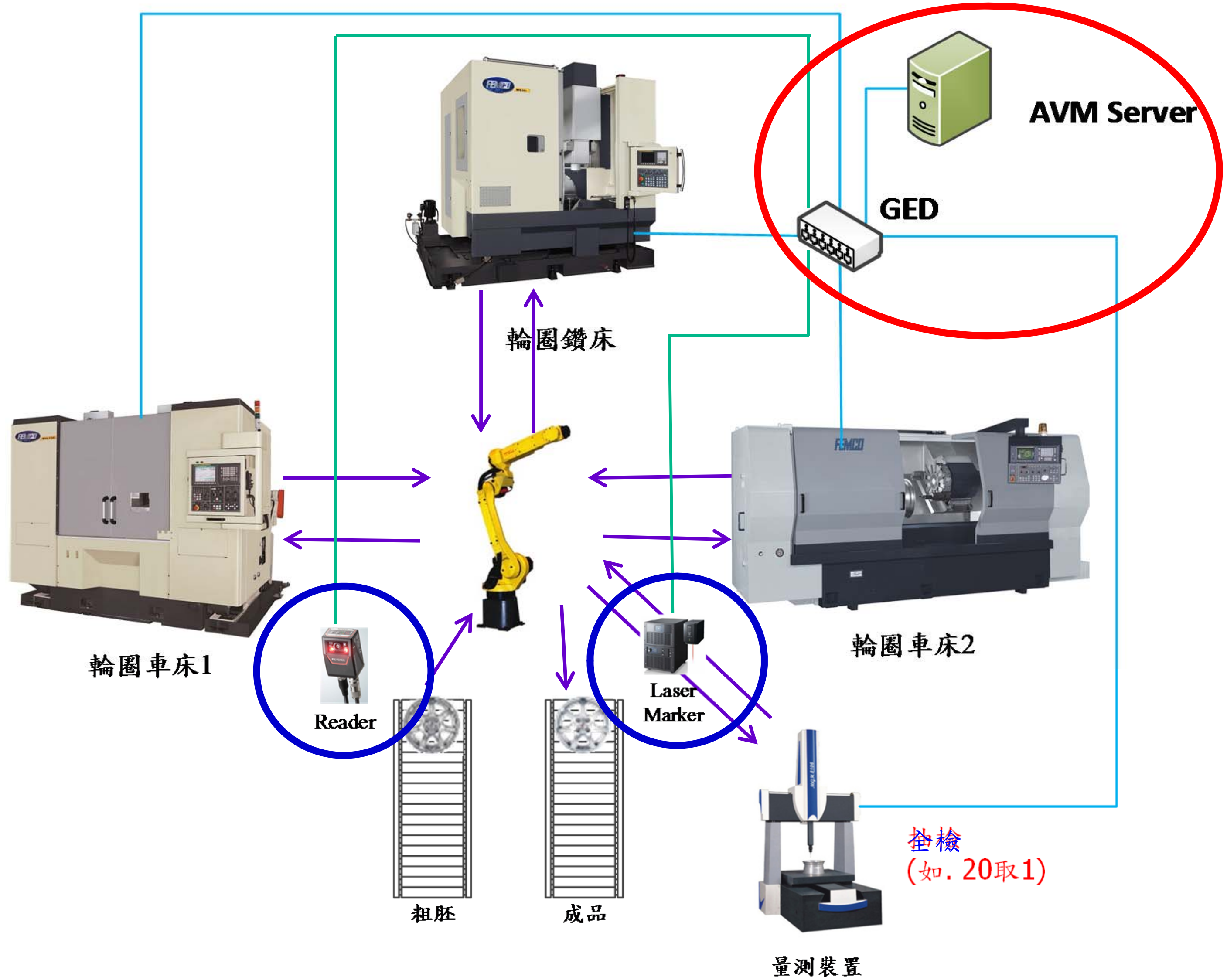
Sampling Rate 1/50



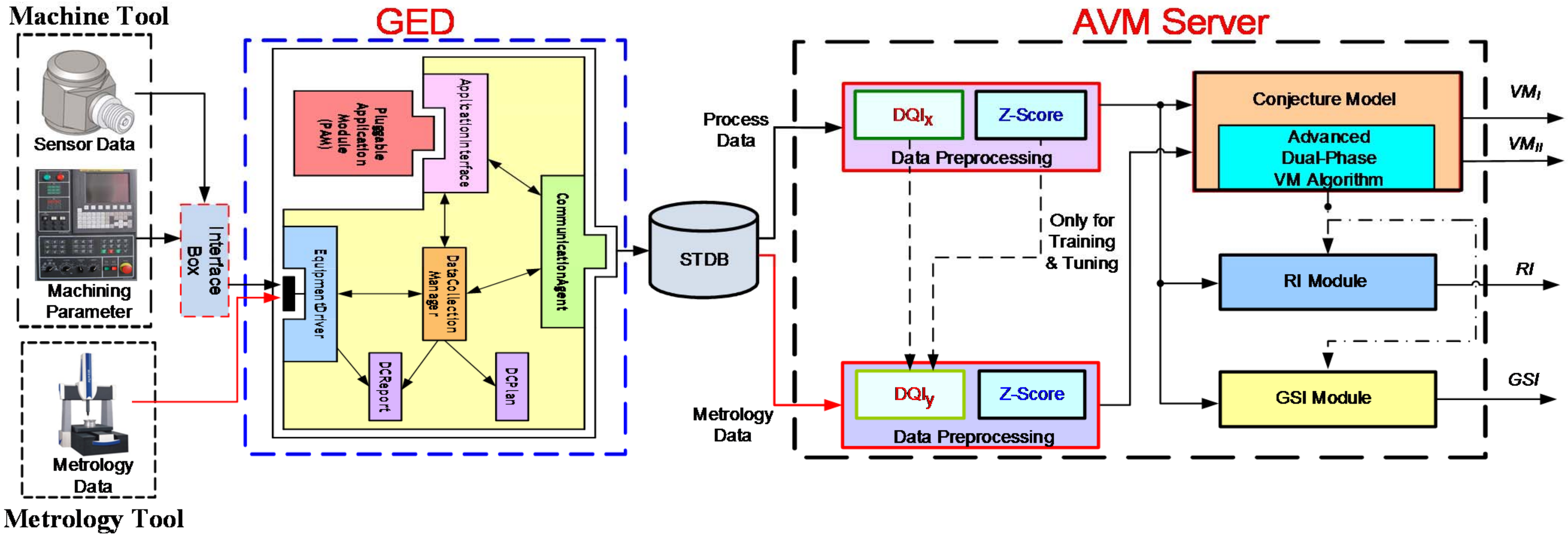
Illustrative Example of CNC Manufacturing

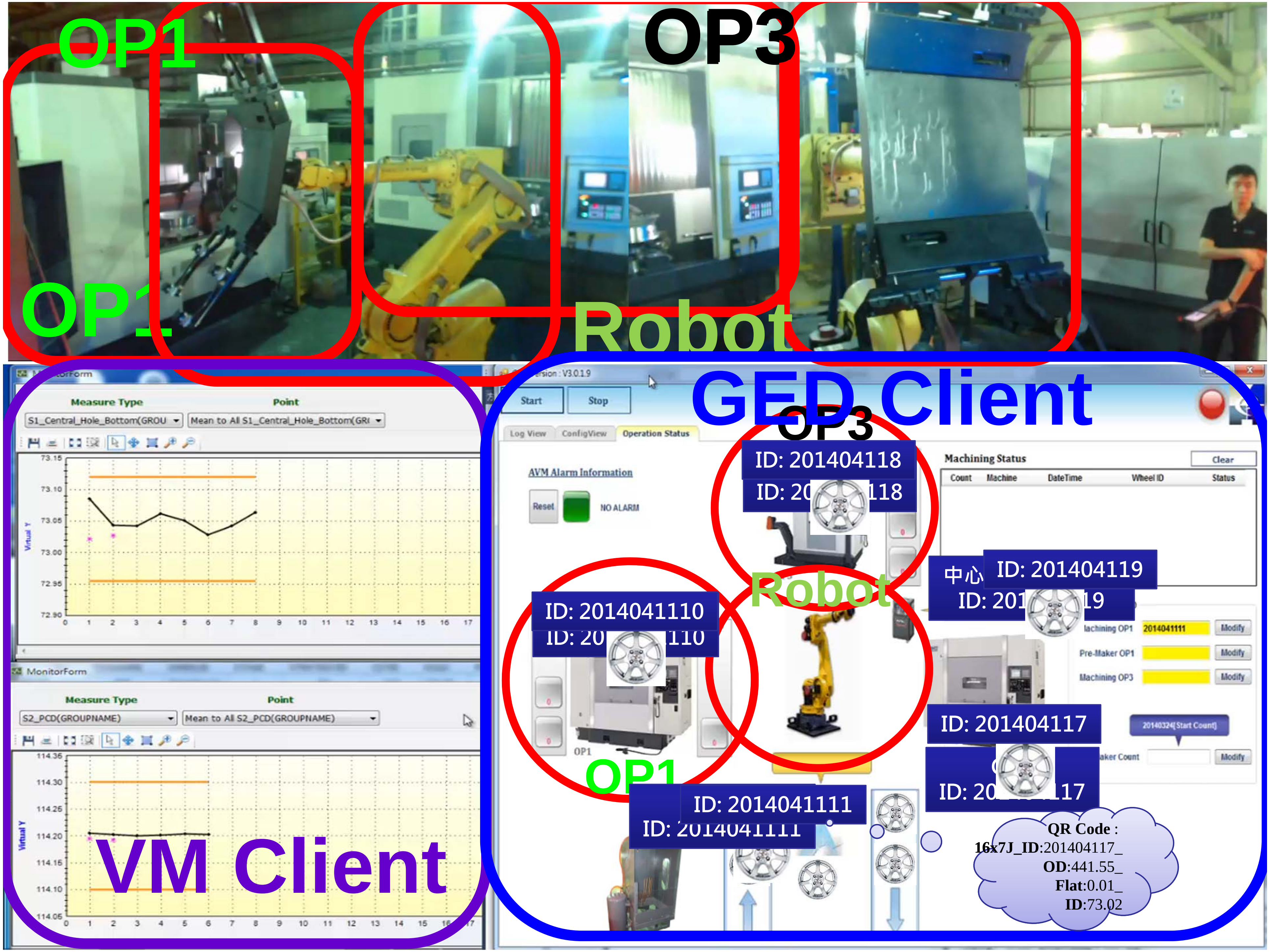
- Wheel Machining Automation

Applying AVM to Wheel Manufacturing Automation



GAVM (GED + AVM) for Machine Tools




OP1
OP1
OP3
Robot
GED Client
OP3
ID: 201404118
Robot
ID: 2014041110
OP1
ID: 201404119
ID: 201404117
ID: 2014041111
VM Client
Measure Type
Point
S1_Central_Hole_Bottom(GROU
Mean to All S1_Central_Hole_Bottom(GR
MonitorForm
S2_PCD(GROUPNAME)
Mean to All S2_PCD(GROUPNAME)
Start
Stop
Log View
ConfigView
Operation Status
AVM Alarm Information
Reset
NO ALARM
Machining Status
Clear
Count
Machine
DateTime
Wheel ID
Status
Pre-Maker OP1
Machining OP3
Modify
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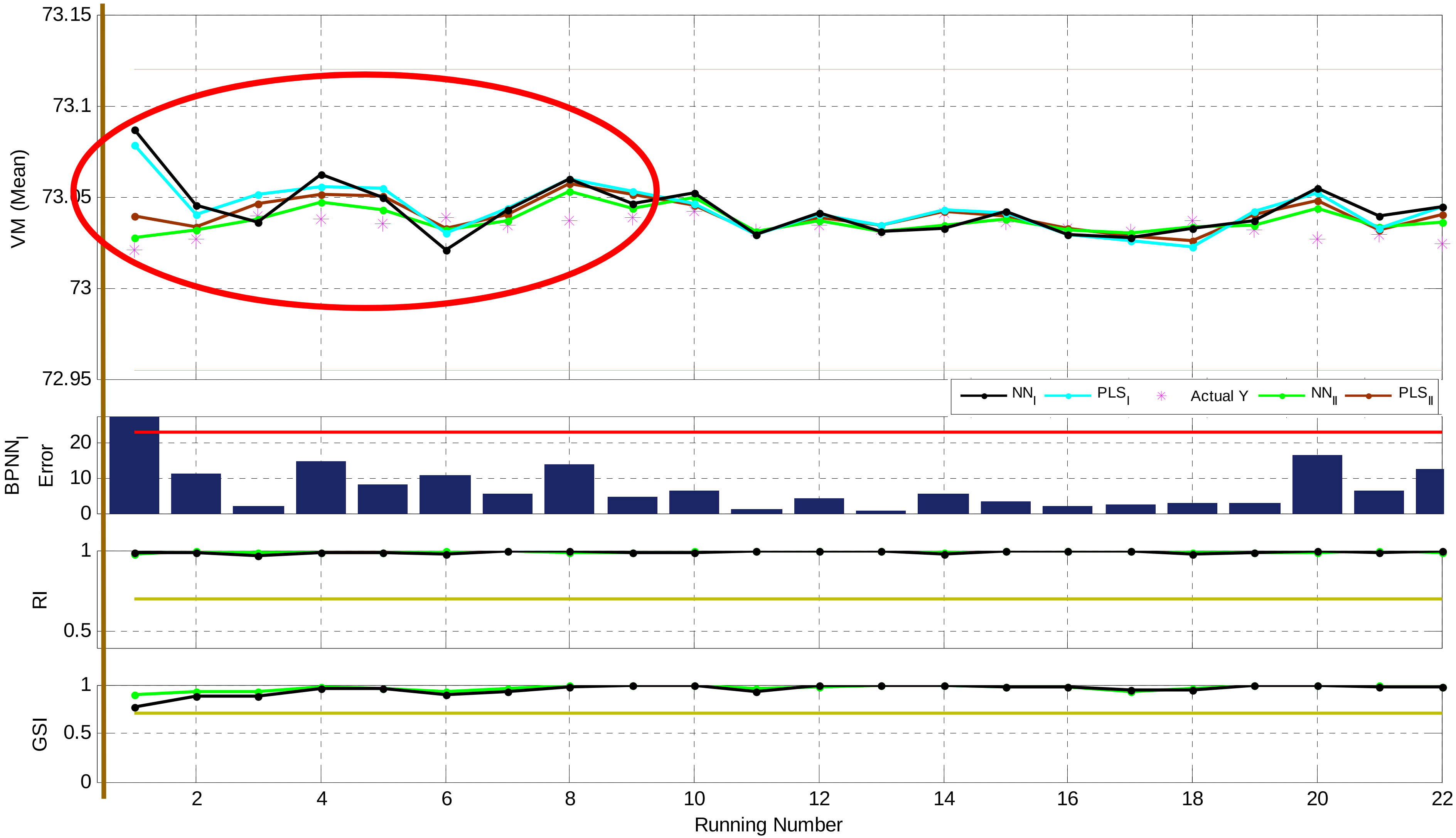
Central-Hole Diameter of OP1



Conclusions

Conclusions

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- The AVM System is a mature technology and has been deployed in various high-tech (semiconductor, TFT-LCD, Solar-Cell, etc.) and traditional (CNC) manufacturing systems.
- The TFT-LCD manufacturing flow and production tools are adopted as illustrative examples for fab-wide deployments of the AVM System.
- It is believed that the AVM technology can make real-time and on-line total inspection a reality.

AVM Related Papers

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[3] Y.-C. Su, T.-H. Lin, F.-T. Cheng, and W.-M. Wu, "Accuracy and Real-Time Considerations for Implementing Various Virtual Metrology Algorithms," *IEEE Transactions on Semiconductor Manufacturing*, vol. 21, no. 3, pp. 426-434, August 2008.

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[7] Y.-T. Huang and F.-T. Cheng, "Automatic Data Quality Evaluation for the AVM System," *IEEE Transactions on Semiconductor Manufacturing*, vol. 24, no. 3, pp. 445-454, August 2011.

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[10]M.-H. Hung, C.-F. Chen, H.-C. Huang, H.-C. Yang, and F.-T. Cheng, “Development of an AVM System Implementation Framework,” *IEEE Transactions on Semiconductor Manufacturing*, vol. 25, no. 4, pp. 598-613, November 2012.

[11]C.-A. Kao, F.-T. Cheng, W.-M. Wu, F.-W. Kong, and H.-H. Huang, "Run-to-Run Control Utilizing Virtual Metrology with Reliance Index,“ *IEEE Transactions on Semiconductor Manufacturing*, vol. 26, no. 1, pp. 69-81, February 2013.

[12]Y.-S. Hsieh, F.-T. Cheng, H.-C. Huang, C.-R. Wang, S.-C. Wang, and H.-C. Yang, “VM-based Baseline Predictive Maintenance Scheme,” *IEEE Transactions on Semiconductor Manufacturing*, vol. 26, no. 1, pp. 132-144, February 2013.

[13]F.-T. Cheng and Y.-C. Chiu, "Applying the Automatic Virtual Metrology System to Obtain Tube-to-Tube Control in a PECVD Tool," *IIE Transactions,* , vol. 45, issue 5, pp. 671-682, June 2013.

[14]H. Tieng, H.-C. Yang, M.-H. Hung, and F.-T. Cheng, “A Novel Virtual Metrology Scheme for Predicting Machining Precision of Machine Tools,” in *Proc. of The 2013 IEEE International Conference on Robotics and Automation (ICRA 2013)*, Karlsruhe, Germany, pp. 264-269, May 6-10, 2013.
[Best Automation Paper Award]

[15]F.-T. Cheng, C.-F. Chen, Y.-S. Hsieh, H.-H. Huang, and C.-C. Wu “Intelligent Sampling Decision Scheme Based on the AVM System,” *International Journal of Production Research*, vol. 53, no. 7, pp. 2073–2088, 2015. DOI: 10.1080/00207543.2014.955924.

[16]F.-T. Cheng, C.-A. Kao, C.-F. Chen, and W.-H. Tsai, “Tutorial on Applying the VM Technology for TFT-LCD Manufacturing,” *IEEE Transactions on Semiconductor Manufacturing*, vol. 28, no. 1, pp. 55-69, February 2015.

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AVM Related Patents

[A] Fan-Tien Cheng, Yeh-Tung Chen, and Yu-Chuan Su, "Method for Evaluating Reliance Level of a Virtual Metrology System in Product Manufacturing," U.S. Patent no.: 7,593,912 B2 and Taiwan R.O.C. Patent no.: I315054.

[B] Fan-Tien Cheng, Hsien-Cheng Huang, and Chi-An Kao, “Dual-Phase Virtual Metrology Method,” U.S. Patent no.: 7,603,328 B2, Taiwan R.O.C. Patent no.: I338916, Japan Patent no.: 4584295, China Patent no.: 823284, and Korea Patent no.: 10-0915339.
{行政院2011年傑出科技貢獻獎}
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{2012經濟部國家發明創作獎 發明獎金牌}
{2013 IEEE Inaba Technical Award for Innovation Leading to Production}

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Q&A