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ILI7807S

In-cell IC Integrates LTPS TFT LCD Driver and

Capacitive Touch Controller into a Single Chip

Display Resolution 1080(RGB) x 2520

Support 10-point Touch Capability

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1. Introduction

The ILI7807S is a single chip highly integrates LTPS TFT LCD driver and in-cell touch controller. ILI7807S combines with in-cell panel technology and provides high performance display and touch control for consumer electronic applications.

The LCD driver in ILI7807S supports resolution up to 1080(RGB) X 2560 and provides the number of colors up to 16.7M. The LCD driver is comprised of a 1080-channel source driver, a Gate-IC-less level shifter and a power supply circuit. In addition, Column / 1-dot / 2-dot / 4-dot liquid crystal inversion mode and IIE (Impressive Image Enhancement) function to achieve high-quality display and vision experience.

For high-speed serial interface, the MIPI DSI interface mode, the LCD driver in ILI7807S supports four data lanes and one clock lane for high-speed and low power transmission in both directions with low EMI noise. The ILI7807S operates a wide range of an analog power supplies. The ILI7807S supports sleep mode and deep standby power management functions, making the ILI7807S an ideal LCD driver for medium or small sized portable products such as digital cellular phones, smart phones, MP3 players, personal media players and similar devices with color graphics display where conserving battery power is desired. Additionally, it has an internal DC/DC converter that generates the LCD driving voltage and the voltage follower circuit for LCD driver.

The touch panel controller of ILI7807S uses a 32-bit high-performance single-cycle instruction-set MCU. With its built-in high-speed high-performance hardware-accelerated computing modules, it provides superior data processing capabilities. ILI7807S AFE can scan and detect panel, so that it reaches point reporting rate over 120Hz. With ILITEK's driving technology and algorithms, the touch controller has excellent waterproof performance, strong anti-noise-and-interference ability and high signal to noise ratio. Its touch experience can achieve up to 10points to provide customers with better touch experience.

As to its application, ILI7807S supports the touch screen display panel, and it can be widely used in smartphones, GPS, digital cameras, portable PDA and other mobile devices.

2. Features

2.1 Display Resolution Options：

- 1080(RGB) x 1920 (16:9) to 1080(RGB) x 2520 (21:9) 1:3 MUX for source
- 720(RGB) x 1280 (16:9) to 720(RGB) x 1680 (21:9) 1:3 MUX for source

2.2 Display Color Modes：

- 16.7M colors (24-bit data, R: 8-bit, G: 8-bit, B: 8-bit)

2.3 Interface types：

- MIPI DSI interface：
  - Supports DSI Version 1.02.00
  - Supports D-PHY Version 1.2
  - Supports D-PHY 4 data lanes / maximum bit rates 1.2Gbps per lane
  - Supports C-PHY Version 1.1
  - Supports C-PHY 3 trios (9 wires) / maximum bit rates 1Gsps per wire
  - Supports VESA DSC version 1.1

2.4 Image Quality for Display：

- Supports 1080(RGB) source channel outputs
- Supports GOUTR[24:1] / GOUTL[24:1] gate/source control signals
- Supports Column / 1-dot / 2-dot / 4-dot
- Support Dynamic frame rate swtich control(30Hz~120Hz)

2.5 Image Process for Display：

- Separate RGB gamma correction
- Supports CABC (Content Adaptive Brightness Control) function
- Support IIE (Impressive Image Enhancement) function
  - Color enhancement
  - Hue adjustment
  - Contrast enhancement
  - Sharpness enhancement
  - Sunlight readability
- Supports up scaling function (HD to FHD)
- Supports white point adjustment
- Supports Notch display compensation
- Supports Adaptive Refresh Rate function

2.6 Other on-chip functions：

- MIPI-DSI supports DC swap and P/N swap
- Supports DC VCOM (60Hz and Low frame rate) driving and adjustable voltage

- Abnormal power off image sticking prevention
- OTP for LTPS control setting, Gamma setting (120/90/60/30Hz) 2 times, VCOM(120/90/60/30Hz) 4 times, ID1/2/3/4 4 times.
- Support BIST (Built-in Self Test) function
- Support COF(chip on film) and COG (Chip on Glasss)
- Support Low frame rate application

2.7 Power Supply Range :

- 3 Power mode (VDDI / AVDD / AVEE)
  - VDDI - VSS：1.65V ~ 1.95V
  - AVDD - VSS：4.5V ~ 6.3V
  - AVEE - VSS：-4.5V ~ -6.3V
- 4 Power mode (VDDI / AVDD / AVEE / VDD)
  - VDDI - VSS：1.65V ~ 1.95V
  - AVDD - VSS：4.5V ~ 6.3V
  - AVEE - VSS：-4.5V ~ -6.3V
  - VDD - VSS：1.25V ~1.32V

2.8 Charge Pump / Regulator Output Voltage for Panel：

- Source driver output：GVDDP ~ 0.2V, -0.2V~ GVDDN
- Gamma voltage：GVDDP = 3V~6.0V (20mv/step), GVDDN = -3V ~ -6.0V (20mv/step)
- Gate driver output：VGHO = 5V ~ 14V (50mv/step), VGLO = -5V ~ -12V (50mv/step)
- VCOM output：+1V ~ -2V (10mv/step)

2.9 Power saving mode：

- Idle Mode (Gesture wake up)

2.10 Operation temperature：

- -30℃ ~ 70℃

2.11 Touch Spec：

- 32-bit embedded MCU
- Flash size 128Kbyte
- Self-type capacitance
- 648 (36*18) channels
- Wake-up gesture
- Water proof
- Multi touch at glove
- Support Passive stylus
- High Accuracy & Linearity

- Noise Imunity
- 10 fingers support
- Anti-Bending
- Host download

3. Device Overview

3.1. Block Diagram

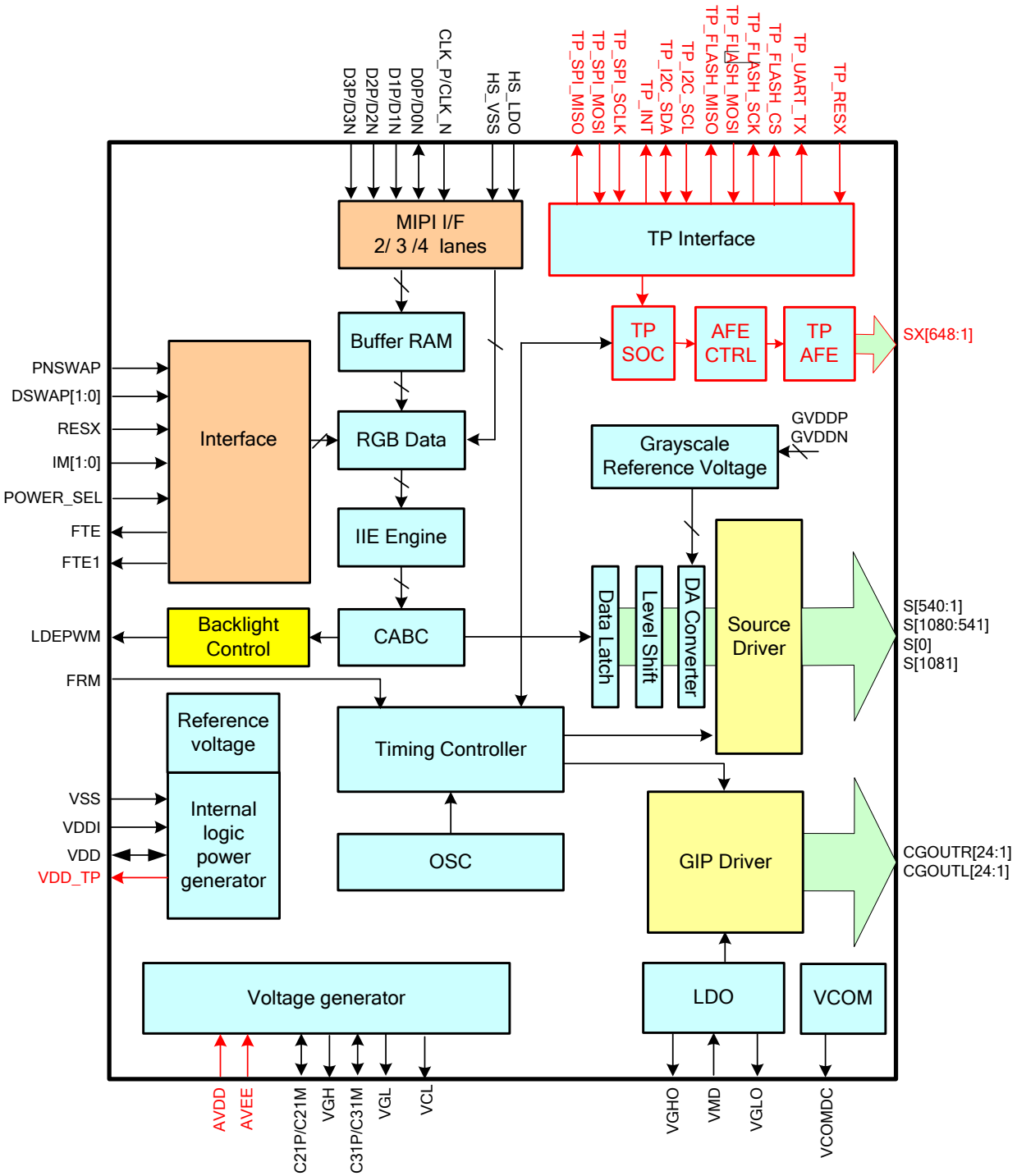


Figure 1. Block Diagram

3.2. Block Function Description

3.2.1. System Interface for Display

The ILI7807S supports DSI interfaces. The swap definition of MIPI DSI output signals is controlled by hardware pins DSWAP[1:0] and PNSWAP.

3.2.2. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates the LCD drive voltage which corresponds to 256 grayscale level set in the gamma correction register. The ILI7807S can display up to 16.7M colors at the maximum.

3.2.3. Timing Controller

The timing generator is used to generate timing signals for operating internal circuits. Timing for display operations and internal operations are outputted separately so that they do not interfere with each other.

3.2.4. Oscillator

The ILI7807S incorporates an RC oscillator circuit.

3.2.5. Source Driver Circuit

The LCD display driver circuit consists of a 1080-output source driver. The display pattern data is latched when 1080RGB pixels of data are input. The voltage is output from the source driver according to the latched data.

3.2.6. GIP Driver Circuit

The panel control circuit outputs GOUTR[24:1] and GOUTL[24:1] signals at either VGHO, VGLO level.

3.2.7. Voltage Generator Circuit

The LCD driver voltage generator circuit generates the voltage levels for driving a panel. Voltage levels are adjusted according to register setting.

3.2.8. MIPI DSI Controller Circuit

The MIPI DSI controller circuit consists of the D-PHY controller, Protocol Control Unit (PCU), Packet Processing Unit (PPU), ECC generating circuit, internal data/command buffer and analog transceiver. The D-PHY controls communication with the analog block and the ECC generating circuit generates the ECC to check the outgoing data stream for accuracy of the receiving data packet. The PCU controls outgoing and incoming data streams and the PPU controls transmitting packet distribution and merging. The internal data and command buffer is used for temporary storage of incoming command and display data.

3.2.9. CABC (Content Adaptive Brightness Control) Function

Content Adaptive Brightness Control (CABC), the backlight control circuit adjusts backlight brightness according to the histogram of image to reduce power consumption at the backlight. Brightness of the backlight and display data is adjusted.

3.2.10. AWB (Auto White Balance) Adjust Function

The color temperature of a light source is the temperature of an ideal black body radiator that radiates light of comparable hue to that of the light source. In LCD, color temperature is mainly determined by backlight LED. ILI7807S uses AWB function to change prefered white balance within a specific range.

3.2.11. Color Correction Function

To make colorimetric performance of all panels from different sources much closer, color correction uses matrix operation within RGB domain to transfer from one color space to the user-defined color space.

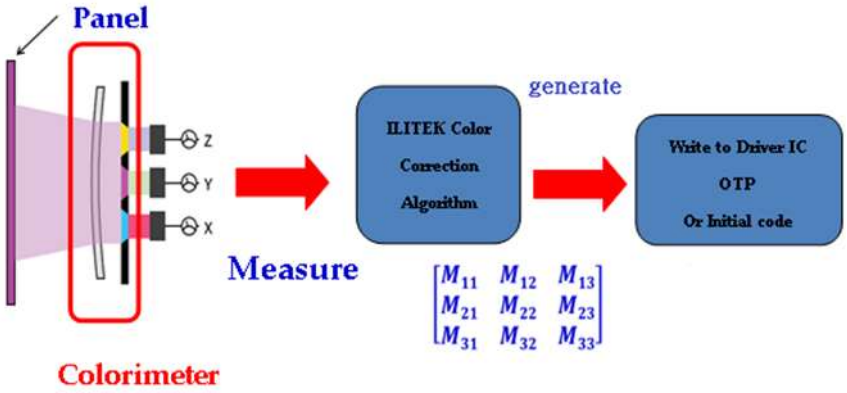


Figure 2 Color Correction Function

3.2.12. IIE (Impressive Image Enhancement) Function

- **Saturation (Color Enhancement)**

The saturation enhancement is used to enhance the color of image vividly.

- **Contrast Enhancement**

Contrast is the difference in color that makes an object distinguishable. The contrast enhancement is used to make the image clearly.

- **Sharpness Enhancement**

Sharpness is related to the edge contrast of an image. The sharpness enhancement IP is used to make the edge of image clearly.

- **Sunlight Readability Enhancement (SRE)**

The sunlight readability control circuit enhances the image data to make it easier to read under strong sunlight.

3.2.13. AFE Controller

AFE controller completes the driving and scanning of the sensors in the touch panel, and sends the data of touch sensors after scanning to the MCU for data processing.

3.2.14. TP SOC (Embedded MCU)

SOC complete the control, data processing, LCD operation and coordination, HOST communication and other functions of the whole touch systems. Firmware, stored in external flash memory, can be loaded into the internal SRAM by HOST via the SPI interface.

3.2.15. TP Interface

The interface of ILI7807S for touch communication with host can be I2C or SPI. Whenever there is effective touch sensed on the touch screen, Touch controller will send data transfer request to the HOST via I2C or SPI port, and complete the point report to the HOST. HOST can communicate with 7807Q via I2C or SPI. HOST can also reset Touch controller through TP_EXT_RSTN port.

3.2.16. External Flash

External flash is used to store the Firmware. ILI7807S supports the flash type of, and uses SPI interface to communicate with it.

3.2.17. SX Driving Circuit

Supply VCOM level when LCD driving. Generates TP sensing pulse when TP driving.

3.3. Pad Descriptions

Power Supply Pads			
Signal	I/O	Pad Type	Description
AVDD AVDD_DC	P	Analog Power	4.5 ~ 6.3V **Connect a capacitor for stabilization**
AVEE AVEE_DC	P	Analog Power	-4.5 ~ -6.3V **Connect a capacitor for stabilization**
VDDI VDDI_DC	P	Digital Power	Power Supply for IO, 1.65V~1.95V **Connect a capacitor for stabilization**
VDDAM	P	Digital Power	Power Supply for MIPI LDO, 1.65V ~ 1.95V
VDD	P	Digital Power	1.25 ~ 1.32V **Connect a capacitor for stabilization** **(Four power mode only)**
VDD_TP	O	Internal Power	Regulator output voltage. **Connect a capacitor for stabilization.** **FPC connect together w/ VDD.**
HS_LDO	O	Internal Power	Regulator output voltage. **Connect a capacitor for stabilization.** **FPC connect together w/ VDD.**
AVSS AVSS_DC	P	Analog Ground	Ground for Analog circuit
VSS	P	Digital Ground	Ground for Digital circuit
HS_VSS	P	Digital Ground	Ground for Analog circuit
VGS	P	Analog Ground	Ground for Analog circuit
CVSS_L CVSS_R	P	Analog Ground	Ground for Analog circuit
VCL	O	Analog Ground	-2.5~-3.3V **Connect a capacitor for stabilization.**
AVSST_L AVSST_R	P	Analog Ground	Ground for Analog circuit

Power Supply Circuit Pads (DC-DC Convereter)			
Signal	I/O	Pad Type	Description
VGH	O	Internal Power	Positive charge pump power **Connect a capacitor for stabilization.**
VGL	O	Internal Power	Negative charge pump power **Connect a capacitor for stabilization.**
C21P/C21M	O	Internal Power	Flying cap for VGH charge pump. **Connect to a Step-up capacitor as requirement.**
C31P/C31M	O	Internal Power	Flying cap for VGL charge pump. **Connect to a Step-up capacitor as requirement.**

Power Supply Circuit Pads (Regulator)			
Signal	I/O	Connection	Description
VGHO_L VGHO_R	O	Internal Power	Regulator output voltage generated from VGH. **Connect a capacitor for stabilization.**
VGLO_L VGLO_R	O	Internal Power	Regulator output voltage generated from VGL. **Connect a capacitor for stabilization.**
VCOM_L/R VCOM	O	Internal Power	Regulator output voltage. **Connect a capacitor for stabilization.** **FPC connect together.**
TPLDO_OUT_L TPLDO_OUT_R	O	Internal Power	Regulator output voltage. **Connect a capacitor for stabilization.** **FPC connect together.**
VMD	O	Internal Power	Touch Modulated voltage pin.

LCD Interface Logic Pad			
Signal	I/O	Connection	Description
RESX	I	Digital (VDDI)	The external reset input for LCD display(Active Low) Be sure to execute a power-on reset after supplying power.
PNSWAP DSWAP[1:0]	I	Digital (VDDI)	MIPI Lane Swap & Polarity control. MIPI Data Lane swap and polarity swap table. DPHY PNSWAP / DSWAP[1:0] / DSI_D2_P / DSI_D2_N / DSI_D1_P / DSI_D1_N / DSI_CLK_P / DSI_CLK_N / DSI_D0_P / DSI_D0_N / DSI_D3_P / DSI_D3_N 0 / 00 / D3_N / D3_P / D2_N / D2_P / CLK_N / CLK_P / D1_N / D1_P / D0_N / D0_P 0 / 01 / D3_N / D3_P / D0_N / D0_P / CLK_N / CLK_P / D1_N / D1_P / D2_N / D2_P 0 / 10 / D0_N / D0_P / D1_N / D1_P / CLK_N / CLK_P / D2_N / D2_P / D3_N / D3_P 0 / 11 / D2_N / D2_P / D1_N / D1_P / CLK_N / CLK_P / D0_N / D0_P / D3_N / D3_P 1 / 00 / D3_P / D3_N / D2_P / D2_N / CLK_P / CLK_N / D1_P / D1_N / D0_P / D0_N 1 / 01 / D3_P / D3_N / D0_P / D0_N / CLK_P / CLK_N / D1_P / D1_N / D2_P / D2_N 1 / 10 / D0_P / D0_N / D1_P / D1_N / CLK_P / CLK_N / D2_P / D2_N / D3_P / D3_N 1 / 11 / D2_P / D2_N / D1_P / D1_N / CLK_P / CLK_N / D0_P / D0_N / D3_P / D3_N CPHY PNSWAP / DSWAP[1:0] / DSI_D2_P / DSI_D2_N / DSI_D1_P / DSI_D1_N / DSI_CLK_P / DSI_CLK_N / DSI_D0_P / DSI_D0_N / DSI_D3_P / DSI_D3_N 0 / 00 / A0 / B0 / C0 / A2 / B2 / C2 / A1 / B1 / C1 0 / 01 / A1 / B1 / C1 / A2 / B2 / C2 / A0 / B0 / C0 0 / 10 / A0 / B0 / C0 / A1 / B1 / C1 / A2 / B2 / C2 0 / 11 / A2 / B2 / C2 / A1 / B1 / C1 / A0 / B0 / C0 1 / 00 / C0 / B0 / A0 / C2 / B2 / A2 / C1 / B1 / A1 1 / 01 / C1 / B1 / A1 / C2 / B2 / A2 / C0 / B0 / A0 1 / 10 / C0 / B0 / A0 / C1 / B1 / A1 / C2 / B2 / A2 1 / 11 / C2 / B2 / A2 / C1 / B1 / A1 / C0 / B0 / A0
TEST[2:0]	I	Digital (VDDI)	TEST input pins. For internal logic function test only. Connect to VSS, If not used.
FRM	I	Digital (VDDI)	Control Built-In Self Test (BIST) function On/Off. 0: Disable ; 1: Enable IC internal pull low. Connect to VSS, If not used.

CABC_PWM_OUT	O	Digital (VDDI)	Backlight on/off control pin. Connect to external LED driver IC. If not used, let it open.
TE TE1	O	Digital (VDDI)	Tearing Effect pin. If not used, let it open.

MIPI-DSI Interface Signal Input Pads			
Signal	I/O	Connection	Description
CLK_P/N	I	MIPI (HS_LDO)	MIPI-DSI CLOCK differential signal input pins. If not used, please connect to HSVSS.
DATA0P/N	I/O	MIPI (HS_LDO)	MIPI-DSI Data differential signal input pins. (Data Lane 0) If not used, please connect to HSVSS.
DATA1P/N	I/O	MIPI (HS_LDO)	MIPI-DSI Data differential signal input pins. (Data Lane 1) If not used, please connect to HSVSS.
DATA2P/N	I/O	MIPI (HS_LDO)	MIPI-DSI Data differential signal input pins. (Data Lane 2) If not used, please connect to HSVSS.
DATA3P/N	I/O	MIPI (HS_LDO)	MIPI-DSI Data differential signal input pins. (Data Lane 3) If not used, please connect to HSVSS.

TP Interface Logic Pads			
Signal	I/O	Connection	Description
TP_RESX	I	Digital (VDDI)	The external reset signal for Touch (Active low) IC internal open drain.
TP_I2C_SCL	I	Digital (VDDI)	I2C Clock. IC internal pull high.
TP_I2C_SDA	I/O	Digital (VDDI)	I2C Data. IC internal pull high.
TP_INT	O	Digital (VDDI)	Touch screen interrupt line. IC internal pull high.
TP_UART_TX	O	Digital (VDDI)	UART TX pad. If not used, please connect to VDDI or open.
TP_FLASH_CS	O	Digital (VDDI)	SPI master chip select output for serial flash interface. If not used, please connect to VDDI or open.
TP_FLASH_SCK	I/O	Digital (VDDI)	SPI master clock output for serial flash interface. If not used, please connect to VSS or open.
TP_FLASH_MOSI	I/O	Digital (VDDI)	SPI master data output for serial flash interface. If not used, please connect to VSS or open.

TP_FLASH_MISO	I/O	Digital (VDDI)	SPI master data input for serial flash interface. If not used, please connect to VDDI or open.
TP_TEST_EN	I	Digital (VDDI)	Touch test pin. If not used, please connect to VSS.
TP_SPI_CS	I	Digital (VDDI)	SPI slave chip select input If not used, please connect to VDDI or open.
TP_ SPI _SCLK	I	Digital (VDDI)	SPI slave clock input If not used, please connect to VSS or open.
TP_ SPI _MOSI	I	Digital (VDDI)	SPI slave master out slave in input If not used, please connect to VSS or open.
TP_ SPI _MISO	O	Digital (VDDI)	SPI slave master in slave out input If not used, please connect to VSS or open.

TEST Pads			
Signal	I/O	Connection	Description
SDO	O	Digital (VDDI)	Test pad, leave It open.
SDI	I	Digital (VDDI)	Test pad, leave It open.
SCL	I	Digital (VDDI)	Test pad, leave It open.
CSX	I	Digital (VDDI)	Test pad, leave It open.
DCX	I	Digital (VDDI)	Test pad, leave It open.
PCLK	I/O	Digital (VDDI)	Test pad, leave It open.
DE	I/O	Digital (VDDI)	Test pad, leave It open.
VSYNC	I/O	Digital (VDDI)	Test pad, leave It open.
HSYNC	I/O	Digital (VDDI)	Test pad, leave It open.
TP_TEST_L[3:0] TP_TEST_R[3:0]	I/O	Digital (AVDD)	Touch digital test pad, not accessible to user. Leave it open.
TP_GPIO[8 :0]	I/O	Digital (VDDI)	Touch digital test pad, not accessible to user. Leave it open.
TS[7 :0]	I/O	Digital (VDDI)	Test pad, leave It open or tie to VSS
OSC	I	Digital (VDDI)	LCD test mode, external clock input. Test pad, leave It open.
IM[1:0]	I	Digital (VDDI)	Test pad, these pins must be connected to VSS. 00: D-PHY 11: C-PHY
TCKC	I/O	Digital (VDDI)	Test pad, leave It open.
TMSC	I/O	Digital (VDDI)	Test pad, leave It open.
TP_EXTCLK	I/O	Digital (VDDI)	Test pad, leave It open.
POWER_SEL	I	Digital (VDDI)	Power mode test pin, please connect to VSS POWER_SEL: Low — 3-power mode; High — 4-power mode

TP_PWR_TEST	O	Digital (VDDI)	Test pad, leave It open.

Driving Pads			
Signal	I/O	Connection	Description
S[1080:1]	O	Analog (AVDD)	Source Output
S[1081] S[0]	O	Analog (AVDD)	Source Dummy Pin (For R/G/B Shift use)
SX[648:1]	I/O	Analog (AVDD)	Separate COM Electrode (TP Sensor Pins)
CGOUTL[24:1]	O	Analog (VGHO/VGLO)	GOA output. CGOUT[24:1] can output CLK signal.
CGOUTR[24:1]			
DUMMY[7:0]	I/O	Analog	Dummy pin
COGTEST12 COGTEST34	-	-	Dummy Pad for ITO trace resistance measurement.

3.4. Pad assignment (COG)

<Chip size with scribe line>

X	Y
32,800	910

PAD Configuration (不含COF DUMMY)	
Total Input Pad Number	739
Total Output Pad Number	1792
Total Pad Number	2531

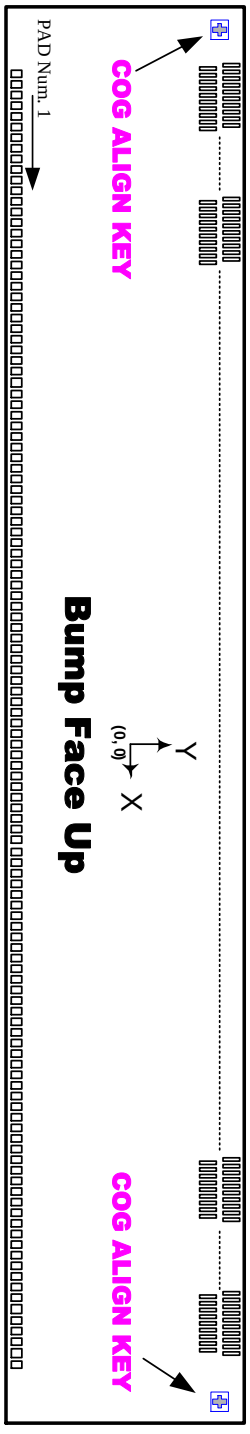
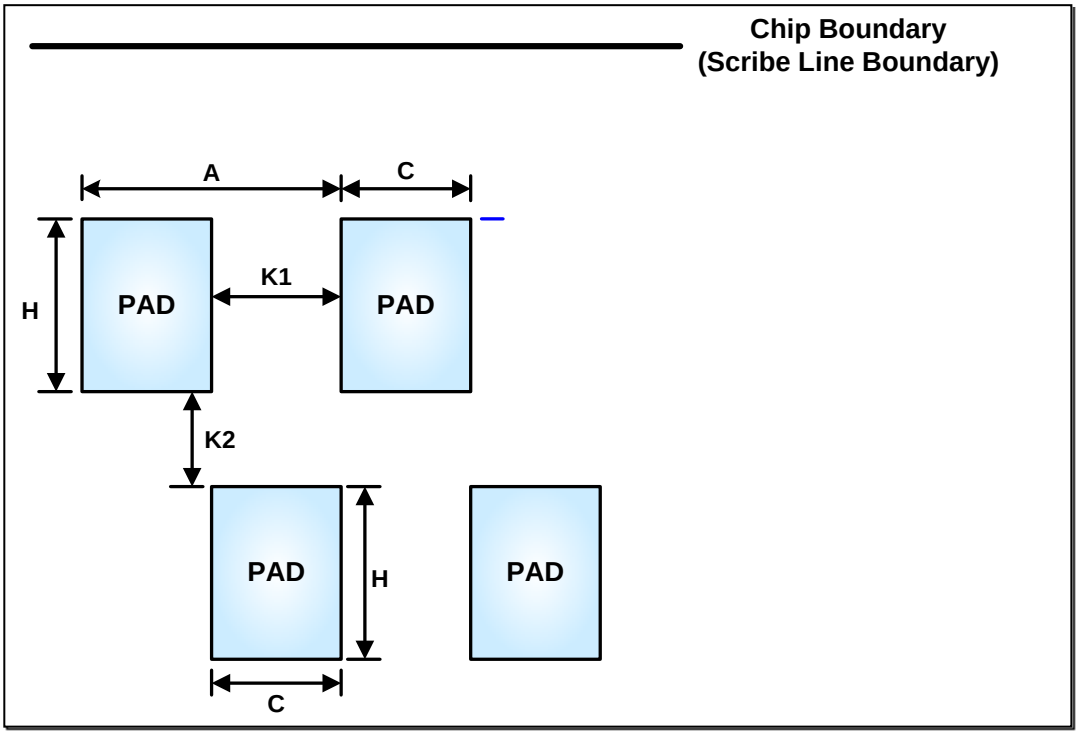


Figure 3. Pad Assignment Diagram

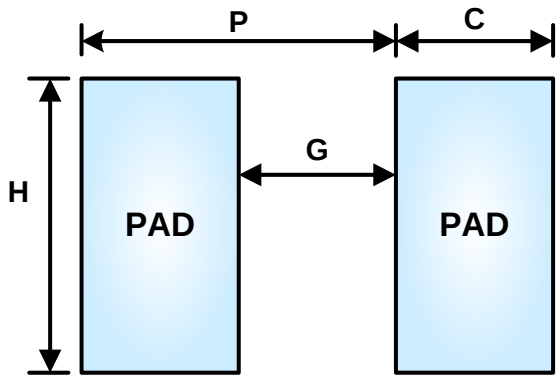
3.5. Bump Arrangement

Output Pad



OLB Bump Dimension	
Bump Width (C)	18
Bump Height (H)	90
Bump Gap (K1) (Horizontal)	18
Bump Gap (K2) (Vertical)	25
Bump Pitch (A)	36
Bump Area (um2)	1620

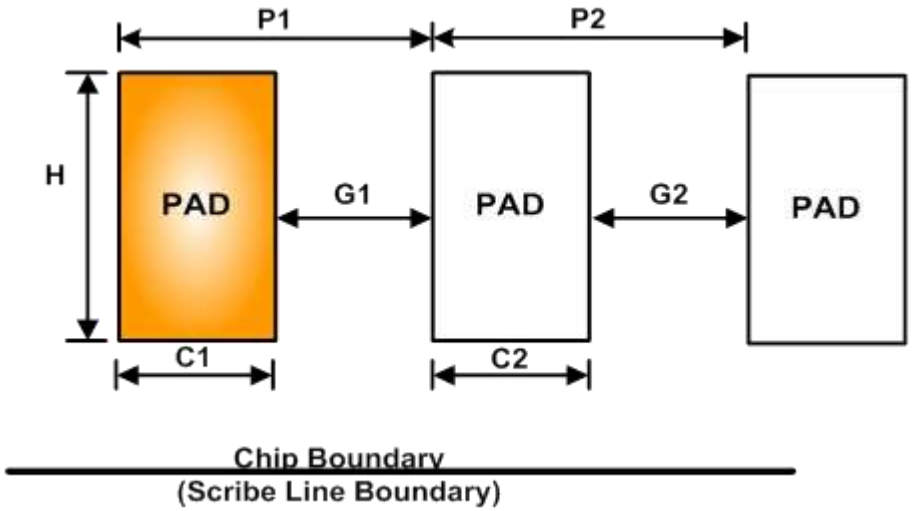
Input Pad



Chip Boundary
(Scribe Line Boundary)

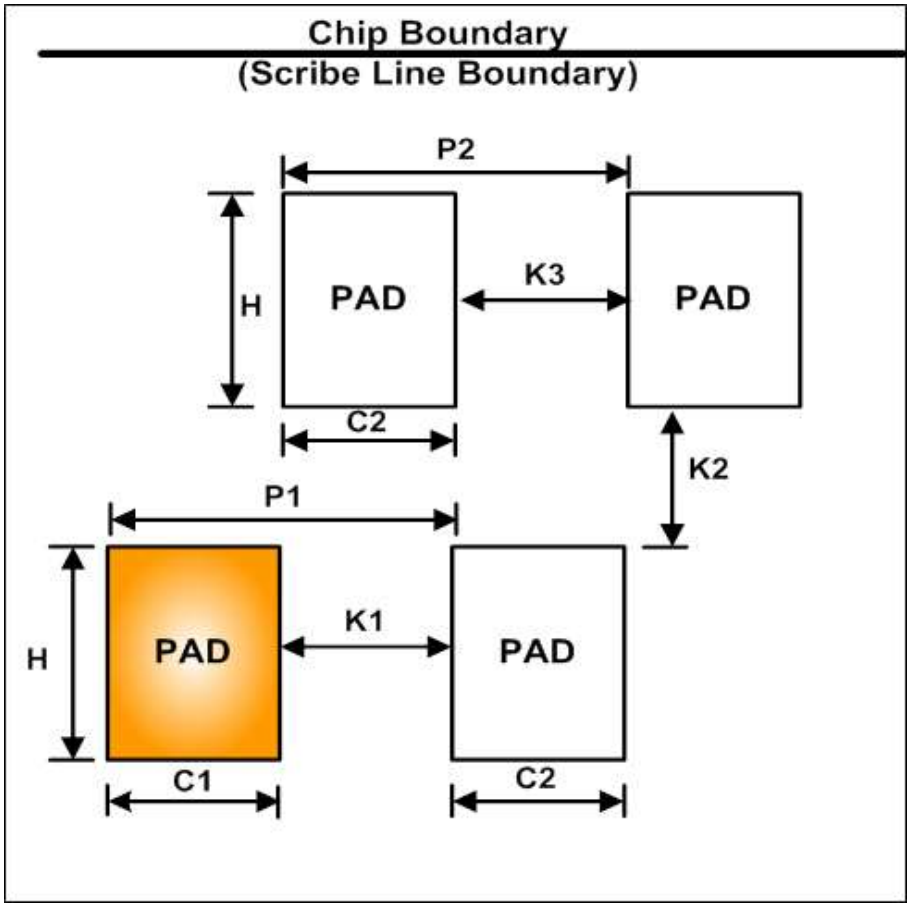
ILB Bump Dimension	
Bump Width (C)	24
Bump Height (H)	115
Bump Gap (G)	20
Bump Pitch (P)	44
Bump Area (um2)	2760

Dummy Pad



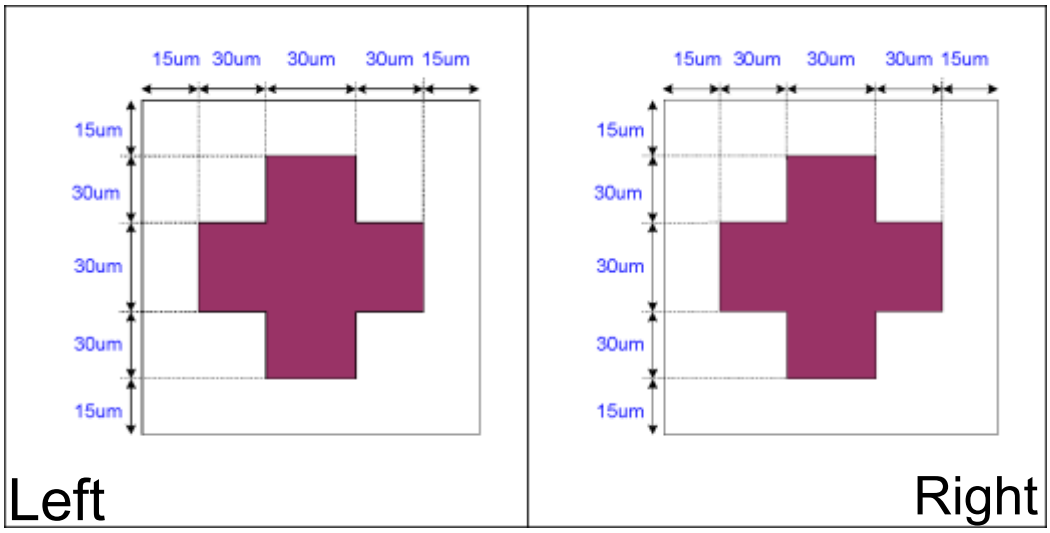
ILB DUMMY Bump Dimension of COF	
Bump Width (C1)	36
Bump Width (C2)	24

Bump Height (H)	50
Bump Gap (G1)	20
Bump Gap (G2)	20
Bump Pitch (P1)	56
Bump Pitch (P2)	44
DUMMY Bump Area (um2)	1800



OLB DUMMY Bump Dimension of COF	
Bump Width (C1)	27
Bump Width (C2)	18
Bump Height (H)	50
Bump Gap (K1) (Horizontal)	193.5
Bump Gap (K2) (Vertical)	25
Bump Gap (K3) (Horizontal)	18
Bump Pitch (P1) (A)	220.5
Bump Pitch (P2) (A)	36
DUMMY Bump Area (um2)	1350

Alignment Mark



Index	X-Position	Y-Postion
Alignment Mark Left	-16235	325
Alignment Mark Right	16235	325

3.6. Pad Coordination

No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
1	TP_TEST_L[0]	-16236	-317.5	61	VMD	-13596	-317.5	121	VGH	-10956	-317.5	181	AVEE	-8316	-317.5
2	TP_TEST_L[1]	-16192	-317.5	62	VMD	-13552	-317.5	122	VGH	-10912	-317.5	182	VDD	-8272	-317.5
3	CGOUTL[24]	-16148	-317.5	63	VMD	-13508	-317.5	123	VGH	-10868	-317.5	183	VDD	-8228	-317.5
4	CGOUTL[23]	-16104	-317.5	64	VMD	-13464	-317.5	124	VGH	-10824	-317.5	184	VDD	-8184	-317.5
5	CGOUTL[22]	-16060	-317.5	65	VMD	-13420	-317.5	125	C21P	-10780	-317.5	185	VDD	-8140	-317.5
6	CGOUTL[21]	-16016	-317.5	66	VMD	-13376	-317.5	126	C21P	-10736	-317.5	186	VDD	-8096	-317.5
7	CGOUTL[20]	-15972	-317.5	67	VMD	-13332	-317.5	127	C21P	-10692	-317.5	187	VDD	-8052	-317.5
8	CGOUTL[19]	-15928	-317.5	68	VMD	-13288	-317.5	128	C21P	-10648	-317.5	188	VDD	-8008	-317.5
9	CGOUTL[18]	-15884	-317.5	69	TPLDO_OUT_L	-13244	-317.5	129	C21P	-10604	-317.5	189	VDD	-7964	-317.5
10	CGOUTL[17]	-15840	-317.5	70	TPLDO_OUT_L	-13200	-317.5	130	C21M	-10560	-317.5	190	VDD	-7920	-317.5
11	CGOUTL[16]	-15796	-317.5	71	TPLDO_OUT_L	-13156	-317.5	131	C21M	-10516	-317.5	191	VDD	-7876	-317.5
12	CGOUTL[15]	-15752	-317.5	72	TPLDO_OUT_L	-13112	-317.5	132	C21M	-10472	-317.5	192	VDD	-7832	-317.5
13	CGOUTL[14]	-15708	-317.5	73	TPLDO_OUT_L	-13068	-317.5	133	C21M	-10428	-317.5	193	VDD	-7788	-317.5
14	CGOUTL[13]	-15664	-317.5	74	TPLDO_OUT_L	-13024	-317.5	134	C21M	-10384	-317.5	194	AVSS	-7744	-317.5
15	CGOUTL[12]	-15620	-317.5	75	TP_TEST_L[2]	-12980	-317.5	135	C21M	-10340	-317.5	195	AVSS	-7700	-317.5
16	CGOUTL[11]	-15576	-317.5	76	TP_TEST_L[3]	-12936	-317.5	136	VGL	-10296	-317.5	196	AVSS	-7656	-317.5
17	CGOUTL[10]	-15532	-317.5	77	AVSS	-12892	-317.5	137	VGL	-10252	-317.5	197	AVSS	-7612	-317.5
18	CGOUTL[9]	-15488	-317.5	78	AVSS	-12848	-317.5	138	VGL	-10208	-317.5	198	AVSS	-7568	-317.5
19	CGOUTL[8]	-15444	-317.5	79	AVSS	-12804	-317.5	139	VGL	-10164	-317.5	199	AVSS	-7524	-317.5
20	CGOUTL[7]	-15400	-317.5	80	AVSS	-12760	-317.5	140	VGL	-10120	-317.5	200	AVSS	-7480	-317.5
21	CGOUTL[6]	-15356	-317.5	81	AVSS	-12716	-317.5	141	CVSS_L	-10076	-317.5	201	AVSS	-7436	-317.5
22	CGOUTL[5]	-15312	-317.5	82	AVSS	-12672	-317.5	142	CVSS_L	-10032	-317.5	202	AVSS	-7392	-317.5
23	CGOUTL[4]	-15268	-317.5	83	AVSS	-12628	-317.5	143	CVSS_L	-9988	-317.5	203	AVSS	-7348	-317.5
24	CGOUTL[3]	-15224	-317.5	84	AVSS	-12584	-317.5	144	CVSS_L	-9944	-317.5	204	AVSS	-7304	-317.5
25	CGOUTL[2]	-15180	-317.5	85	AVSS	-12540	-317.5	145	CVSS_L	-9900	-317.5	205	AVSS	-7260	-317.5
26	CGOUTL[1]	-15136	-317.5	86	AVSS	-12496	-317.5	146	CVSS_L	-9856	-317.5	206	AVSS	-7216	-317.5
27	COGTEST12	-15092	-317.5	87	AVSS	-12452	-317.5	147	CVSS_L	-9812	-317.5	207	VSS	-7172	-317.5
28	COGTEST12	-15048	-317.5	88	AVSS	-12408	-317.5	148	CVSS_L	-9768	-317.5	208	VSS	-7128	-317.5
29	VGLO_L	-15004	-317.5	89	AVSS	-12364	-317.5	149	AVDD	-9724	-317.5	209	VSS	-7084	-317.5
30	VGLO_L	-14960	-317.5	90	TPLDO_OUT_L	-12320	-317.5	150	AVDD	-9680	-317.5	210	VSS	-7040	-317.5
31	VGLO_L	-14916	-317.5	91	TPLDO_OUT_L	-12276	-317.5	151	AVDD	-9636	-317.5	211	VSS	-6996	-317.5
32	VGLO_L	-14872	-317.5	92	TPLDO_OUT_L	-12232	-317.5	152	AVDD	-9592	-317.5	212	VSS	-6952	-317.5
33	VGHO_L	-14828	-317.5	93	TPLDO_OUT_L	-12188	-317.5	153	AVDD	-9548	-317.5	213	VSS	-6908	-317.5
34	VGHO_L	-14784	-317.5	94	TPLDO_OUT_L	-12144	-317.5	154	AVDD	-9504	-317.5	214	VSS	-6864	-317.5
35	VGHO_L	-14740	-317.5	95	TPLDO_OUT_L	-12100	-317.5	155	AVDD	-9460	-317.5	215	VDD_TP	-6820	-317.5
36	VGHO_L	-14696	-317.5	96	TPLDO_OUT_L	-12056	-317.5	156	AVDD	-9416	-317.5	216	VDD_TP	-6776	-317.5
37	AVSST_L	-14652	-317.5	97	TPLDO_OUT_L	-12012	-317.5	157	AVDD	-9372	-317.5	217	VDD_TP	-6732	-317.5
38	AVSST_L	-14608	-317.5	98	TPLDO_OUT_L	-11968	-317.5	158	AVDD	-9328	-317.5	218	VDD_TP	-6688	-317.5
39	AVSST_L	-14564	-317.5	99	TPLDO_OUT_L	-11924	-317.5	159	AVDD	-9284	-317.5	219	VDD_TP	-6644	-317.5
40	AVSST_L	-14520	-317.5	100	TPLDO_OUT_L	-11880	-317.5	160	AVDD	-9240	-317.5	220	VDD_TP	-6600	-317.5
41	AVSST_L	-14476	-317.5	101	TPLDO_OUT_L	-11836	-317.5	161	AVDD	-9196	-317.5	221	VDD_TP	-6556	-317.5
42	AVSST_L	-14432	-317.5	102	VGS	-11792	-317.5	162	AVDD	-9152	-317.5	222	VDD_TP	-6512	-317.5
43	AVSST_L	-14388	-317.5	103	VGS	-11748	-317.5	163	AVDD	-9108	-317.5	223	AVDD_DC	-6468	-317.5
44	AVSST_L	-14344	-317.5	104	VGS	-11704	-317.5	164	AVDD	-9064	-317.5	224	AVDD_DC	-6424	-317.5
45	AVSST_L	-14300	-317.5	105	VGS	-11660	-317.5	165	AVDD	-9020	-317.5	225	AVDD_DC	-6380	-317.5
46	VCOM_L	-14256	-317.5	106	VGS	-11616	-317.5	166	AVDD	-8976	-317.5	226	AVSS_DC	-6336	-317.5
47	VCOM_L	-14212	-317.5	107	VSS	-11572	-317.5	167	AVDD	-8932	-317.5	227	AVSS_DC	-6292	-317.5
48	VCOM_L	-14168	-317.5	108	VSS	-11528	-317.5	168	AVDD	-8888	-317.5	228	AVSS_DC	-6248	-317.5
49	AVEE	-14124	-317.5	109	VSS	-11484	-317.5	169	AVDD	-8844	-317.5	229	AVEE_DC	-6204	-317.5
50	AVEE	-14080	-317.5	110	VSS	-11440	-317.5	170	AVEE	-8800	-317.5	230	AVEE_DC	-6160	-317.5
51	AVEE	-14036	-317.5	111	VSS	-11396	-317.5	171	AVEE	-8756	-317.5	231	AVEE_DC	-6116	-317.5
52	AVEE	-13992	-317.5	112	VSS	-11352	-317.5	172	AVEE	-8712	-317.5	232	GVDDN	-6072	-317.5
53	AVEE	-13948	-317.5	113	VDD_TP	-11308	-317.5	173	AVEE	-8668	-317.5	233	GVDDP	-6028	-317.5
54	AVEE	-13904	-317.5	114	VDD_TP	-11264	-317.5	174	AVEE	-8624	-317.5	234	EXT_REF	-5984	-317.5
55	AVDD	-13860	-317.5	115	VDD_TP	-11220	-317.5	175	AVEE	-8580	-317.5	235	EXT_REF	-5940	-317.5
56	AVDD	-13816	-317.5	116	VDD_TP	-11176	-317.5	176	AVEE	-8536	-317.5	236	EXT_REF	-5896	-317.5
57	AVDD	-13772	-317.5	117	VDD_TP	-11132	-317.5	177	AVEE	-8492	-317.5	237	EXT_REF	-5852	-317.5
58	AVDD	-13728	-317.5	118	VDD_TP	-11088	-317.5	178	AVEE	-8448	-317.5	238	EXT_REF	-5808	-317.5
59	AVDD	-13684	-317.5	119	VGH	-11044	-317.5	179	AVEE	-8404	-317.5	239	EXT_REF	-5764	-317.5
60	AVDD	-13640	-317.5	120	VGH	-11000	-317.5	180	AVEE	-8360	-317.5	240	VCL	-5720	-317.5

No.	Text Name	X-axis	Y-axis
241	VCL	-5676	-317.5
242	VCL	-5632	-317.5
243	VCL	-5588	-317.5
244	VCL	-5544	-317.5
245	VCL	-5500	-317.5
246	VSS	-5456	-317.5
247	VSS	-5412	-317.5
248	VSS	-5368	-317.5
249	VSS	-5324	-317.5
250	VSS	-5280	-317.5
251	VSS	-5236	-317.5
252	VSS	-5192	-317.5
253	VDD	-5148	-317.5
254	VDD	-5104	-317.5
255	VDD	-5060	-317.5
256	VDD	-5016	-317.5
257	VDD	-4972	-317.5
258	VDD	-4928	-317.5
259	VDD	-4884	-317.5
260	VDDI_DC	-4840	-317.5
261	VDDI_DC	-4796	-317.5
262	VDDI_DC	-4752	-317.5
263	AVSS	-4708	-317.5
264	AVSS	-4664	-317.5
265	AVSS	-4620	-317.5
266	AVSS	-4576	-317.5
267	AVSS	-4532	-317.5
268	AVSS	-4488	-317.5
269	AVSS	-4444	-317.5
270	AVSS	-4400	-317.5
271	AVSS	-4356	-317.5
272	AVSS	-4312	-317.5
273	VDDI	-4268	-317.5
274	VDDI	-4224	-317.5
275	VDDI	-4180	-317.5
276	VDDI	-4136	-317.5
277	VDDI	-4092	-317.5
278	VDDI	-4048	-317.5
279	VDDI	-4004	-317.5
280	VDDI	-3960	-317.5
281	VDDI	-3916	-317.5
282	VDDI	-3872	-317.5
283	VDDI	-3828	-317.5
284	VDDI	-3784	-317.5
285	VDDI	-3740	-317.5
286	VDDI	-3696	-317.5
287	VDDI	-3652	-317.5
288	VDDI	-3608	-317.5
289	VDDI	-3564	-317.5
290	VDDI	-3520	-317.5
291	VDDI	-3476	-317.5
292	VDDI	-3432	-317.5
293	VDDI	-3388	-317.5
294	VDDI	-3344	-317.5
295	VSS	-3300	-317.5
296	VSS	-3256	-317.5
297	VSS	-3212	-317.5
298	VSS	-3168	-317.5
299	VSS	-3124	-317.5
300	VSS	-3080	-317.5

No.	Text Name	X-axis	Y-axis
301	VSS	-3036	-317.5
302	VSS	-2992	-317.5
303	VDD_TP	-2948	-317.5
304	VDD_TP	-2904	-317.5
305	VDD_TP	-2860	-317.5
306	VDD_TP	-2816	-317.5
307	VDD_TP	-2772	-317.5
308	VDD_TP	-2728	-317.5
309	VDD_TP	-2684	-317.5
310	VDD_TP	-2640	-317.5
311	VCOM	-2596	-317.5
312	VCOM	-2552	-317.5
313	VCOM	-2508	-317.5
314	VCOM	-2464	-317.5
315	VCOM	-2420	-317.5
316	VCOM	-2376	-317.5
317	VCOM	-2332	-317.5
318	VCOM	-2288	-317.5
319	VCOM	-2244	-317.5
320	VCOM	-2200	-317.5
321	VCOM	-2156	-317.5
322	VCOM	-2112	-317.5
323	VCOM	-2068	-317.5
324	VCOM	-2024	-317.5
325	VCOM	-1980	-317.5
326	VCOM	-1936	-317.5
327	VDD	-1892	-317.5
328	VDD	-1848	-317.5
329	VDD	-1804	-317.5
330	VDD	-1760	-317.5
331	VDD	-1716	-317.5
332	VDD	-1672	-317.5
333	VDD	-1628	-317.5
334	VDD	-1584	-317.5
335	VDD	-1540	-317.5
336	VDD	-1496	-317.5
337	VDD	-1452	-317.5
338	VDD	-1408	-317.5
339	TP_GPIO[6]	-1364	-317.5
340	TP_GPIO[6]	-1320	-317.5
341	POWER_SEL	-1276	-317.5
342	POWER_SEL	-1232	-317.5
343	TP_GPIO[5]	-1188	-317.5
344	VSS	-1144	-317.5
345	VSS	-1100	-317.5
346	VSS	-1056	-317.5
347	VSS	-1012	-317.5
348	VSS	-968	-317.5
349	VSS	-924	-317.5
350	VSS	-880	-317.5
351	VSS	-836	-317.5
352	VSS	-792	-317.5
353	VSS	-748	-317.5
354	VSS	-704	-317.5
355	VSS	-660	-317.5
356	VSS	-616	-317.5
357	VSS	-572	-317.5
358	TP_PWR_TEST	-528	-317.5
359	RESX	-484	-317.5
360	RESX	-440	-317.5

No.	Text Name	X-axis	Y-axis
361	TP_RESX	-396	-317.5
362	TP_RESX	-352	-317.5
363	TP_INT	-308	-317.5
364	TP_INT	-264	-317.5
365	TP_I2C_SDA	-220	-317.5
366	TP_I2C_SDA	-176	-317.5
367	TP_I2C_SCL	-132	-317.5
368	TP_I2C_SCL	-88	-317.5
369	TP_SPI_CS	-44	-317.5
370	TP_SPI_CS	0	-317.5
371	TP_SPI_MISO	44	-317.5
372	TP_SPI_MISO	88	-317.5
373	TP_SPI_MOSI	132	-317.5
374	TP_SPI_MOSI	176	-317.5
375	TP_SPI_SCLK	220	-317.5
376	TP_SPI_SCLK	264	-317.5
377	TP_EXTCLK	308	-317.5
378	TP_GPIO[4]	352	-317.5
379	TP_GPIO[7]	396	-317.5
380	TP_GPIO[8]	440	-317.5
381	TP_FLASH_CS	484	-317.5
382	TP_FLASH_MISO	528	-317.5
383	TP_FLASH_MOSI	572	-317.5
384	TP_FLASH_MOSI	616	-317.5
385	TP_FLASH_MOSI	660	-317.5
386	TP_FLASH_SCK	704	-317.5
387	TP_FLASH_SCK	748	-317.5
388	TP_FLASH_SCK	792	-317.5
389	VSS	836	-317.5
390	VSS	880	-317.5
391	VSS	924	-317.5
392	VSS	968	-317.5
393	VSS	1012	-317.5
394	VSS	1056	-317.5
395	VSS	1100	-317.5
396	VSS	1144	-317.5
397	VDD	1188	-317.5
398	VDD	1232	-317.5
399	VDD	1276	-317.5
400	VDD	1320	-317.5
401	VDD	1364	-317.5
402	VDD	1408	-317.5
403	VDD	1452	-317.5
404	VDD	1496	-317.5
405	VDD	1540	-317.5
406	TP_TEST_EN	1584	-317.5
407	TP_TCKC	1628	-317.5
408	TP_TMSC	1672	-317.5
409	TP_UART_TX	1716	-317.5
410	TP_GPIO[3]	1760	-317.5
411	TP_GPIO[2]	1804	-317.5
412	TP_GPIO[1]	1848	-317.5
413	TP_GPIO[0]	1892	-317.5
414	SDO	1936	-317.5
415	SDI	1980	-317.5
416	TEST[2]	2024	-317.5
417	TEST[1]	2068	-317.5
418	TEST[0]	2112	-317.5
419	PCLK	2156	-317.5
420	DE	2200	-317.5

No.	Text Name	X-axis	Y-axis
421	VSYNC	2244	-317.5
422	HSYNC	2288	-317.5
423	IM[1]	2332	-317.5
424	IM[0]	2376	-317.5
425	FRM	2420	-317.5
426	OSC	2464	-317.5
427	SCL	2508	-317.5
428	CSX	2552	-317.5
429	DCX	2596	-317.5
430	DSWAP[1]	2640	-317.5
431	DSWAP[0]	2684	-317.5
432	PNSWAP	2728	-317.5
433	TS[7]	2772	-317.5
434	TS[6]	2816	-317.5
435	TS[5]	2860	-317.5
436	TS[4]	2904	-317.5
437	CABC_PWM_OUT	2948	-317.5
438	TS[3]	2992	-317.5
439	TS[2]	3036	-317.5
440	TS[1]	3080	-317.5
441	TS[0]	3124	-317.5
442	TE	3168	-317.5
443	TE1	3212	-317.5
444	VDDI	3256	-317.5
445	VDDI	3300	-317.5
446	VDDI	3344	-317.5
447	VDDI	3388	-317.5
448	VDDI	3432	-317.5
449	VDDI	3476	-317.5
450	VDDI	3520	-317.5
451	VDDI	3564	-317.5
452	VDDI	3608	-317.5
453	VDDI	3652	-317.5
454	VDDI	3696	-317.5
455	VDDI	3740	-317.5
456	HS_LDO	3784	-317.5
457	HS_LDO	3828	-317.5
458	HS_LDO	3872	-317.5
459	HS_LDO	3916	-317.5
460	HS_LDO	3960	-317.5
461	HS_VSS	4004	-317.5
462	HS_VSS	4048	-317.5
463	HS_VSS	4092	-317.5
464	HS_VSS	4136	-317.5
465	HS_VSS	4180	-317.5
466	HS_VSS	4224	-317.5
467	DATA2_P	4268	-317.5
468	DATA2_P	4312	-317.5
469	DATA2_P	4356	-317.5
470	DATA2_P	4400	-317.5
471	HS_VSS	4444	-317.5
472	HS_VSS	4488	-317.5
473	DATA2_N	4532	-317.5
474	DATA2_N	4576	-317.5
475	DATA2_N	4620	-317.5
476	DATA2_N	4664	-317.5
477	HS_VSS	4708	-317.5
478	HS_VSS	4752	-317.5
479	DATA1_P	4796	-317.5
480	DATA1_P	4840	-317.5

No.	Text Name	X-axis	Y-axis
481	DATA1_P	4884	-317.5
482	DATA1_P	4928	-317.5
483	HS_VSS	4972	-317.5
484	HS_VSS	5016	-317.5
485	DATA1_N	5060	-317.5
486	DATA1_N	5104	-317.5
487	DATA1_N	5148	-317.5
488	DATA1_N	5192	-317.5
489	HS_VSS	5236	-317.5
490	HS_VSS	5280	-317.5
491	CLOCK_P	5324	-317.5
492	CLOCK_P	5368	-317.5
493	CLOCK_P	5412	-317.5
494	CLOCK_P	5456	-317.5
495	HS_VSS	5500	-317.5
496	HS_VSS	5544	-317.5
497	CLOCK_N	5588	-317.5
498	CLOCK_N	5632	-317.5
499	CLOCK_N	5676	-317.5
500	CLOCK_N	5720	-317.5
501	HS_VSS	5764	-317.5
502	HS_VSS	5808	-317.5
503	DATA0_P	5852	-317.5
504	DATA0_P	5896	-317.5
505	DATA0_P	5940	-317.5
506	DATA0_P	5984	-317.5
507	HS_VSS	6028	-317.5
508	HS_VSS	6072	-317.5
509	DATA0_N	6116	-317.5
510	DATA0_N	6160	-317.5
511	DATA0_N	6204	-317.5
512	DATA0_N	6248	-317.5
513	HS_VSS	6292	-317.5
514	HS_VSS	6336	-317.5
515	DATA3_P	6380	-317.5
516	DATA3_P	6424	-317.5
517	DATA3_P	6468	-317.5
518	DATA3_P	6512	-317.5
519	HS_VSS	6556	-317.5
520	HS_VSS	6600	-317.5
521	DATA3_N	6644	-317.5
522	DATA3_N	6688	-317.5
523	DATA3_N	6732	-317.5
524	DATA3_N	6776	-317.5
525	HS_VSS	6820	-317.5
526	HS_VSS	6864	-317.5
527	HS_LDO	6908	-317.5
528	HS_LDO	6952	-317.5
529	HS_LDO	6996	-317.5
530	HS_LDO	7040	-317.5
531	HS_LDO	7084	-317.5
532	HS_LDO	7128	-317.5
533	HS_LDO	7172	-317.5
534	HS_LDO	7216	-317.5
535	VSS	7260	-317.5
536	VSS	7304	-317.5
537	VSS	7348	-317.5
538	VSS	7392	-317.5
539	VSS	7436	-317.5
540	VSS	7480	-317.5

No.	Text Name	X-axis	Y-axis
541	VSS	7524	-317.5
542	VSS	7568	-317.5
543	VSS	7612	-317.5
544	VSS	7656	-317.5
545	VSS	7700	-317.5
546	VSS	7744	-317.5
547	VSS	7788	-317.5
548	VDDAM	7832	-317.5
549	VDDAM	7876	-317.5
550	VDDAM	7920	-317.5
551	VDDAM	7964	-317.5
552	VDDAM	8008	-317.5
553	VDDAM	8052	-317.5
554	VDDI	8096	-317.5
555	VDDI	8140	-317.5
556	VDDI	8184	-317.5
557	VDD	8228	-317.5
558	VDD	8272	-317.5
559	VDD	8316	-317.5
560	VDD	8360	-317.5
561	VDD	8404	-317.5
562	VDD	8448	-317.5
563	VDD	8492	-317.5
564	VDD	8536	-317.5
565	AVDD	8580	-317.5
566	AVDD	8624	-317.5
567	AVDD	8668	-317.5
568	AVDD	8712	-317.5
569	AVDD	8756	-317.5
570	AVDD	8800	-317.5
571	AVEE	8844	-317.5
572	AVEE	8888	-317.5
573	AVEE	8932	-317.5
574	AVEE	8976	-317.5
575	AVEE	9020	-317.5
576	AVEE	9064	-317.5
577	AVSS	9108	-317.5
578	AVSS	9152	-317.5
579	AVSS	9196	-317.5
580	AVSS	9240	-317.5
581	AVSS	9284	-317.5
582	AVSS	9328	-317.5
583	AVSS	9372	-317.5
584	CVSS_R	9416	-317.5
585	CVSS_R	9460	-317.5
586	CVSS_R	9504	-317.5
587	CVSS_R	9548	-317.5
588	CVSS_R	9592	-317.5
589	CVSS_R	9636	-317.5
590	CVSS_R	9680	-317.5
591	CVSS_R	9724	-317.5
592	VGL	9768	-317.5
593	VGL	9812	-317.5
594	VGL	9856	-317.5
595	VGL	9900	-317.5
596	VGL	9944	-317.5
597	VGL	9988	-317.5
598	VGL	10032	-317.5
599	VGL	10076	-317.5
600	C31P	10120	-317.5

No.	Text Name	X-axis	Y-axis
601	C31P	10164	-317.5
602	C31P	10208	-317.5
603	C31P	10252	-317.5
604	C31P	10296	-317.5
605	C31M	10340	-317.5
606	C31M	10384	-317.5
607	C31M	10428	-317.5
608	C31M	10472	-317.5
609	C31M	10516	-317.5
610	C31M	10560	-317.5
611	C31M	10604	-317.5
612	VDD_TP	10648	-317.5
613	VDD_TP	10692	-317.5
614	VDD_TP	10736	-317.5
615	VDD_TP	10780	-317.5
616	VDD_TP	10824	-317.5
617	VSS	10868	-317.5
618	VSS	10912	-317.5
619	VSS	10956	-317.5
620	VSS	11000	-317.5
621	VSS	11044	-317.5
622	VSS	11088	-317.5
623	AVSS	11132	-317.5
624	AVSS	11176	-317.5
625	AVSS	11220	-317.5
626	AVSS	11264	-317.5
627	AVSS	11308	-317.5
628	AVSS	11352	-317.5
629	AVSS	11396	-317.5
630	AVSS	11440	-317.5
631	AVSS	11484	-317.5
632	AVSS	11528	-317.5
633	AVSS	11572	-317.5
634	AVSS	11616	-317.5
635	AVSS	11660	-317.5
636	AVSS	11704	-317.5
637	AVSS	11748	-317.5
638	AVSS	11792	-317.5
639	AVSS	11836	-317.5
640	AVSS	11880	-317.5
641	AVSS	11924	-317.5
642	AVSS	11968	-317.5
643	TPLDO_OUT_R	12012	-317.5
644	TPLDO_OUT_R	12056	-317.5
645	TPLDO_OUT_R	12100	-317.5
646	TPLDO_OUT_R	12144	-317.5
647	TPLDO_OUT_R	12188	-317.5
648	TPLDO_OUT_R	12232	-317.5
649	TPLDO_OUT_R	12276	-317.5
650	TPLDO_OUT_R	12320	-317.5
651	TPLDO_OUT_R	12364	-317.5
652	TPLDO_OUT_R	12408	-317.5
653	TPLDO_OUT_R	12452	-317.5
654	TPLDO_OUT_R	12496	-317.5
655	TPLDO_OUT_R	12540	-317.5
656	TPLDO_OUT_R	12584	-317.5
657	TPLDO_OUT_R	12628	-317.5
658	TPLDO_OUT_R	12672	-317.5
659	TPLDO_OUT_R	12716	-317.5
660	TPLDO_OUT_R	12760	-317.5

No.	Text Name	X-axis	Y-axis
661	TP_TEST_R[3]	12804	-317.5
662	TP_TEST_R[2]	12848	-317.5
663	VCOM_OPT	12892	-317.5
664	VCOM_OPT	12936	-317.5
665	VCOM_OPT	12980	-317.5
666	VCOM_OPT	13024	-317.5
667	VCOM_OPT	13068	-317.5
668	TPLDO_OUT_R	13112	-317.5
669	TPLDO_OUT_R	13156	-317.5
670	TPLDO_OUT_R	13200	-317.5
671	TPLDO_OUT_R	13244	-317.5
672	TPLDO_OUT_R	13288	-317.5
673	TPLDO_OUT_R	13332	-317.5
674	TPLDO_OUT_R	13376	-317.5
675	TPLDO_OUT_R	13420	-317.5
676	TPLDO_OUT_R	13464	-317.5
677	TPLDO_OUT_R	13508	-317.5
678	AVDD	13552	-317.5
679	AVDD	13596	-317.5
680	AVDD	13640	-317.5
681	AVDD	13684	-317.5
682	AVDD	13728	-317.5
683	AVDD	13772	-317.5
684	AVDD	13816	-317.5
685	AVDD	13860	-317.5
686	AVEE	13904	-317.5
687	AVEE	13948	-317.5
688	AVEE	13992	-317.5
689	AVEE	14036	-317.5
690	AVEE	14080	-317.5
691	AVEE	14124	-317.5
692	VCOM_R	14168	-317.5
693	VCOM_R	14212	-317.5
694	VCOM_R	14256	-317.5
695	AVSST_R	14300	-317.5
696	AVSST_R	14344	-317.5
697	AVSST_R	14388	-317.5
698	AVSST_R	14432	-317.5
699	AVSST_R	14476	-317.5
700	AVSST_R	14520	-317.5
701	AVSST_R	14564	-317.5
702	AVSST_R	14608	-317.5
703	AVSST_R	14652	-317.5
704	VGHO_R	14696	-317.5
705	VGHO_R	14740	-317.5
706	VGHO_R	14784	-317.5
707	VGHO_R	14828	-317.5
708	VGLO_R	14872	-317.5
709	VGLO_R	14916	-317.5
710	VGLO_R	14960	-317.5
711	VGLO_R	15004	-317.5
712	COGTEST34	15048	-317.5
713	COGTEST34	15092	-317.5
714	CGOUTR[1]	15136	-317.5
715	CGOUTR[2]	15180	-317.5
716	CGOUTR[3]	15224	-317.5
717	CGOUTR[4]	15268	-317.5
718	CGOUTR[5]	15312	-317.5
719	CGOUTR[6]	15356	-317.5
720	CGOUTR[7]	15400	-317.5

No.	Text Name	X-axis	Y-axis
721	CGOUTR[8]	15444	-317.5
722	CGOUTR[9]	15488	-317.5
723	CGOUTR[10]	15532	-317.5
724	CGOUTR[11]	15576	-317.5
725	CGOUTR[12]	15620	-317.5
726	CGOUTR[13]	15664	-317.5
727	CGOUTR[14]	15708	-317.5
728	CGOUTR[15]	15752	-317.5
729	CGOUTR[16]	15796	-317.5
730	CGOUTR[17]	15840	-317.5
731	CGOUTR[18]	15884	-317.5
732	CGOUTR[19]	15928	-317.5
733	CGOUTR[20]	15972	-317.5
734	CGOUTR[21]	16016	-317.5
735	CGOUTR[22]	16060	-317.5
736	CGOUTR[23]	16104	-317.5
737	CGOUTR[24]	16148	-317.5
738	TP_TEST_R[1]	16192	-317.5
739	TP_TEST_R[0]	16236	-317.5
740	DUMMY[2]	16119	225
741	DUMMY[2]	16101	340
742	GRID[4]	16083	225
743	GRID[4]	16065	340
744	GRID[4]	16047	225
745	GRID[4]	16029	340
746	S[1081]	16011	225
747	RX[648]	15993	340
748	S[1080]	15975	225
749	S[1079]	15957	340
750	RX[647]	15939	225
751	S[1078]	15921	340
752	S[1077]	15903	225
753	RX[646]	15885	340
754	S[1076]	15867	225
755	S[1075]	15849	340
756	RX[645]	15831	225
757	S[1074]	15813	340
758	S[1073]	15795	225
759	RX[644]	15777	340
760	S[1072]	15759	225
761	S[1071]	15741	340
762	RX[643]	15723	225
763	RX[642]	15705	340
764	S[1070]	15687	225
765	S[1069]	15669	340
766	RX[641]	15651	225
767	S[1068]	15633	340
768	S[1067]	15615	225
769	RX[640]	15597	340
770	S[1066]	15579	225
771	S[1065]	15561	340
772	RX[639]	15543	225
773	S[1064]	15525	340
774	S[1063]	15507	225
775	RX[638]	15489	340
776	S[1062]	15471	225
777	S[1061]	15453	340
778	RX[637]	15435	225
779	RX[636]	15417	340
780	S[1060]	15399	225
781	S[1059]	15381	340
782	RX[635]	15363	225
783	S[1058]	15345	340
784	S[1057]	15327	225
785	RX[634]	15309	340
786	S[1056]	15291	225
787	S[1055]	15273	340
788	RX[633]	15255	225
789	S[1054]	15237	340
790	S[1053]	15219	225
791	RX[632]	15201	340
792	S[1052]	15183	225
793	S[1051]	15165	340
794	RX[631]	15147	225
795	RX[630]	15129	340
796	S[1050]	15111	225
797	S[1049]	15093	340
798	RX[629]	15075	225
799	S[1048]	15057	340
800	S[1047]	15039	225
801	RX[628]	15021	340
802	S[1046]	15003	225
803	S[1045]	14985	340
804	RX[627]	14967	225
805	S[1044]	14949	340
806	S[1043]	14931	225
807	RX[626]	14913	340
808	S[1042]	14895	225
809	S[1041]	14877	340
810	RX[625]	14859	225
811	RX[624]	14841	340
812	S[1040]	14823	225
813	S[1039]	14805	340
814	RX[623]	14787	225
815	S[1038]	14769	340
816	S[1037]	14751	225
817	RX[622]	14733	340
818	S[1036]	14715	225
819	S[1035]	14697	340
820	RX[621]	14679	225
821	S[1034]	14661	340
822	S[1033]	14643	225
823	RX[620]	14625	340
824	S[1032]	14607	225
825	S[1031]	14589	340
826	RX[619]	14571	225
827	RX[618]	14553	340
828	S[1030]	14535	225
829	S[1029]	14517	340
830	RX[617]	14499	225
831	S[1028]	14481	340
832	S[1027]	14463	225
833	RX[616]	14445	340
834	S[1026]	14427	225
835	S[1025]	14409	340
836	RX[615]	14391	225
837	S[1024]	14373	340
838	S[1023]	14355	225
839	RX[614]	14337	340
840	S[1022]	14319	225
841	S[1021]	14301	340
842	RX[613]	14283	225
843	RX[612]	14265	340
844	S[1020]	14247	225
845	S[1019]	14229	340
846	RX[611]	14211	225
847	S[1018]	14193	340
848	S[1017]	14175	225
849	RX[610]	14157	340
850	S[1016]	14139	225
851	S[1015]	14121	340
852	RX[609]	14103	225
853	S[1014]	14085	340
854	S[1013]	14067	225
855	RX[608]	14049	340
856	S[1012]	14031	225
857	S[1011]	14013	340
858	RX[607]	13995	225
859	RX[606]	13977	340
860	S[1010]	13959	225
861	S[1009]	13941	340
862	RX[605]	13923	225
863	S[1008]	13905	340
864	S[1007]	13887	225
865	RX[604]	13869	340
866	S[1006]	13851	225
867	S[1005]	13833	340
868	RX[603]	13815	225
869	S[1004]	13797	340
870	S[1003]	13779	225
871	RX[602]	13761	340
872	S[1002]	13743	225
873	S[1001]	13725	340
874	RX[601]	13707	225
875	RX[600]	13689	340
876	S[1000]	13671	225
877	S[999]	13653	340
878	RX[599]	13635	225
879	S[998]	13617	340
880	S[997]	13599	225
881	RX[598]	13581	340
882	S[996]	13563	225
883	S[995]	13545	340
884	RX[597]	13527	225
885	S[994]	13509	340
886	S[993]	13491	225
887	RX[596]	13473	340
888	S[992]	13455	225
889	S[991]	13437	340
890	RX[595]	13419	225
891	RX[594]	13401	340
892	S[990]	13383	225
893	S[989]	13365	340
894	RX[593]	13347	225
895	S[988]	13329	340
896	S[987]	13311	225
897	RX[592]	13293	340
898	S[986]	13275	225
899	S[985]	13257	340
900	RX[591]	13239	225
901	S[984]	13221	340
902	S[983]	13203	225
903	RX[590]	13185	340
904	S[982]	13167	225
905	S[981]	13149	340
906	RX[589]	13131	225
907	RX[588]	13113	340
908	S[980]	13095	225
909	S[979]	13077	340
910	RX[587]	13059	225
911	S[978]	13041	340
912	S[977]	13023	225
913	RX[586]	13005	340
914	S[976]	12987	225
915	S[975]	12969	340
916	RX[585]	12951	225
917	S[974]	12933	340
918	S[973]	12915	225
919	RX[584]	12897	340
920	S[972]	12879	225
921	S[971]	12861	340
922	RX[583]	12843	225
923	RX[582]	12825	340
924	S[970]	12807	225
925	S[969]	12789	340
926	RX[581]	12771	225
927	S[968]	12753	340
928	S[967]	12735	225
929	RX[580]	12717	340
930	S[966]	12699	225
931	S[965]	12681	340
932	RX[579]	12663	225
933	S[964]	12645	340
934	S[963]	12627	225
935	RX[578]	12609	340
936	S[962]	12591	225
937	S[961]	12573	340
938	RX[577]	12555	225
939	RX[576]	12537	340
940	S[960]	12519	225
941	S[959]	12501	340
942	RX[575]	12483	225
943	S[958]	12465	340
944	S[957]	12447	225
945	RX[574]	12429	340
946	S[956]	12411	225
947	S[955]	12393	340
948	RX[573]	12375	225
949	S[954]	12357	340
950	S[953]	12339	225
951	RX[572]	12321	340
952	S[952]	12303	225
953	S[951]	12285	340
954	RX[571]	12267	225
955	RX[570]	12249	340
956	S[950]	12231	225
957	S[949]	12213	340
958	RX[569]	12195	225
959	S[948]	12177	340
960	S[947]	12159	225

No.	Text Name	X-axis	Y-axis
961	RX[568]	12141	340
962	S[946]	12123	225
963	S[945]	12105	340
964	RX[567]	12087	225
965	S[944]	12069	340
966	S[943]	12051	225
967	RX[566]	12033	340
968	S[942]	12015	225
969	S[941]	11997	340
970	RX[565]	11979	225
971	RX[564]	11961	340
972	S[940]	11943	225
973	S[939]	11925	340
974	RX[563]	11907	225
975	S[938]	11889	340
976	S[937]	11871	225
977	RX[562]	11853	340
978	S[936]	11835	225
979	S[935]	11817	340
980	RX[561]	11799	225
981	S[934]	11781	340
982	S[933]	11763	225
983	RX[560]	11745	340
984	S[932]	11727	225
985	S[931]	11709	340
986	RX[559]	11691	225
987	RX[558]	11673	340
988	S[930]	11655	225
989	S[929]	11637	340
990	RX[557]	11619	225
991	S[928]	11601	340
992	S[927]	11583	225
993	RX[556]	11565	340
994	S[926]	11547	225
995	S[925]	11529	340
996	RX[555]	11511	225
997	S[924]	11493	340
998	S[923]	11475	225
999	RX[554]	11457	340
1000	S[922]	11439	225
1001	S[921]	11421	340
1002	RX[553]	11403	225
1003	RX[552]	11385	340
1004	S[920]	11367	225
1005	S[919]	11349	340
1006	RX[551]	11331	225
1007	S[918]	11313	340
1008	S[917]	11295	225
1009	RX[550]	11277	340
1010	S[916]	11259	225
1011	S[915]	11241	340
1012	RX[549]	11223	225
1013	S[914]	11205	340
1014	S[913]	11187	225
1015	RX[548]	11169	340
1016	S[912]	11151	225
1017	S[911]	11133	340
1018	RX[547]	11115	225
1019	RX[546]	11097	340
1020	S[910]	11079	225

No.	Text Name	X-axis	Y-axis
1021	S[909]	11061	340
1022	RX[545]	11043	225
1023	S[908]	11025	340
1024	S[907]	11007	225
1025	RX[544]	10989	340
1026	S[906]	10971	225
1027	S[905]	10953	340
1028	RX[543]	10935	225
1029	S[904]	10917	340
1030	S[903]	10899	225
1031	RX[542]	10881	340
1032	S[902]	10863	225
1033	S[901]	10845	340
1034	RX[541]	10827	225
1035	RX[540]	10809	340
1036	S[900]	10791	225
1037	S[899]	10773	340
1038	RX[539]	10755	225
1039	S[898]	10737	340
1040	S[897]	10719	225
1041	RX[538]	10701	340
1042	S[896]	10683	225
1043	S[895]	10665	340
1044	RX[537]	10647	225
1045	S[894]	10629	340
1046	S[893]	10611	225
1047	RX[536]	10593	340
1048	S[892]	10575	225
1049	S[891]	10557	340
1050	RX[535]	10539	225
1051	RX[534]	10521	340
1052	S[890]	10503	225
1053	S[889]	10485	340
1054	RX[533]	10467	225
1055	S[888]	10449	340
1056	S[887]	10431	225
1057	RX[532]	10413	340
1058	S[886]	10395	225
1059	S[885]	10377	340
1060	RX[531]	10359	225
1061	S[884]	10341	340
1062	S[883]	10323	225
1063	RX[530]	10305	340
1064	S[882]	10287	225
1065	S[881]	10269	340
1066	RX[529]	10251	225
1067	RX[528]	10233	340
1068	S[880]	10215	225
1069	S[879]	10197	340
1070	RX[527]	10179	225
1071	S[878]	10161	340
1072	S[877]	10143	225
1073	RX[526]	10125	340
1074	S[876]	10107	225
1075	S[875]	10089	340
1076	RX[525]	10071	225
1077	S[874]	10053	340
1078	S[873]	10035	225
1079	RX[524]	10017	340
1080	S[872]	9999	225

No.	Text Name	X-axis	Y-axis
1081	S[871]	9981	340
1082	RX[523]	9963	225
1083	RX[522]	9945	340
1084	S[870]	9927	225
1085	S[869]	9909	340
1086	RX[521]	9891	225
1087	S[868]	9873	340
1088	S[867]	9855	225
1089	RX[520]	9837	340
1090	S[866]	9819	225
1091	S[865]	9801	340
1092	RX[519]	9783	225
1093	S[864]	9765	340
1094	S[863]	9747	225
1095	RX[518]	9729	340
1096	S[862]	9711	225
1097	S[861]	9693	340
1098	RX[517]	9675	225
1099	RX[516]	9657	340
1100	S[860]	9639	225
1101	S[859]	9621	340
1102	RX[515]	9603	225
1103	S[858]	9585	340
1104	S[857]	9567	225
1105	RX[514]	9549	340
1106	S[856]	9531	225
1107	S[855]	9513	340
1108	RX[513]	9495	225
1109	S[854]	9477	340
1110	S[853]	9459	225
1111	RX[512]	9441	340
1112	S[852]	9423	225
1113	S[851]	9405	340
1114	RX[511]	9387	225
1115	RX[510]	9369	340
1116	S[850]	9351	225
1117	S[849]	9333	340
1118	RX[509]	9315	225
1119	S[848]	9297	340
1120	S[847]	9279	225
1121	RX[508]	9261	340
1122	S[846]	9243	225
1123	S[845]	9225	340
1124	RX[507]	9207	225
1125	S[844]	9189	340
1126	S[843]	9171	225
1127	RX[506]	9153	340
1128	S[842]	9135	225
1129	S[841]	9117	340
1130	RX[505]	9099	225
1131	RX[504]	9081	340
1132	S[840]	9063	225
1133	S[839]	9045	340
1134	RX[503]	9027	225
1135	S[838]	9009	340
1136	S[837]	8991	225
1137	RX[502]	8973	340
1138	S[836]	8955	225
1139	S[835]	8937	340
1140	RX[501]	8919	225

No.	Text Name	X-axis	Y-axis
1141	S[834]	8901	340
1142	S[833]	8883	225
1143	RX[500]	8865	340
1144	S[832]	8847	225
1145	S[831]	8829	340
1146	RX[499]	8811	225
1147	RX[498]	8793	340
1148	S[830]	8775	225
1149	S[829]	8757	340
1150	RX[497]	8739	225
1151	S[828]	8721	340
1152	S[827]	8703	225
1153	RX[496]	8685	340
1154	S[826]	8667	225
1155	S[825]	8649	340
1156	RX[495]	8631	225
1157	S[824]	8613	340
1158	S[823]	8595	225
1159	RX[494]	8577	340
1160	S[822]	8559	225
1161	S[821]	8541	340
1162	RX[493]	8523	225
1163	RX[492]	8505	340
1164	S[820]	8487	225
1165	S[819]	8469	340
1166	RX[491]	8451	225
1167	S[818]	8433	340
1168	S[817]	8415	225
1169	RX[490]	8397	340
1170	S[816]	8379	225
1171	S[815]	8361	340
1172	RX[489]	8343	225
1173	S[814]	8325	340
1174	S[813]	8307	225
1175	RX[488]	8289	340
1176	S[812]	8271	225
1177	S[811]	8253	340
1178	RX[487]	8235	225
1179	RX[486]	8217	340
1180	S[810]	8199	225
1181	S[809]	8181	340
1182	RX[485]	8163	225
1183	S[808]	8145	340
1184	S[807]	8127	225
1185	RX[484]	8109	340
1186	S[806]	8091	225
1187	S[805]	8073	340
1188	RX[483]	8055	225
1189	S[804]	8037	340
1190	S[803]	8019	225
1191	RX[482]	8001	340
1192	S[802]	7983	225
1193	S[801]	7965	340
1194	RX[481]	7947	225
1195	RX[480]	7929	340
1196	S[800]	7911	225
1197	S[799]	7893	340
1198	RX[479]	7875	225
1199	S[798]	7857	340
1200	S[797]	7839	225

No.	Text Name	X-axis	Y-axis
1201	RX[478]	7821	340
1202	S[796]	7803	225
1203	S[795]	7785	340
1204	RX[477]	7767	225
1205	S[794]	7749	340
1206	S[793]	7731	225
1207	RX[476]	7713	340
1208	S[792]	7695	225
1209	S[791]	7677	340
1210	RX[475]	7659	225
1211	RX[474]	7641	340
1212	S[790]	7623	225
1213	S[789]	7605	340
1214	RX[473]	7587	225
1215	S[788]	7569	340
1216	S[787]	7551	225
1217	RX[472]	7533	340
1218	S[786]	7515	225
1219	S[785]	7497	340
1220	RX[471]	7479	225
1221	S[784]	7461	340
1222	S[783]	7443	225
1223	RX[470]	7425	340
1224	S[782]	7407	225
1225	S[781]	7389	340
1226	RX[469]	7371	225
1227	RX[468]	7353	340
1228	S[780]	7335	225
1229	S[779]	7317	340
1230	RX[467]	7299	225
1231	S[778]	7281	340
1232	S[777]	7263	225
1233	RX[466]	7245	340
1234	S[776]	7227	225
1235	S[775]	7209	340
1236	RX[465]	7191	225
1237	S[774]	7173	340
1238	S[773]	7155	225
1239	RX[464]	7137	340
1240	S[772]	7119	225
1241	S[771]	7101	340
1242	RX[463]	7083	225
1243	RX[462]	7065	340
1244	S[770]	7047	225
1245	S[769]	7029	340
1246	RX[461]	7011	225
1247	S[768]	6993	340
1248	S[767]	6975	225
1249	RX[460]	6957	340
1250	S[766]	6939	225
1251	S[765]	6921	340
1252	RX[459]	6903	225
1253	S[764]	6885	340
1254	S[763]	6867	225
1255	RX[458]	6849	340
1256	S[762]	6831	225
1257	S[761]	6813	340
1258	RX[457]	6795	225
1259	RX[456]	6777	340
1260	S[760]	6759	225

No.	Text Name	X-axis	Y-axis
1261	S[759]	6741	340
1262	RX[455]	6723	225
1263	S[758]	6705	340
1264	S[757]	6687	225
1265	RX[454]	6669	340
1266	S[756]	6651	225
1267	S[755]	6633	340
1268	RX[453]	6615	225
1269	S[754]	6597	340
1270	S[753]	6579	225
1271	RX[452]	6561	340
1272	S[752]	6543	225
1273	S[751]	6525	340
1274	RX[451]	6507	225
1275	RX[450]	6489	340
1276	S[750]	6471	225
1277	S[749]	6453	340
1278	RX[449]	6435	225
1279	S[748]	6417	340
1280	S[747]	6399	225
1281	RX[448]	6381	340
1282	S[746]	6363	225
1283	S[745]	6345	340
1284	RX[447]	6327	225
1285	S[744]	6309	340
1286	S[743]	6291	225
1287	RX[446]	6273	340
1288	S[742]	6255	225
1289	S[741]	6237	340
1290	RX[445]	6219	225
1291	RX[444]	6201	340
1292	S[740]	6183	225
1293	S[739]	6165	340
1294	RX[443]	6147	225
1295	S[738]	6129	340
1296	S[737]	6111	225
1297	RX[442]	6093	340
1298	S[736]	6075	225
1299	S[735]	6057	340
1300	RX[441]	6039	225
1301	S[734]	6021	340
1302	S[733]	6003	225
1303	RX[440]	5985	340
1304	S[732]	5967	225
1305	S[731]	5949	340
1306	RX[439]	5931	225
1307	RX[438]	5913	340
1308	S[730]	5895	225
1309	S[729]	5877	340
1310	RX[437]	5859	225
1311	S[728]	5841	340
1312	S[727]	5823	225
1313	RX[436]	5805	340
1314	S[726]	5787	225
1315	S[725]	5769	340
1316	RX[435]	5751	225
1317	S[724]	5733	340
1318	S[723]	5715	225
1319	RX[434]	5697	340
1320	S[722]	5679	225

No.	Text Name	X-axis	Y-axis
1321	S[721]	5661	340
1322	RX[433]	5643	225
1323	RX[432]	5625	340
1324	S[720]	5607	225
1325	S[719]	5589	340
1326	RX[431]	5571	225
1327	S[718]	5553	340
1328	S[717]	5535	225
1329	RX[430]	5517	340
1330	S[716]	5499	225
1331	S[715]	5481	340
1332	RX[429]	5463	225
1333	S[714]	5445	340
1334	S[713]	5427	225
1335	RX[428]	5409	340
1336	S[712]	5391	225
1337	S[711]	5373	340
1338	RX[427]	5355	225
1339	RX[426]	5337	340
1340	S[710]	5319	225
1341	S[709]	5301	340
1342	RX[425]	5283	225
1343	S[708]	5265	340
1344	S[707]	5247	225
1345	RX[424]	5229	340
1346	S[706]	5211	225
1347	S[705]	5193	340
1348	RX[423]	5175	225
1349	S[704]	5157	340
1350	S[703]	5139	225
1351	RX[422]	5121	340
1352	S[702]	5103	225
1353	S[701]	5085	340
1354	RX[421]	5067	225
1355	RX[420]	5049	340
1356	S[700]	5031	225
1357	S[699]	5013	340
1358	RX[419]	4995	225
1359	S[698]	4977	340
1360	S[697]	4959	225
1361	RX[418]	4941	340
1362	S[696]	4923	225
1363	S[695]	4905	340
1364	RX[417]	4887	225
1365	S[694]	4869	340
1366	S[693]	4851	225
1367	RX[416]	4833	340
1368	S[692]	4815	225
1369	S[691]	4797	340
1370	RX[415]	4779	225
1371	RX[414]	4761	340
1372	S[690]	4743	225
1373	S[689]	4725	340
1374	RX[413]	4707	225
1375	S[688]	4689	340
1376	S[687]	4671	225
1377	RX[412]	4653	340
1378	S[686]	4635	225
1379	S[685]	4617	340
1380	RX[411]	4599	225

No.	Text Name	X-axis	Y-axis
1381	S[684]	4581	340
1382	S[683]	4563	225
1383	RX[410]	4545	340
1384	S[682]	4527	225
1385	S[681]	4509	340
1386	RX[409]	4491	225
1387	RX[408]	4473	340
1388	S[680]	4455	225
1389	S[679]	4437	340
1390	RX[407]	4419	225
1391	S[678]	4401	340
1392	S[677]	4383	225
1393	RX[406]	4365	340
1394	S[676]	4347	225
1395	S[675]	4329	340
1396	RX[405]	4311	225
1397	S[674]	4293	340
1398	S[673]	4275	225
1399	RX[404]	4257	340
1400	S[672]	4239	225
1401	S[671]	4221	340
1402	RX[403]	4203	225
1403	RX[402]	4185	340
1404	S[670]	4167	225
1405	S[669]	4149	340
1406	RX[401]	4131	225
1407	S[668]	4113	340
1408	S[667]	4095	225
1409	RX[400]	4077	340
1410	S[666]	4059	225
1411	S[665]	4041	340
1412	RX[399]	4023	225
1413	S[664]	4005	340
1414	S[663]	3987	225
1415	RX[398]	3969	340
1416	S[662]	3951	225
1417	S[661]	3933	340
1418	RX[397]	3915	225
1419	RX[396]	3897	340
1420	S[660]	3879	225
1421	S[659]	3861	340
1422	RX[395]	3843	225
1423	S[658]	3825	340
1424	S[657]	3807	225
1425	RX[394]	3789	340
1426	S[656]	3771	225
1427	S[655]	3753	340
1428	RX[393]	3735	225
1429	S[654]	3717	340
1430	S[653]	3699	225
1431	RX[392]	3681	340
1432	S[652]	3663	225
1433	S[651]	3645	340
1434	RX[391]	3627	225
1435	RX[390]	3609	340
1436	S[650]	3591	225
1437	S[649]	3573	340
1438	RX[389]	3555	225
1439	S[648]	3537	340
1440	S[647]	3519	225

No.	Text Name	X-axis	Y-axis
1441	RX[388]	3501	340
1442	S[646]	3483	225
1443	S[645]	3465	340
1444	RX[387]	3447	225
1445	S[644]	3429	340
1446	S[643]	3411	225
1447	RX[386]	3393	340
1448	S[642]	3375	225
1449	S[641]	3357	340
1450	RX[385]	3339	225
1451	RX[384]	3321	340
1452	S[640]	3303	225
1453	S[639]	3285	340
1454	RX[383]	3267	225
1455	S[638]	3249	340
1456	S[637]	3231	225
1457	RX[382]	3213	340
1458	S[636]	3195	225
1459	S[635]	3177	340
1460	RX[381]	3159	225
1461	S[634]	3141	340
1462	S[633]	3123	225
1463	RX[380]	3105	340
1464	S[632]	3087	225
1465	S[631]	3069	340
1466	RX[379]	3051	225
1467	RX[378]	3033	340
1468	S[630]	3015	225
1469	S[629]	2997	340
1470	RX[377]	2979	225
1471	S[628]	2961	340
1472	S[627]	2943	225
1473	RX[376]	2925	340
1474	S[626]	2907	225
1475	S[625]	2889	340
1476	RX[375]	2871	225
1477	S[624]	2853	340
1478	S[623]	2835	225
1479	RX[374]	2817	340
1480	S[622]	2799	225
1481	S[621]	2781	340
1482	RX[373]	2763	225
1483	RX[372]	2745	340
1484	S[620]	2727	225
1485	S[619]	2709	340
1486	RX[371]	2691	225
1487	S[618]	2673	340
1488	S[617]	2655	225
1489	RX[370]	2637	340
1490	S[616]	2619	225
1491	S[615]	2601	340
1492	RX[369]	2583	225
1493	S[614]	2565	340
1494	S[613]	2547	225
1495	RX[368]	2529	340
1496	S[612]	2511	225
1497	S[611]	2493	340
1498	RX[367]	2475	225
1499	RX[366]	2457	340
1500	S[610]	2439	225

No.	Text Name	X-axis	Y-axis
1501	S[609]	2421	340
1502	RX[365]	2403	225
1503	S[608]	2385	340
1504	S[607]	2367	225
1505	RX[364]	2349	340
1506	S[606]	2331	225
1507	S[605]	2313	340
1508	RX[363]	2295	225
1509	S[604]	2277	340
1510	S[603]	2259	225
1511	RX[362]	2241	340
1512	S[602]	2223	225
1513	S[601]	2205	340
1514	RX[361]	2187	225
1515	RX[360]	2169	340
1516	S[600]	2151	225
1517	S[599]	2133	340
1518	RX[359]	2115	225
1519	S[598]	2097	340
1520	S[597]	2079	225
1521	RX[358]	2061	340
1522	S[596]	2043	225
1523	S[595]	2025	340
1524	RX[357]	2007	225
1525	S[594]	1989	340
1526	S[593]	1971	225
1527	RX[356]	1953	340
1528	S[592]	1935	225
1529	S[591]	1917	340
1530	RX[355]	1899	225
1531	RX[354]	1881	340
1532	S[590]	1863	225
1533	S[589]	1845	340
1534	RX[353]	1827	225
1535	S[588]	1809	340
1536	S[587]	1791	225
1537	RX[352]	1773	340
1538	S[586]	1755	225
1539	S[585]	1737	340
1540	RX[351]	1719	225
1541	S[584]	1701	340
1542	S[583]	1683	225
1543	RX[350]	1665	340
1544	S[582]	1647	225
1545	S[581]	1629	340
1546	RX[349]	1611	225
1547	RX[348]	1593	340
1548	S[580]	1575	225
1549	S[579]	1557	340
1550	RX[347]	1539	225
1551	S[578]	1521	340
1552	S[577]	1503	225
1553	RX[346]	1485	340
1554	S[576]	1467	225
1555	S[575]	1449	340
1556	RX[345]	1431	225
1557	S[574]	1413	340
1558	S[573]	1395	225
1559	RX[344]	1377	340
1560	S[572]	1359	225

No.	Text Name	X-axis	Y-axis
1561	S[571]	1341	340
1562	RX[343]	1323	225
1563	RX[342]	1305	340
1564	S[570]	1287	225
1565	S[569]	1269	340
1566	RX[341]	1251	225
1567	S[568]	1233	340
1568	S[567]	1215	225
1569	RX[340]	1197	340
1570	S[566]	1179	225
1571	S[565]	1161	340
1572	RX[339]	1143	225
1573	S[564]	1125	340
1574	S[563]	1107	225
1575	RX[338]	1089	340
1576	S[562]	1071	225
1577	S[561]	1053	340
1578	RX[337]	1035	225
1579	RX[336]	1017	340
1580	S[560]	999	225
1581	S[559]	981	340
1582	RX[335]	963	225
1583	S[558]	945	340
1584	S[557]	927	225
1585	RX[334]	909	340
1586	S[556]	891	225
1587	S[555]	873	340
1588	RX[333]	855	225
1589	S[554]	837	340
1590	S[553]	819	225
1591	RX[332]	801	340
1592	S[552]	783	225
1593	S[551]	765	340
1594	RX[331]	747	225
1595	RX[330]	729	340
1596	S[550]	711	225
1597	S[549]	693	340
1598	RX[329]	675	225
1599	S[548]	657	340
1600	S[547]	639	225
1601	RX[328]	621	340
1602	S[546]	603	225
1603	S[545]	585	340
1604	RX[327]	567	225
1605	S[544]	549	340
1606	S[543]	531	225
1607	RX[326]	513	340
1608	S[542]	495	225
1609	S[541]	477	340
1610	RX[325]	459	225
1611	GRID[3]	441	340
1612	GRID[3]	423	225
1613	GRID[3]	405	340
1614	GRID[3]	387	225
1615	GRID[3]	369	340
1616	GRID[3]	351	225
1617	DUMMY[1]	333	340
1618	DUMMY[1]	315	225
1619	DUMMY[1]	297	340
1620	DUMMY[1]	279	225

No.	Text Name	X-axis	Y-axis
1621	DUMMY[1]	261	340
1622	DUMMY[1]	243	225
1623	DUMMY[1]	225	340
1624	DUMMY[1]	207	225
1625	DUMMY[1]	189	340
1626	DUMMY[1]	171	225
1627	DUMMY[1]	153	340
1628	DUMMY[1]	135	225
1629	DUMMY[1]	117	340
1630	DUMMY[1]	99	225
1631	DUMMY[1]	81	340
1632	DUMMY[1]	63	225
1633	DUMMY[1]	45	340
1634	DUMMY[1]	27	225
1635	DUMMY[1]	9	340
1636	DUMMY[1]	-9	225
1637	DUMMY[1]	-27	340
1638	DUMMY[1]	-45	225
1639	DUMMY[1]	-63	340
1640	DUMMY[1]	-81	225
1641	DUMMY[1]	-99	340
1642	DUMMY[1]	-117	225
1643	DUMMY[1]	-135	340
1644	DUMMY[1]	-153	225
1645	DUMMY[1]	-171	340
1646	DUMMY[1]	-189	225
1647	DUMMY[1]	-207	340
1648	DUMMY[1]	-225	225
1649	DUMMY[1]	-243	340
1650	DUMMY[1]	-261	225
1651	DUMMY[1]	-279	340
1652	DUMMY[1]	-297	225
1653	DUMMY[1]	-315	340
1654	DUMMY[1]	-333	225
1655	GRID[2]	-351	340
1656	GRID[2]	-369	225
1657	GRID[2]	-387	340
1658	GRID[2]	-405	225
1659	GRID[2]	-423	340
1660	GRID[2]	-441	225
1661	RX[324]	-459	340
1662	S[540]	-477	225
1663	S[539]	-495	340
1664	RX[323]	-513	225
1665	S[538]	-531	340
1666	S[537]	-549	225
1667	RX[322]	-567	340
1668	S[536]	-585	225
1669	S[535]	-603	340
1670	RX[321]	-621	225
1671	S[534]	-639	340
1672	S[533]	-657	225
1673	RX[320]	-675	340
1674	S[532]	-693	225
1675	S[531]	-711	340
1676	RX[319]	-729	225
1677	RX[318]	-747	340
1678	S[530]	-765	225
1679	S[529]	-783	340
1680	RX[317]	-801	225

No.	Text Name	X-axis	Y-axis
1681	S[528]	-819	340
1682	S[527]	-837	225
1683	RX[316]	-855	340
1684	S[526]	-873	225
1685	S[525]	-891	340
1686	RX[315]	-909	225
1687	S[524]	-927	340
1688	S[523]	-945	225
1689	RX[314]	-963	340
1690	S[522]	-981	225
1691	S[521]	-999	340
1692	RX[313]	-1017	225
1693	RX[312]	-1035	340
1694	S[520]	-1053	225
1695	S[519]	-1071	340
1696	RX[311]	-1089	225
1697	S[518]	-1107	340
1698	S[517]	-1125	225
1699	RX[310]	-1143	340
1700	S[516]	-1161	225
1701	S[515]	-1179	340
1702	RX[309]	-1197	225
1703	S[514]	-1215	340
1704	S[513]	-1233	225
1705	RX[308]	-1251	340
1706	S[512]	-1269	225
1707	S[511]	-1287	340
1708	RX[307]	-1305	225
1709	RX[306]	-1323	340
1710	S[510]	-1341	225
1711	S[509]	-1359	340
1712	RX[305]	-1377	225
1713	S[508]	-1395	340
1714	S[507]	-1413	225
1715	RX[304]	-1431	340
1716	S[506]	-1449	225
1717	S[505]	-1467	340
1718	RX[303]	-1485	225
1719	S[504]	-1503	340
1720	S[503]	-1521	225
1721	RX[302]	-1539	340
1722	S[502]	-1557	225
1723	S[501]	-1575	340
1724	RX[301]	-1593	225
1725	RX[300]	-1611	340
1726	S[500]	-1629	225
1727	S[499]	-1647	340
1728	RX[299]	-1665	225
1729	S[498]	-1683	340
1730	S[497]	-1701	225
1731	RX[298]	-1719	340
1732	S[496]	-1737	225
1733	S[495]	-1755	340
1734	RX[297]	-1773	225
1735	S[494]	-1791	340
1736	S[493]	-1809	225
1737	RX[296]	-1827	340
1738	S[492]	-1845	225
1739	S[491]	-1863	340
1740	RX[295]	-1881	225

No.	Text Name	X-axis	Y-axis
1741	RX[294]	-1899	340
1742	S[490]	-1917	225
1743	S[489]	-1935	340
1744	RX[293]	-1953	225
1745	S[488]	-1971	340
1746	S[487]	-1989	225
1747	RX[292]	-2007	340
1748	S[486]	-2025	225
1749	S[485]	-2043	340
1750	RX[291]	-2061	225
1751	S[484]	-2079	340
1752	S[483]	-2097	225
1753	RX[290]	-2115	340
1754	S[482]	-2133	225
1755	S[481]	-2151	340
1756	RX[289]	-2169	225
1757	RX[288]	-2187	340
1758	S[480]	-2205	225
1759	S[479]	-2223	340
1760	RX[287]	-2241	225
1761	S[478]	-2259	340
1762	S[477]	-2277	225
1763	RX[286]	-2295	340
1764	S[476]	-2313	225
1765	S[475]	-2331	340
1766	RX[285]	-2349	225
1767	S[474]	-2367	340
1768	S[473]	-2385	225
1769	RX[284]	-2403	340
1770	S[472]	-2421	225
1771	S[471]	-2439	340
1772	RX[283]	-2457	225
1773	RX[282]	-2475	340
1774	S[470]	-2493	225
1775	S[469]	-2511	340
1776	RX[281]	-2529	225
1777	S[468]	-2547	340
1778	S[467]	-2565	225
1779	RX[280]	-2583	340
1780	S[466]	-2601	225
1781	S[465]	-2619	340
1782	RX[279]	-2637	225
1783	S[464]	-2655	340
1784	S[463]	-2673	225
1785	RX[278]	-2691	340
1786	S[462]	-2709	225
1787	S[461]	-2727	340
1788	RX[277]	-2745	225
1789	RX[276]	-2763	340
1790	S[460]	-2781	225
1791	S[459]	-2799	340
1792	RX[275]	-2817	225
1793	S[458]	-2835	340
1794	S[457]	-2853	225
1795	RX[274]	-2871	340
1796	S[456]	-2889	225
1797	S[455]	-2907	340
1798	RX[273]	-2925	225
1799	S[454]	-2943	340
1800	S[453]	-2961	225

No.	Text Name	X-axis	Y-axis
1801	RX[272]	-2979	340
1802	S[452]	-2997	225
1803	S[451]	-3015	340
1804	RX[271]	-3033	225
1805	RX[270]	-3051	340
1806	S[450]	-3069	225
1807	S[449]	-3087	340
1808	RX[269]	-3105	225
1809	S[448]	-3123	340
1810	S[447]	-3141	225
1811	RX[268]	-3159	340
1812	S[446]	-3177	225
1813	S[445]	-3195	340
1814	RX[267]	-3213	225
1815	S[444]	-3231	340
1816	S[443]	-3249	225
1817	RX[266]	-3267	340
1818	S[442]	-3285	225
1819	S[441]	-3303	340
1820	RX[265]	-3321	225
1821	RX[264]	-3339	340
1822	S[440]	-3357	225
1823	S[439]	-3375	340
1824	RX[263]	-3393	225
1825	S[438]	-3411	340
1826	S[437]	-3429	225
1827	RX[262]	-3447	340
1828	S[436]	-3465	225
1829	S[435]	-3483	340
1830	RX[261]	-3501	225
1831	S[434]	-3519	340
1832	S[433]	-3537	225
1833	RX[260]	-3555	340
1834	S[432]	-3573	225
1835	S[431]	-3591	340
1836	RX[259]	-3609	225
1837	RX[258]	-3627	340
1838	S[430]	-3645	225
1839	S[429]	-3663	340
1840	RX[257]	-3681	225
1841	S[428]	-3699	340
1842	S[427]	-3717	225
1843	RX[256]	-3735	340
1844	S[426]	-3753	225
1845	S[425]	-3771	340
1846	RX[255]	-3789	225
1847	S[424]	-3807	340
1848	S[423]	-3825	225
1849	RX[254]	-3843	340
1850	S[422]	-3861	225
1851	S[421]	-3879	340
1852	RX[253]	-3897	225
1853	RX[252]	-3915	340
1854	S[420]	-3933	225
1855	S[419]	-3951	340
1856	RX[251]	-3969	225
1857	S[418]	-3987	340
1858	S[417]	-4005	225
1859	RX[250]	-4023	340
1860	S[416]	-4041	225

No.	Text Name	X-axis	Y-axis
1861	S[415]	-4059	340
1862	RX[249]	-4077	225
1863	S[414]	-4095	340
1864	S[413]	-4113	225
1865	RX[248]	-4131	340
1866	S[412]	-4149	225
1867	S[411]	-4167	340
1868	RX[247]	-4185	225
1869	RX[246]	-4203	340
1870	S[410]	-4221	225
1871	S[409]	-4239	340
1872	RX[245]	-4257	225
1873	S[408]	-4275	340
1874	S[407]	-4293	225
1875	RX[244]	-4311	340
1876	S[406]	-4329	225
1877	S[405]	-4347	340
1878	RX[243]	-4365	225
1879	S[404]	-4383	340
1880	S[403]	-4401	225
1881	RX[242]	-4419	340
1882	S[402]	-4437	225
1883	S[401]	-4455	340
1884	RX[241]	-4473	225
1885	RX[240]	-4491	340
1886	S[400]	-4509	225
1887	S[399]	-4527	340
1888	RX[239]	-4545	225
1889	S[398]	-4563	340
1890	S[397]	-4581	225
1891	RX[238]	-4599	340
1892	S[396]	-4617	225
1893	S[395]	-4635	340
1894	RX[237]	-4653	225
1895	S[394]	-4671	340
1896	S[393]	-4689	225
1897	RX[236]	-4707	340
1898	S[392]	-4725	225
1899	S[391]	-4743	340
1900	RX[235]	-4761	225
1901	RX[234]	-4779	340
1902	S[390]	-4797	225
1903	S[389]	-4815	340
1904	RX[233]	-4833	225
1905	S[388]	-4851	340
1906	S[387]	-4869	225
1907	RX[232]	-4887	340
1908	S[386]	-4905	225
1909	S[385]	-4923	340
1910	RX[231]	-4941	225
1911	S[384]	-4959	340
1912	S[383]	-4977	225
1913	RX[230]	-4995	340
1914	S[382]	-5013	225
1915	S[381]	-5031	340
1916	RX[229]	-5049	225
1917	RX[228]	-5067	340
1918	S[380]	-5085	225
1919	S[379]	-5103	340
1920	RX[227]	-5121	225

No.	Text Name	X-axis	Y-axis
1921	S[378]	-5139	340
1922	S[377]	-5157	225
1923	RX[226]	-5175	340
1924	S[376]	-5193	225
1925	S[375]	-5211	340
1926	RX[225]	-5229	225
1927	S[374]	-5247	340
1928	S[373]	-5265	225
1929	RX[224]	-5283	340
1930	S[372]	-5301	225
1931	S[371]	-5319	340
1932	RX[223]	-5337	225
1933	RX[222]	-5355	340
1934	S[370]	-5373	225
1935	S[369]	-5391	340
1936	RX[221]	-5409	225
1937	S[368]	-5427	340
1938	S[367]	-5445	225
1939	RX[220]	-5463	340
1940	S[366]	-5481	225
1941	S[365]	-5499	340
1942	RX[219]	-5517	225
1943	S[364]	-5535	340
1944	S[363]	-5553	225
1945	RX[218]	-5571	340
1946	S[362]	-5589	225
1947	S[361]	-5607	340
1948	RX[217]	-5625	225
1949	RX[216]	-5643	340
1950	S[360]	-5661	225
1951	S[359]	-5679	340
1952	RX[215]	-5697	225
1953	S[358]	-5715	340
1954	S[357]	-5733	225
1955	RX[214]	-5751	340
1956	S[356]	-5769	225
1957	S[355]	-5787	340
1958	RX[213]	-5805	225
1959	S[354]	-5823	340
1960	S[353]	-5841	225
1961	RX[212]	-5859	340
1962	S[352]	-5877	225
1963	S[351]	-5895	340
1964	RX[211]	-5913	225
1965	RX[210]	-5931	340
1966	S[350]	-5949	225
1967	S[349]	-5967	340
1968	RX[209]	-5985	225
1969	S[348]	-6003	340
1970	S[347]	-6021	225
1971	RX[208]	-6039	340
1972	S[346]	-6057	225
1973	S[345]	-6075	340
1974	RX[207]	-6093	225
1975	S[344]	-6111	340
1976	S[343]	-6129	225
1977	RX[206]	-6147	340
1978	S[342]	-6165	225
1979	S[341]	-6183	340
1980	RX[205]	-6201	225

No.	Text Name	X-axis	Y-axis
1981	RX[204]	-6219	340
1982	S[340]	-6237	225
1983	S[339]	-6255	340
1984	RX[203]	-6273	225
1985	S[338]	-6291	340
1986	S[337]	-6309	225
1987	RX[202]	-6327	340
1988	S[336]	-6345	225
1989	S[335]	-6363	340
1990	RX[201]	-6381	225
1991	S[334]	-6399	340
1992	S[333]	-6417	225
1993	RX[200]	-6435	340
1994	S[332]	-6453	225
1995	S[331]	-6471	340
1996	RX[199]	-6489	225
1997	RX[198]	-6507	340
1998	S[330]	-6525	225
1999	S[329]	-6543	340
2000	RX[197]	-6561	225
2001	S[328]	-6579	340
2002	S[327]	-6597	225
2003	RX[196]	-6615	340
2004	S[326]	-6633	225
2005	S[325]	-6651	340
2006	RX[195]	-6669	225
2007	S[324]	-6687	340
2008	S[323]	-6705	225
2009	RX[194]	-6723	340
2010	S[322]	-6741	225
2011	S[321]	-6759	340
2012	RX[193]	-6777	225
2013	RX[192]	-6795	340
2014	S[320]	-6813	225
2015	S[319]	-6831	340
2016	RX[191]	-6849	225
2017	S[318]	-6867	340
2018	S[317]	-6885	225
2019	RX[190]	-6903	340
2020	S[316]	-6921	225
2021	S[315]	-6939	340
2022	RX[189]	-6957	225
2023	S[314]	-6975	340
2024	S[313]	-6993	225
2025	RX[188]	-7011	340
2026	S[312]	-7029	225
2027	S[311]	-7047	340
2028	RX[187]	-7065	225
2029	RX[186]	-7083	340
2030	S[310]	-7101	225
2031	S[309]	-7119	340
2032	RX[185]	-7137	225
2033	S[308]	-7155	340
2034	S[307]	-7173	225
2035	RX[184]	-7191	340
2036	S[306]	-7209	225
2037	S[305]	-7227	340
2038	RX[183]	-7245	225
2039	S[304]	-7263	340
2040	S[303]	-7281	225

No.	Text Name	X-axis	Y-axis
2041	RX[182]	-7299	340
2042	S[302]	-7317	225
2043	S[301]	-7335	340
2044	RX[181]	-7353	225
2045	RX[180]	-7371	340
2046	S[300]	-7389	225
2047	S[299]	-7407	340
2048	RX[179]	-7425	225
2049	S[298]	-7443	340
2050	S[297]	-7461	225
2051	RX[178]	-7479	340
2052	S[296]	-7497	225
2053	S[295]	-7515	340
2054	RX[177]	-7533	225
2055	S[294]	-7551	340
2056	S[293]	-7569	225
2057	RX[176]	-7587	340
2058	S[292]	-7605	225
2059	S[291]	-7623	340
2060	RX[175]	-7641	225
2061	RX[174]	-7659	340
2062	S[290]	-7677	225
2063	S[289]	-7695	340
2064	RX[173]	-7713	225
2065	S[288]	-7731	340
2066	S[287]	-7749	225
2067	RX[172]	-7767	340
2068	S[286]	-7785	225
2069	S[285]	-7803	340
2070	RX[171]	-7821	225
2071	S[284]	-7839	340
2072	S[283]	-7857	225
2073	RX[170]	-7875	340
2074	S[282]	-7893	225
2075	S[281]	-7911	340
2076	RX[169]	-7929	225
2077	RX[168]	-7947	340
2078	S[280]	-7965	225
2079	S[279]	-7983	340
2080	RX[167]	-8001	225
2081	S[278]	-8019	340
2082	S[277]	-8037	225
2083	RX[166]	-8055	340
2084	S[276]	-8073	225
2085	S[275]	-8091	340
2086	RX[165]	-8109	225
2087	S[274]	-8127	340
2088	S[273]	-8145	225
2089	RX[164]	-8163	340
2090	S[272]	-8181	225
2091	S[271]	-8199	340
2092	RX[163]	-8217	225
2093	RX[162]	-8235	340
2094	S[270]	-8253	225
2095	S[269]	-8271	340
2096	RX[161]	-8289	225
2097	S[268]	-8307	340
2098	S[267]	-8325	225
2099	RX[160]	-8343	340
2100	S[266]	-8361	225

No.	Text Name	X-axis	Y-axis
2101	S[265]	-8379	340
2102	RX[159]	-8397	225
2103	S[264]	-8415	340
2104	S[263]	-8433	225
2105	RX[158]	-8451	340
2106	S[262]	-8469	225
2107	S[261]	-8487	340
2108	RX[157]	-8505	225
2109	RX[156]	-8523	340
2110	S[260]	-8541	225
2111	S[259]	-8559	340
2112	RX[155]	-8577	225
2113	S[258]	-8595	340
2114	S[257]	-8613	225
2115	RX[154]	-8631	340
2116	S[256]	-8649	225
2117	S[255]	-8667	340
2118	RX[153]	-8685	225
2119	S[254]	-8703	340
2120	S[253]	-8721	225
2121	RX[152]	-8739	340
2122	S[252]	-8757	225
2123	S[251]	-8775	340
2124	RX[151]	-8793	225
2125	RX[150]	-8811	340
2126	S[250]	-8829	225
2127	S[249]	-8847	340
2128	RX[149]	-8865	225
2129	S[248]	-8883	340
2130	S[247]	-8901	225
2131	RX[148]	-8919	340
2132	S[246]	-8937	225
2133	S[245]	-8955	340
2134	RX[147]	-8973	225
2135	S[244]	-8991	340
2136	S[243]	-9009	225
2137	RX[146]	-9027	340
2138	S[242]	-9045	225
2139	S[241]	-9063	340
2140	RX[145]	-9081	225
2141	RX[144]	-9099	340
2142	S[240]	-9117	225
2143	S[239]	-9135	340
2144	RX[143]	-9153	225
2145	S[238]	-9171	340
2146	S[237]	-9189	225
2147	RX[142]	-9207	340
2148	S[236]	-9225	225
2149	S[235]	-9243	340
2150	RX[141]	-9261	225
2151	S[234]	-9279	340
2152	S[233]	-9297	225
2153	RX[140]	-9315	340
2154	S[232]	-9333	225
2155	S[231]	-9351	340
2156	RX[139]	-9369	225
2157	RX[138]	-9387	340
2158	S[230]	-9405	225
2159	S[229]	-9423	340
2160	RX[137]	-9441	225

No.	Text Name	X-axis	Y-axis
2161	S[228]	-9459	340
2162	S[227]	-9477	225
2163	RX[136]	-9495	340
2164	S[226]	-9513	225
2165	S[225]	-9531	340
2166	RX[135]	-9549	225
2167	S[224]	-9567	340
2168	S[223]	-9585	225
2169	RX[134]	-9603	340
2170	S[222]	-9621	225
2171	S[221]	-9639	340
2172	RX[133]	-9657	225
2173	RX[132]	-9675	340
2174	S[220]	-9693	225
2175	S[219]	-9711	340
2176	RX[131]	-9729	225
2177	S[218]	-9747	340
2178	S[217]	-9765	225
2179	RX[130]	-9783	340
2180	S[216]	-9801	225
2181	S[215]	-9819	340
2182	RX[129]	-9837	225
2183	S[214]	-9855	340
2184	S[213]	-9873	225
2185	RX[128]	-9891	340
2186	S[212]	-9909	225
2187	S[211]	-9927	340
2188	RX[127]	-9945	225
2189	RX[126]	-9963	340
2190	S[210]	-9981	225
2191	S[209]	-9999	340
2192	RX[125]	-10017	225
2193	S[208]	-10035	340
2194	S[207]	-10053	225
2195	RX[124]	-10071	340
2196	S[206]	-10089	225
2197	S[205]	-10107	340
2198	RX[123]	-10125	225
2199	S[204]	-10143	340
2200	S[203]	-10161	225
2201	RX[122]	-10179	340
2202	S[202]	-10197	225
2203	S[201]	-10215	340
2204	RX[121]	-10233	225
2205	RX[120]	-10251	340
2206	S[200]	-10269	225
2207	S[199]	-10287	340
2208	RX[119]	-10305	225
2209	S[198]	-10323	340
2210	S[197]	-10341	225
2211	RX[118]	-10359	340
2212	S[196]	-10377	225
2213	S[195]	-10395	340
2214	RX[117]	-10413	225
2215	S[194]	-10431	340
2216	S[193]	-10449	225
2217	RX[116]	-10467	340
2218	S[192]	-10485	225
2219	S[191]	-10503	340
2220	RX[115]	-10521	225

No.	Text Name	X-axis	Y-axis
2221	RX[114]	-10539	340
2222	S[190]	-10557	225
2223	S[189]	-10575	340
2224	RX[113]	-10593	225
2225	S[188]	-10611	340
2226	S[187]	-10629	225
2227	RX[112]	-10647	340
2228	S[186]	-10665	225
2229	S[185]	-10683	340
2230	RX[111]	-10701	225
2231	S[184]	-10719	340
2232	S[183]	-10737	225
2233	RX[110]	-10755	340
2234	S[182]	-10773	225
2235	S[181]	-10791	340
2236	RX[109]	-10809	225
2237	RX[108]	-10827	340
2238	S[180]	-10845	225
2239	S[179]	-10863	340
2240	RX[107]	-10881	225
2241	S[178]	-10899	340
2242	S[177]	-10917	225
2243	RX[106]	-10935	340
2244	S[176]	-10953	225
2245	S[175]	-10971	340
2246	RX[105]	-10989	225
2247	S[174]	-11007	340
2248	S[173]	-11025	225
2249	RX[104]	-11043	340
2250	S[172]	-11061	225
2251	S[171]	-11079	340
2252	RX[103]	-11097	225
2253	RX[102]	-11115	340
2254	S[170]	-11133	225
2255	S[169]	-11151	340
2256	RX[101]	-11169	225
2257	S[168]	-11187	340
2258	S[167]	-11205	225
2259	RX[100]	-11223	340
2260	S[166]	-11241	225
2261	S[165]	-11259	340
2262	RX[99]	-11277	225
2263	S[164]	-11295	340
2264	S[163]	-11313	225
2265	RX[98]	-11331	340
2266	S[162]	-11349	225
2267	S[161]	-11367	340
2268	RX[97]	-11385	225
2269	RX[96]	-11403	340
2270	S[160]	-11421	225
2271	S[159]	-11439	340
2272	RX[95]	-11457	225
2273	S[158]	-11475	340
2274	S[157]	-11493	225
2275	RX[94]	-11511	340
2276	S[156]	-11529	225
2277	S[155]	-11547	340
2278	RX[93]	-11565	225
2279	S[154]	-11583	340
2280	S[153]	-11601	225

No.	Text Name	X-axis	Y-axis
2281	RX[92]	-11619	340
2282	S[152]	-11637	225
2283	S[151]	-11655	340
2284	RX[91]	-11673	225
2285	RX[90]	-11691	340
2286	S[150]	-11709	225
2287	S[149]	-11727	340
2288	RX[89]	-11745	225
2289	S[148]	-11763	340
2290	S[147]	-11781	225
2291	RX[88]	-11799	340
2292	S[146]	-11817	225
2293	S[145]	-11835	340
2294	RX[87]	-11853	225
2295	S[144]	-11871	340
2296	S[143]	-11889	225
2297	RX[86]	-11907	340
2298	S[142]	-11925	225
2299	S[141]	-11943	340
2300	RX[85]	-11961	225
2301	RX[84]	-11979	340
2302	S[140]	-11997	225
2303	S[139]	-12015	340
2304	RX[83]	-12033	225
2305	S[138]	-12051	340
2306	S[137]	-12069	225
2307	RX[82]	-12087	340
2308	S[136]	-12105	225
2309	S[135]	-12123	340
2310	RX[81]	-12141	225
2311	S[134]	-12159	340
2312	S[133]	-12177	225
2313	RX[80]	-12195	340
2314	S[132]	-12213	225
2315	S[131]	-12231	340
2316	RX[79]	-12249	225
2317	RX[78]	-12267	340
2318	S[130]	-12285	225
2319	S[129]	-12303	340
2320	RX[77]	-12321	225
2321	S[128]	-12339	340
2322	S[127]	-12357	225
2323	RX[76]	-12375	340
2324	S[126]	-12393	225
2325	S[125]	-12411	340
2326	RX[75]	-12429	225
2327	S[124]	-12447	340
2328	S[123]	-12465	225
2329	RX[74]	-12483	340
2330	S[122]	-12501	225
2331	S[121]	-12519	340
2332	RX[73]	-12537	225
2333	RX[72]	-12555	340
2334	S[120]	-12573	225
2335	S[119]	-12591	340
2336	RX[71]	-12609	225
2337	S[118]	-12627	340
2338	S[117]	-12645	225
2339	RX[70]	-12663	340
2340	S[116]	-12681	225

No.	Text Name	X-axis	Y-axis
2341	S[115]	-12699	340
2342	RX[69]	-12717	225
2343	S[114]	-12735	340
2344	S[113]	-12753	225
2345	RX[68]	-12771	340
2346	S[112]	-12789	225
2347	S[111]	-12807	340
2348	RX[67]	-12825	225
2349	RX[66]	-12843	340
2350	S[110]	-12861	225
2351	S[109]	-12879	340
2352	RX[65]	-12897	225
2353	S[108]	-12915	340
2354	S[107]	-12933	225
2355	RX[64]	-12951	340
2356	S[106]	-12969	225
2357	S[105]	-12987	340
2358	RX[63]	-13005	225
2359	S[104]	-13023	340
2360	S[103]	-13041	225
2361	RX[62]	-13059	340
2362	S[102]	-13077	225
2363	S[101]	-13095	340
2364	RX[61]	-13113	225
2365	RX[60]	-13131	340
2366	S[100]	-13149	225
2367	S[99]	-13167	340
2368	RX[59]	-13185	225
2369	S[98]	-13203	340
2370	S[97]	-13221	225
2371	RX[58]	-13239	340
2372	S[96]	-13257	225
2373	S[95]	-13275	340
2374	RX[57]	-13293	225
2375	S[94]	-13311	340
2376	S[93]	-13329	225
2377	RX[56]	-13347	340
2378	S[92]	-13365	225
2379	S[91]	-13383	340
2380	RX[55]	-13401	225
2381	RX[54]	-13419	340
2382	S[90]	-13437	225
2383	S[89]	-13455	340
2384	RX[53]	-13473	225
2385	S[88]	-13491	340
2386	S[87]	-13509	225
2387	RX[52]	-13527	340
2388	S[86]	-13545	225
2389	S[85]	-13563	340
2390	RX[51]	-13581	225
2391	S[84]	-13599	340
2392	S[83]	-13617	225
2393	RX[50]	-13635	340
2394	S[82]	-13653	225
2395	S[81]	-13671	340
2396	RX[49]	-13689	225
2397	RX[48]	-13707	340
2398	S[80]	-13725	225
2399	S[79]	-13743	340
2400	RX[47]	-13761	225

No.	Text Name	X-axis	Y-axis
2401	S[78]	-13779	340
2402	S[77]	-13797	225
2403	RX[46]	-13815	340
2404	S[76]	-13833	225
2405	S[75]	-13851	340
2406	RX[45]	-13869	225
2407	S[74]	-13887	340
2408	S[73]	-13905	225
2409	RX[44]	-13923	340
2410	S[72]	-13941	225
2411	S[71]	-13959	340
2412	RX[43]	-13977	225
2413	RX[42]	-13995	340
2414	S[70]	-14013	225
2415	S[69]	-14031	340
2416	RX[41]	-14049	225
2417	S[68]	-14067	340
2418	S[67]	-14085	225
2419	RX[40]	-14103	340
2420	S[66]	-14121	225
2421	S[65]	-14139	340
2422	RX[39]	-14157	225
2423	S[64]	-14175	340
2424	S[63]	-14193	225
2425	RX[38]	-14211	340
2426	S[62]	-14229	225
2427	S[61]	-14247	340
2428	RX[37]	-14265	225
2429	RX[36]	-14283	340
2430	S[60]	-14301	225
2431	S[59]	-14319	340
2432	RX[35]	-14337	225
2433	S[58]	-14355	340
2434	S[57]	-14373	225
2435	RX[34]	-14391	340
2436	S[56]	-14409	225
2437	S[55]	-14427	340
2438	RX[33]	-14445	225
2439	S[54]	-14463	340
2440	S[53]	-14481	225
2441	RX[32]	-14499	340
2442	S[52]	-14517	225
2443	S[51]	-14535	340
2444	RX[31]	-14553	225
2445	RX[30]	-14571	340
2446	S[50]	-14589	225
2447	S[49]	-14607	340
2448	RX[29]	-14625	225
2449	S[48]	-14643	340
2450	S[47]	-14661	225
2451	RX[28]	-14679	340
2452	S[46]	-14697	225
2453	S[45]	-14715	340
2454	RX[27]	-14733	225
2455	S[44]	-14751	340
2456	S[43]	-14769	225
2457	RX[26]	-14787	340
2458	S[42]	-14805	225
2459	S[41]	-14823	340
2460	RX[25]	-14841	225
2461	RX[24]	-14859	340
2462	S[40]	-14877	225
2463	S[39]	-14895	340
2464	RX[23]	-14913	225
2465	S[38]	-14931	340
2466	S[37]	-14949	225
2467	RX[22]	-14967	340
2468	S[36]	-14985	225
2469	S[35]	-15003	340
2470	RX[21]	-15021	225
2471	S[34]	-15039	340
2472	S[33]	-15057	225
2473	RX[20]	-15075	340
2474	S[32]	-15093	225
2475	S[31]	-15111	340
2476	RX[19]	-15129	225
2477	RX[18]	-15147	340
2478	S[30]	-15165	225
2479	S[29]	-15183	340
2480	RX[17]	-15201	225
2481	S[28]	-15219	340
2482	S[27]	-15237	225
2483	RX[16]	-15255	340
2484	S[26]	-15273	225
2485	S[25]	-15291	340
2486	RX[15]	-15309	225
2487	S[24]	-15327	340
2488	S[23]	-15345	225
2489	RX[14]	-15363	340
2490	S[22]	-15381	225
2491	S[21]	-15399	340
2492	RX[13]	-15417	225
2493	RX[12]	-15435	340
2494	S[20]	-15453	225
2495	S[19]	-15471	340
2496	RX[11]	-15489	225
2497	S[18]	-15507	340
2498	S[17]	-15525	225
2499	RX[10]	-15543	340
2500	S[16]	-15561	225
2501	S[15]	-15579	340
2502	RX[9]	-15597	225
2503	S[14]	-15615	340
2504	S[13]	-15633	225
2505	RX[8]	-15651	340
2506	S[12]	-15669	225
2507	S[11]	-15687	340
2508	RX[7]	-15705	225
2509	RX[6]	-15723	340
2510	S[10]	-15741	225
2511	S[9]	-15759	340
2512	RX[5]	-15777	225
2513	S[8]	-15795	340
2514	S[7]	-15813	225
2515	RX[4]	-15831	340
2516	S[6]	-15849	225
2517	S[5]	-15867	340
2518	RX[3]	-15885	225
2519	S[4]	-15903	340
2520	S[3]	-15921	225
2521	RX[2]	-15939	340
2522	S[2]	-15957	225
2523	S[1]	-15975	340
2524	RX[1]	-15993	225
2525	S[0]	-16011	340
2526	GRID[1]	-16029	225
2527	GRID[1]	-16047	340
2528	GRID[1]	-16065	225
2529	GRID[1]	-16083	340
2530	DUMMY[0]	-16101	225
2531	DUMMY[0]	-16119	340

3.7. Power Supply Generating Circuit

The following figure shows the configuration of the liquid crystal drive voltage generating circuit.

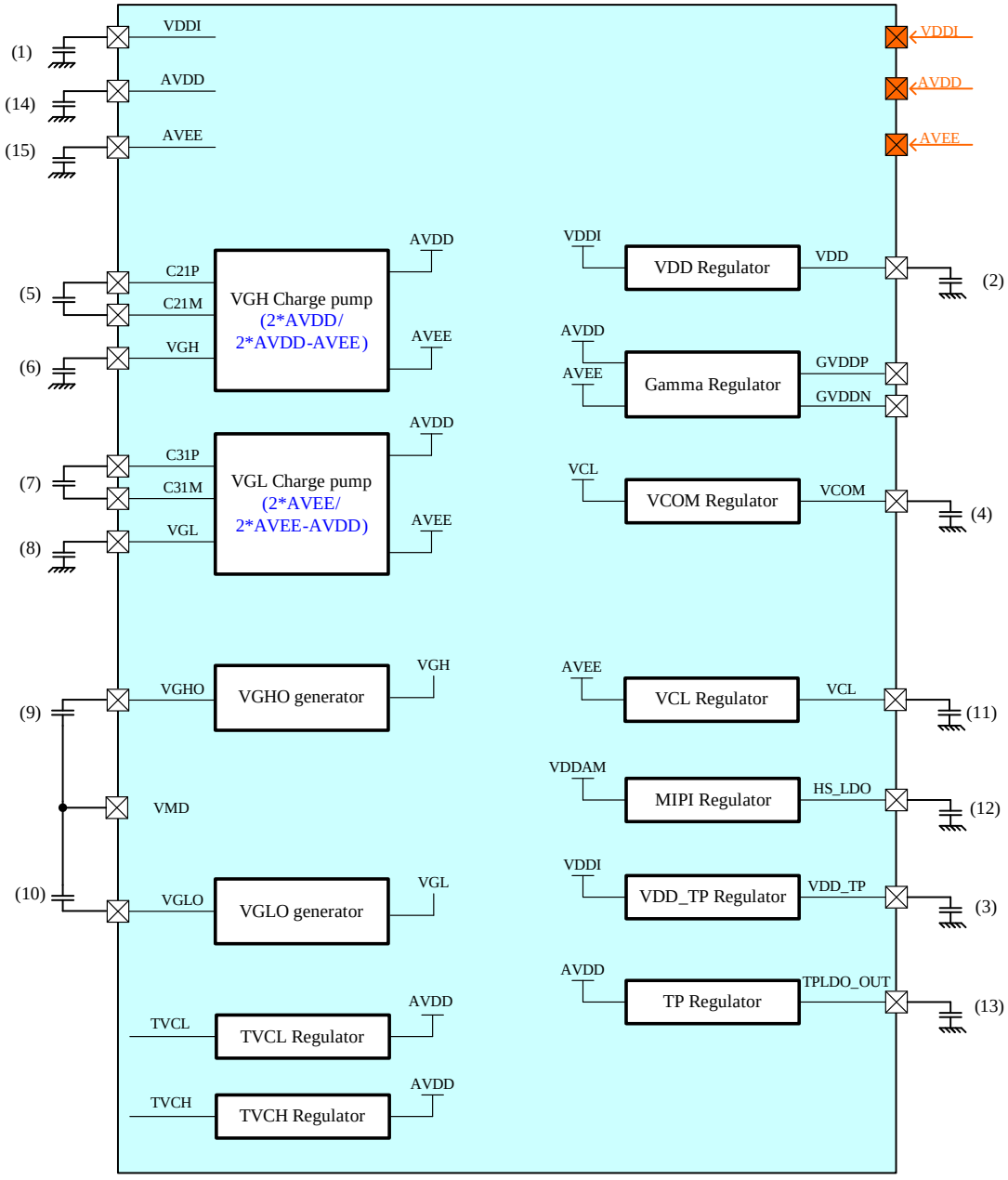


Figure 4. Three Power mode Supply Generating Circuit

3.8. Specifications of External Elements

The following table shows specifications of external elements

The numbers of following table correspond to the numbers shown in “Figure 3. Three Power mode Supply Generating Circuit and “Figure 4. Two Power Mode With PowerIC Supply Generating Circuit”

Table 1. External Component Table

ILI7807S					
Capacitor					
NO.	Pad Name	Connection		Value	Note
1	VDDI/VDDAM	VDDI	GND	2.2uF/6V	
2	VDD	VDD	GND	2.2uF/6V	
3	VDD_TP	VDD_TP	GND	2.2uF/6V	
4	VCOM	VCOM	GND	2.2uF/6V	
5	C21	C21P	C21M	1.0uF/25V	
6	VGH	VGH	GND	1.0uF/25V	
7	C31	C31P	C31M	1.0uF/25V	
8	VGL	VGL	GND	1.0uF/25V	
9	VGHO	VGHO	VMOD	1.0uF/25V	
10	VGLO	VGLO	VMOD	1.0uF/25V	
11	VCL	VCL	GND	1.0uF/6V	
12	HS_LDO	HS_LDO	GND	1.0uF/6V	
13	TPLDO_OUT	TPLDO_OUT	GND	2.2uF/10V	
14	AVDD	AVDD	GND	2.2uF/10V	
15	AVEE	AVEE	GND	2.2uF/10V	
Note: Capacitance ±10% at temperature range -25 to 85℃					

Diode					
NO.	Pad Name	Connection		Value	Note
1	D1	AVDD	VGH	VF<0.4Vat 20mA , VR>30V	Option
2	D2	VGL	AVEE	VF<0.4Vat 20mA , VR>30V	Option
3	D3	VGL	GND	VF<0.4Vat 20mA , VR>30V	Option
4	D4	GND	AVDD	VF<0.4Vat 20mA , VR>30V	Option
5	D5	AVEE	GND	VF<0.4Vat 20mA , VR>30V	Option
6	D6	VGHO	VGH	VF<0.4Vat 20mA , VR>30V	Option
7	D7	VGL	VGLO	VF<0.4Vat 20mA , VR>30V	Option

TVS					
NO.	Pad Name	Connection		Value	Note
1	T1	VDDI	GND		Option
2	T2	VSP	GND		Option
3	T3	VSN	GND		Option
8	T8	TP_INT	GND		Option
9	T9	RESX	GND		Option
10	T10	TP_RESX	GND		Option
11	T11	TP_SPI_SCLK	GND		Option , Host download
12	T12	TP_SPI_CS	GND		Option , Host download
13	T13	TP_SPI_MOSI	GND		Option , Host download
14	T14	TP_SPI_MISO	GND		Option , Host download
15	T15	TP_I2C_SDA	GND		Option
16	T16	TP_I2C_SCL	GND		Option
17	T17	VDD	GND		Option
18	T18	VDD_TP	GND		Option

Resistance					
NO.	Pad Name	Connection		Value	Note
1	R1	RESX	RESX	0 ohm	Option
2	R2	LEDP WM	LED PWM	0 ohm	Option
3	R3	TP_RESX	TP_RESX	0 ohm	Option
4	R4	TP_I2C_SDA	TP_I2C_SDA	0 ohm	Option
5	R5	TP_I2C_SCL	TP_I2C_SCL	0 ohm	Option
6	R6	TE1	TE1	0 ohm	Option
7	R7	TE	TE	0 ohm	Option
8	R8	RESX	TP_RESX	0 ohm	Option
10	R9	VDD	HS_LDO	0 ohm	Option
11	R10	VDD	VDD_TP	0 ohm	Option

3.9. Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation using “3 Power Mode” and “4 Power Mode”in the LCD driver and the relationship between TFT display application voltages.

3 PWR Mode

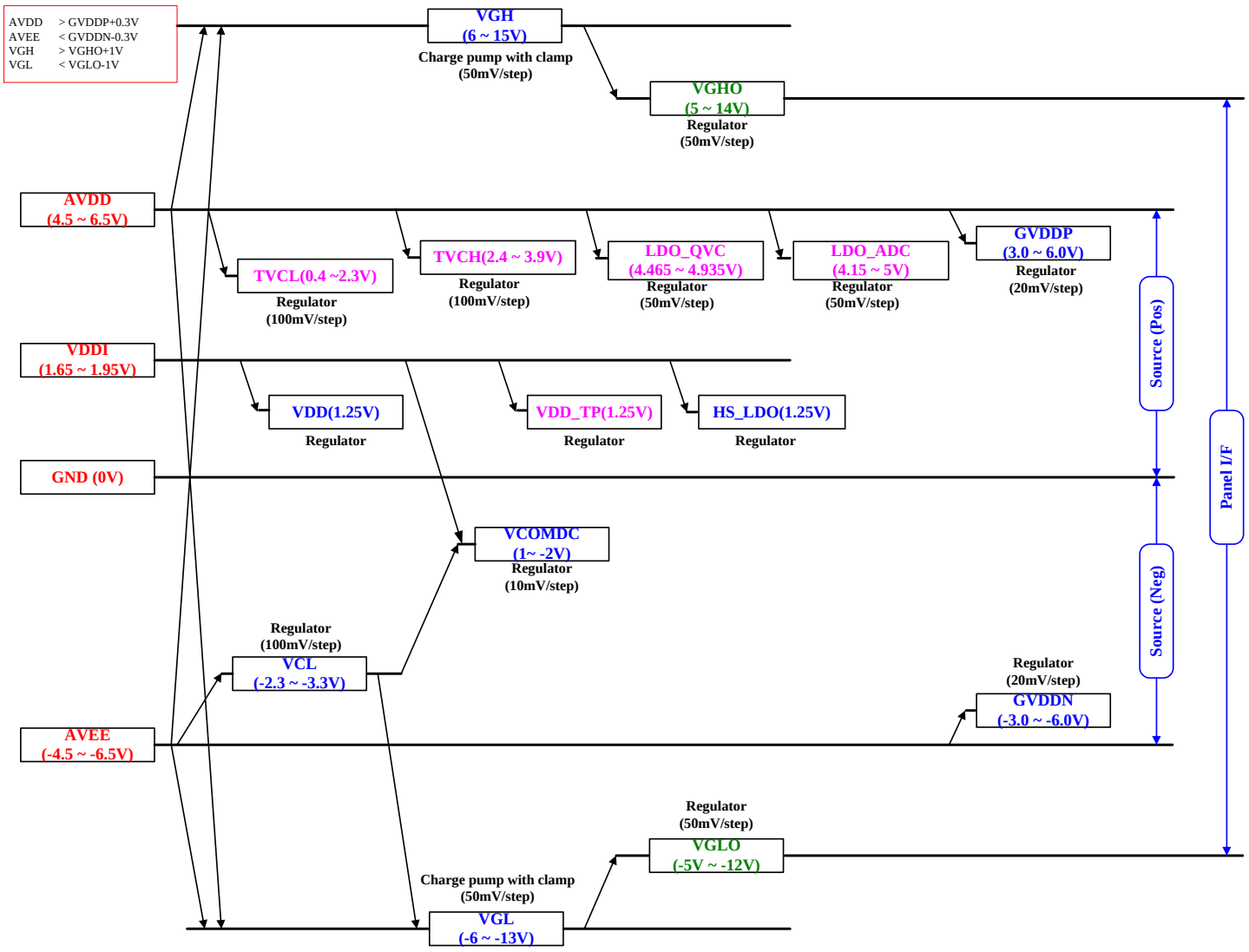


Figure 5. Three Power Mode Structure Diagram

4 PWR Mode

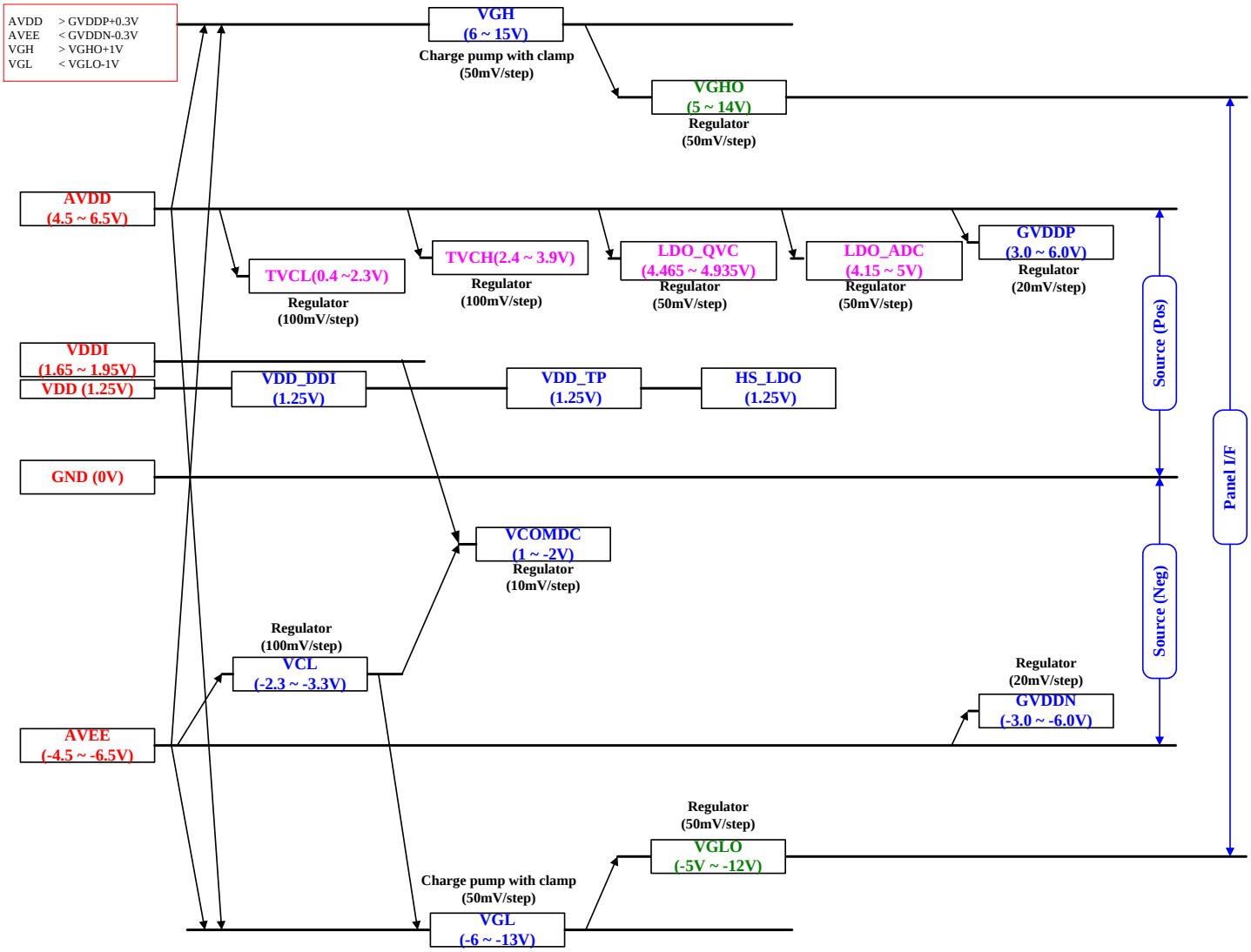


Figure 6 Four Power Mode Structure Diagram

Note:

1. The above voltage ranges are recommended.
2. All of the output voltage levels are lower than their theoretical levels (Ideal voltage levels) due to current consumption at respective outputs.

3.10. Power On/Off Sequence

3.10.1. 3 power mode

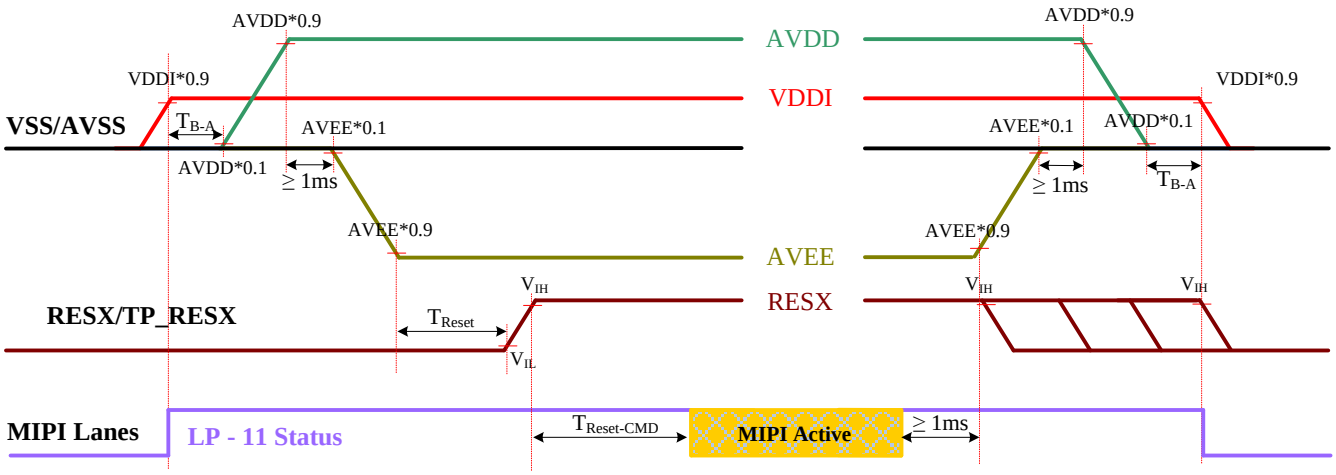


Figure 7. 3 power mode Power on/off sequence

3.10.2. 4 power mode

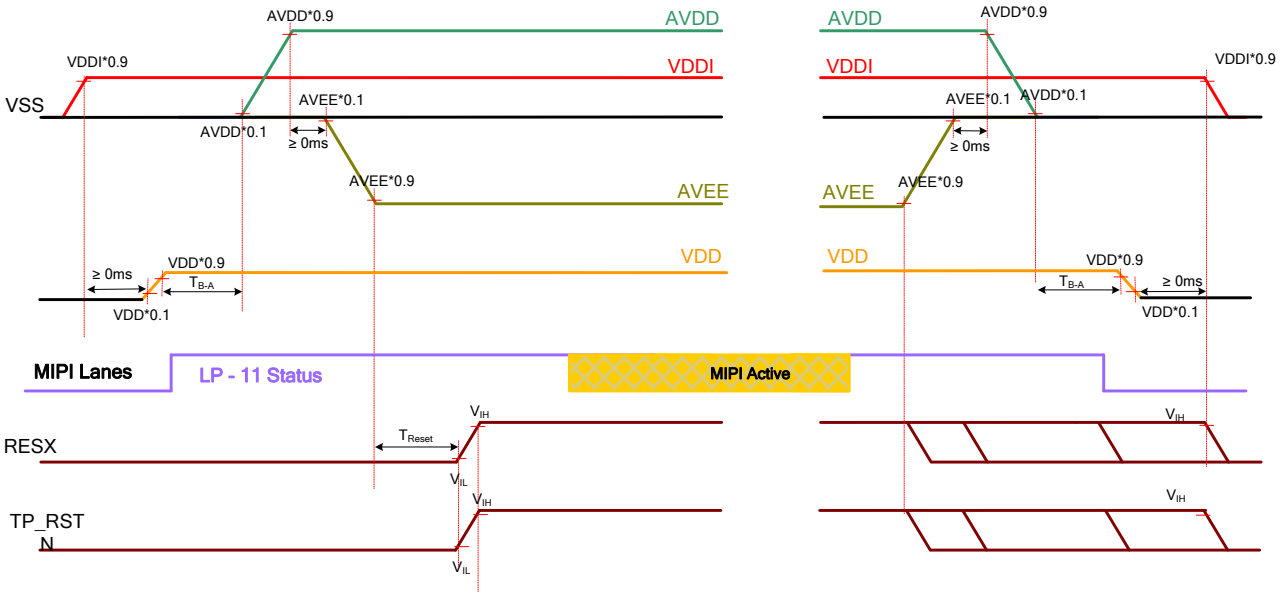


Figure 8. 4 power mode Power on/off sequence

4PWR Note:

1. Need HW-pin to set 4 power mode

Table 2. Timing Relation of Power On/Off Sequence

Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{Rise}	External Power Rise Time	0.2	-	20	ms
T_{Fall}	External Power Fall Time	0.2	-	20	ms
T_{B-A}	Delay Time between Two External Power	2	5	-	ms
T_{Reset}	Delay Time between External Power and Reset	4	10	-	ms
$T_{Reset-CMD}$	Reset to First Command in Display Sleep In Mode	10	-	-	ms

4. System Interface Description

4.1. SPI Interface

SPI interface is used to communicate with external flash, which used to store the Firmware.

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol which operates in full duplex mode. Devices communicate in Master/Slave mode with 4-wire bi-direction interface.

The main features of the SPI bus are:

- Communication speed up to 12 MHz. Master mode operation.
- Configurable 8-bit length of a transfer word.
- MSB first transfer.

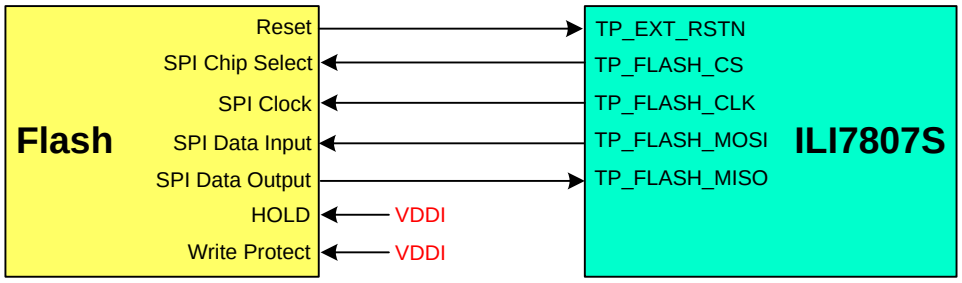


Figure 9. SPI Interface System

4.2. I²C System Interface Configuration

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP).

The Slave end of I²C in ILI7807S is the only interface for touch communication with HOST. Whenever there is effective touch sensed on the touch screen, Touch controller will send data transfer request to the HOST via I²C interface and complete the point report to the HOST. HOST can communicate with ILI7807S via I²C. HOST can also reset Touch controller through TP_RESX pad.

The main features of the I²C bus are:

- Communication speed up to 400 kHz.
- Support variableness of I²C Slave Address. (default:0x55)
- MSB first transfer.
- External pull-up resistors are necessary for I²C fast mode. The resistors are 2.0KΩ for the fastest speed SCL (max. 400KHz), the maximum loading CL (max.<150pF) and the IO power supply VDDI=1.8V

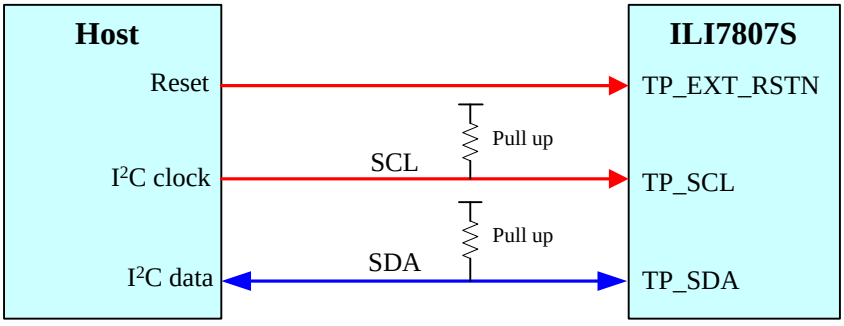


Figure 10. I²C System Interface Diagram

4.3. DSI system interface

4.3.1. General Description

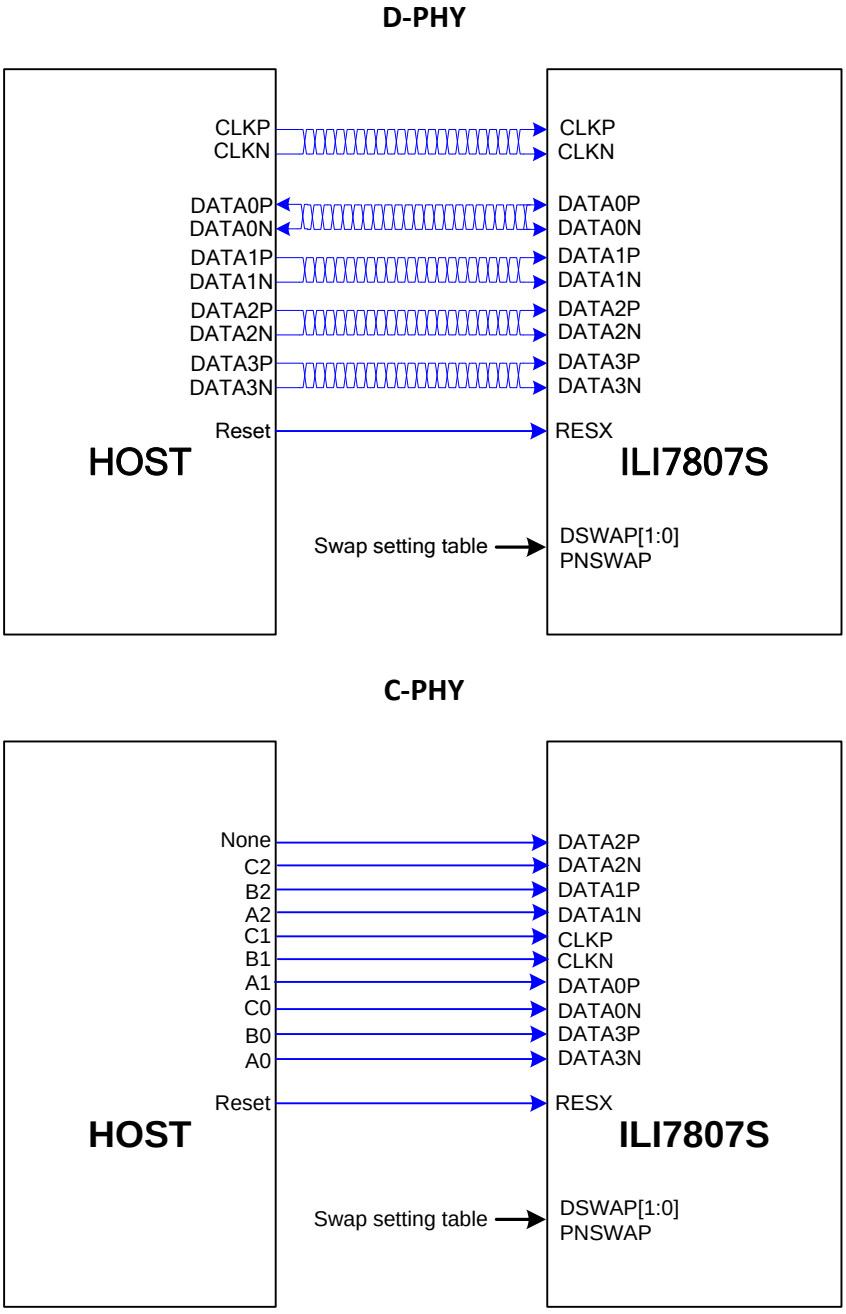


Figure 11. DSI System Interface Diagram

The communication is separated into two different levels between the MCU and the display module:

- Low level communication is done on the interface level.
- High level communication is done on the packet level.

4.3.2. Interface Level Communication

4.3.2.1. General

The display module uses data and clock lane differential pairs for DSI. The differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 3. High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

4.3.2.2. DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

Note 1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

Note 2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

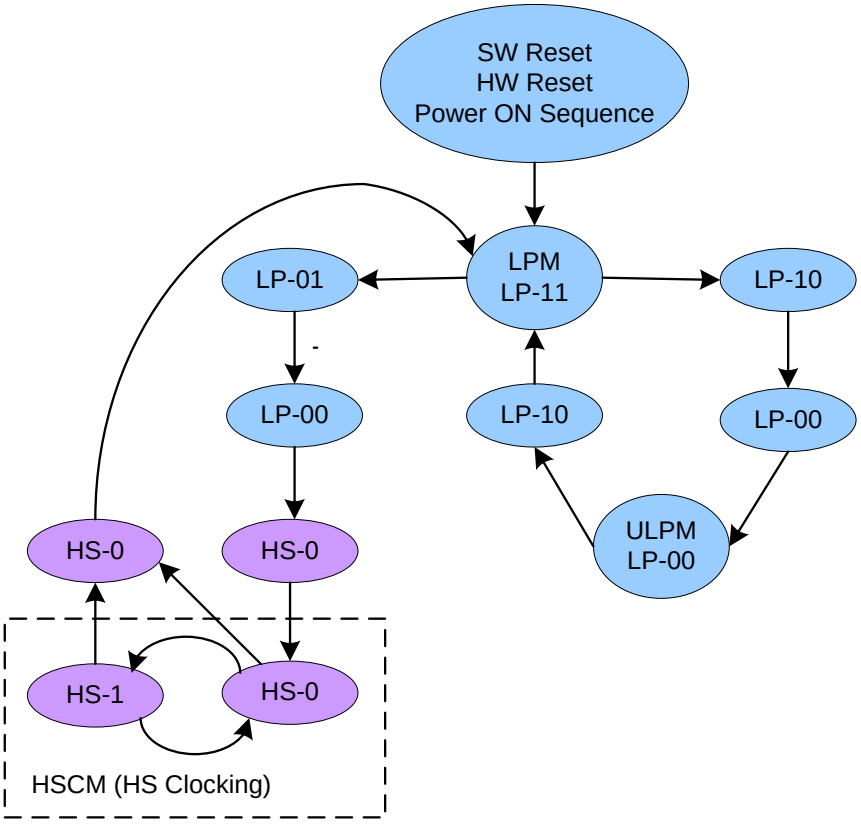


Figure 12. Clock Lanes Power Modes

4.3.2.2.1. Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

1) After HW Reset or Power On Sequence =>LP-11

2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM).

This sequence is illustrated below.

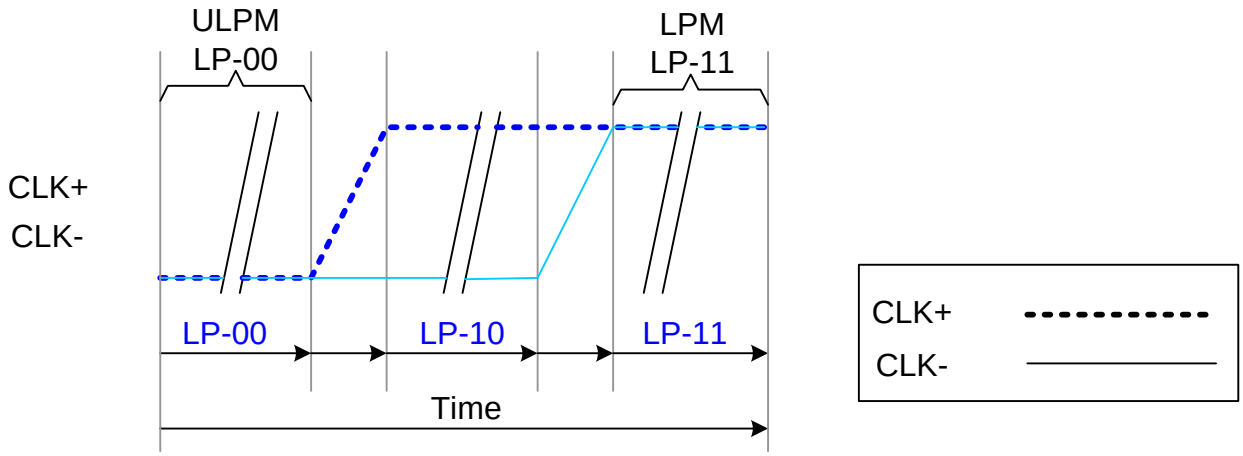


Figure 13. From ULPM to LPM

3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0=>LP-11 (LPM). This sequence is illustrated below.

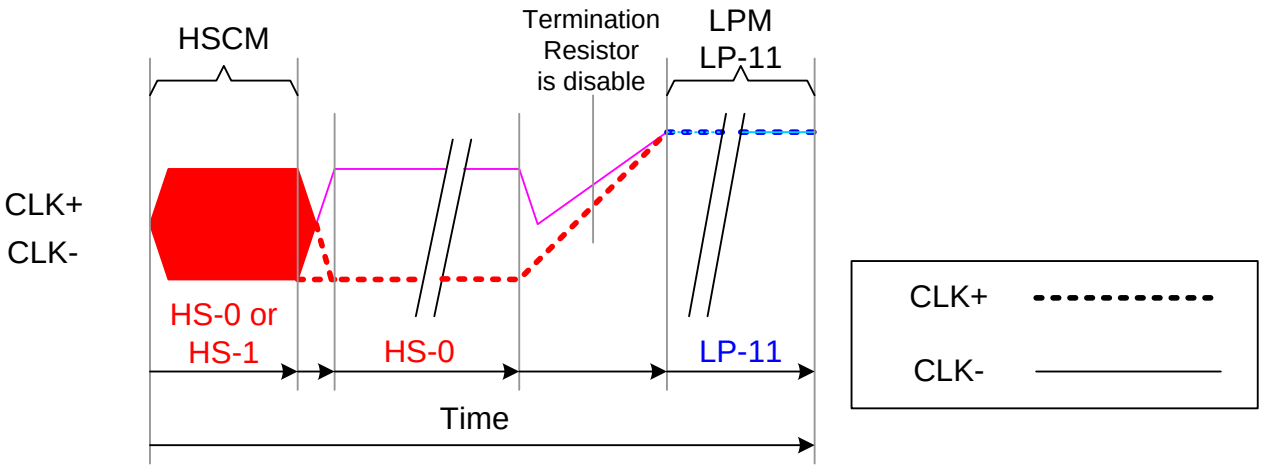


Figure 14. From High Speed Clock Mode (HSCM) to LPM

All three mode changes are illustrated a flow chart below.

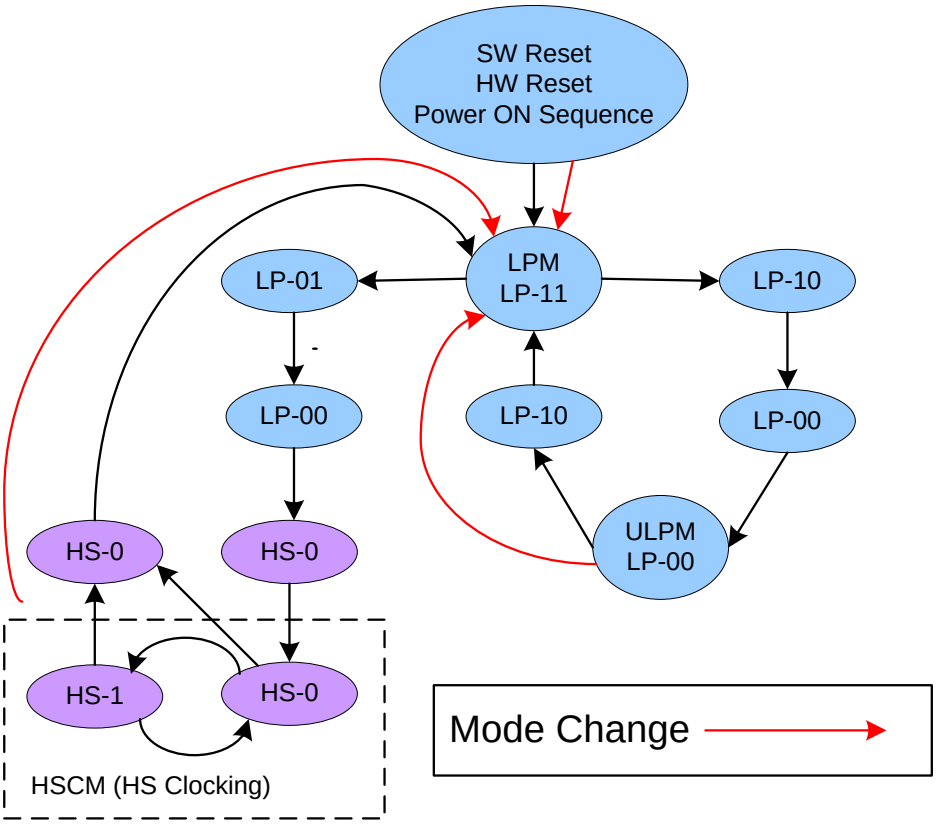


Figure 15. All Three Mode Changes to LPM on the Flow Chart

4.3.2.2.2. Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPM).

This sequence is illustrated below.

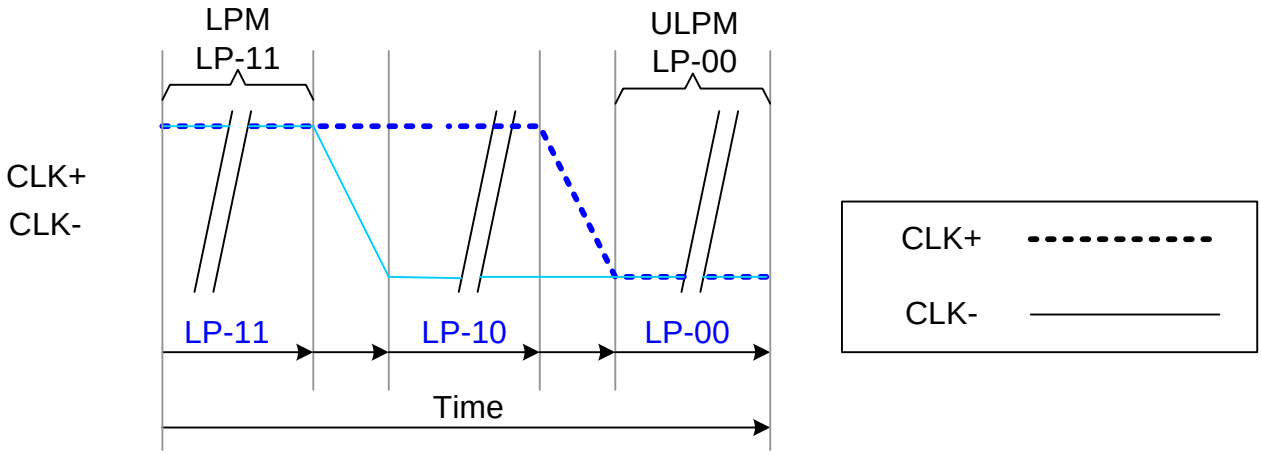


Figure 16. From LPM to ULPM

The mode change is also illustrated below.

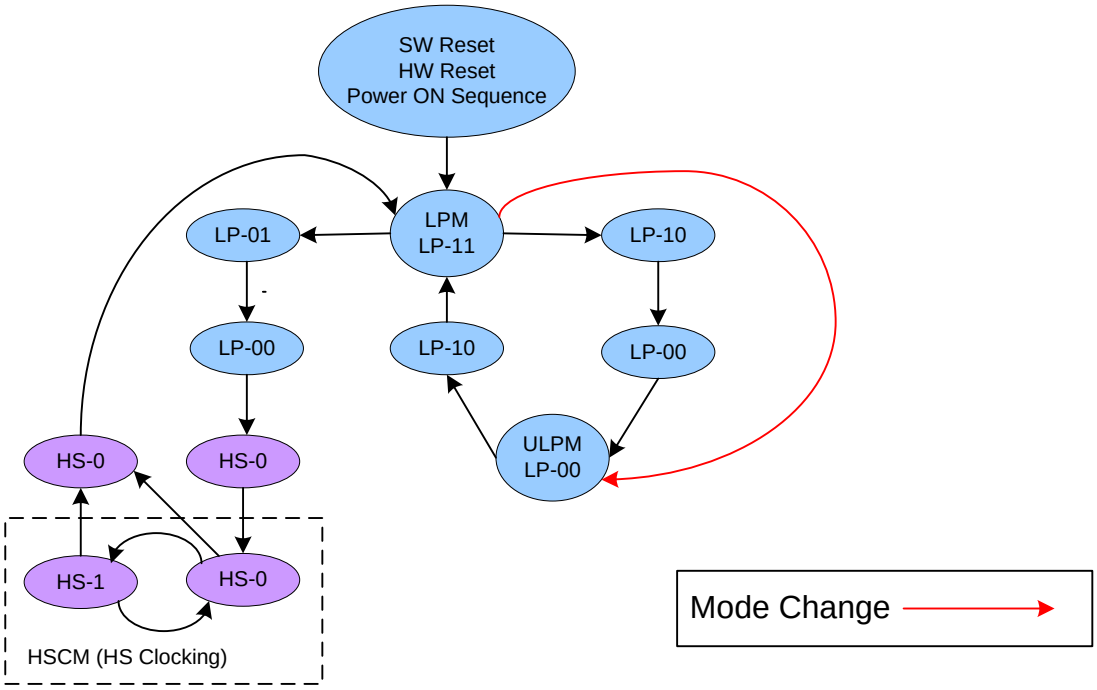


Figure 17. Mode Change from LPM to ULPM on the Flow Chart

4.3.2.2.3. High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

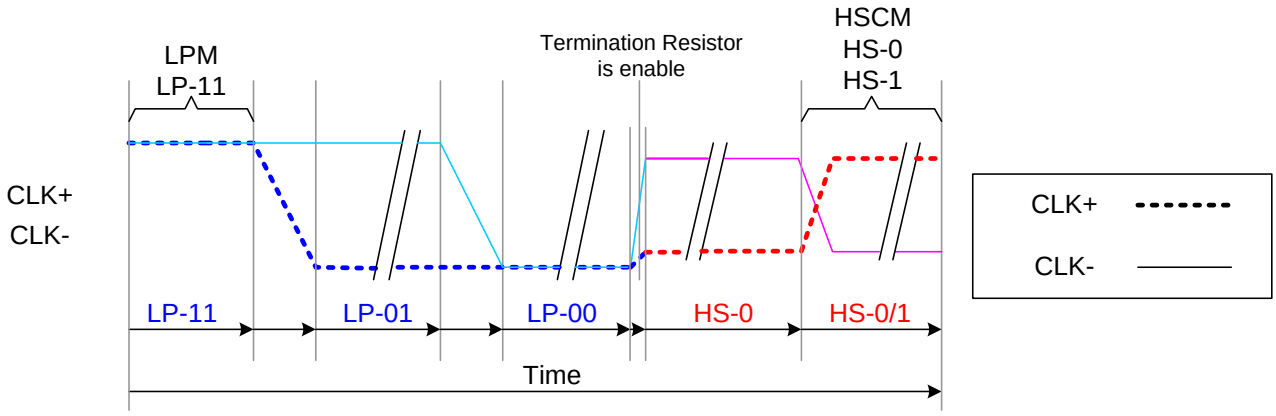


Figure 18. From LPM to HSCM

The mode change is also illustrated below.

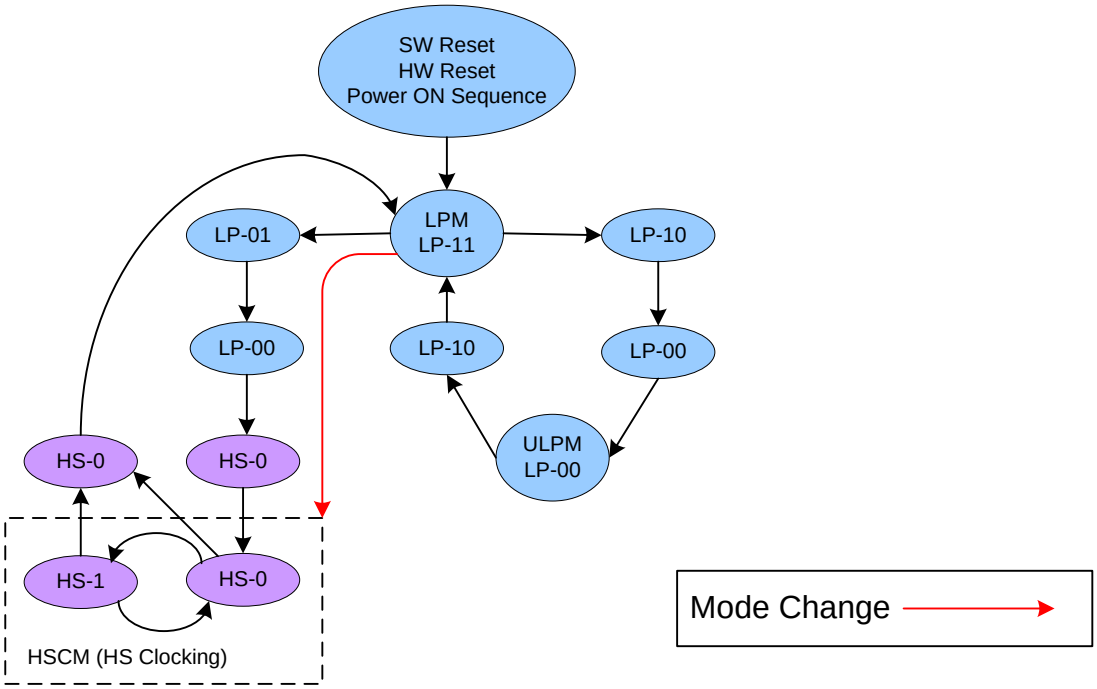


Figure 19. Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- or DSI-D0+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

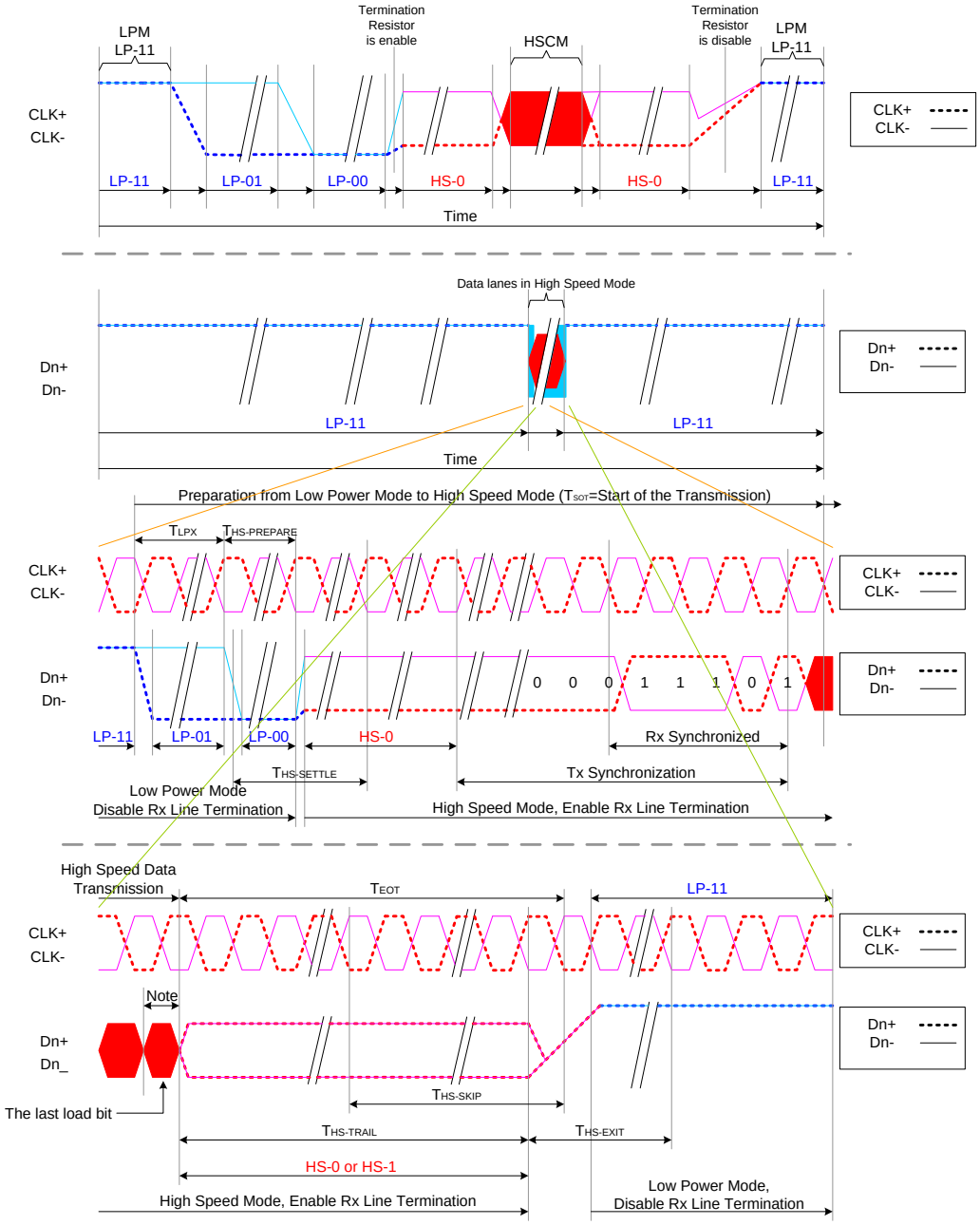


Figure 20. High Speed Clock Burst [Note]

Note:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.3.2.3. DSI-Dn and DSI-D0 Data Lanes

4.3.2.3.1. General

DSI-Dn +/-, n=1,2,3 and DSI-D0+/- Data Lanes can be driven in different modes which are:

- Escape Mode (Only DSI-D0+/- data lanes are used)
- High-Speed Data Transmission (DSI-Dn +/-, n=1,2,3 and DSI-D0+/- data lanes are used)
- Bus Turnaround Request (Only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined on the following table.

Table 4. Entering and Leaving Sequences [Note]

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 → LP-10 → LP-00 → LP-01 → LP-00	LP-00 → LP-10 → LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 → LP-01 → LP-00 → HS-0	(HS-0 or HS-1) → LP-11
Bus Turnaround Request	LP-11 → LP-10 → LP-00 → LP-10 → LP-00	Hi-Z

3. DSI-Dn+/-, n=0,1,2,3.

Note:
1. DSI-Dn+/-, n=1,2,3 and DSI-D0+/- data lanes are used.
2. More information on chapter “4.3.2.3.4. Bus Turnaround (BTA)”.

4.3.2.3.2. Escape Modes

DSI-D0+/- data lanes can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which is resetting the display module,
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU.

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0-= 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below.

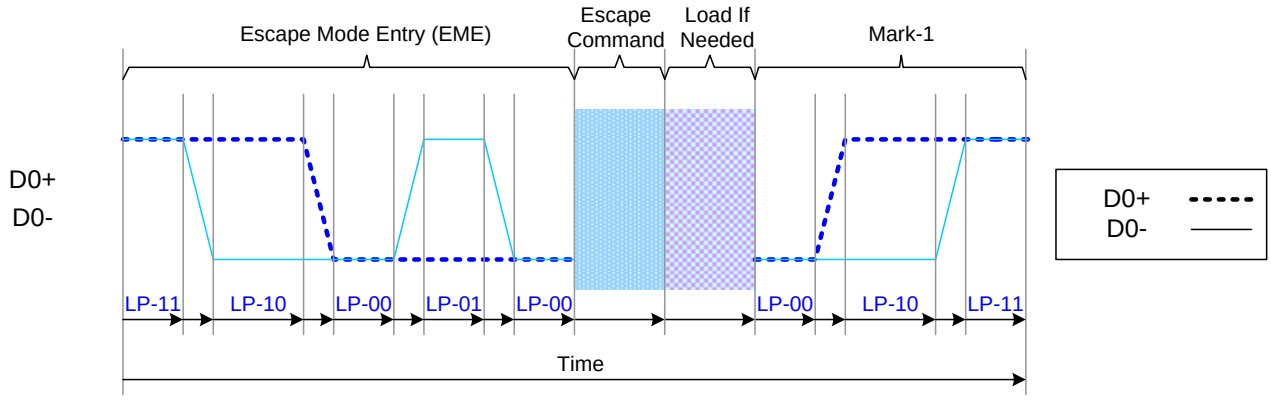


Figure 21. General Escape Mode Sequence

There are a total of eight Escape Commands (EC) divided into two types, Modes and Triggers (see the following table).

An example of a Mode type Escape Command is 'Ultra-Low Power Mode' where the MCU instructs the display module to enter it's Ultra-Low Power Mode.

Escape commands are defined on the next table.

Table 5. Escape Commands [Note]

Escape command	Command Type Mode / Trigger	Entry command Pattern (First Bit ➔ Last Bit Transmitted)	Dn (n = 1,2,3)	D0
Low-Power Data Transmission	Mode	1110 0001 b	-	X
Ultra-Low Power Mode	Mode	0001 1110 b	X	X
Undefined-1, [Note 1]	Mode	1001 1111 b	-	-
Undefined-2, [Note 1]	Mode	1101 1110 b	-	-
Remote Application Reset	Trigger	0110 0010 b	-	X
Tearing Effect	Trigger	0101 1101 b	-	X
Acknowledge	Trigger	0010 0001 b	-	X
Uknown-5, [Note 1]	Trigger	1010 0000 b	-	-

Note:
1. This Escape command support has not been implemented on the display module.
2. x = Supported.
3. - = Not Supported.

4.3.2.3.2.1. Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):
  - One or more bytes (8 bit)
  - Data lanes are in pause mode when data lanes are stopped (lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below.

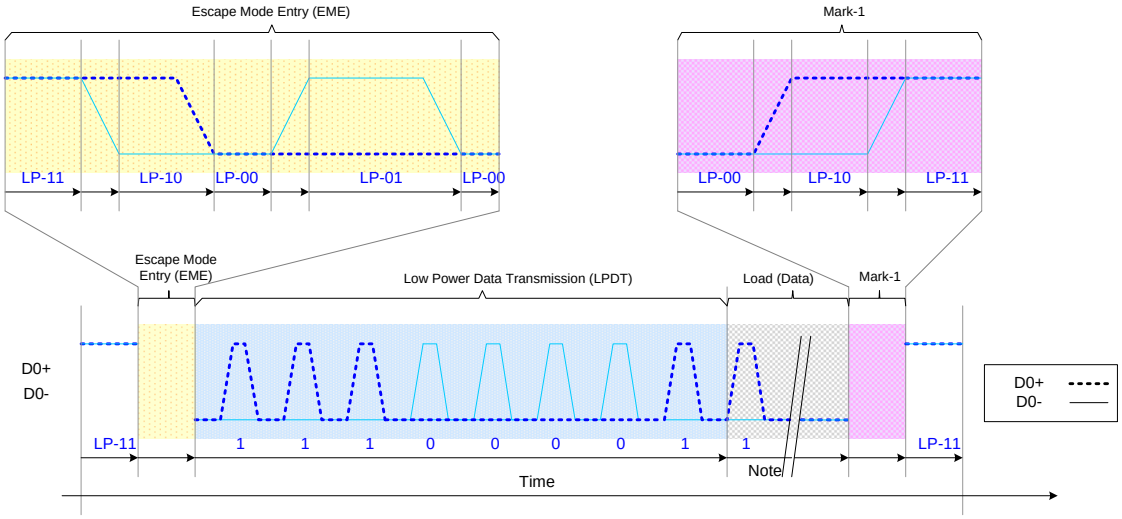


Figure 22. Low-Power Data Transmission (LPDT) [Note]

Note:
Load (Data) is presenting that the first bit is logical '1' in this example.

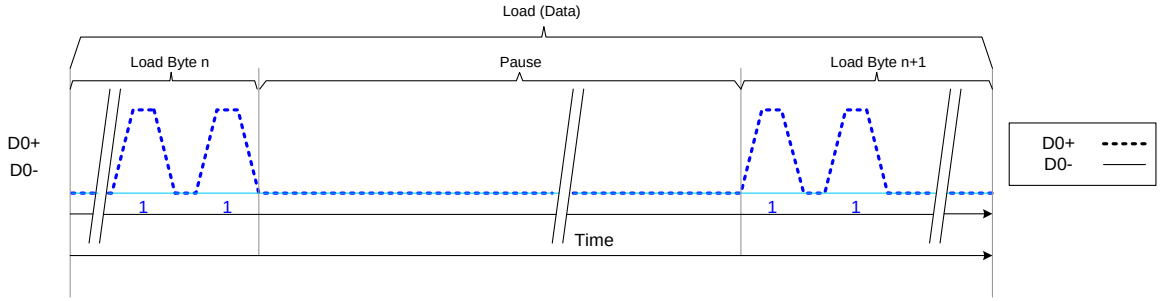


Figure 23. Pause (Example)

4.3.2.3.2.2. Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below.

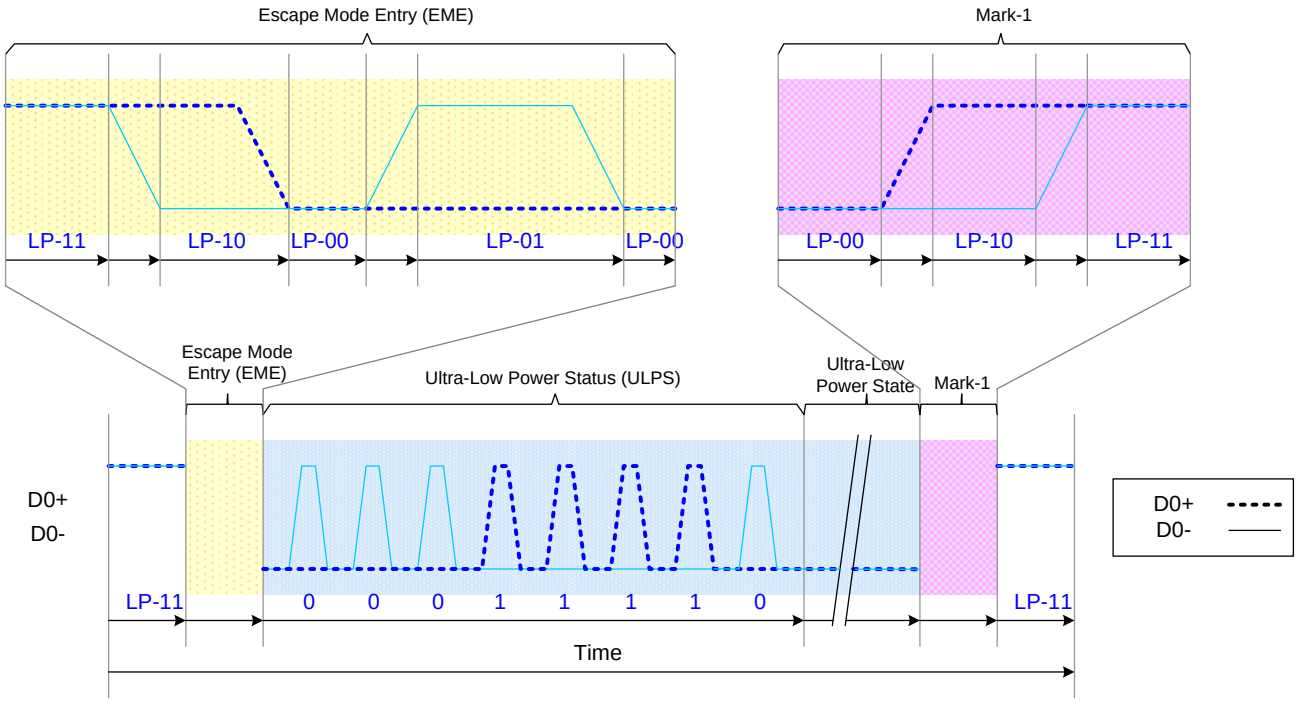


Figure 24. Ultra-Low Power State (ULPS)

4.3.2.3.2.3. Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below.

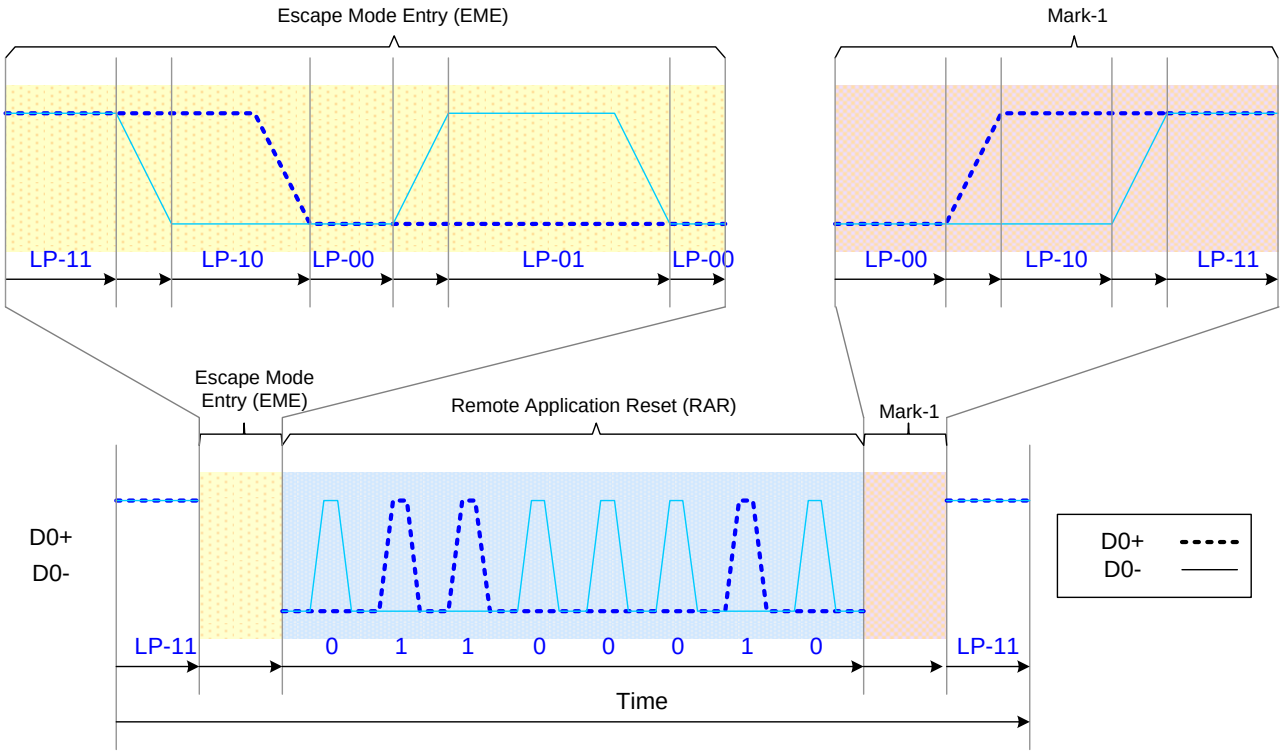


Figure 25. Remote Application Reset (RAR)

4.3.2.3.2.4. Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happened on the display module by Tearing Effect (TEE).

The display module is sending the Tearing Effect (TEE) what is a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below.

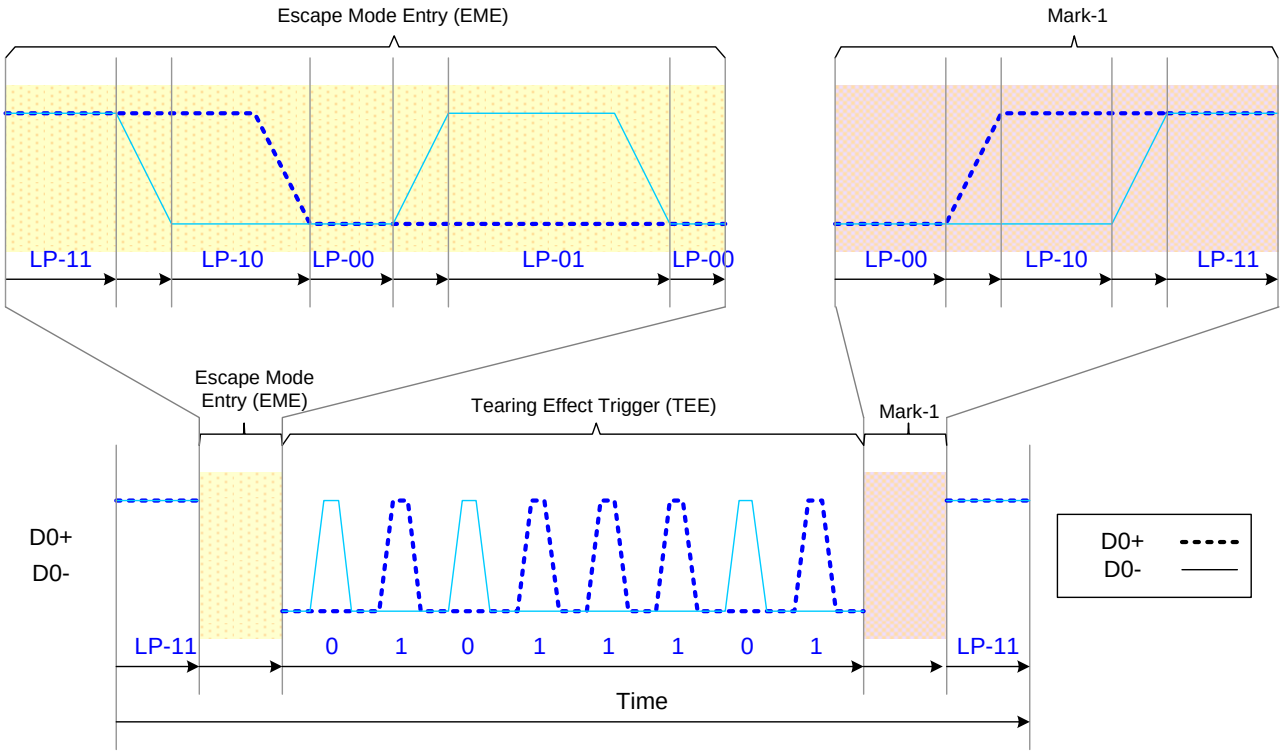


Figure 26. Tearing Effect (TEE)

4.3.2.3.2.5. Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The display module is sending the Acknowledge (ACK) what is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below.

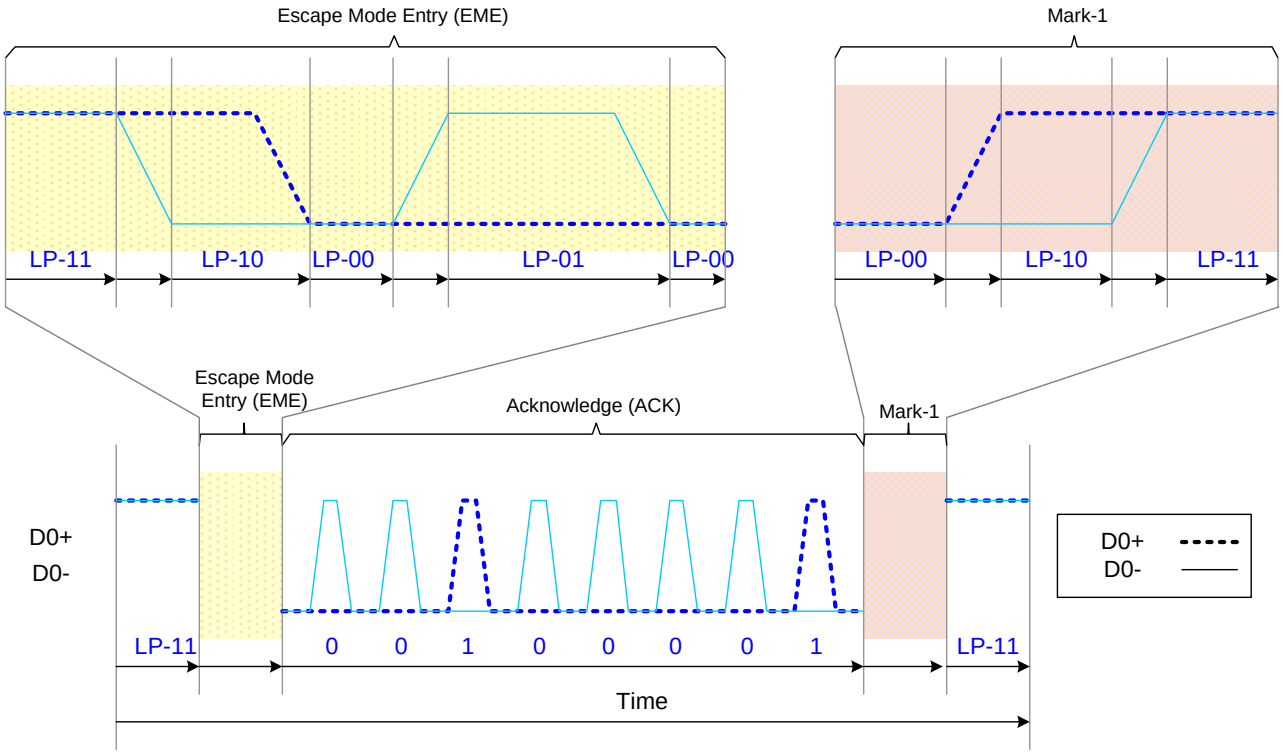


Figure 27. Acknowledge (ACK)

4.3.2.3.3. High-Speed Data Transmission (HSDT)

4.3.2.3.3.1. Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter "4.3.2.2.3. High-Speed Clock Mode (HSCM)".

Data lanes DSI-Dn+/-,n=1,2,3 and DSI-D0+/- of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below.

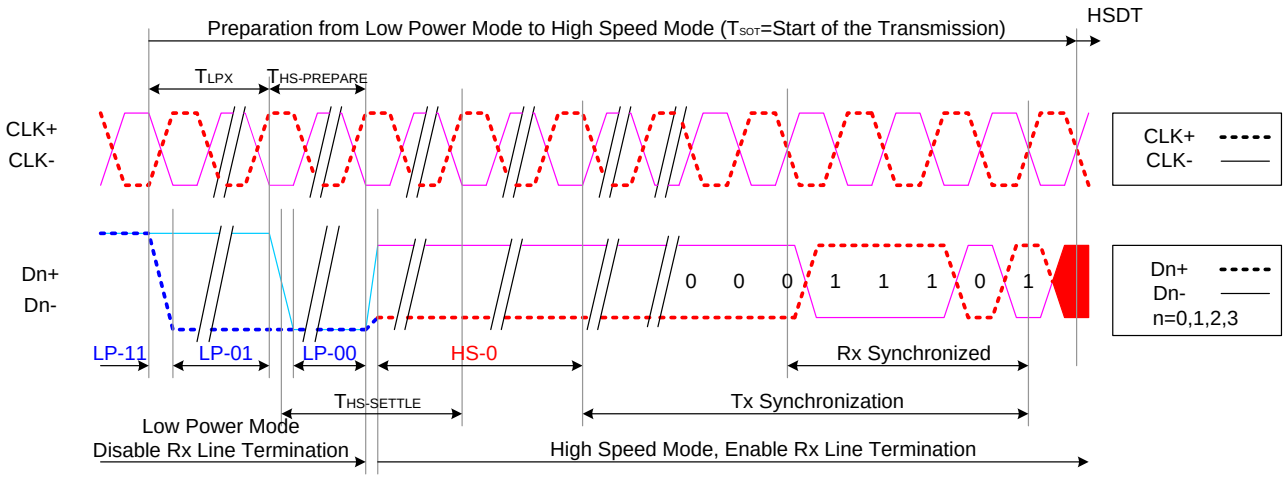


Figure 28. Entering High-Speed Data Transmission (T_{SOT} of HSDT)

4.3.2.3.3.2. Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes DSI-Dn+/-, n=1,2,3 and DSI-D0+/- are in LP-11 mode. See more information on chapter "4.3.2.2.3. High-Speed Clock Mode (HSCM)".

Data lanes DSI-Dn+/-, n=1,2,3 and DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stop: High-Speed Data Transmission
- MCU changes to HS-1, if the last load bit is HS-0
- MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below.

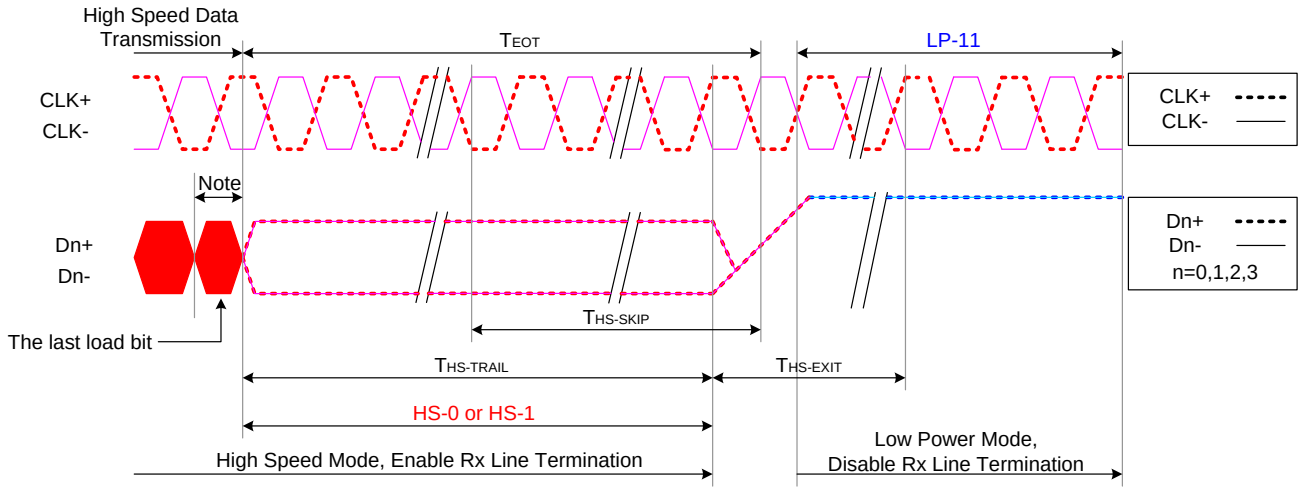


Figure 29. Leaving High-Speed Data Transmission (T_{EOT} of HSDT) Note

Note:
1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.3.2.3.3.3. Burst of the High-Speed Data Transmission (HSDT)

The burst of the "High-Speed Data Transmission" (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter "4.3.3.1. Short Packet (SPa) and Long Packet (LPa) Structures".

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

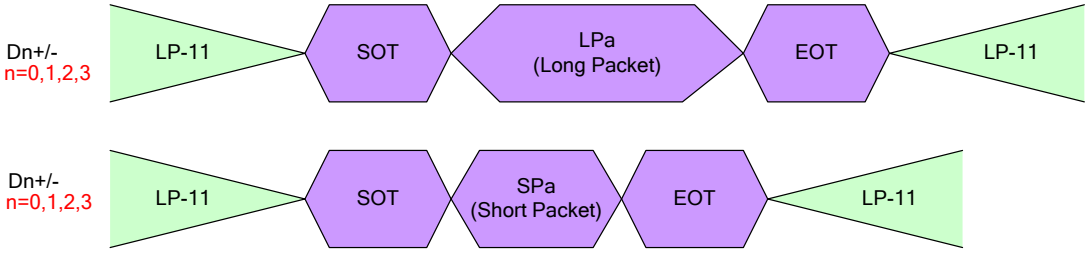


Figure 30. Single Packet in High-Speed Data Transmissions

The multiple packets in High-Speed Data Transmission is illustrated for reference purposes below.

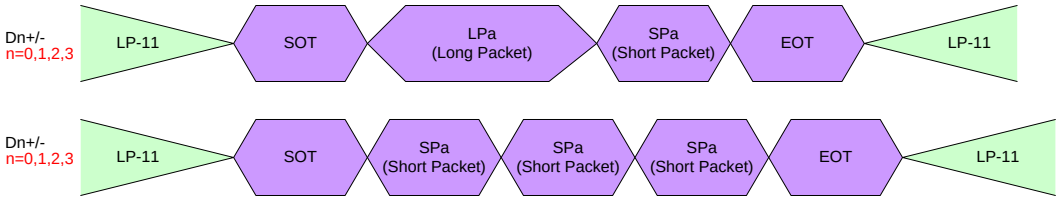


Figure 31. Multiple Packets in High-Speed Data Transmission – Examples

Table 6. Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are '1's (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Byte orders of the sent packet is in High-Speed Data Transmission (HSDT) as follows.

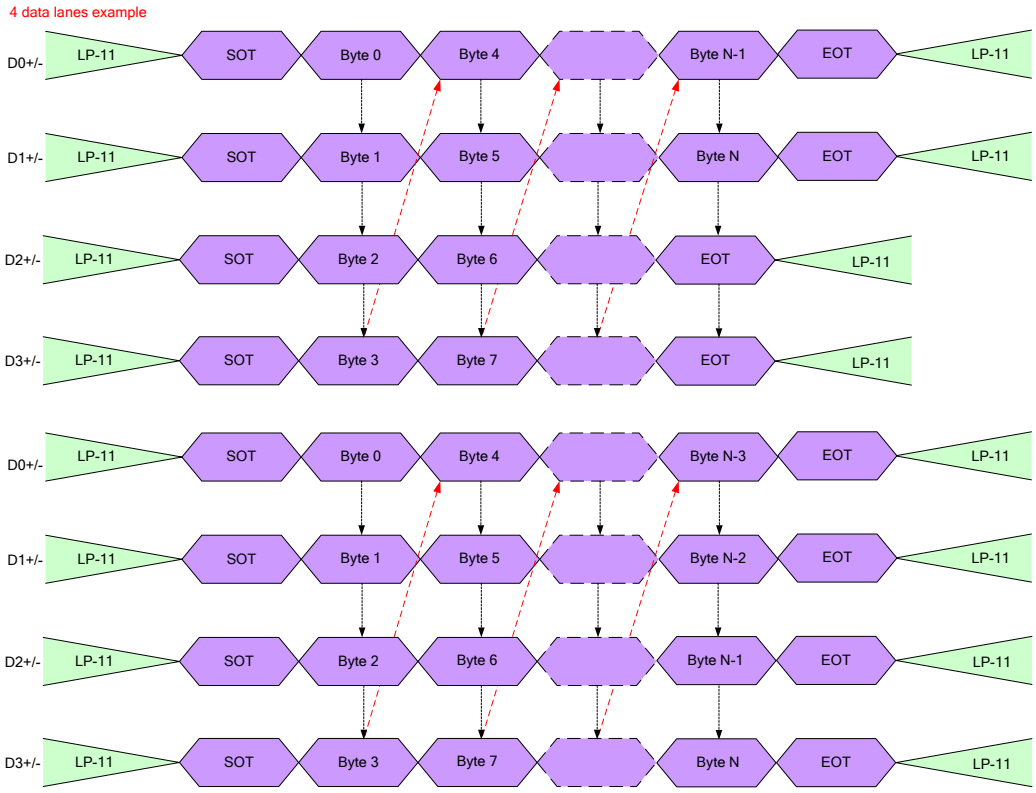


Figure 32. A Single Packet in HSDT – Even Number of Bytes

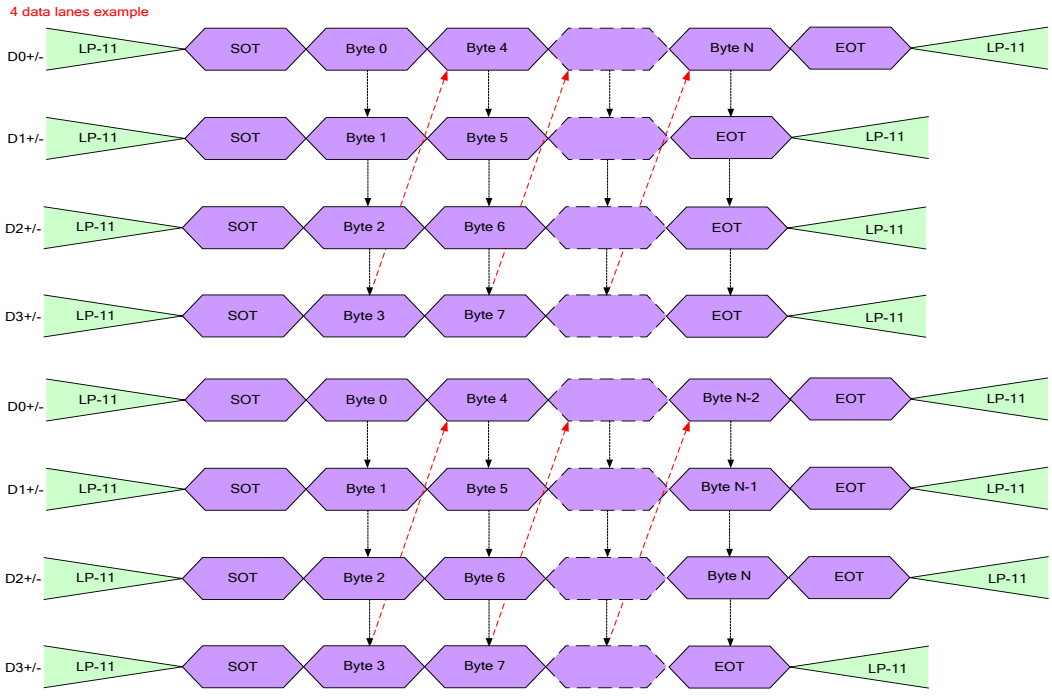


Figure 33. Single Packet in HSDT – Odd Number of Byte

4.3.2.3.4. Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU and display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follows.

• Start (MCU): LP-11

• Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00 => LP-10 => LP-00

• The MCU waits until the display module is starting to control DSI-D0+/- data lanes and the MCU stops to control DSI-D0+/- data lanes (= High-Z)

• The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MCU to the display module) is illustrated below.

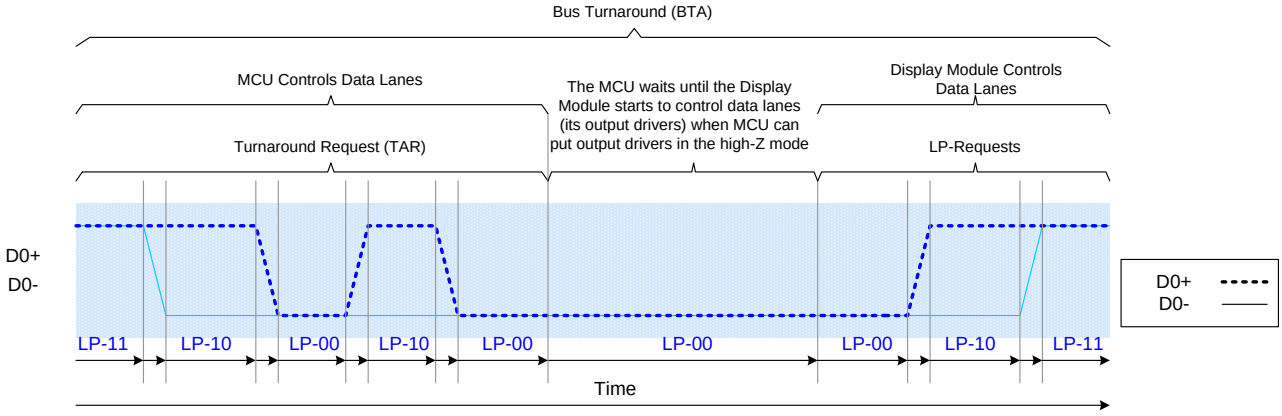


Figure 34. Bus Turnaround Procedure

MCU and display module terms are switched on the chapter " 4.3.3.2.2.2 Acknowledge with Error Report (AwER)", if the Bus Turnaround (BTA) is from the display module to the MCU.

4.3.3. Packet Level Communication

4.3.3.1. Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes [Note].

The lengths of the packets are

• Short Packet (SPa): 4 bytes

• Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

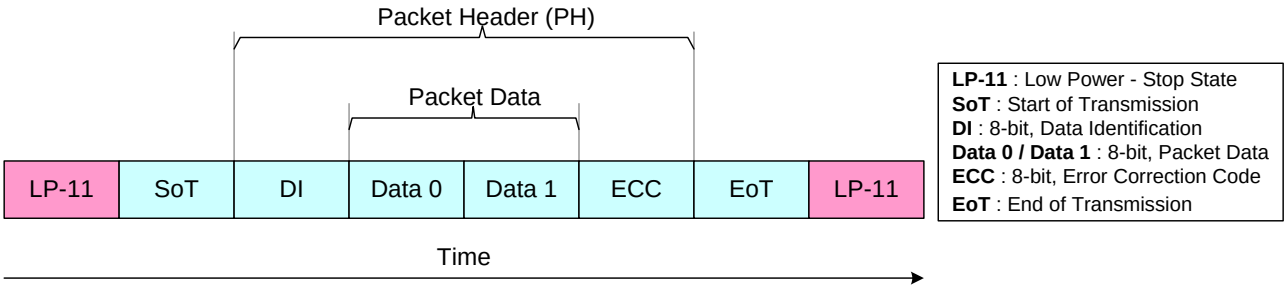


Figure 35. Short Packet (SPa) Structure

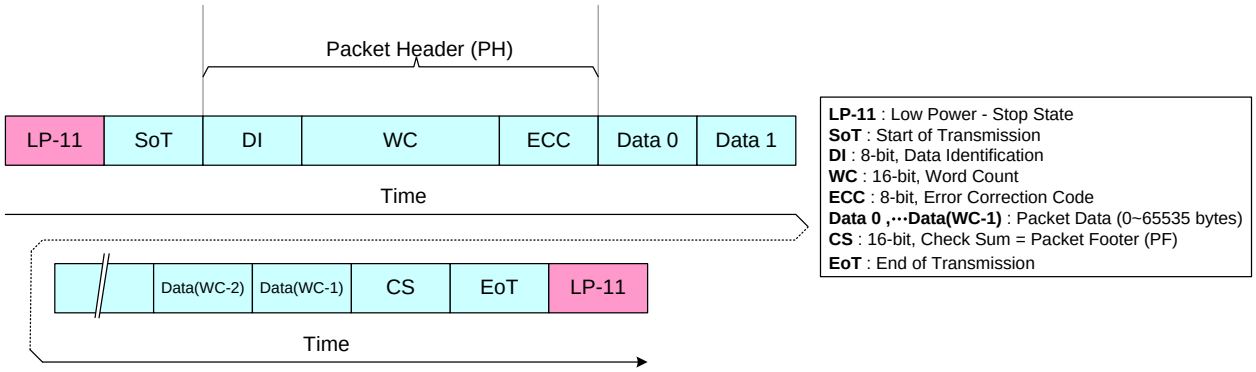


Figure 36. Long Packet (LPa) Structure

Note:
Short Packet (SPa) and Long Packet (LPa) are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).
The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

- LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

4.3.3.1.1. Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.

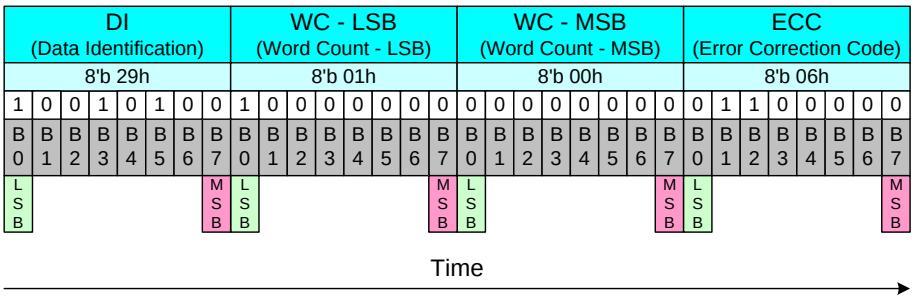


Figure 37. Bit Order of the Byte on Packets

4.3.3.1.2. Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

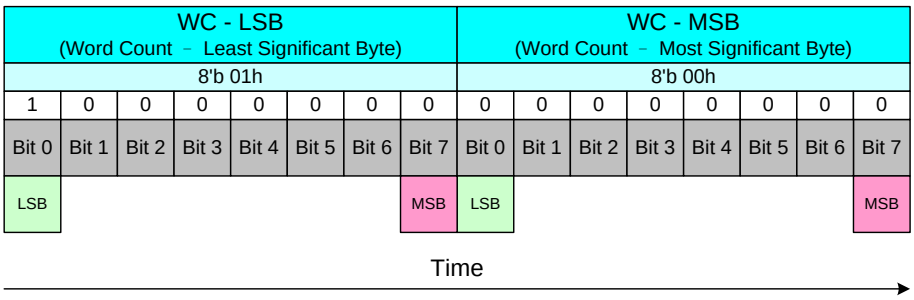


Figure 38. Byte Order of the Multiple Byte Information on Packets

4.3.3.1.3. Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

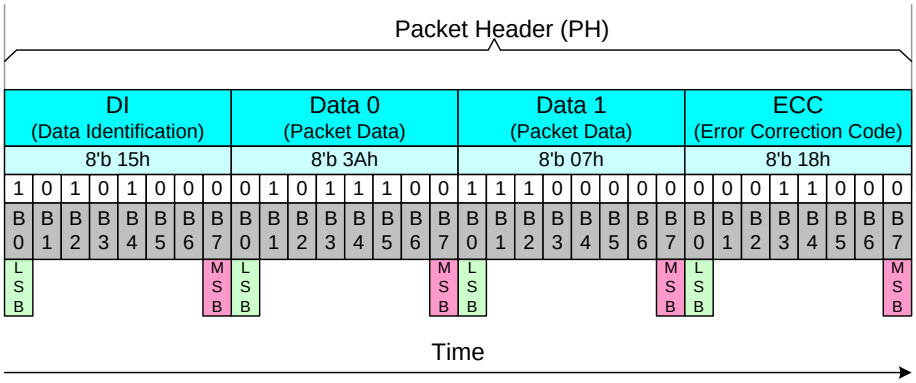


Figure 39. Packet Header (PH) on Short Packet (SPa)

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

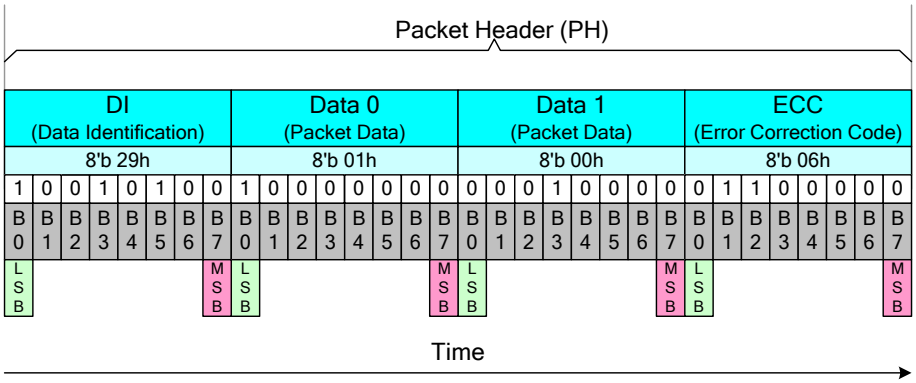


Figure 40. Packet Header (PH) on Long Packet (LPa)

4.3.3.1.3.1. Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated, see figure below.

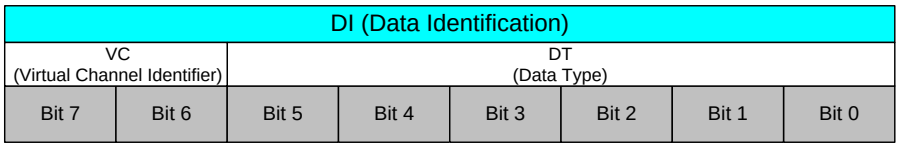


Figure 41. Data Identification (DI) Structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

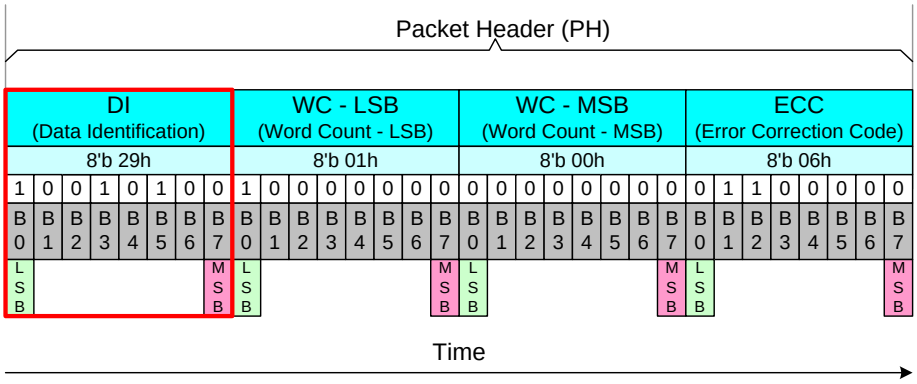


Figure 42. Data Identification (DI) on the Packet Header (PH)

4.3.3.1.3.1.1. Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

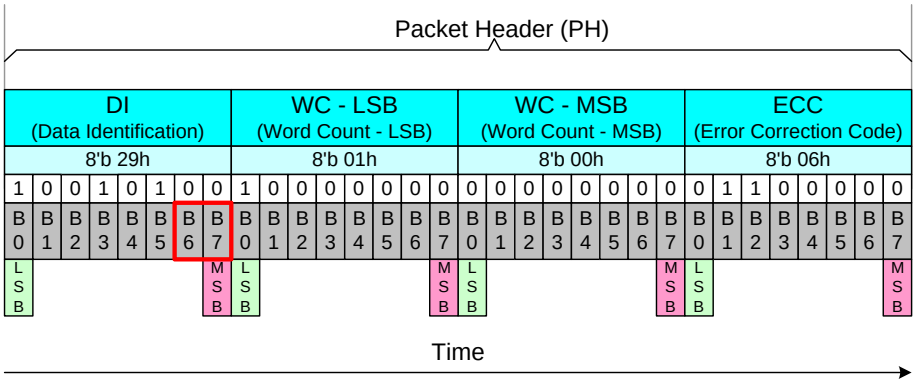


Figure 43. Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules.

Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.

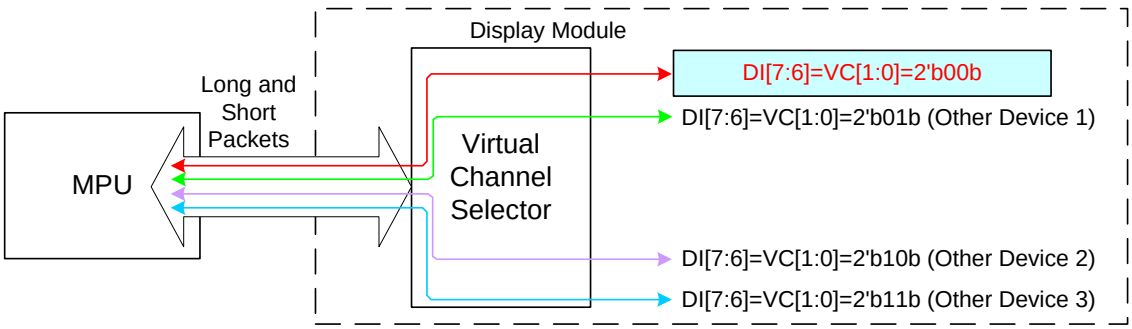


Figure 44. Virtual Channel (VC) Configuration

Virtual Channel (VC) is always 0 (DI[7..6]=VC[1..0]=00_b) when the MCU is sending “End of Transmission Packet” to the display module. See chapter “4.3.3.2.1.9. End of Transmission Packet (EoTP)”.

This display module is not supporting the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC[1..0]) is 00b for this display module.

4.3.3.1.3.1.2. Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

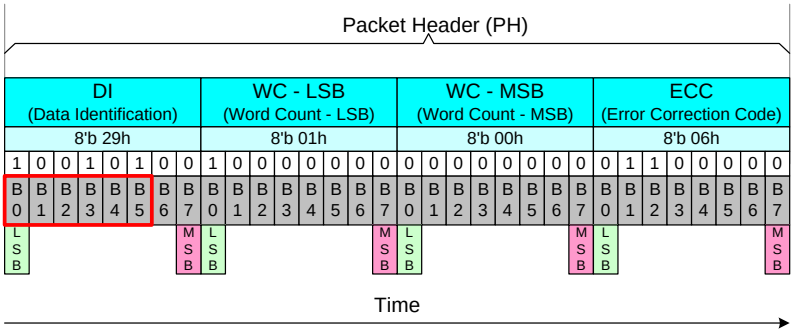


Figure 45. Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa).

Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Table 7. Data Type (DT) from the MCU to the Display Module

From the MCU to the Display Module									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviation
0	0	1	0	0	0	08	End of Transmission Packet Note 1	SPa (Short Packet)	EoTP
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)	DCSWN-S
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)	DCSW1-S
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)	DCSRN-S
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)	SMRPS-S
0	0	1	0	0	1	09	Null Packet, No Data Note 2	LPa (Long Packet)	NP-L
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)	DCSW-L

Note 1. This can be used when the MCU wants to secure that there is the end of the transmission in High Speed Data Transferring (HSDT) mode.

Note 2. This can be used when data lanes are wanted to keep in High Speed Data Transferring (HSDT) Mode.

Table 8. Data Type (DT) from the Display Module to the MCU

From the Display Module to the MCU									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviation
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)	AwER
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)	DCSRR-L
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)	DCSRR1-S
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)	DCSRR2-S

The receiver is ignored other Data Type (DT) if they are not defined on tables: “Table 9. Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “Table 10. Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

4.3.3.1.3.2. Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet Data (PD) sent after the Packet Header (PH).

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)

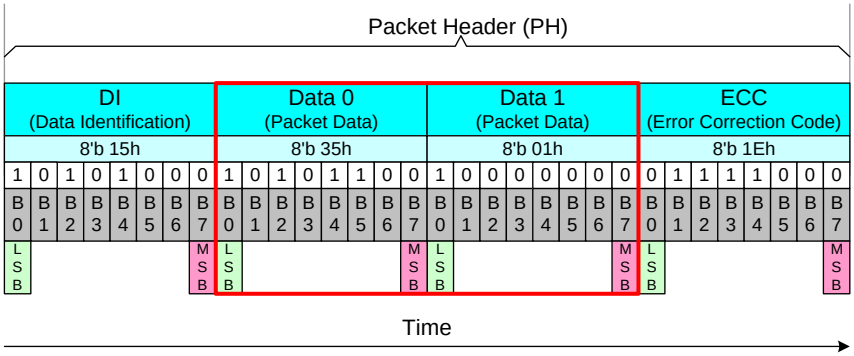


Figure 46. Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

- Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)

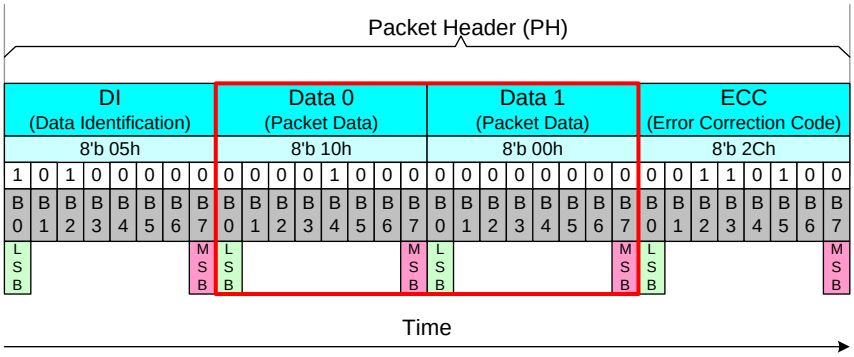


Figure 47. Packet Data (PD) for Short Packet (SPa), 1 Byte Information

4.3.3.1.3.3. Word Count (WC) on the Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

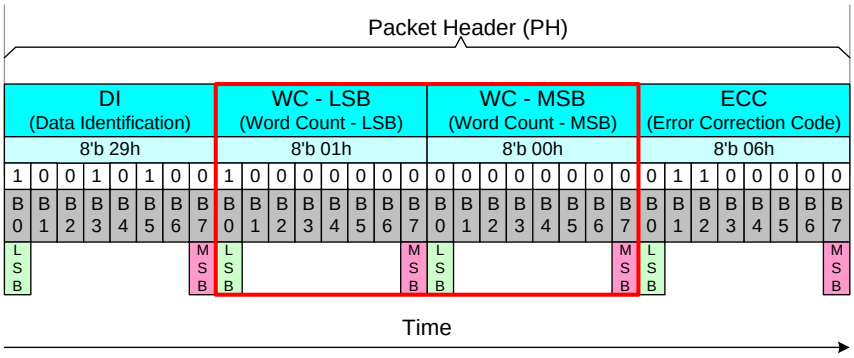


Figure 48. Word Count (WC) on the Long Packet (LPa)

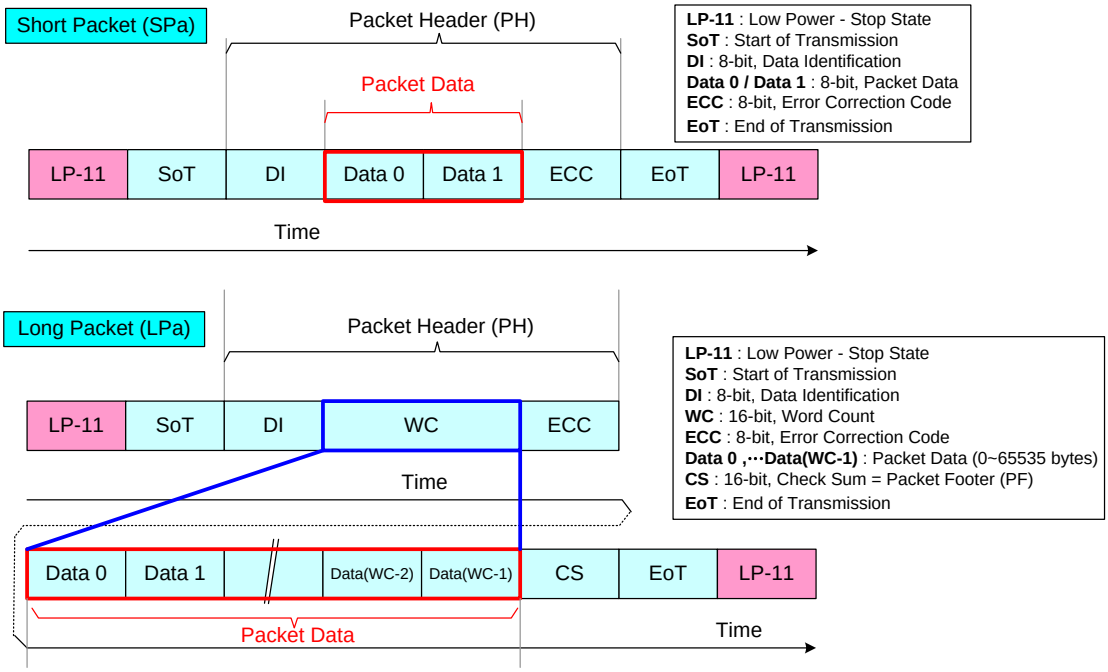


Figure 49. Packet Data in Short and Long Packets

4.3.3.1.3.4. Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors. The ECC protects the following fields:

• Short Packet (SPa): Data Identification (DI) byte (8 bits: D[0…7]), Packet Data (PD) bytes (16 bits: D[8…23]) and ECC (8 bits: P[0…7])

• Long Packet (LPa): Data Identification (DI) byte (8 bits: D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits: P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.

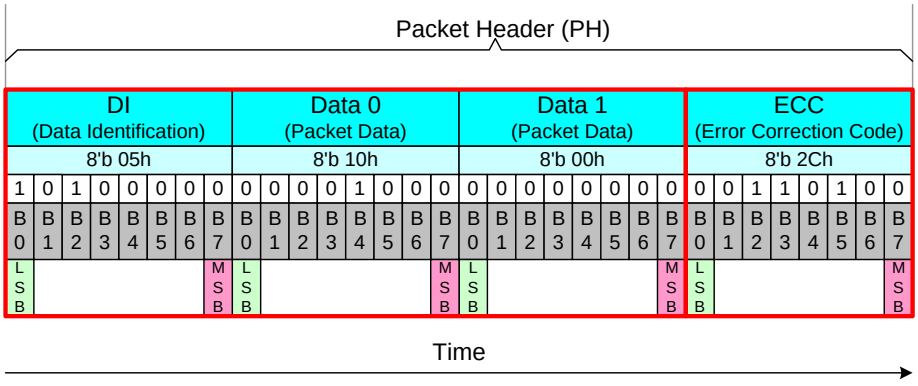


Figure 50. D[23…0] and P[7…0] on the Short Packet (SPa)

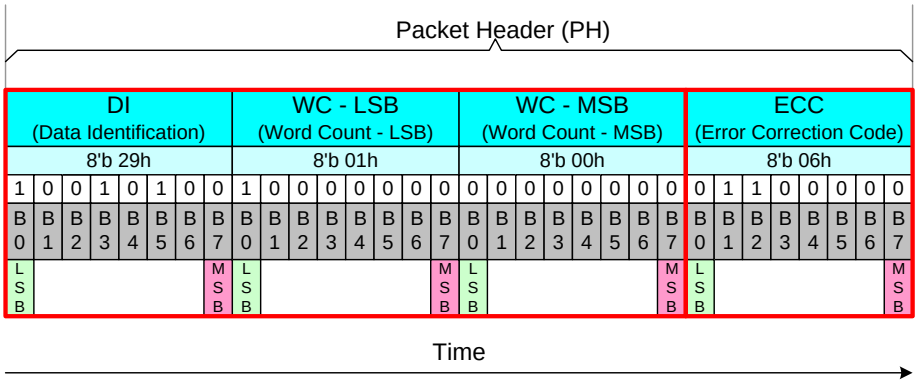


Figure 51. D[23…0] and P[7…0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

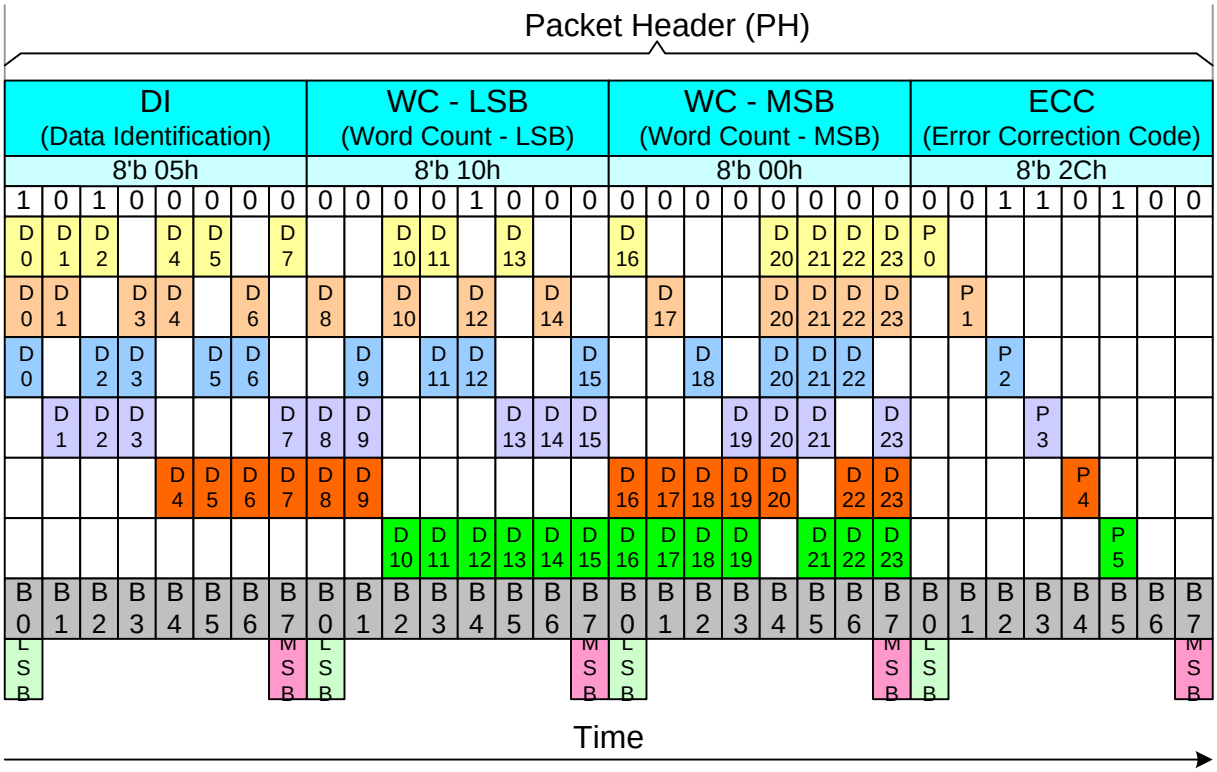


Figure 52. XOR Functionality on the Short Packet (SPa)

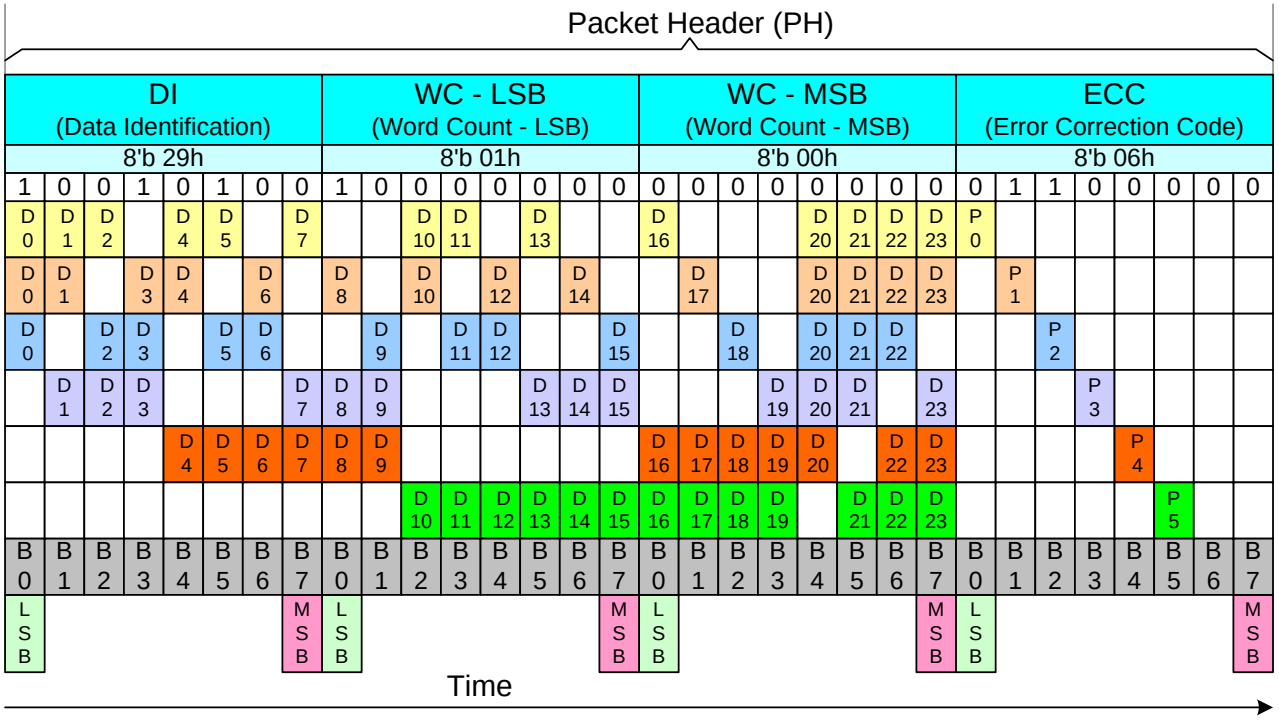


Figure 53. XOR Functionality on the Long Packet (LPa)

The transmitter (The MCU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

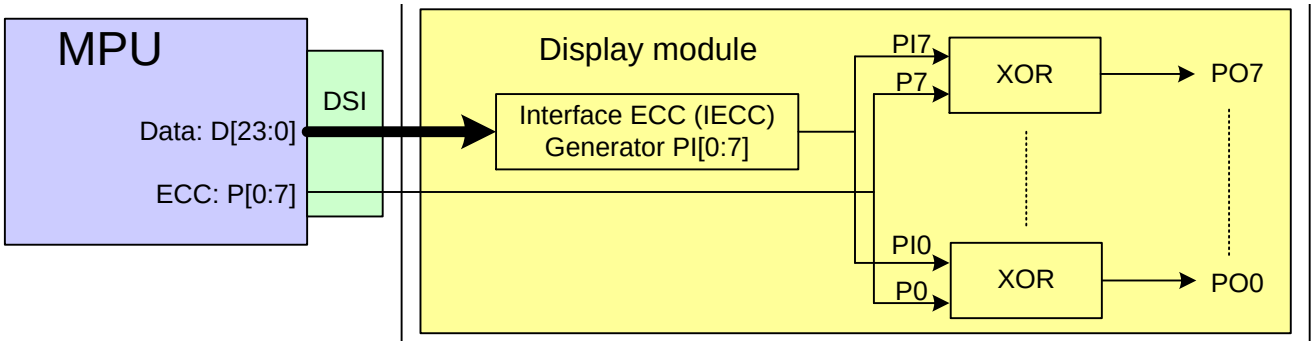


Figure 54. Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h.

The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7…0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L							M	
	S							S	
	B							B	

Figure 55. Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC, IECC) => PO[7…0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L							M	
	S							S	
	B							B	

Figure 56. Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

Table 9. One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7…0] is on Table 9 : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO[7…0] = 0Eh
- The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on Table 9: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

4.3.3.1.4. Packet Data (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa).
The number of the data bytes is defined on chapter “4.3.3.1.3.3. Word Count (WC) on the Long Packet (LPa)”.

4.3.3.1.5. Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa).
The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).
The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

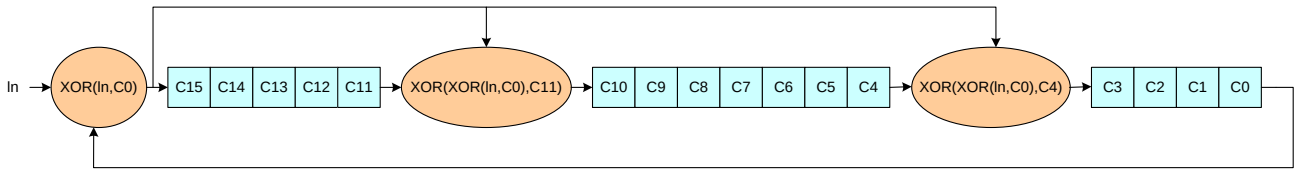
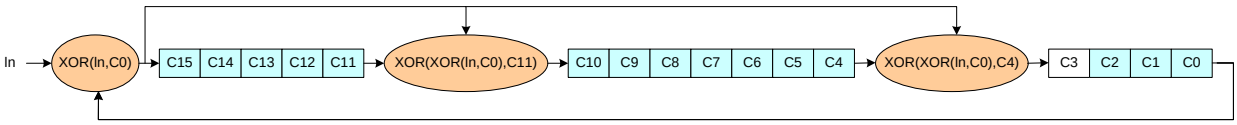


Figure 57. 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.
The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).
An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

Figure 58. CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.

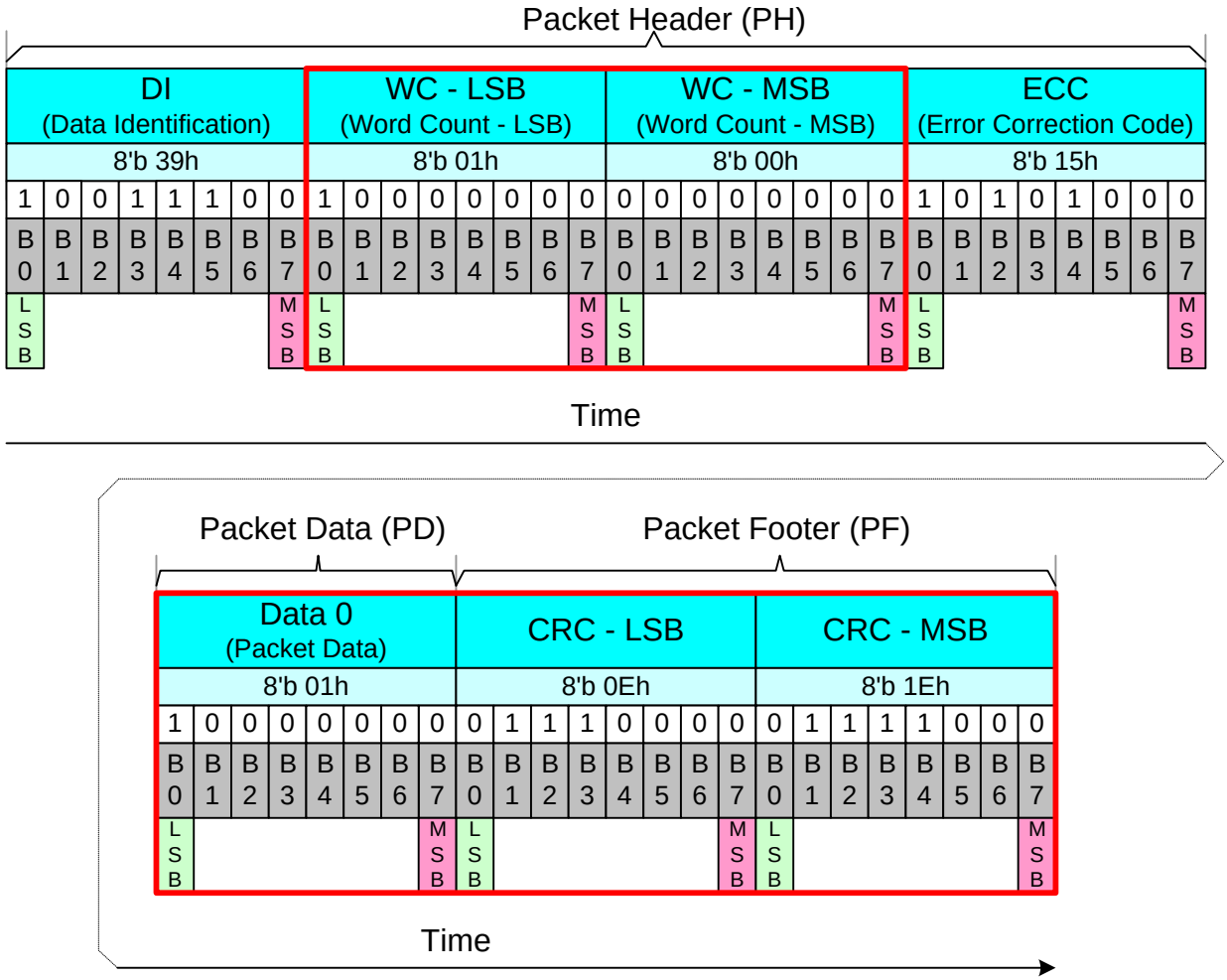


Figure 59. Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

4.3.3.2. Packet Transmissions

4.3.3.2.1. Packet from the MCU to the Display Module

4.3.3.2.1.1. Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter "5.6. User Command Description" is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

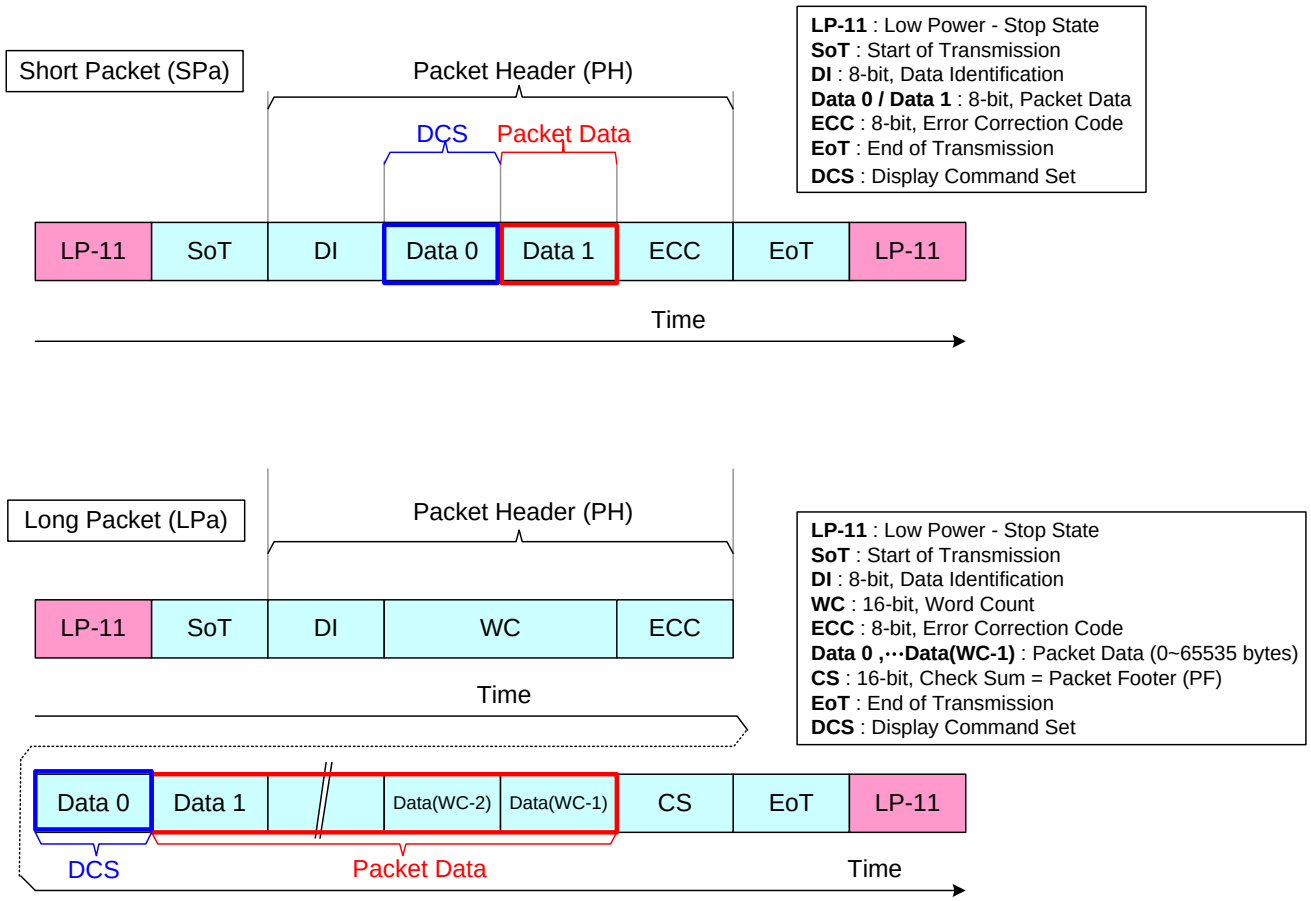


Figure 60. Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

4.3.3.2.1.2. Display Command Set (DCS) Write, No Parameter (DCSWN-S)

"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to the display module. These commands are defined on a table below.

(See chapter "5.6. User Command Description")

Table 10. Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Page 0 Command
NOP (00h)
Software Reset (01h)
Sleep In(10h)
Sleep Out (11h)
Normal Display Mode On (13h)
Display Inversion Off (20h) (Reserved for ILITEK)
Display Inversion On (21h) (Reserved for ILITEK)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display ON (29h)
Memory Write (2Ch) (only used for GRAM test)
Tearing Effect Line OFF (34h)
Idle Mode Off (38h)
Idle Mode On (39h)
Stop Transition (59h)

Note: No Subpixel has been written

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 00 0101b

• Packet Data (PD)

o Data 0: "Sleep In (10h)", Display Command Set (DCS)

o Data 1: Always 00hex

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

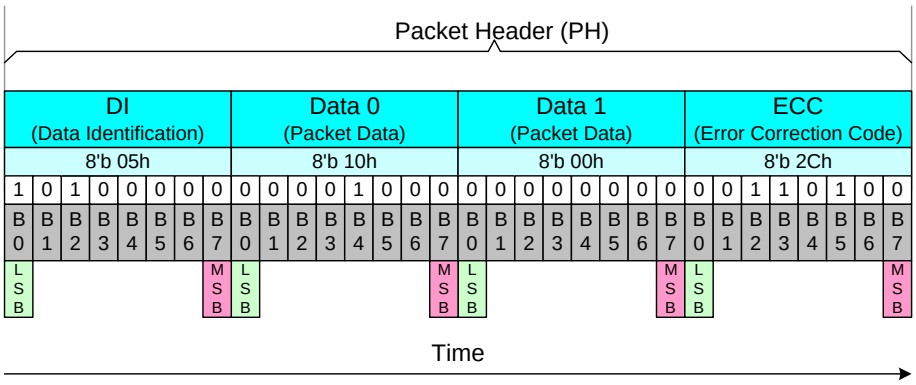


Figure 61. Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

4.3.3.2.1.3. Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to the display module. These commands are defined on a table (See chapter "5.6. User Command Description") below.

Table 11. Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

Page 0 Command
Gamma Set (26h)
Memory Write (2Ch) (only used for GRAM test)
Tearing Effect Line Onl (35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch) (only used for GRAM test)
Write CTRL Display (53h)
Write Content Adaptive Brightness control (55h)
Write CABC Minimum Brightness (5Eh)

Note: Any used MIPI DCS commands should be appended to the table also

Short Packet (SPa) is defined e.g.

- Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 01 0101b

- Packet Data (PD)

o Data 0: "Gamma Set (26h)", Display Command Set (DCS)

o Data 1: 01hex, Parameter of the DCS

- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

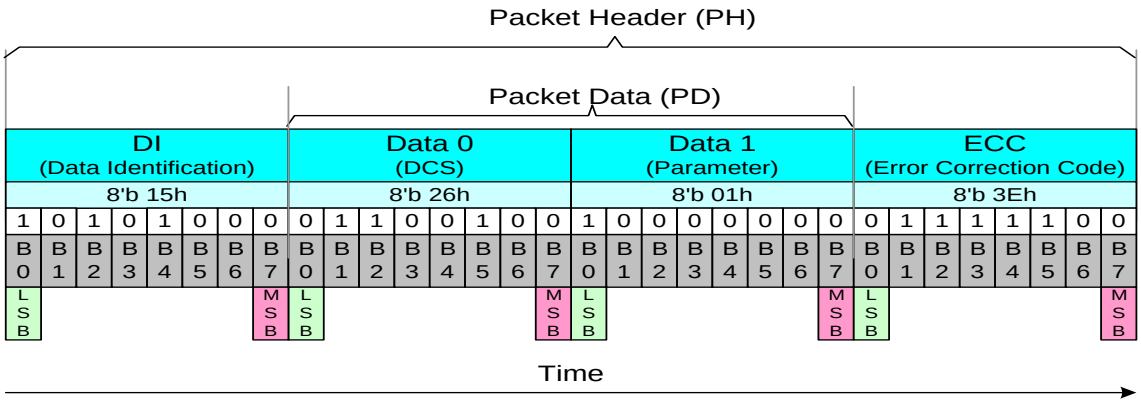


Figure 62. Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

4.3.3.2.1.4. Display Command Set (DCS) Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "5.6. User Command Description") below.

Table 12. Display Command Set (DCS) Write Long (DCSW-L)

Command
NOP (00h) Note 1
Software Reset (01h) Note 1
Sleep In(10h) Note 1
Sleep Out (11h) Note 1
Normal Display Mode On (13h) Note 1
Display Inversion Off (20h) Note 1 (Reserved for ILITEK)
Display Inversion On (21h) Note 1 (Reserved for ILITEK)
All Pixel Off (22h) Note 1
All Pixel On (23h) Note 1
Gamma Set (26h) Note 2
Display Off (28h) Note 1
Display ON (29h) Note 1
Memory Write (2Ch) Note 2 (only used for GRAM test)
Tearing Effect Line Off (34h) Note 1
Tearing Effect Line On (35h) Note 2
Memory Access Control (36h) Note 2
Idle Mode Off (38h) Note 1
Idle Mode On (39h) Note 1
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch) Note 2 (only used for GRAM test)
Set_tear_scanline (44h)
Write Display Brightness (51h)
Write CTRL Display (53h) Note 2
Write Content Adaptive Brightness control (55h) Note 2
Stop Transition (59h) Note 1
Write CABC Minimum Brightness (5Eh) Note 2
Set Transition Time (68h)

Note 1. Also Short Packet (SPa) can be used. See chapter "4.3.3.2.1.2. Display Command Set (DCS) Write, No Parameter".

Note 2. Also Short Packet (SPa) can be used. See chapter "4.3.3.2.1.3. Display Command Set (DCS) Write, 1 Parameter".

Note 3. Any used MIPI DCS commands should be appended to the table also.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

o Word Count (WC): 0001h

• Error Correction Code (ECC)

• Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

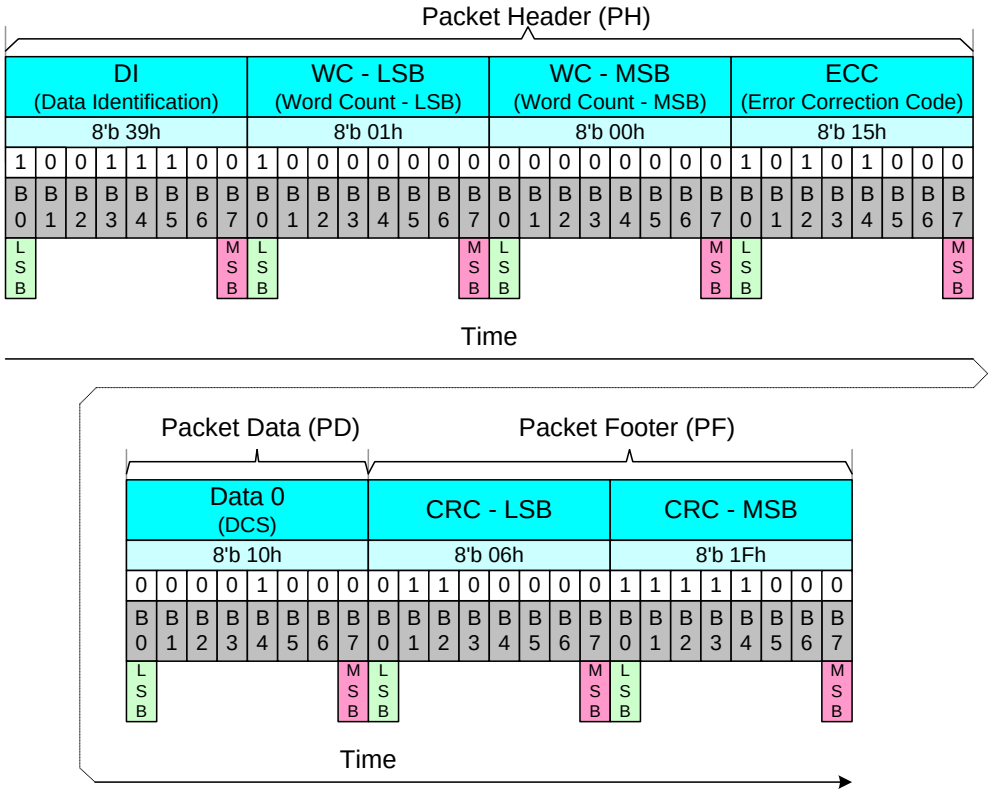


Figure 63. Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

o Word Count (WC): 0002h

• Error Correction Code (ECC)

• Packet Data (PD):

o Data 0: “Display Access Control (26h)”, Display Command Set (DCS)

o Data 1: 01hex, Parameter of the DCS

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

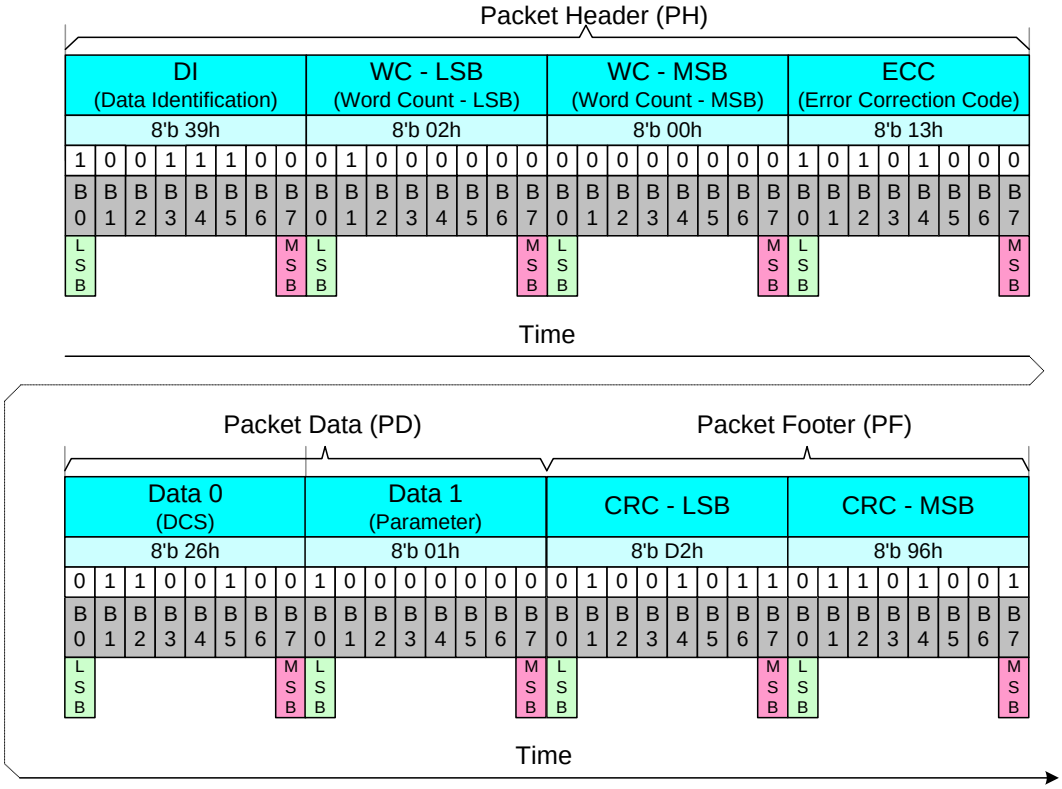


Figure 64. Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

o Word Count (WC): 0005h

• Error Correction Code (ECC)

• Packet Data (PD):

o Data 0: “Column Address Set (2Ah)”, Display Command Set (DCS)

o Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15…8]

o Data 2: 12hex, 2nd Parameter of the DCS, Start Column EC[7…0]

o Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15…8]

o Data 4: EFhex, 4th Parameter of the DCS, End Column EC[7…0]

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

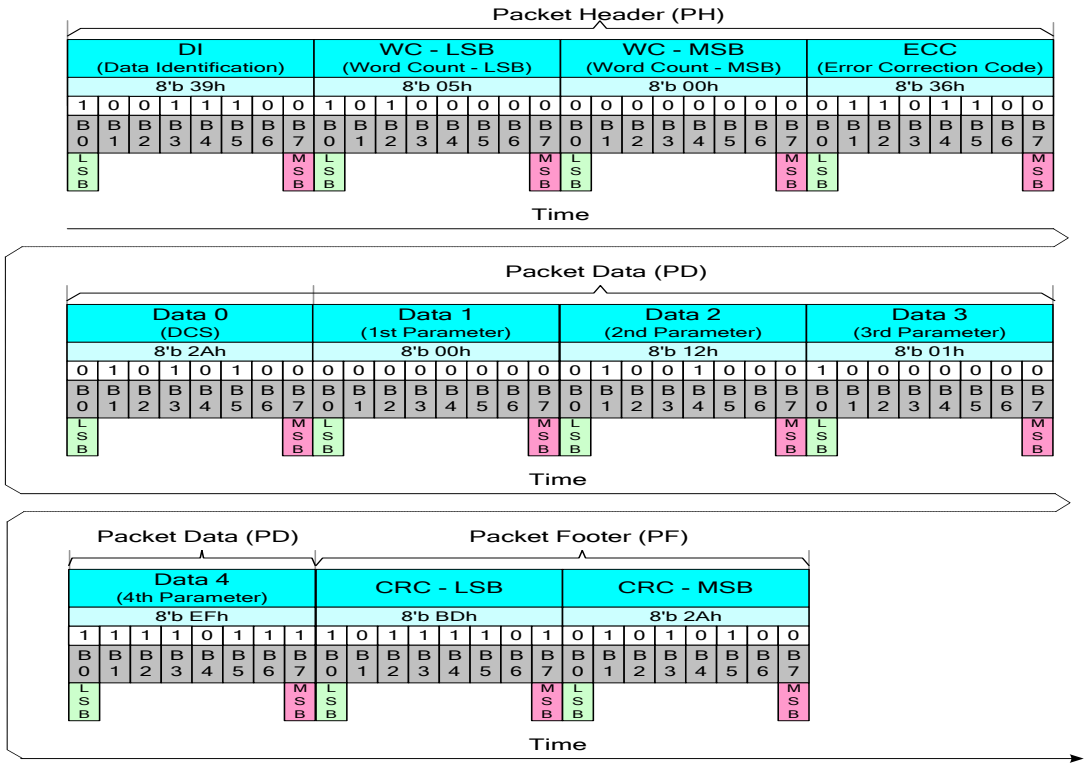


Figure 65. Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

4.3.3.2.1.5. Display Command Set (DCS) Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to the display module. These commands are defined on a table (See chapter "5.6. User Command Description") below.

Table 13. Display Command Set (DCS) Read, No Parameter (DCSRN-S)

Page 0 Command
Read Number of the Errors on DSI (05h)
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Memory Read (2Eh) (only used for GRAM test)
Memory Read Continue (3Eh) (only used for GRAM test)
Get Tear Scan Line (45h)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Content Adaptive Brightness Control (56h)
Read CABC Minimum Brightness (5Fh)
Get Transition Time (69h)
Read DDB Start (A1h)
Read DDB Continue (A8h)
Read First Checksum (AA)h
Read Continue Checksum (AFh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

4.3.3.2.1.6. Display Command Set (DCS) Read Long (DCSR-L)

"Display Command Set (DCS) Read, No Parameter" (DCSR-L) is always using a Long Packet (SPa), defined on Data Type (DT, 01 1100b), from the MCU to the display module. These commands are defined on a table (See chapter "5.6. User Command Description") below.

Table 14. Display Command Set (DCS) Read Long (DCSR-L)

Page 0 Command
Memory Read (2Eh) (only used for GRAM test)
Memory Read Continue (3Eh) (only used for GRAM test)
Get Tear Scan Line (45h)
Read Display Brightness Value (52h)
Read CABC Minimum Brightness (5Fh)
Get Transition Time (69h)
Read DDB Start (A1h)
Read DDB Continue (A8h)

4.3.3.2.1.7. Seat Maximum Return Packet Size (SMRPS)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

• The MCU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 11 0111b

• Maximum Return Packet Size (MRPS)

o Data 0: 01hex

o Data 1: 00hex

• Error Correction Code (ECC)

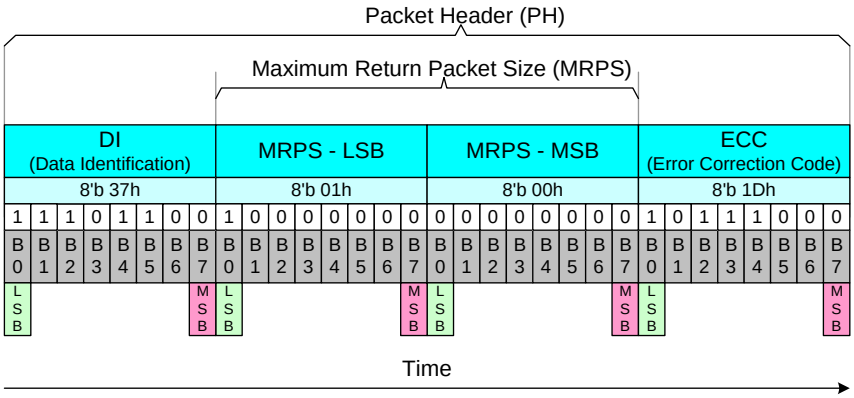


Figure 66. Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

• The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to the display module

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 00 0110b

• Packet Data (PD)

o Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)

o Data 1: Always 00hex

• Error Correction Code (ECC)

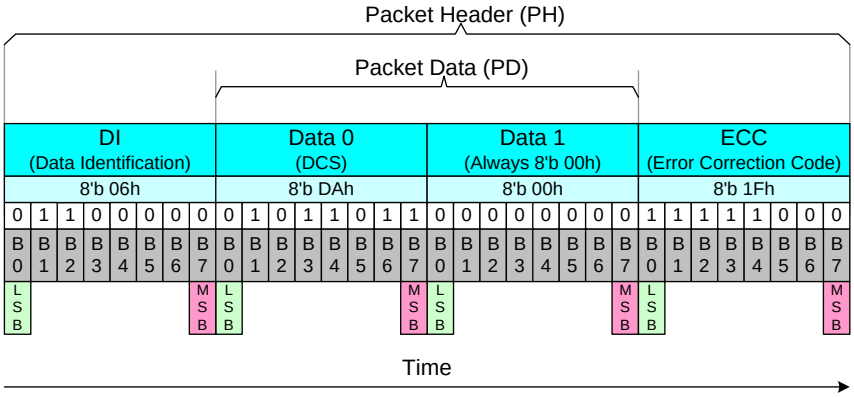


Figure 67. Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)
An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command, See chapter “4.3.3.2.2.2. Acknowledge with Error Report (AwER)”
Information of the received command. Short Packet (SPa) or Long Packet (LPa)

4.3.3.2.1.8. Null Packet, No Data (NP-L)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b), from the MCU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed.

The display module is ignored Packet Data (PD) what the MCU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

- Data Identification (DI)
  - o Virtual Channel (VC, DI[7…6]): 00b
  - o Data Type (DT, DI[5…0]): 00 1001b
- Word Count (WC)
  - o Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - o Data 0: 89hex (Random data)
  - o Data 1: 23hex (Random data)
  - o Data 2: 12hex (Random data)
  - o Data 3: A2hex (Random data)
  - o Data 4: E2hex (Random data)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

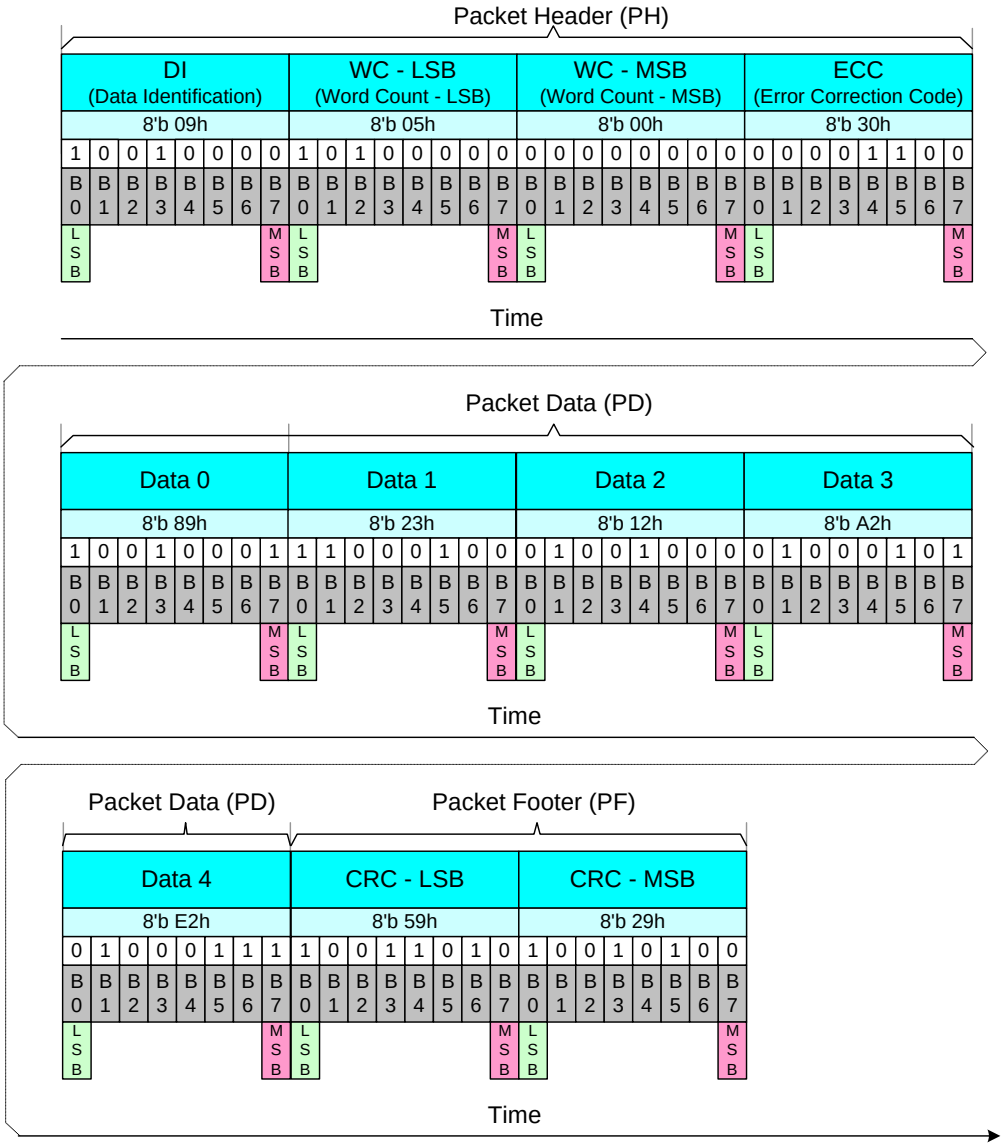


Figure 68. Null Packet, No Data (NP-L) - Example

4.3.3.2.1.9. End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 1000b), from the MCU to the display module. The purposes of this command is terminated the high Speed Data Transmission (HSDT) mode properly when there is added this extra packet after the last payload packet before "End of Transmission" (EoT), which is an interface level functionality.

The MCU can decide if it wants to use the "End of Transmission Packet" (EoTP) or not. The display shall have the capability to support both: i.e. If the MCU applies the EoTP, it shall report the "DSI Protocol Violation Error" when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module is or isn't receiving "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Mark-1" (= Leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send "End of Transmission Packet" (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode.

The summary of the receiving and transmitting EoTP is listed below.

Table 15. Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU => Display Module	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Module => MCU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

Short Packet (SPa) is using a fixed format as follows

- Data Identification (DI)
  - o Virtual Channel (VC, DI[7…6]): 00b
  - o Data Type (DT, DI[5…0]): 00 1000b
- Packet Data (PD)
  - o Data 0: 0Fhex
  - o Data 1: 0Fhex
- Error Correction Code (ECC)
  - o ECC: 01hex

This is defined on the Short Packet (SPa) as follows.

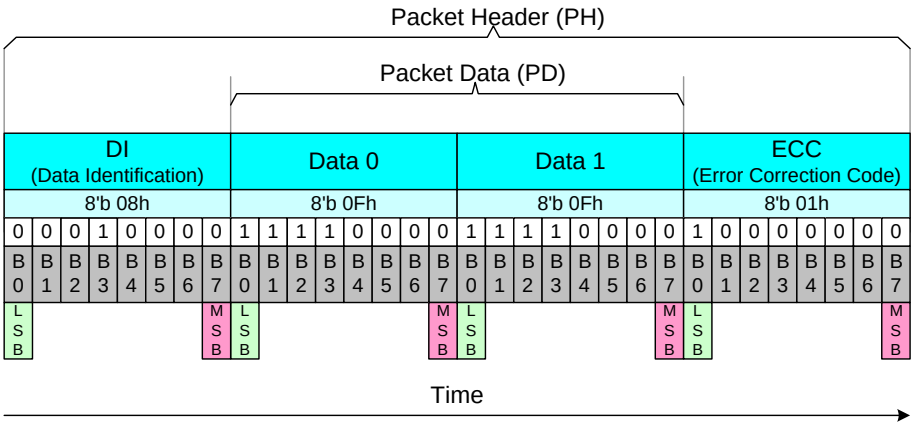


Figure 69. End of Transmission Packet (EoTP)

Some use cases of the “End of Transmission Packet” (EoTP) are illustrated only for reference purposes below.

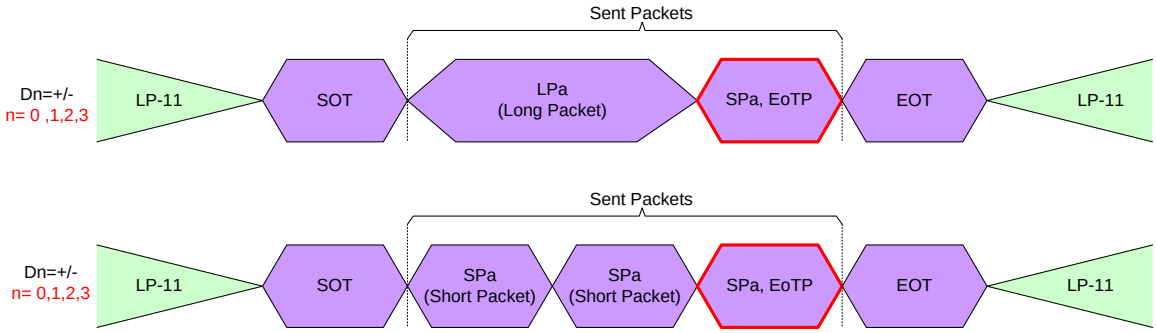


Figure 70. End of Transmission Packet (EoTP)-Examples

4.3.3.2.2. Packet from the Display Module to the MCU

4.3.3.2.2.1. Used Packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See chapter “4.3.3.2.1.5.Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See chapter: “4.3.3.2.2.2. Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined on Data Type (DT). See chapter “4.3.3.1.3.1.2. Data Type (DT)”. It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent in one packet.

Both cases are illustrated for reference purposes below.

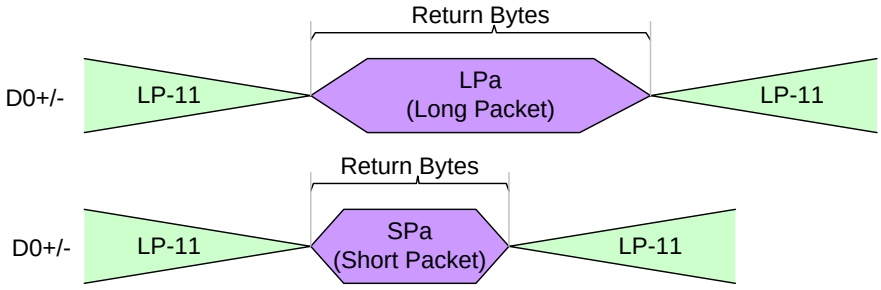


Figure 71. Return Bytes on Single Packet

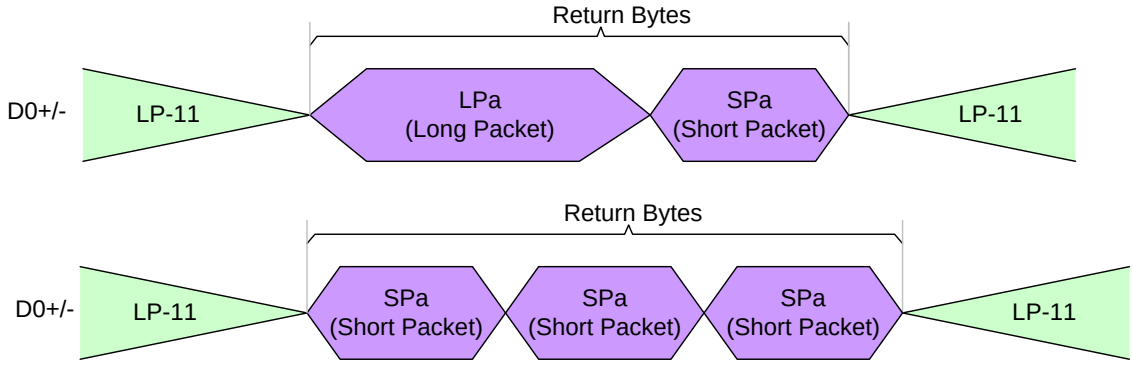


Figure 72. Return Bytes on Several Packets – Not Possible

Exception:

The display module is returning 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MCU when the display module has received a read command (See chapter "4.3.3.2.1.5. Display Command Set (DCS) Read, No Parameter (DCSRN-S)") where has been detected and corrected a single bit error by the EEC (See bit 8 on Table 19. Acknowledge with Error Report (AwER) for Short Packet (SPa) Response).

These return packets are illustrated for reference purposes below.

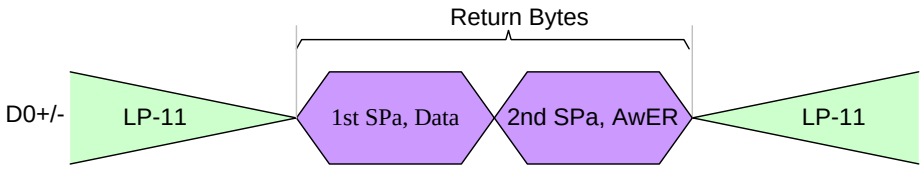


Figure 73. Exception when Return Bytes on Several Packets

AwER = Acknowledge with Error Report

4.3.3.2.2.2. Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU. The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

Table 16. Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Table 17. Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Reserved, Set to '0' internally, Only for Long Packet (LP)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

These errors are included from all packages what has been received from the MCU to the display module, before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 00 0010b

• Packet Data (PD)

o Bit 8: ECC Error, single-bit (detected and corrected)

o AwER: 0100h

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

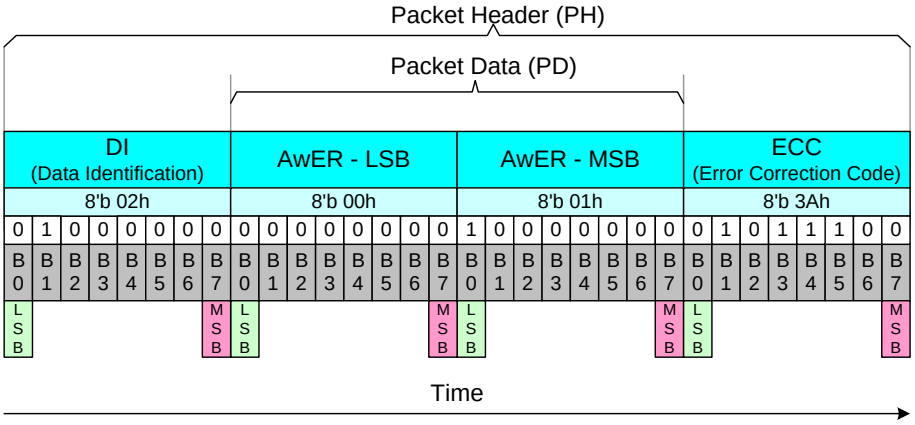


Figure 74. Acknowledge with Error Report (AwER) – Example

It is possible that the display module has received several packets, which have included errors, from the MCU before the MCU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

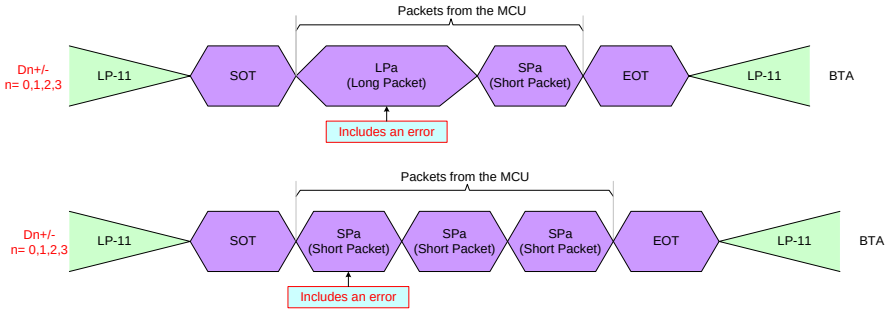


Figure 75. Errors Packets

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check Read Display Signal Mode (0Eh) command and Read Number of the Errors on DSI (05h) command. The bit D0 of the Read Display Signal Mode (0Eh) command has been set to '1' if a received packet includes an error.

The number of the packets, which are including an ***ECC or CRC*** error, are calculated on the RDNUMED register, which can read "Read Number of the Errors on DSI (05h)" command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the "Read Display Signal Mode (0Eh)" command to '0' after the MCU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.

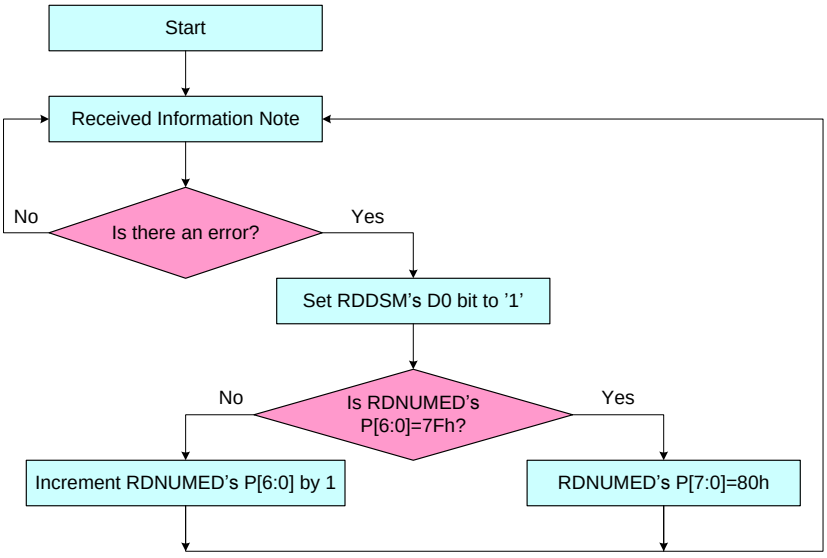


Figure 76. Flow Chart for Errors on DSI [Note]

Note:

1. This information can be Interface or Packet Level Communication but it is always from the MCU to the display module in this case.
2. CRC or ECC error

4.3.3.2.2.3. DCS Read Long Response (DCSRR-L)

"DCS Read Long Response" (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 011100b), from the display module to the MCU."DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module. Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
  - o Virtual Channel (VC, DI[7…6]): 00b
  - o Data Type (DT, DI[5…0]): 01 1100b
- Word Count (WC)
  - o Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - o Data 0: 89hex
  - o Data 1: 23hex
  - o Data 2: 12hex
  - o Data 3: A2hex
  - o Data 4: E2hex
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.

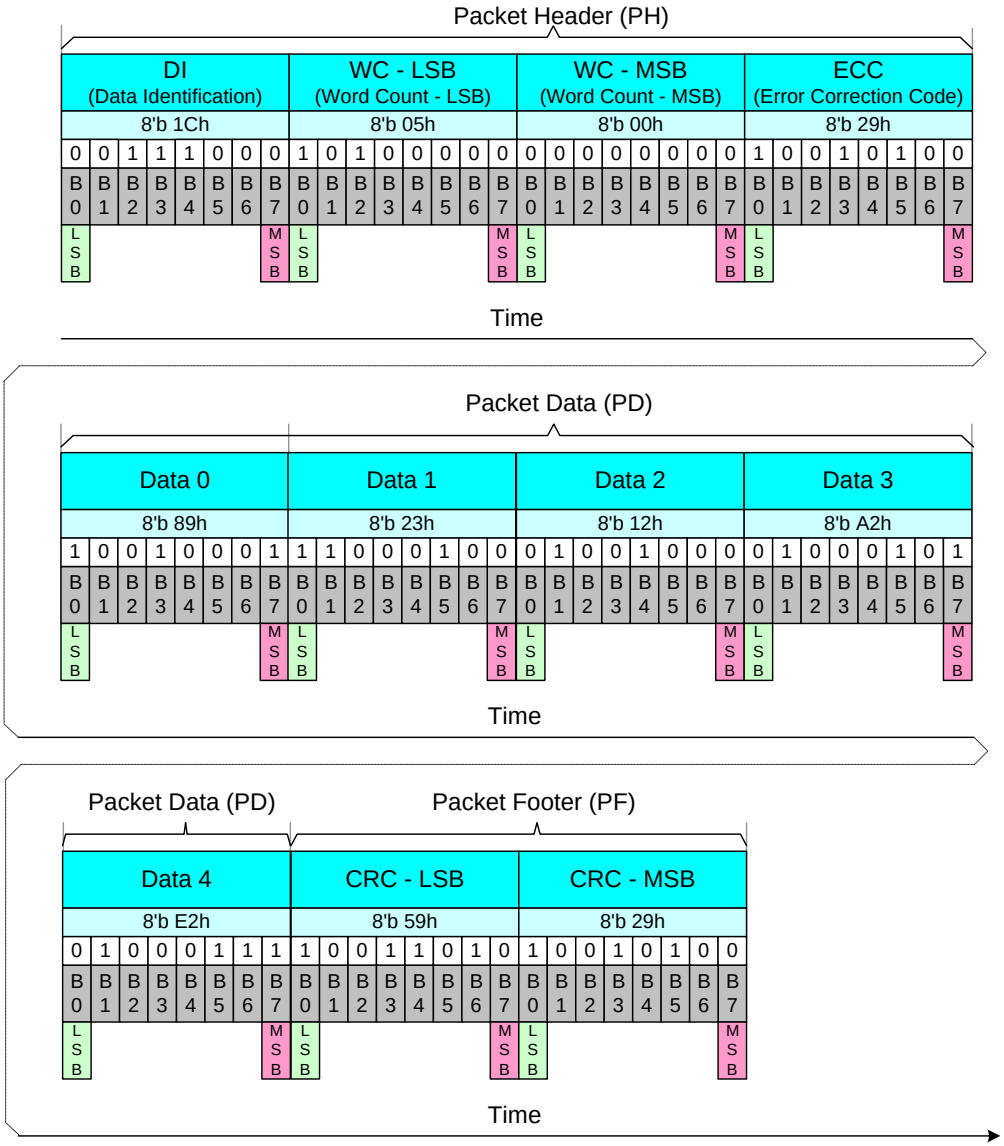


Figure 77. DCS Read Long Response (DCSRR-L) - Example

4.3.3.2.2.4. DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MCU."DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 10 0001b

- Packet Data (PD)

o Data 0: 45hex

o Data 1: 00hex (Always)

- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

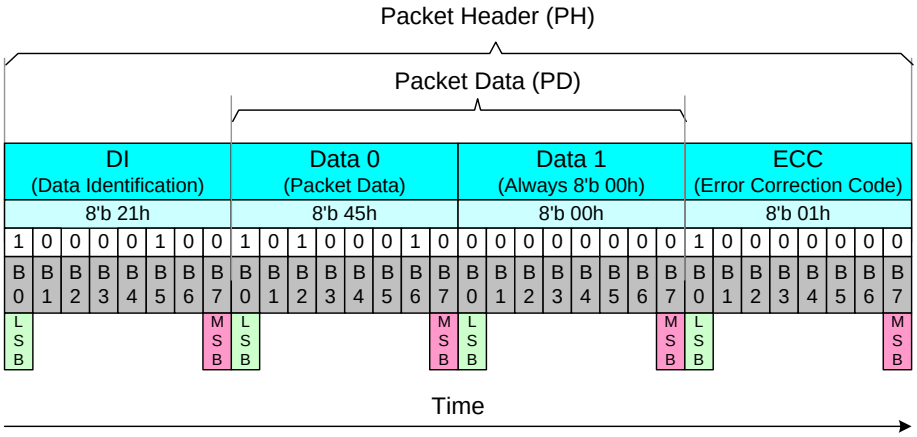


Figure 78. DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

4.3.3.2.2.5. DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MCU."DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 10 0010b

- Packet Data (PD)

o Data 0: 45hex

o Data 1: 32hex

- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

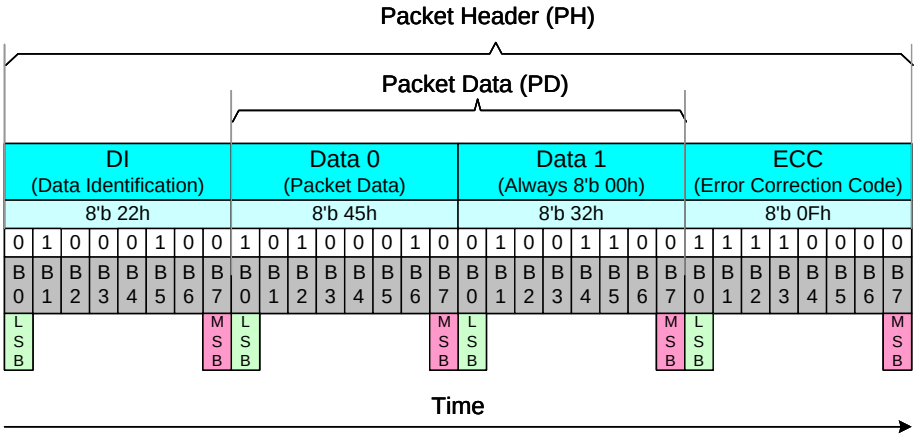


Figure 79. DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

4.3.3.3. Communication Sequences

4.3.3.3.1. General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See chapters “4.3.2. Interface Level Communication” and “4.3.3. Packet Level Communication”.
This communication sequence description is for DSI data lanes (DSI-Dn+/- ,n=0,1,2,3) and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically. See chapter “DSI-CLK Lanes”.
Function of the interface level communication is described on the following table.

Table 18. Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data Transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described on the following table.

Table 19. Packet Level Communication

Interface Mode	Abbreviation	Packet Size	Interface Action Description
MCU	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW-L	Long Packet	DCS Write Long
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data
	EoTP	Short Packet	End of Transmission Packet
Display Module	AwER	Short Packet	Acknowledge with Error Packet
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response
	DCSRR2-S	Short Packet	DCS Read Short Response

4.3.3.3.2. Sequences

4.3.3.3.2.1. DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" is defined on chapter "4.3.3.2.1.3. Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" and example sequences, how this packet is used, is described on following tables.

Table 20. DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 21. DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 22. DCS Write, 1 Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

4.3.3.3.2.2. DCS Write, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" is defined on chapter "4.3.3.2.1.2. Display Command Set (DCS) Write, No Parameter (DCSWN-S)" and example sequences, how this packet is used, is described on following tables.

Table 23. DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 24. DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 25. DCS Write, No Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

4.3.3.3.2.3. DCS Write Long Sequence

A Long Packet (LPa) of "Display Command Set (DCS) Write Long (DCSW-L)" is defined on chapter "4.3.3.2.1.4. Display Command Set (DCS) Write Long (DCSW-L)" and example sequences, how this packet is used, is described on following tables.

Table 26. DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 27. DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSRN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 28. DCS Write Long Sequence – Example 3

DCS Write Long Sequence – Example 3						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSRN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

4.3.3.3.2.4. DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined on chapter "4.3.3.2.1.5. Display Command Set (DCS) Read, No Parameter (DCSRN-S)" and example sequences, how this packet is used, is described on following tables.

Table 29. DCS Read, No Parameter Sequence – Example 1

DCS Read, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 1 byte
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	→	--	--	End

Table 30. DCS Read, No Parameter Sequence – Example 2

DCS Read, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 200 bytes
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response ID1(DAh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR-L	Response 200 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR-S	Response 200 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	→	--	--	End

4.3.3.3.2.5. Null Packet, No Data Sequence

A Long Packet (LPa) of "Null Packet, No Data (NP-L)" is defined on chapter "4.3.3.2.1.8. Null Packet, No Data (NP-L)" and an example sequence, how this packet is used, is described on the following table.

Table 31. Null Packet, No Data Sequence - Example

Null Packet, No Data Sequence – Example						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

4.3.3.3.2.6. End of Transmission Packet

A Short Packet (SPa) of "End of Transmission (EoTP)" is defined on chapter "4.3.3.2.1.9. End of Transmission Packet (EoTP)" and an example sequence, how this packet is used, is described on the following table.

Table 32. End of Transmission Packet – Example

End of Transmission Packet – Example						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

4.4. DSI transmission data format

4.4.1. 18-bit per Pixel, Long packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

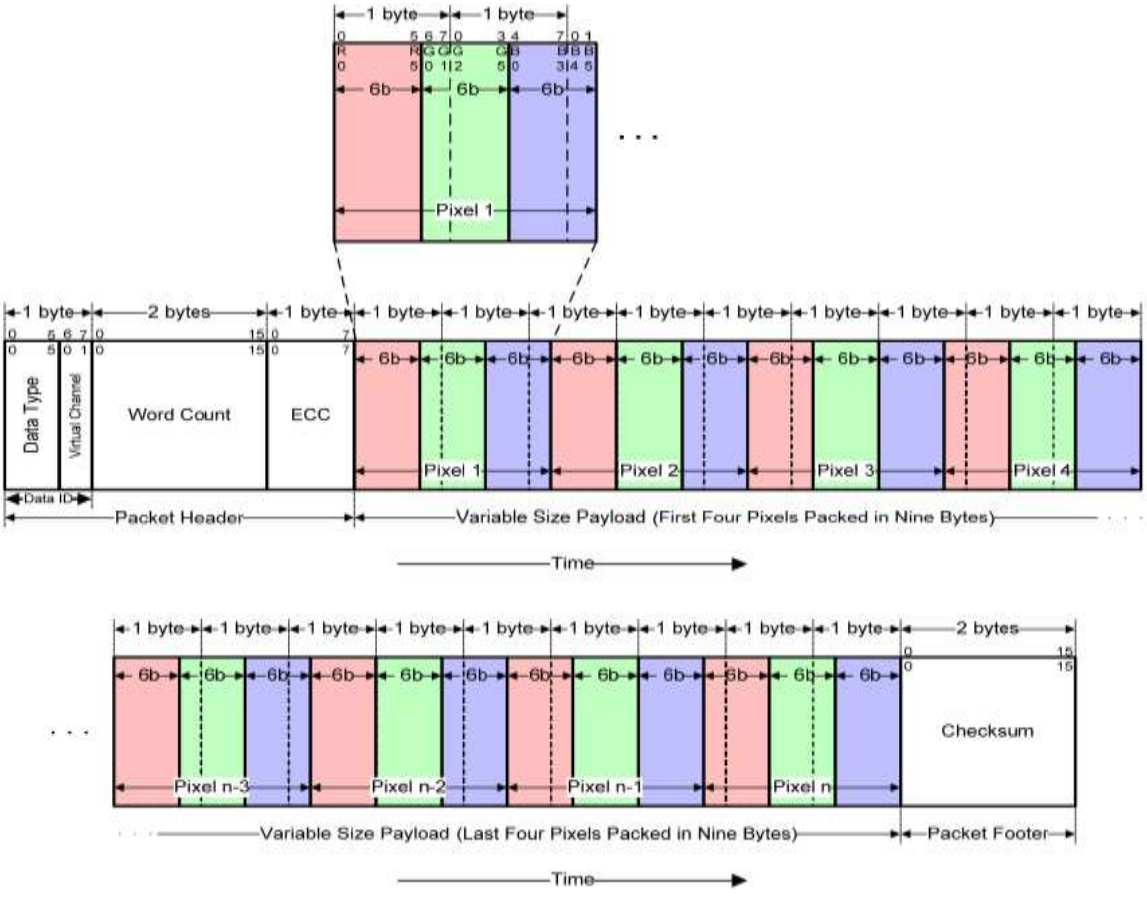


Figure 80. 18-bit per Pixel, Data Type = 01 1110 (1Eh)

4.4.2. 18-bit per Pixel, Long packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes, the total line width (displayed plus non-displayed pixels) should be a multiple of two pixels (six bytes).

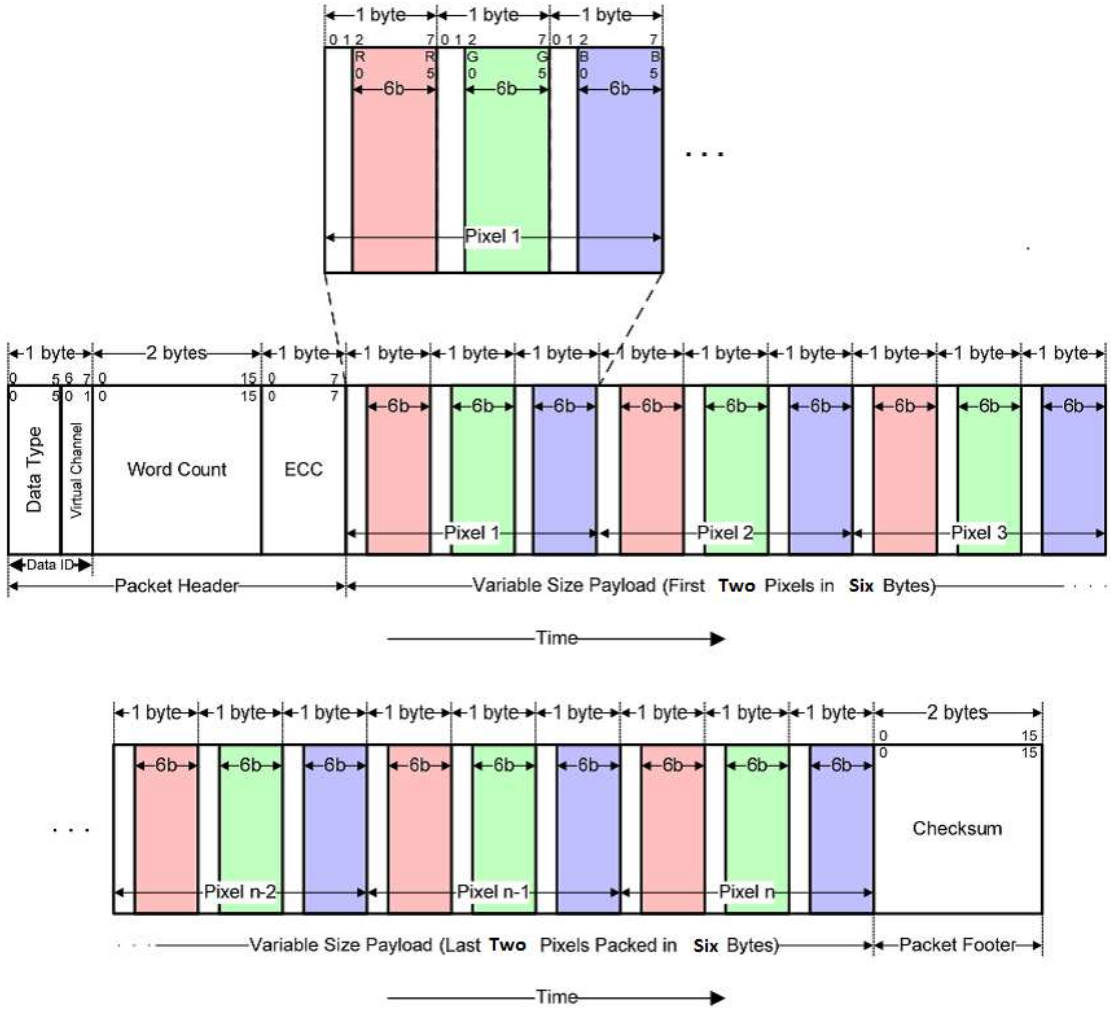


Figure 81. 18-bit per Pixel, Data Type = 10 1110 (2Eh)

4.4.3. 24-bit per Pixel, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes, the total line width (displayed plus non-displayed pixels) should be a multiple of two pixels (six bytes).

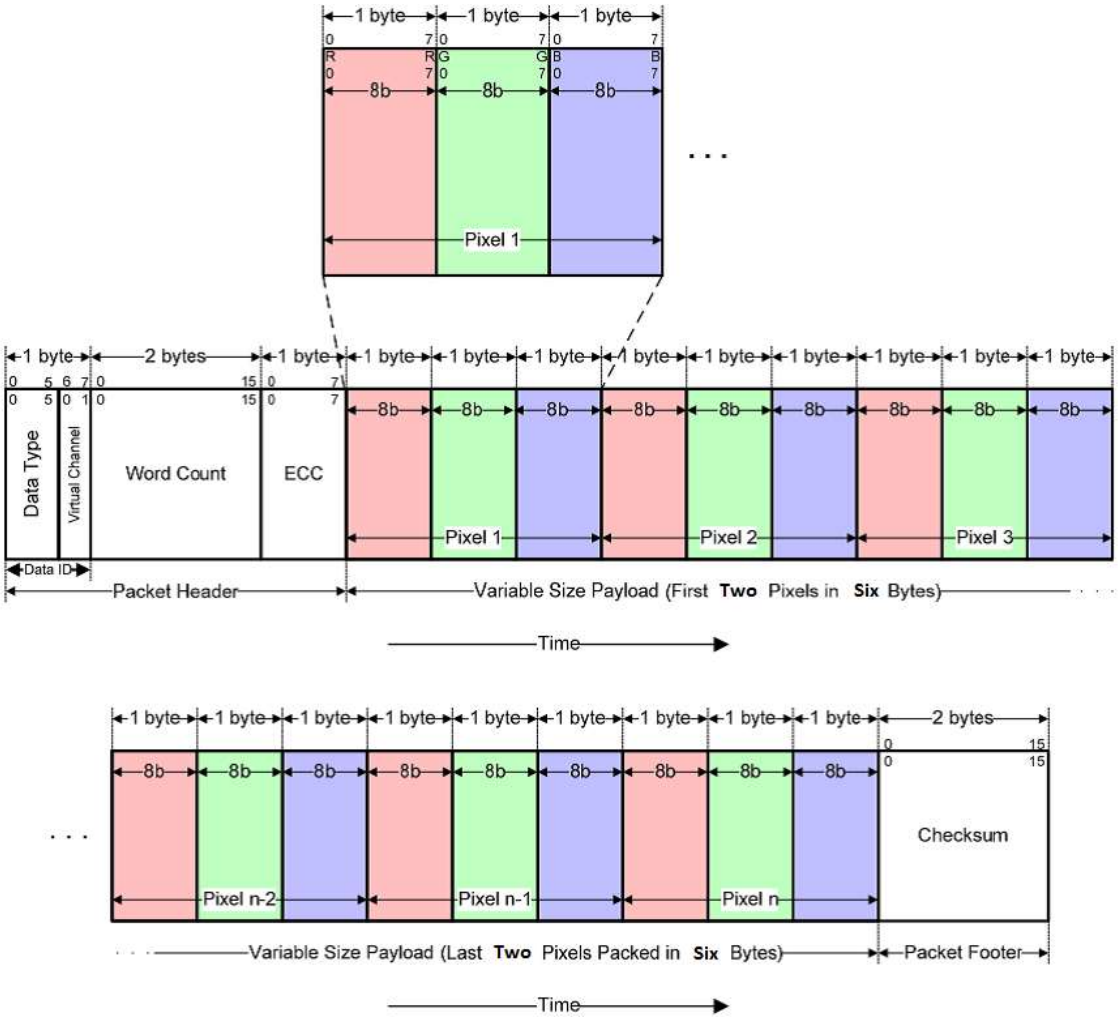


Figure 82. 24-bit per Pixel, Data Type = 11 1110 (3Eh)

4.4.4. 18-bit Color Data Mapping to 24-bit Pixel Data Operation

Table 33 lists settings for 24-bit data mapping. Set the bit EPF[1:0] of the Data Complement Setting register (Page 6 Cmd. 26h) that define three types of data formats for 24-bit data (pixel data r, g, b).

Table 33. 18-bit Color Data Mapping to 24-bit Pixel Data Operation

EPF[1:0]	Expand 18-bit color data (R,G,B) to 24-bit subpixel data (r, g, b)
00	"0" is written to the LSB. 8 bits subpixel, data r[7:0] = {18-bit color data R[5:0], 2'h0} 8 bits subpixel, data g[7:0] = {18-bit color data G[5:0], 2'h0} 8 bits subpixel, data b[7:0] = {18-bit color data B[5:0], 2'h0} (Note1): the data are converted as follows. If 18-bit color pixel data R[5:0] = 6'h3F, G[5:0] = 6'h3F and B[5:0] = 6'h3F, the 24-bit pixel data r, g, b[7:0] will be 24'hFFFFFF.
01	"1" is written to the LSB. 8 bits subpixel, data r[7:0] = {18-bit color data R[5:0], 2'h3} 8 bits subpixel, data g[7:0] = {18-bit color data G[5:0], 2'h3} 8 bits subpixel, data b[7:0] = {18-bit color data B[5:0], 2'h3} (Note2): the data are converted as follows. If 18-bit color pixel data R[5:0] = 6'h0, G[5:0] = 6'h0 and B[5:0] = 6'h0, the 24-bit pixel data r, g, b[7:0] will be 24'h000000
10 **(Default)**	The MSB value is written to the LSB. 8 bits subpixel, data r[7:0] = {18-bit color data R[5:0], R[5:4]} 8 bits subpixel, data g[7:0] = {18-bit color data G[5:0], G[5:4]} 8 bits subpixel, data b[7:0] = {18-bit color data B[5:0], B[5:4]}
11	Same as setting EPF[1:0] = 10

	Display Frame Pixel Data (24 bits)																							
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
24-bit	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
18-bit EPF[1:0]=00	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	0	0
18-bit EPF[1:0]=01	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	1	1
18-bit EPF[1:0]=10 or 11	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	R[5]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	B[5]	B[4]

For example 18-bit data mapping to 24-bit when EPF[1:0] = 10

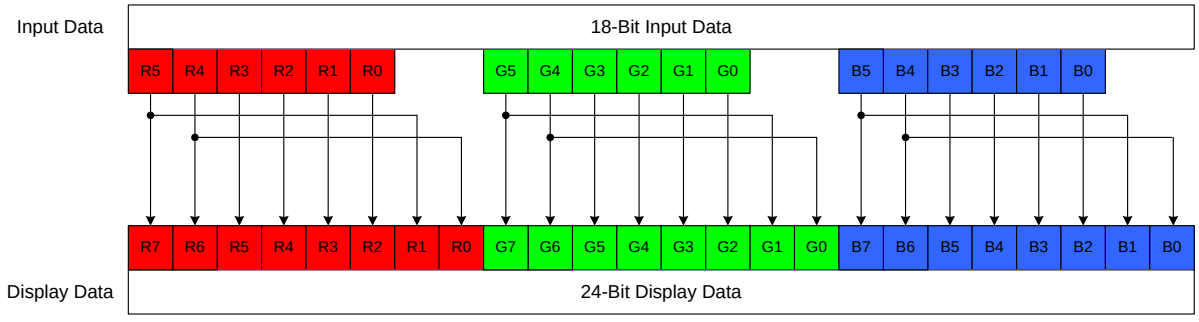


Figure 83. EPF[1:0] = 10 for 18-bit Data Mapping to 24 Bit

5. Command

5.1. Command Flow

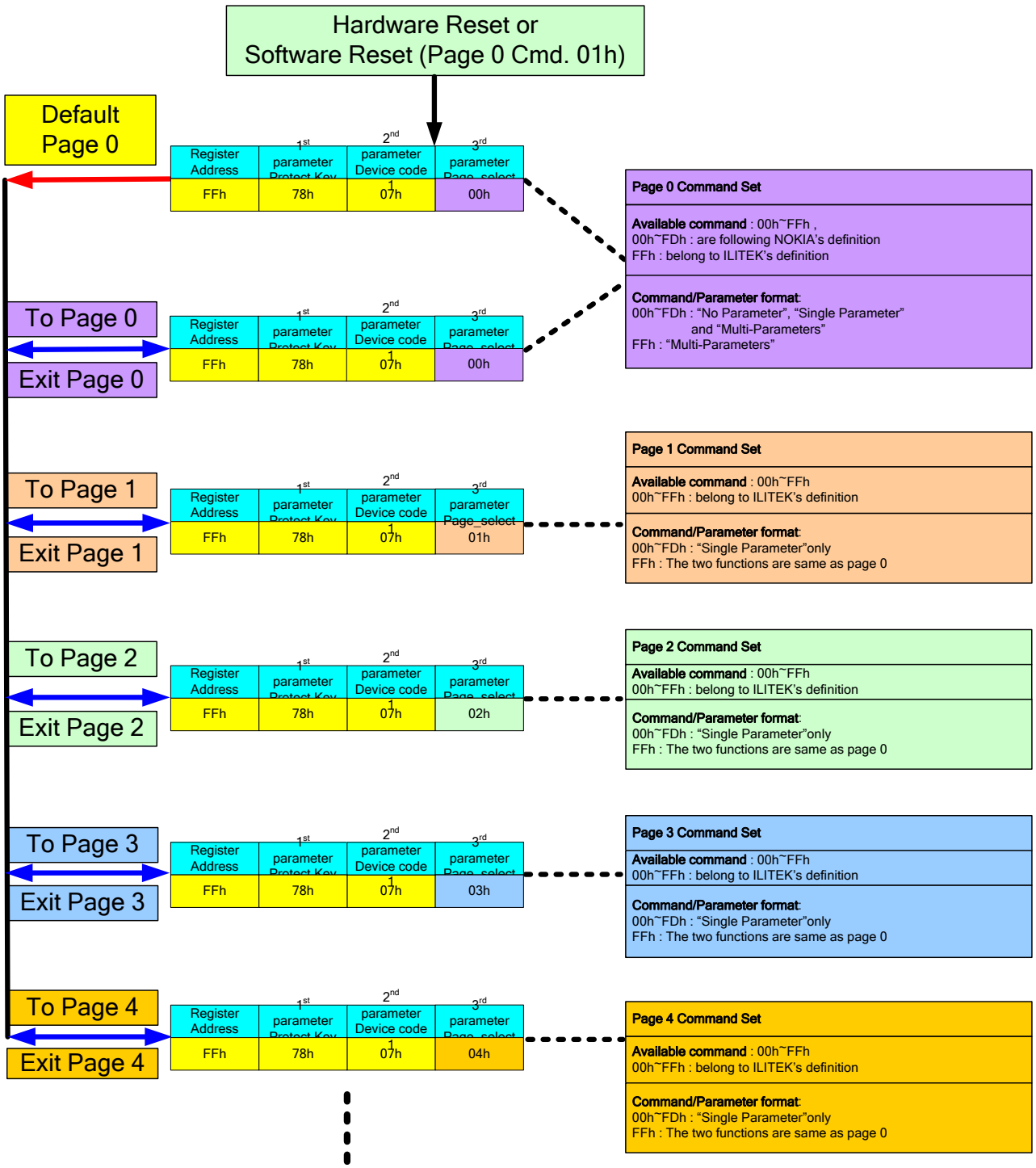


Figure 84. Command Flow

5.2. Implementation command

Table 34. Implementation command

Operational Code (Hex)	Command	Command (C) Read (R) Write (W)	Number Of Parameter	LCD Driver Implementation
00h	NOP	C	0	Yes
01h	Software Reset	C	0	Yes
04h	Read Display Identification	R	3	Yes
05h	Read Number of the Errors on DSI	R	1	Yes
09h	Read Display Status	R	4	Yes
0Ah	Read Display Power Mode	R	1	Yes
0Bh	Read Display MADCTL	R	1	Yes
0Ch	Read Display Pixel Format	R	1	Yes
0Dh	Read Display Image Mode	R	1	Yes
0Eh	Read Display Signal Mode	R	1	Yes
0Fh	Read Display Self-Diagnostic Result	R	1	Yes
10h	Sleep In	C	0	Yes
11h	Sleep Out	C	0	Yes
13h	Normal Display Mode On	C	0	Yes
20h	Display Inversion Off	C	0	Yes
21h	Display Inversion ON	C	0	Yes
22h	All Pixel Off	C	0	Yes
23h	All Pixel On	C	0	Yes
26h	Gamma Set	W	1	Yes
28h	Display Off	C	0	Yes
29h	Display ON	C	0	Yes
34h	Tearing Effect Line Off	C	0	Yes
35h	Tearing Effect Line On	W	1	Yes
36h	Memory Access Control	W	1	Yes
3Ah	Interface Pixel Format	W	1	Yes
51h	Write Display Brightness Value	W	2	Yes
52h	Read Display Brightness Value	R	2	Yes
53h	Write Control Display Value	W	1	Yes
54h	Read Control Display Value	R	1	Yes
55h	Write Power Save	W	1	Yes
56h	Read Power Save	R	1	Yes
5Eh	Write CABC Minimum Brightness	W	2	Yes
5Fh	Read CABC Minimum Brightness	R	2	Yes
68h	Set Transition Time	W	2	Yes
69h	Get Transition Time	R	2	Yes
A1h	Read DDB Start	R	7	Yes
A8h	Read DDB Continue	R	Variable	Yes
AAh	Read First Checksum	R	1	Yes
AFh	Read Continue Checksum	R	1	Yes
DAh	Read ID1	R	1	Yes
DBh	Read ID2	R	1	Yes

DCh	Read ID3	R	1	Yes

5.3. Command Accessibility

In the default status, only User Commands and Manufacturer Command Access Protect (MCAP) register can be accessed. Other commands are recognized as “NOP”.

Manufacturer Commands except the MCAP register are accessible by releasing Access Protect. See Command the description of the MCAP register for details.

Table 35. User Command Accessibility

Operational Code Command (Hex)		Command Accessibility		
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
00h	NOP	Yes	Yes	Yes
01h	Software Reset	Yes	Yes	Yes
04h	Read Display Identification	Yes	Yes	Yes
05h	Read Number of the Errors on DSI	Yes	Yes	Yes
09h	Read Display Status	Yes	Yes	Yes
0Ah	Read Display Power Mode	Yes	Yes	Yes
0Bh	Read Display MADCTL	Yes	Yes	Yes
0Ch	Read Display Pixel Format	Yes	Yes	Yes
0Dh	Read Display Image Mode	Yes	Yes	Yes
0Eh	Read Display Signal Mode	Yes	Yes	Yes
0Fh	Read Display Self-Diagnostic Result	Yes	Yes	Yes
10h	Sleep In	Yes	Yes	Yes
11h	Sleep Out	Yes	Yes	Yes
13h	Normal Display Mode On	Yes	Yes	Yes
20h	Display Inversion Off	Yes	Yes	Yes
21h	Display Inversion ON	Yes	Yes	Yes
22h	All Pixel Off	Yes	Yes	Yes
23h	All Pixel On	Yes	Yes	Yes
26h	Gamma curve Set	Yes	Yes	Yes
28h	Display Off	Yes	Yes	Yes
29h	Display ON	Yes	Yes	Yes
34h	Tearing Effect Line Off	Yes	Yes	Yes
35h	Tearing Effect Line On	Yes	Yes	Yes
36h	Memory Access Control	Yes	Yes	Yes
3Ah	Interface Pixel Format	Yes	Yes	Yes

Table 36. User Command Accessibility (continued)

Operational Code Command (Hex)		Command Accessibility		
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
51h	Write Display Brightness	Yes	Yes	Yes
52h	Read Display Brightness Value	Yes	Yes	Yes
53h	Write Control Display	Yes	Yes	Yes
54h	Read Control Display Value	Yes	Yes	Yes
55h	Write Power Save	Yes	Yes	Yes
56h	Read Power Save	Yes	Yes	Yes
5Eh	Write CABC Minimum Brightness	Yes	Yes	Yes
5Fh	Read CABC Minimum Brightness	Yes	Yes	Yes
68h	Set Transition	Yes	Yes	Yes
69h	Get Transition	Yes	Yes	Yes
A1h	Read DDB Start	Yes	Yes	Yes
A8h	Read DDB Continue	Yes	Yes	Yes
AAh	Read First Checksum	Yes	Yes	Yes
AFh	Read Continue Checksum	Yes	Yes	Yes
DAh	Read ID1	Yes	Yes	Yes
DBh	Read ID2	Yes	Yes	Yes
DCh	Read ID3	Yes	Yes	Yes

5.4. Default Modes and values

Table 37. User Command's Default Modes and Vaules

Operational Code Command (Hex)	Command	Parameters	Default Modes and Vaules(Hex)		
			After Power-on	After SW Reset	After HW Reset
00h	NOP	None	N/A	N/A	N/A
01h	Software Reset	None	N/A	N/A	N/A
04h	Read Display Identification	1st	00h (Note)	Don't Change	00h (Note)
		2nd	80h (Note)	Don't Change	80h (Note)
		3rd	00h (Note)	Don't Change	00h (Note)
05h	Read Number of the Errors on DSI	1st	00h	00h	00h
09h	Read Display Status	1st	00h	00h	00h
		2nd	01h	01h	01h
		3rd	00h	00h	00h
		4th	00h	00h	00h
0Ah	Read Display Power Mode	1st	08h	08h	08h
0Bh	Read Display MADCTL	1st	00h	00h	00h
0Ch	Read Display Pixel Format	1st	07h	07h	07h
0Dh	Read Display Image Mode	1st	00h	00h	00h
0Eh	Read Display Signal Mode	1st	00h	00h	00h
0Fh	Read Display Self-Diagnostic Result	1st	00h	00h	00h
10h	Sleep In	None	Sleep In Mode	Sleep In Mode	Sleep In Mode

11h	Sleep Out	None	Sleep In Mode	Sleep In Mode	Sleep In Mode
20h	Display Inversion Off	None	Display Inversion Off	Display Inversion Off	Display Inversion Off
21h	Display Inversion On	None	Display Inversion Off	Display Inversion Off	Display Inversion Off
22h	All Pixel Off	None	Off	Off	Off
23h	All Pixel On	None	Off	Off	Off
26h	Gamma curve Set	1st	01h	01h	01h
28h	Display Off	None	Display off	Display off	Display off
29h	Display ON	None	Display off	Display off	Display off
34h	Tearing Effect Line Off	None	TE line output Off	TE line output Off	TE line output Off
35h	Tearing Effect Line On	1st	TE line output Off	TE line output Off	TE line output Off
36h	Memory Access Control	1st	00h	00h	00h
3Ah	Interface Pixel Format	1st	07h	07h	07h
51h	Write Display Brightness	1st/2nd	00h	00h	00h
52h	Read Display Brightness Value	1st/2nd	00h	00h	00h
53h	Write Control Display	1st	00h	00h	00h
54h	Read Control Display Value	1st	00h	00h	00h
55h	Write Power Save	1st	00h	00h	00h
56h	Read Power Save	1st	00h	00h	00h
5Eh	Write CABC Minimum Brightness	1st/2nd	00h	00h	00h
5Fh	Read CABC Minimum Brightness	1st/2nd	00h	00h	00h
68h	Set Transition	1st/2nd	00h	00h	00h
69h	Get Transition	1st/2nd	00h	00h	00h
A1h	Read DDB Start	1st/2nd/3rd/ 4th/5th/6th	00h (Note)	Don't Change	00h (Note)
		7th	FFh	FFh	FFh
A8h	Read DDB Continue	Variable	(See Read DDB Start Default)	(See Read DDB Start Default)	(See Read DDB Start Default)
AAh	Read First Checksum	1st	Checksum	Checksum	Checksum
AFh	Read Continue Checksum	1st	Checksum	Checksum	Checksum
DAh	Read ID1	1st	00h (Note)	Don't Change	00h (Note)
DBh	Read ID2	1st	80h (Note)	Don't Change	80h (Note)
DCh	Read ID3	1st	00h (Note)	Don't Change	00h (Note)

Note: Default Data is loaded from intimal NVM. If user writes ID register values into the NVM, the values are set as default.

5.5. User Command List

5.5.1. User Command List

Page	CMD	Para.	W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)
P0	00h	-	W	NOP	No Argument								-
P0	01h	-	W	Software Reset	No Argument								-
P0	04h	1st	R	Read Display Identification	ID1[7:0]								00h
		2nd			ID2[7:0]								80h
		3rd			ID3[7:0]								00h
P0	05h	1st	R	Read Number of the Errors on DSI	P[7:0]								00h
P0	09h	1st	R	Read Display Status	D31	0	0	0	0	D26	0	D24	00h
		2nd	R		D23	0	0	0	D19	0	D17	D16	01h
		3rd	R		0	0	D13	D12	D11	D10	D9	D8	00h
		4th	R		D7	D6	D5	0	0	0	0	D0	00h
P0	0Ah	1st	R	Read Display Power Mode	BVSTA	IDMON	0	SLPOUT	NORON	DSPON	0	0	08h
P0	0Bh	1st	R	Read Display MADCTL	0	0	0	0	BGR	0	SS	GS	00h
P0	0Ch	1st	R	Read Display Pixel Format	0	0	0	0	0	DBI[2:0]			07h
P0	0Dh	1st	R	Read Display Image Mode	0	0	INVON	ALLPON	ALLPOFF	GCS[2:0]			00h
P0	0Eh	1st	R	Read Display Signal Mode	TEON	TELOM	0	0	0	0	0	EODSI	00h
P0	0Fh	1st	R	Read Display Self-Diagnostic Result	REGLD	FUNDT	0	GLSBK	0	0	0	CHKSC	00h
P0	10h	-	W	Sleep In	No Argument								-
P0	11h	-	W	Sleep Out	No Argument								-
P0	13h	-	W	Normal Display Mode On	No Argument								-
P0	20h	-	W	Display Inversion Off	No Argument								-
P0	21h	-	W	Display Inversion ON	No Argument								-
P0	22h	-	W	All Pixel Off	No Argument								-
P0	23h	-	W	All Pixel On	No Argument								-
P0	26h	1st	W	Gamma Curve Set	0	0	0	0	GC[3:0]				01h
P0	28h	-	W	Display Off	No Argument								-
P0	29h	-	W	Display On	No Argument								-
P0	34h	-	W	Tear Effect Line Off	No Argument								-
P0	35h	1st	W	Tear Effect Line On	0	0	0	0	0	0	0	M	00h
P0	36h	1st	W	Memory Access Control	0	0	0	0	BGR	0	SS	GS	00h
P0	3Ah	1st	W	Interface Pixel Format	0	0	0	0	0	DBI[2:0]			07h
P0	51h	1st	W	Write Display Brightness	0	0	0	0	DBV[11:8]				00h
		2nd			DBV[7:0]								00h
P0	52h	1st	R	Read Display Brightness Value	0	0	0	0	DBV[11:8]				00h
		2nd			DBV[7:0]								00h
P0	53h	1st	W	Write Control Display	HBM[1:0]		BCTRL	0	DD	BL	0	0	00h
P0	54h	1st	R	Read Control Display value	HBM[1:0]		BCTRL	0	DD	BL	0	0	00h
P0	55h	1st	W	Write Power Save	PWRSAVE[7:0]								00h
P0	56h	1st	R	Read Power Save	PWRSAVE[7:0]								00h
P0	59h	-	W	Stop Transition	No Argument								-
P0	5Eh	1st	W	Write CABC Minimum Brightness	0	0	0	0	CMB[11:8]				00h
		2nd			CMB[7:0]								00h
P0	5Fh	1st	R	Read CABC Minimum Brightness	0	0	0	0	CMB[11:8]				00h
		2nd			CMB[7:0]								00h
P0	68h	1st	W	Set Transition	TT_STP[7:0]								00h
		2nd			ST_TIM[7:0]								00h
P0	69h	1st	R	Get Transition	TT_STP[7:0]								00h
		2nd			ST_TIM[7:0]								00h

P0	A8h	2nd	R	Read DDB Continue	D2[7:0]								00h
		:			:								00h
		Nth			DN[7:0]								00h
P0	AAh	1st	R	Read First Checksum	FCS[7:0]								00h
P0	AFh	1st	R	Read Continue Checksum	CCS[7:0]								00h
P0	DAh	1st	R	Read ID1	ID1[7:0]								00h
P0	DBh	1st	R	Read ID2	ID2[7:0]								80h
P0	DCh	1st	R	Read ID3	ID3[7:0]								00h
P0	FFh	1st	W	EXTC CMD Set Enable	0	1	1	1	1	0	0	0	78h
		2nd	W		0	0	0	0	0	1	1	1	07h
		3rd	W		PAGE[7:0]								00h

Note:

1. Undefined commands are treated as NOP (00h) command.

2. FFh are display supplier for usage of factory.

3. Commands 10h,13h, 22h, 23h, 26h, 36h, 51h, 53h, 55h and 5Eh are updated during V-SYNC when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh), Read Display Self-Diagnostic Result (0Fh), Read Display Brightness Value (52h), Read CTRL Value Display (54h), Read Content Adaptive Brightness Control (56h), Read CABC Minimum Brightness (5Fh) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

5.6. User Command Description

5.6.1. NOP (00h)

Page 0 Command Set		00h : NOP (No Operation)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	0	00h
1st Parameter	-	No Parameter								-
Description	This command is an empty command; it does not have any effect on the ILI7807S.									
Restriction	None									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

5.6.2. Software Reset (01h)

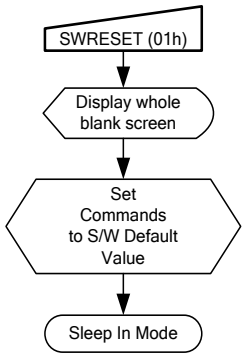
Page 0 Command Set		01h : SWRESET (Software Reset)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	1	01h
1st Parameter	-	No parameter								-
Description	When the Software Reset command (01h) is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description). The display is blank immediately.									
Restriction	It is necessary to wait 5msec before sending a new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5msec. If Software Reset command (01h) is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command (11h). The Software Reset command (01h) cannot be sent during Sleep Out sequence.									
Register Availability										

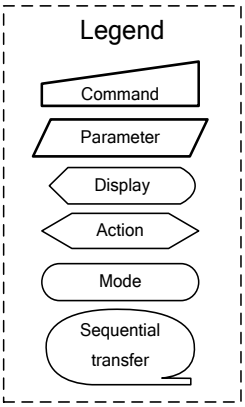
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart





5.6.3. Read Display Identification (04h)

Page 0 Command Set		04h : RDDID (Read Display Identification)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	0	0	04h
1st Parameter	Read	ID1[7:0]								00h
2nd Parameter	Read	ID2[7:0]								80h
3rd Parameter	Read	ID3[7:0]								00h

Description

These read bytes are used to track the LCD module/driver version. It is defined by the display supplier and changes each time a revision is made to the display, material or construction specifications.

The ID1, DI2 and ID3 are programmed by NVM function.

Restriction

None

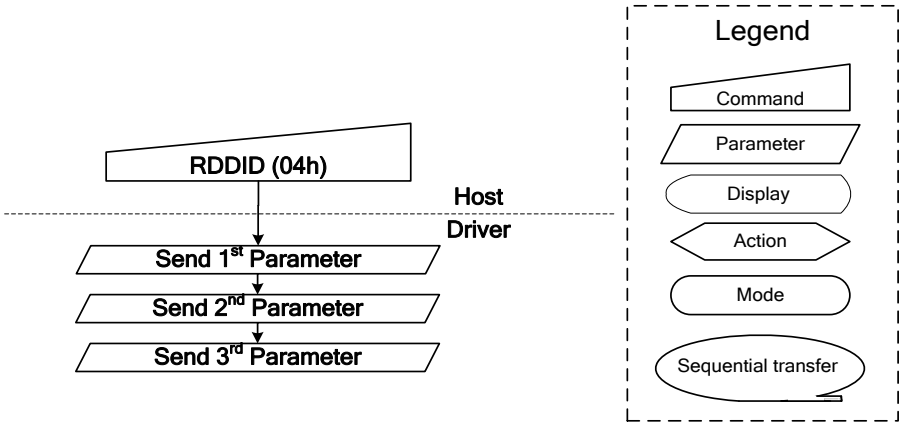
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before NVM program)	Default Value (After NVM program)
Power On Sequence	00h_80h_00h	NVM value
S/W Reset	00h_80h_00h	NVM value
H/W Reset	00h_80h_00h	NVM value

Flow Chart



5.6.4. Read Number of the Errors on DSI (05h)

Page 0 Command Set		05h : RDNUMED (Read Number of the Errors on DSI)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	0	1	05h
1st Parameter	Read	P[7:0]								00h
Description	The 1st parameter tells the number of errors on DSI. The more detailed description of this parameter is below. P[6:0] tells the number of the errors. P[7] is set to '1' if there is overflow with P[6:0]. P[7:0] is set to '0's (as well as Read Display Signal Mode command (0Eh)'s D0 is set '0' at the same time) after the parameter information is sent (read cmd. 05h is completed).									
Restriction	None									

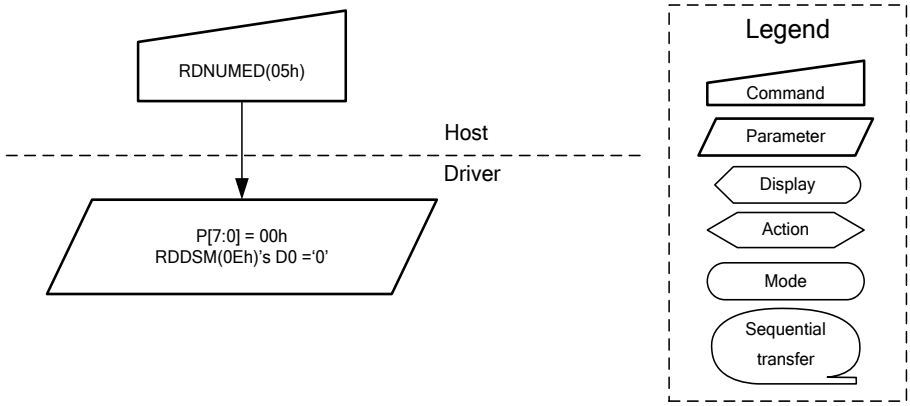
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.6.5. Read Display Status (09h)

Page 0 Command Set		09h : RDDSTU (Read Display Status)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	0	1	09h
1st Parameter	Read	D31	0	0	0	0	D26	0	D24	00h
2nd Parameter	Read	D23	0	0	0	D19	0	D17	D16	01h
3rd Parameter	Read	0	0	D13	D12	D11	D10	D9	D8	00h
4th Parameter	Read	D7	D6	D5	0	0	0	0	D0	00h

Description

This command indicates the current status of the display, as described in the table below.

Bit	Description	Value	Status
D31	Booster voltage status	0	Booster Off
		1	Booster On
D26	BGR (RGB/BGR order)	0	RGB
		1	BGR
D24	SS (Source Scan sequence)	0	Source output Left to Right
		1	Source output Right to Left
D23	GS (Gate Scan sequence)	0	Gate output Top to Bottom
		1	Gate output Bottom to Top
D19	Idle Mode On/Off	0	Idle Mode Off
		1	Idle Mode On
D17	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
D16	Display Normal Mode On/Off	0	Display Normal Mode Off (All Pixels Off or All Pixels On mode)
		1	Display Normal Mode On
D13	Inversion On/Off	0	Inversion Off
		1	Inversion On
D12	All Pixel On	0	Normal mode
		1	All Pixels On
D11	All Pixel Off	0	Normal mode
		1	All Pixels Off
D10	Display On/Off	0	Display is OFF
		1	Display is ON
D9	TE On/Off	0	Tearing Effect Line OFF
		1	Tearing Effect Line ON
D8, D7, D6	Gamma Curve Selection (GCS[2:0])	000	Gamma Curve 1 (Gamma 2.2)
		others	Reserved
D5	TE Mode	0	Tearing Effect Line Mode 1
		1	Tearing Effect Line Mode 2
D0	Parity Error on DSI	0	No Parity Error
		1	Parity Error

Note: For D26, D24 and D23 defintion refer to Memory Access Control command (36h).

Restriction: None

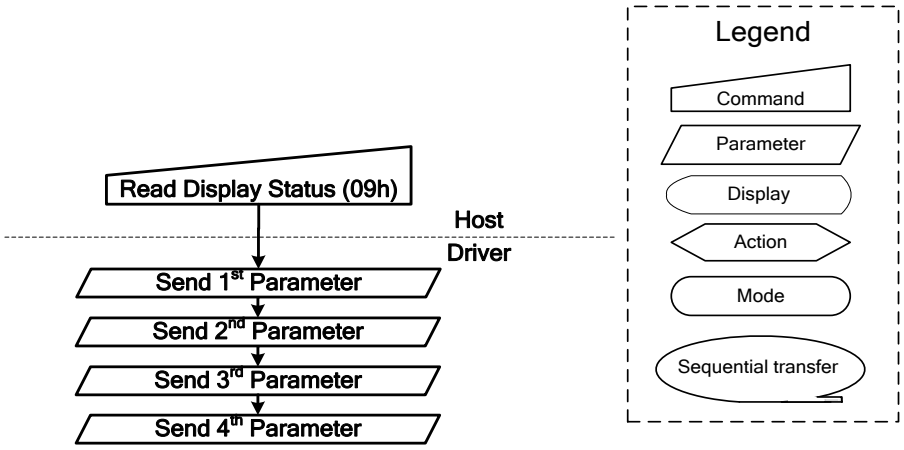
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_01h_00h_00h
S/W Reset	00h_01h_00h_00h
H/W Reset	00h_01h_00h_00h

Flow Chart



5.6.6. Read Display Power Mode (0Ah)

Page 0 Command Set		0Ah : RDDPM (Read Display Power Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	1	0	0Ah
1st Parameter	Read	BVSTA	IDMON	0	SLPOUT	NORON	DSPON	0	0	08h

Description

This command indicates the current status of the display as described in the table below.

Bit	Description	Value	Status
D7	Booster Voltage Status	0	Booster Off or Has a fault
		1	Booster On and Working OK
D6	Idle Mode On/Off	0	Idle Mode Off
		1	Idle Mode On
D4	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
D3	Display Normal Mode On/Off	0	Display Normal Mode Off
		1	Display Normal Mode On
D2	Display On/Off	0	Display Off
		1	Display On

Restriction

None

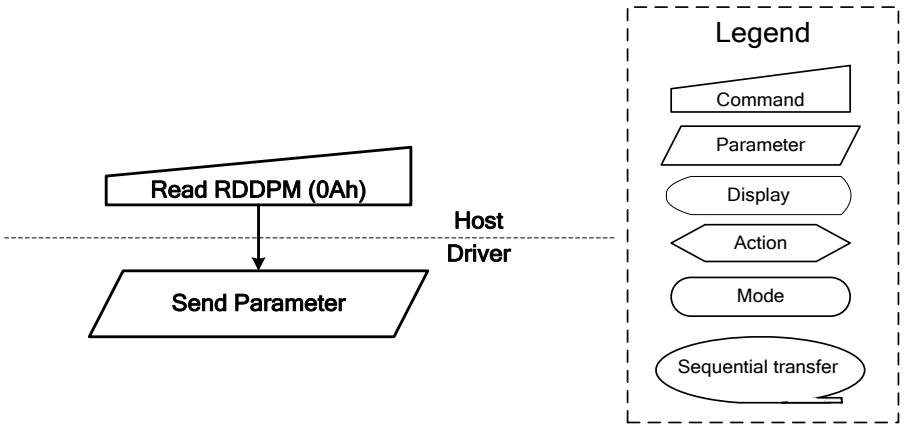
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart



5.6.7. Read Display MADCTL (0Bh)

Page 0 Command Set		0Bh : RDDMADCTL (Read Display MADCTL)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	1	1	0Bh
1st Parameter	Read	0	0	0	0	BGR	0	SS	GS	00h

Description

This command depends on Memory Access Control command (36h) and indicates the current status of the display as described in the table below.

Bit	Description	Value	Status
D3	BGR (RGB/BGR Order)	0	RGB
		1	BGR
D1	SS (Source Scan sequence)	0	Source output Left to Right
		1	Source output Right to Left
D0	GS (Gate Scan sequence)	0	Gate output Top to Bottom
		1	Gate output Bottom to Top

Restriction

None

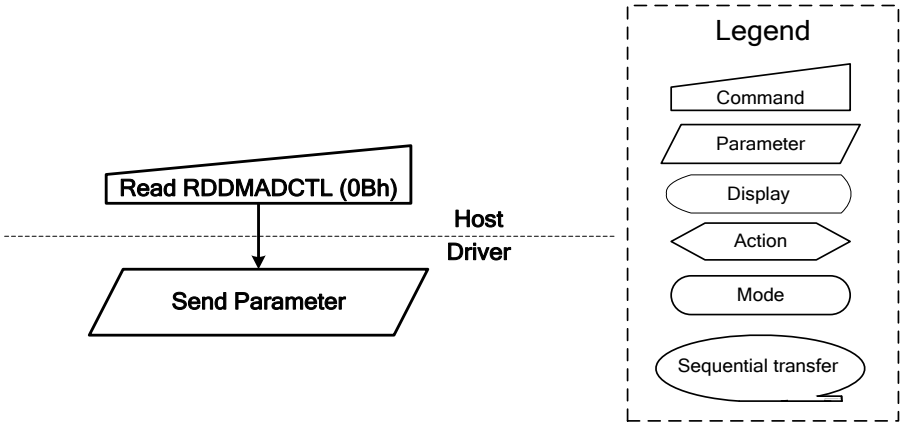
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.6.8. Read Display Pixel Format (0Ch)

Page 0 Command Set		0Ch : RDDCOLMOD (Read Display COLMOD)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	1	0	0	0Ch
1st Parameter	Read	0	0	0	0	0	DBI[2:0]			07h

Description

This command indicates the current status of the display as described in the table below.

DBI[2:0]			Control Interface Color Format
0h~4h			Reserved
1	0	1	16-bit / pixel
1	1	0	18-bit / pixel
1	1	1	24-bit / pixel

Note: For DBI[2:0] definition refer to Interface Pixel Format (3Ah)

Restriction

None

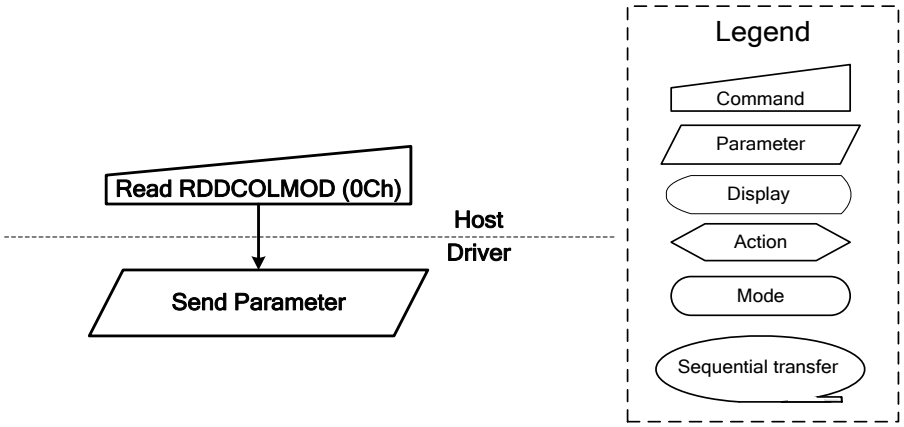
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

Flow Chart



5.6.9. Read Display Image Mode (0Dh)

Page 0 Command Set		0Dh : RDDIM (Read Display Image Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	1	0	1	0Dh
1st Parameter	Read	0	0	INVON	ALLPON	ALLPOFF	GCS[2:0]			00h

Description

This command indicates the Image Mode status of the display as described in the table below :

Bit	Description	Value	Status
D5	Inversion On/Off (Reserved)	0	Inversion Off
		1	Inversion On
D4	All Pixels On	0	Normal Display
		1	White Display
D3	All Pixels Off	0	Normal Display
		1	Black Display
D2, D1, D0	Gamma Curve Selection (GCS[2:0])	000	Gamma Curve 1 (Gamma 2.2)
		Others	Reserved

Restriction

None

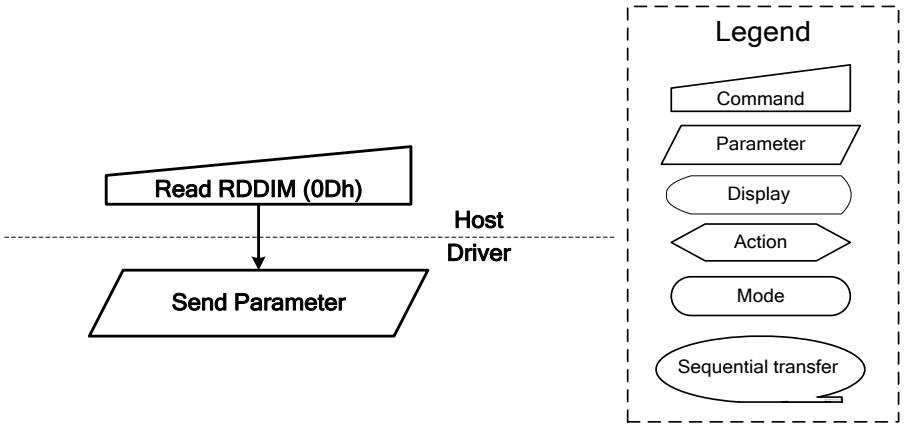
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.6.10. Read Display Signal Mode (0Eh)

Page 0 Command Set		0Eh : RDDSM (Read Display Signal Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	1	1	0	0Eh
1st Parameter	Read	TEON	TELOM	0	0	0	0	0	EODSI	00h

Description

This command indicates the current status of the display as described in the table below.

Bit	Description	Value	Status
D7	Tearing Effect Line On/Off	0	Tearing Effect Line Off
		1	Tearing Effect Line On
D6	Tearing Effect Line Output Mode	0	Tearing Effect Line Mode 1
		1	Tearing Effect Line Mode 2
D0	Error on DSI	0	No Error on DSI
		1	Error on DSI

Note: For D0 definition see chapter "4.3.3.2.2.2. Acknowledge with Error Report (AwER)" and "5.6.4. Read Number of the Errors on DSI (05h)".

Restriction

None

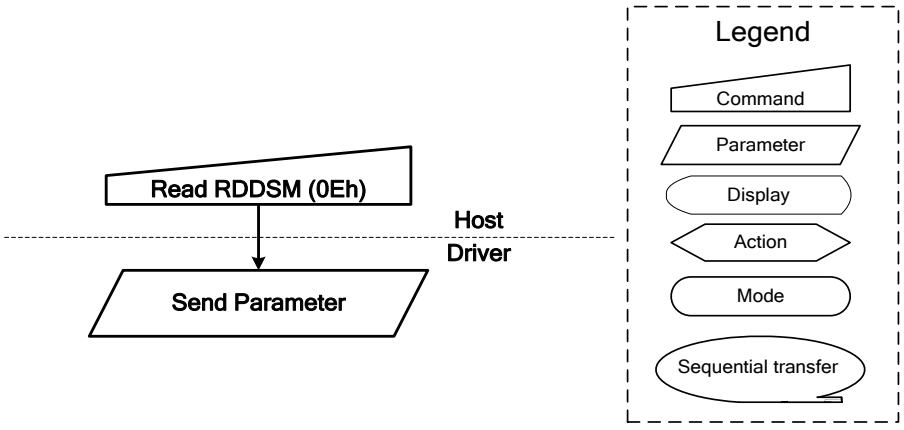
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.6.11. Read Display Self-Diagnostic Result (0Fh)

Page 0 Command Set		0Fh : RDDSDR (Read Display Self-Diagnostic Result)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	1	1	1	0Fh
1st Parameter	Read	REGLD	FUNDT	0	**0**	0	0	0	CHKSC	00h

Description

This command indicates the status of the display self-diagnostic results after Sleep Out command (11h) as described in the table below.

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit when the NVM and register values are same.
D6	Functionality Detection	Invert the D6 bit when the chip met User's functionality requirements
D0	Checksums Comparison	'0' = Checksums are same
		'1' = Checksums are not same

Restriction

It will be necessary to wait 300ms after there is the last write access on Page 0 area registers before there can read Bit D0 value.

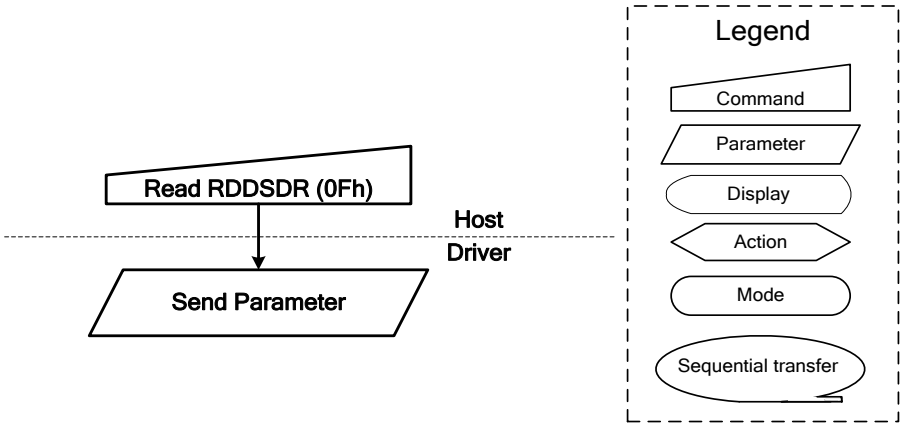
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



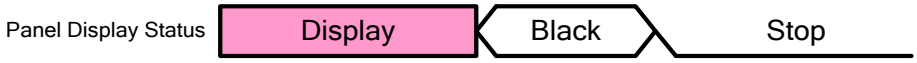
5.6.12. Sleep In (10h)

Page 0 Command Set		10h : SLPIN (Sleep In)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	0	0	10h
1st Parameter	-	No parameter								-

Description

This command causes the ILI7807S to enter the minimum power consumption mode.

In this mode e.g. the DC/DC converter is stopped, DDI's internal oscillator is stopped, and panel scanning is stopped.



MIPI DSI interface is still working.

Ambient light based control is off.

Backlights and display are off.

Dimming function does not work when there is changing mode from Sleep Out to Sleep In.

Restriction

This command has no effect when module is already in Sleep In mode. Sleep In Mode can only be left by the Sleep Out command (11h).

It is necessary to wait 5msec before sending the next command; this wait time (5msec) is to allow time for the supply voltages and clock circuits to stabilize.

When in Sleep In Mode, It is necessary to wait 120msec for exchanging into Sleep Out Mode after sending Sleep Out command (11h) and before the next Sleep In command (10h) can be sent.

When in Sleep Out Mode, It takes 120msec to get into Sleep In mode after sending Sleep In command (10h).

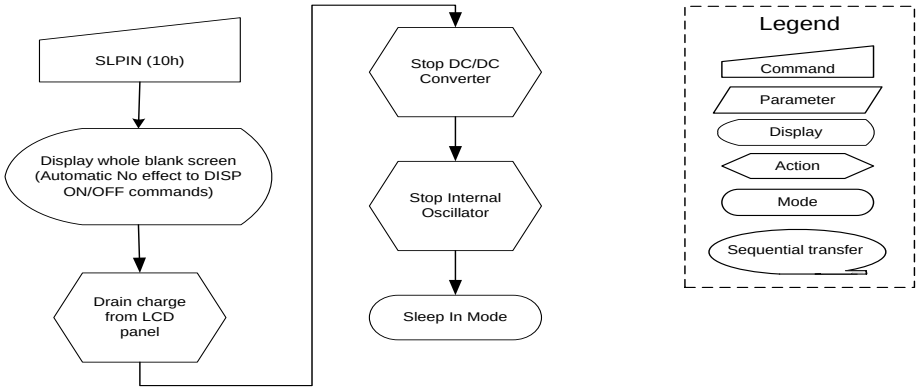
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart



5.6.13. Sleep Out (11h)

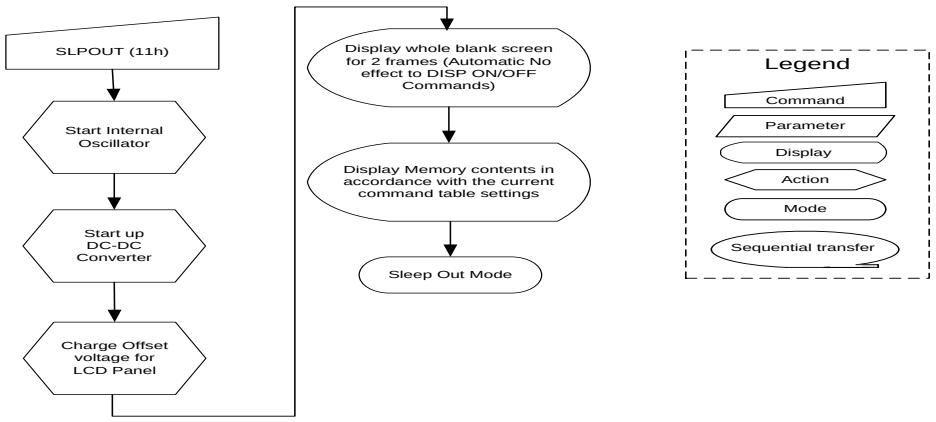
Page 0 Command Set		11h : SLPOUT (Sleep Out)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	0	1	11h
1st Parameter	-	No parameter								-
Description	This command turns off sleep mode. In this mode e.g. the DC/DC converter is enabled, DDI's Internal oscillator is started, and panel scanning is started. Panel Display Status: Stop → Black → Display									
Restriction	This command has no effect when module is already in Sleep Out mode. Sleep Out mode can be left by the Sleep In command (10h), S/W reset command (01h) or H/W reset. It is necessary to wait 5msec before sending next command; this wait time (5msec) is to allow time for the supply voltages and clock circuits to stabilize. The ILI7807S loads all display supplier's factory default values into the registers during this 5msec waiting time. There cannot be any abnormal visual effect on the display image, if factory default and register values are same when this load is done and when the ILI7807S is already Sleep Out mode. During this 5msec, ILI7807S is running self-diagnostic functions. When in Sleep Out Mode, It is necessary to wait 120msec for exchanging into Sleep In Mode after sending Sleep In command (10h) and before the next Sleep Out command (11h) can be sent. When in Sleep In Mode, It takes 120msec to get into Sleep Out mode after sending Sleep Out command (11h).									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart



5.6.14. Normal Display Mode On (13h)

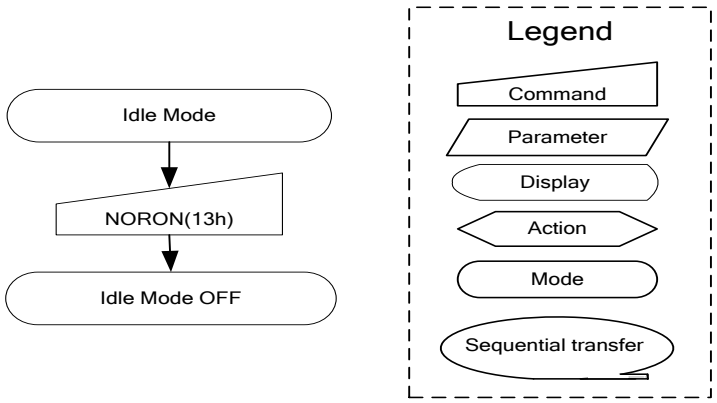
Page 0 Command Set		13h : NORON (Normal Display Mode On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	1	1	13h
1st Parameter	-	No parameter								-
Description	This command returns the display to Normal Display Mode. Using Normal Display Mode On command (13h) to exit All Pixel On/Off Mode into Normal Display Mode.									
Restriction	This command has no effect when Normal Display Mode is active.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Display Mode On
S/W Reset	Normal Display Mode On
H/W Reset	Normal Display Mode On

Flow Chart



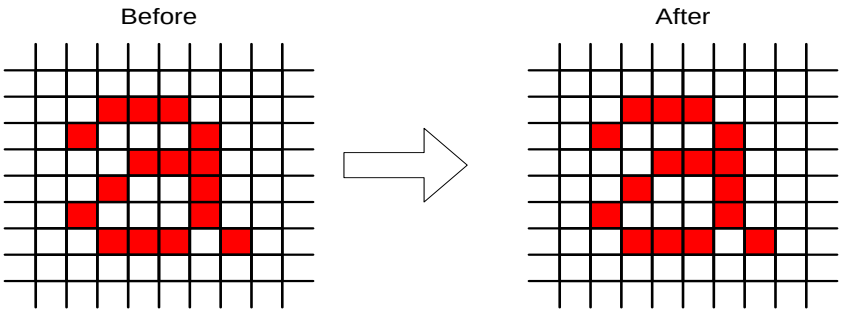
5.6.15. Display Inversion Off (20h)

Page 0 Command Set		20h : INVOFF (Display Inversion Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	0	20h
1st Parameter	-	No parameter								-

Description

This command is used to recover from Display Inversion On mode.

This command doesn't change any other status.



Restriction

This command has no effect when module is already in Display Inversion Off mode.

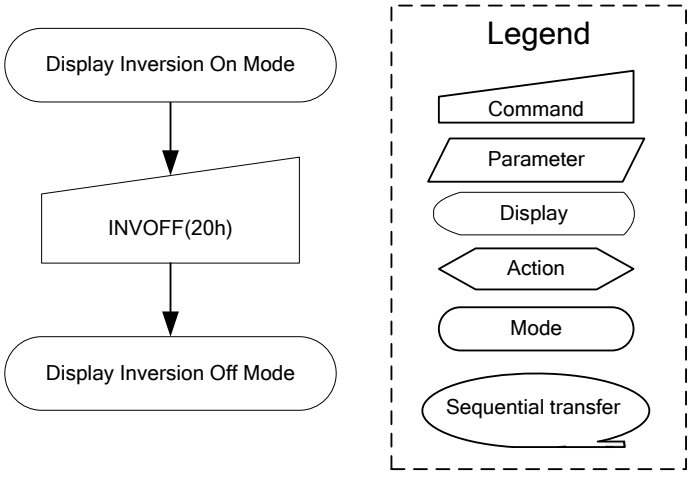
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



5.6.16. Display Inversion On (21h)

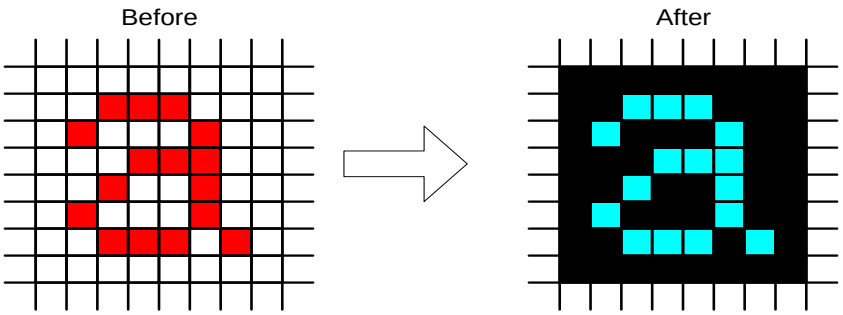
Page 0 Command Set		21h : INVON (Display Inversion ON)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	1	21h
1st Parameter	-	No parameter								-

Description

This command is used to enter into Display Inversion On mode.

This command doesn't change any other status.

To exit Display Inversion On mode, the Display Inversion Off command (20h) should be written.



Restriction

This command has no effect when the ILI7807S is already in Inversion On mode.

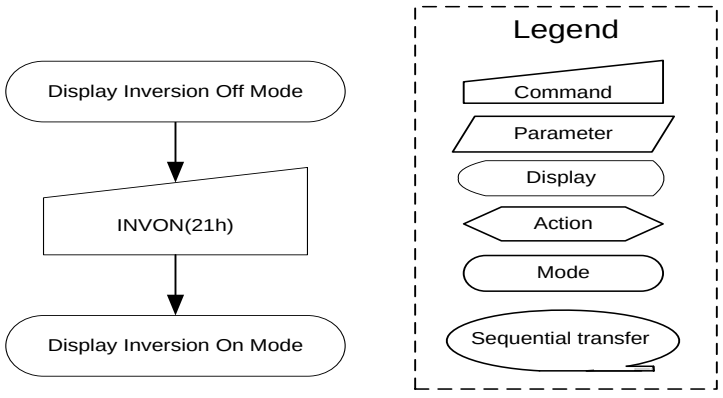
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart

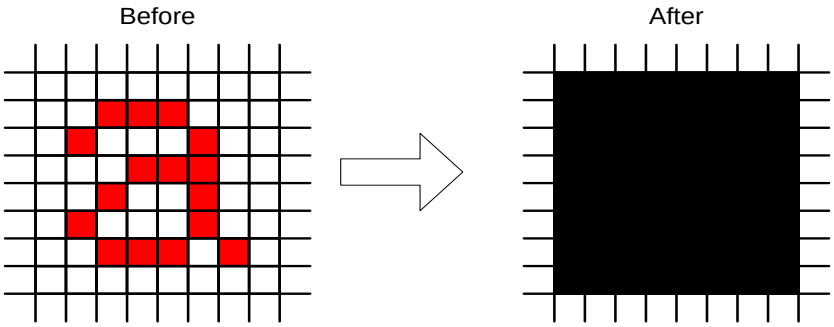


5.6.17. All Pixel Off (22h)

Page 0 Command Set		22h : ALLPOFF (All pixels off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	0	22h
1st Parameter	-	No parameter								-

Description

This command turns the display panel black in Sleep Out Mode and a status bit of the Read Display Image Mode command (0Dh) can be read. This command does not change any other status.



All Pixels On command (23h) and Normal Display Mode On command (13h) are used to leave All Pixel Off Mode.

Restriction

This command has no effect when the ILI7807S is already in All Pixels Off mode.

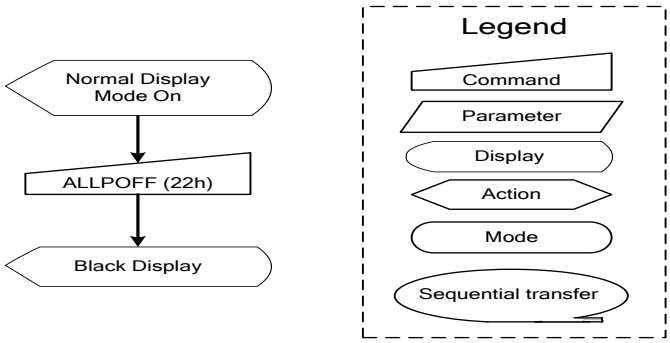
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart

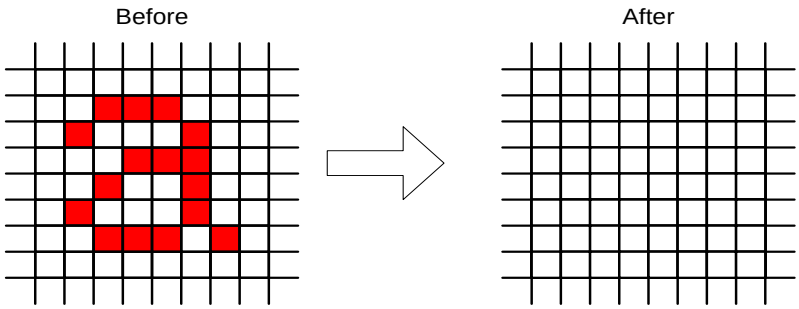


5.6.18. All Pixel On (23h)

Page 0 Command Set		23h : ALLPON (All pixels on)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	1	23h
1st Parameter	-	No parameter								-

Description

This command turns the display panel white in Sleep Out Mode and a status bit of the Read Display Image Mode command (0Dh) can be read. This command does not change any other status.



All Pixels Off command (22h) and Normal Display Mode On command (13h) are used to leave All Pixel On Mode.

Restriction

This command has no effect when ILI7807S is already in All Pixels On mode.

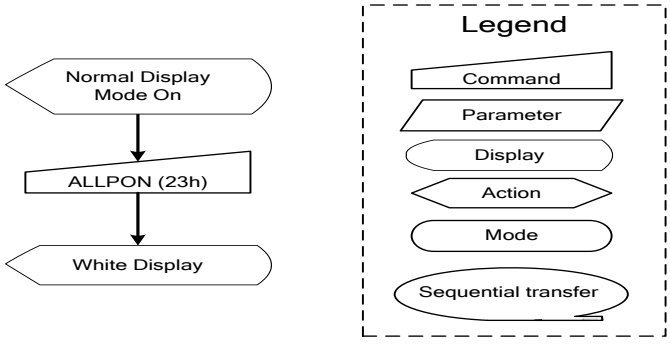
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



5.6.19. Gamma Set (26h)

Page 0 Command Set		26h : GAMSET (Gamma Set)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	1	1	0	26h
1st Parameter	Write	0	0	0	0	GC[3:0]				01h

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 1 fixed Gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the table below:

GC[3:0]	Curve Selected
1h	Gamma curve 1 (Gamma 2.2)
Others	Reserved

Note: All others value are undefined.

Restriction

Values of GC [3:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

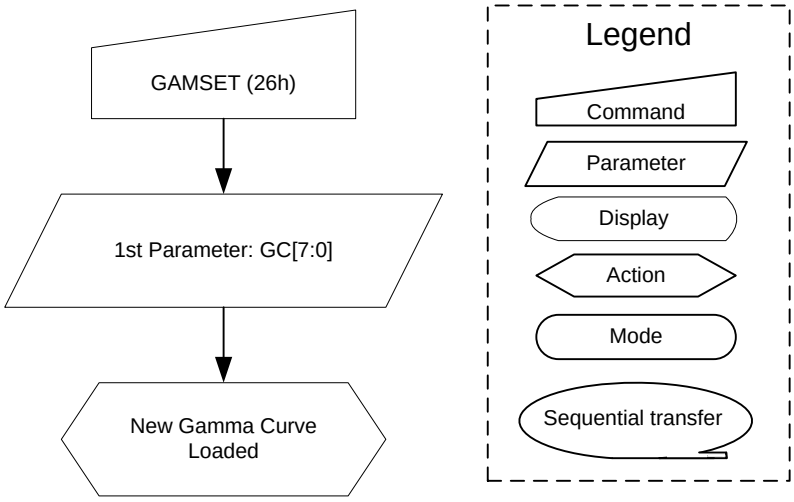
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



5.6.20. Display Off (28h)

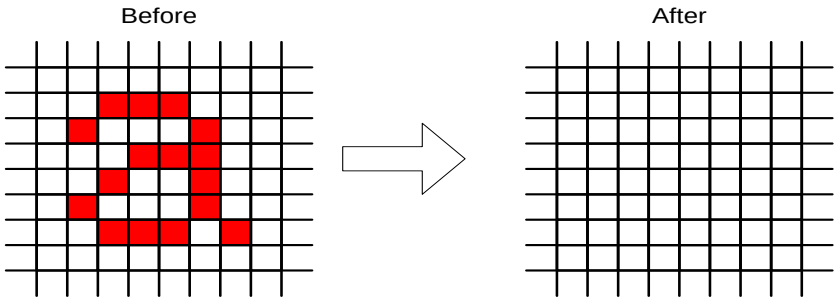
Page 0 Command Set		28h : DISOFF (Display Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	1	0	0	0	28h
1st Parameter	-	No parameter								-

Description

This command is used to enter into Display Off mode. In this mode, the output data is disabled and blank page inserted.

This command makes no change any other status.

There will be no abnormal visible effect on the display.



Restriction

This command has no effect when module is already in Display Off mode.

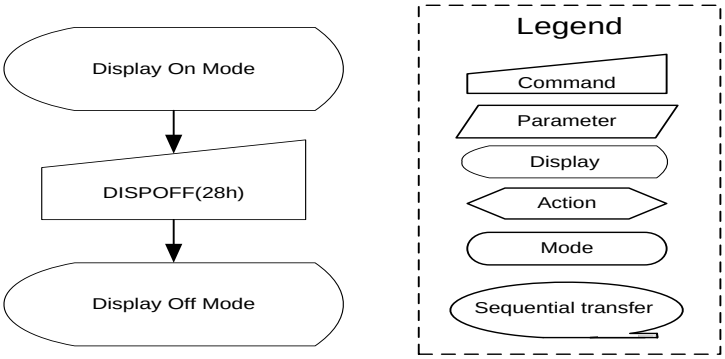
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



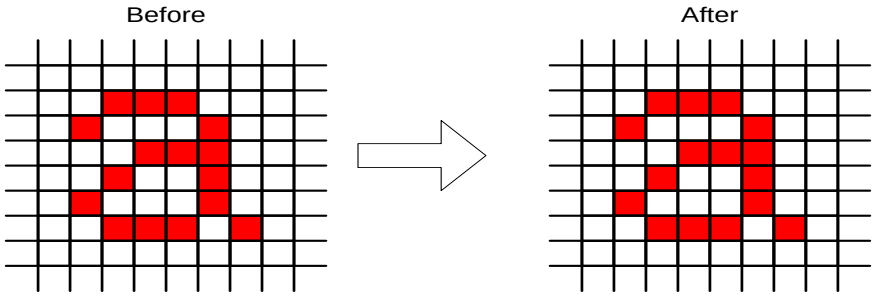
5.6.21. Display On (29h)

Page 0 Command Set		29h : DISON (Display ON)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	1	0	0	1	29h
1st Parameter	-	No parameter								-

Description

This command is used to recover from Display Off mode. Output data is enabled.

This command does not change any other status.



Restriction

This command has no effect when the ILI7807S is already in Display On Mode.

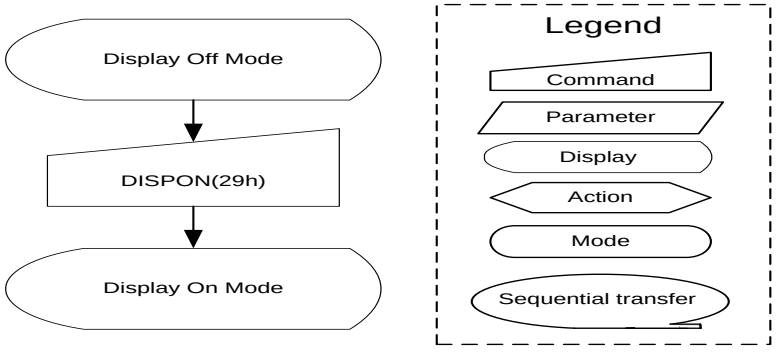
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



5.6.22. Tearing Effect Line Off (34h)

Page 0 Command Set		34h : TEOFF (Tearing Effect Line OFF)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	0	34h
1st Parameter	-	No parameter								-
Description	This command is used to turn off Display module's Tearing Effect output signal through TE pad.									
Restriction	This command has no effect when the Tearing Effect output is already off.									

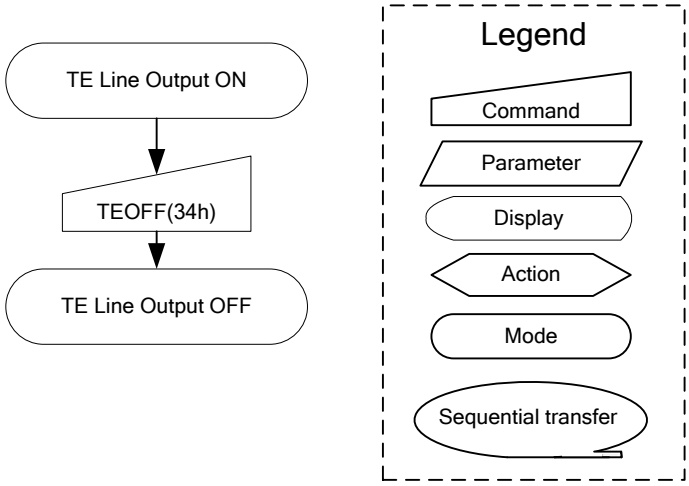
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	TE Line output Off
S/W Reset	TE Line output Off
H/W Reset	TE Line output Off

Flow Chart



5.6.23. Tearing Effect Line On (35h)

Page 0 Command Set		35h : TEON (Tearing Effect Line ON)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	1	35h
1st Parameter	Write	0	0	0	0	0	0	0	M	00h

Description

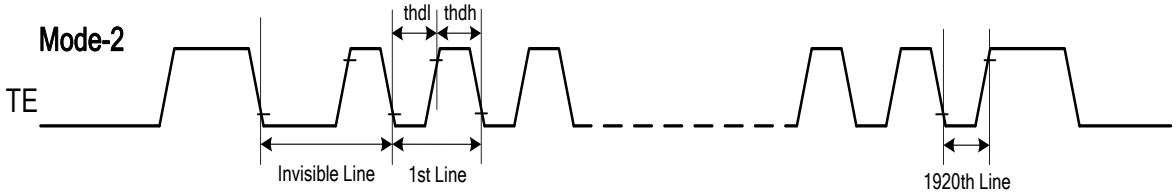
This command is used to turn on Tearing Effect output signal through TE pad.

The Tearing Effect Line On command (35h) has one parameter which describes the mode of Tearing Effect Output Line.

When **M=0**, the Tearing Effect Output line consists of V-Blanking information only.

The Tearing Effect Output line shall be high during vertical blanking period.

When **M=1**, the Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.



Vertical blanking period : VBP + VFP

Note 1: The Tearing Effect Output line shall be low when the display module is in Sleep mode.

Note 2: When DSI TE reporting function is used, Tearing Effect Line Mode must be set Mode-1 (M = 0).

Restriction

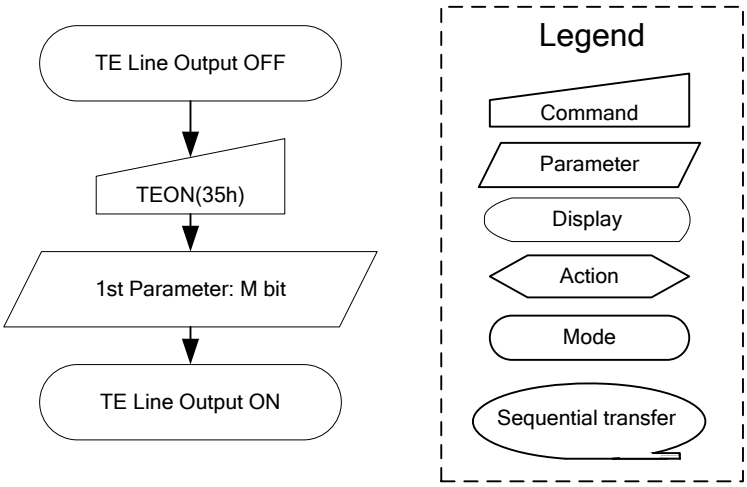
This command has no effect when the Tearing Effect output is already on.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	TE Line output Off
S/W Reset	TE Line output Off
H/W Reset	TE Line output Off

Flow Chart	

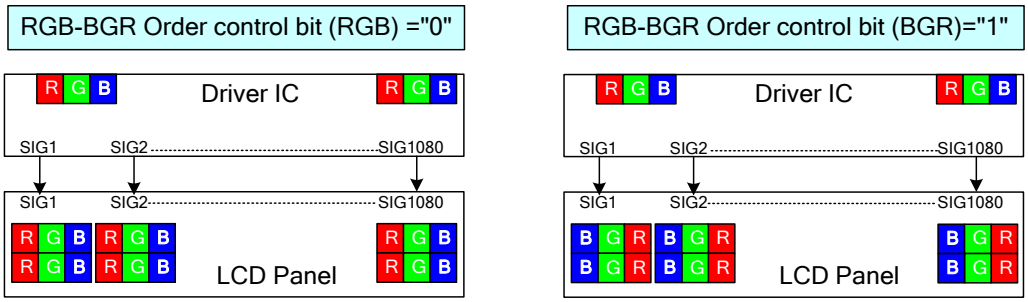
5.6.24. Memory Access Control (36h)

Page 0 Command Set		36h : MADCTL (Display Access Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	1	0	36h
1st Parameter	Write	0	0	0	0	BGR	0	SS	GS	00h

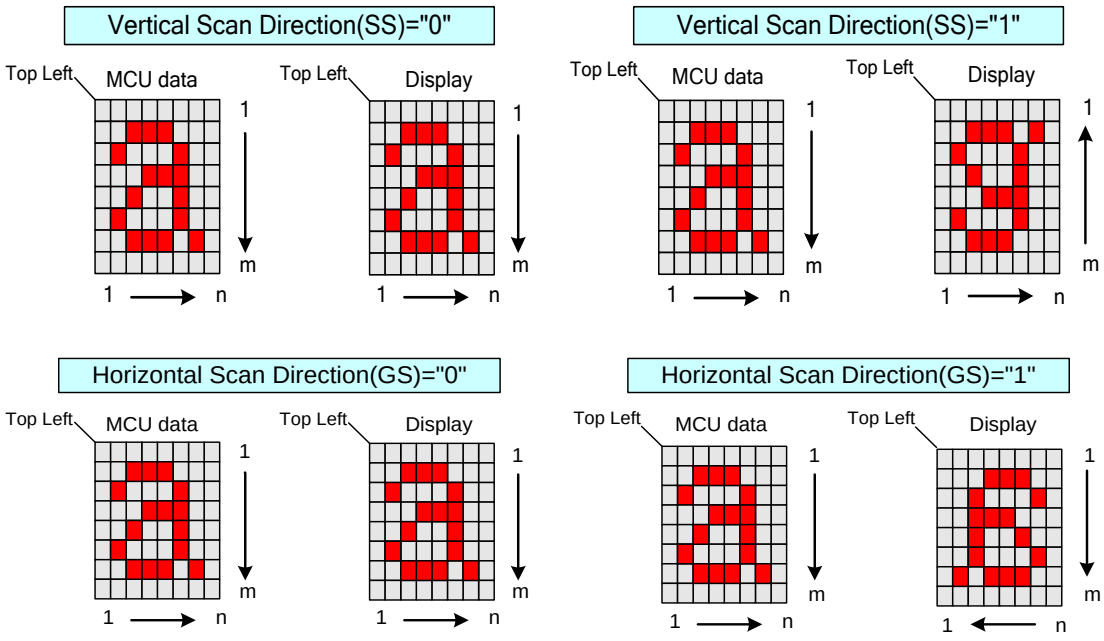
Description

This command makes no change on the other driver status.

Bit	Description	Value	Status
D3	RGB/BGR Order	0	RGB
		1	BGR
D1	SS	0	Source output Left to Right
		1	Source output Right to Left
D0	GS	0	Gate output Top to Bottom
		1	Gate output Bottom to Top



Top-Left (0,0) means a physical display location



Restriction: None.

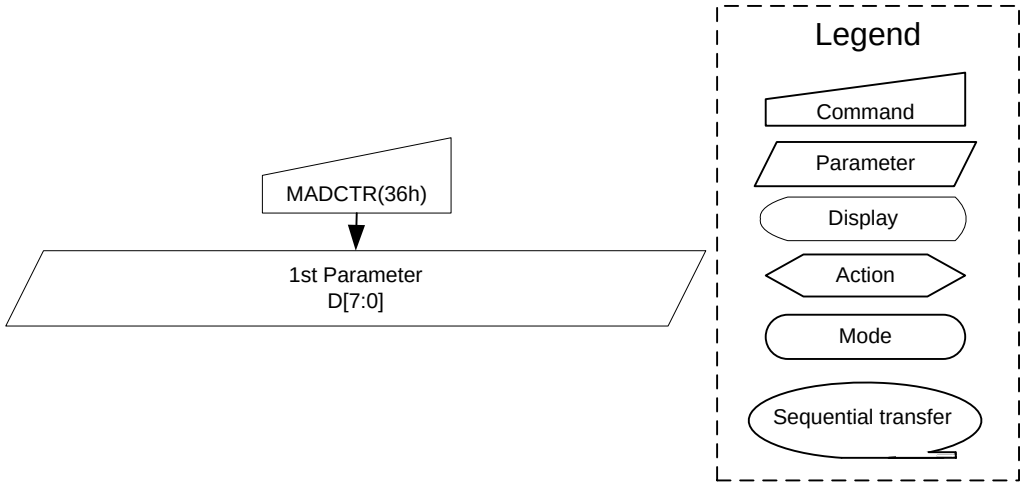
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.6.25. Write Display Brightness Value (51h)

Page 0 Command Set		51h : WRDISBV (Write Display Brightness)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	0	1	51h
1st Parameter	Write	0	0	DBV[13:8]						00h
2nd Parameter	Write	DBV[7:0]								00h
Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 0000h value means the lowest brightness and 3FFFh value means the highest brightness.									
Restriction	None									

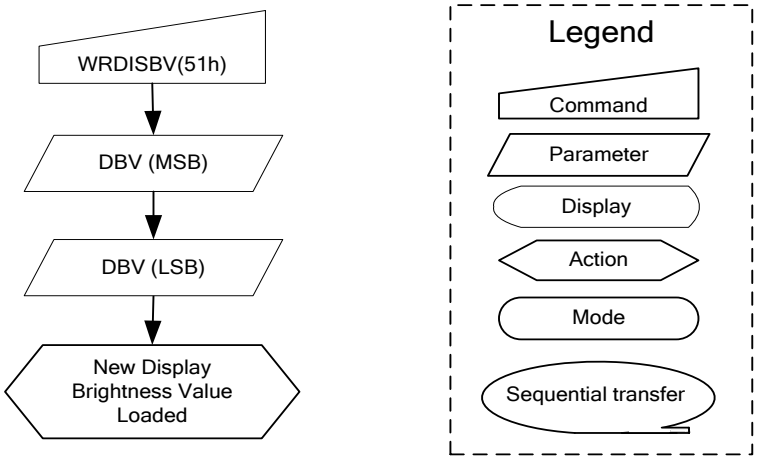
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



5.6.26. Read Display Brightness Value (52h)

Page 0 Command Set		52h : RDDISBV (Read Display Brightness Value)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	0	52h
1st Parameter	Read	0	0	DBV[13:8]						00h
2nd Parameter	Read	DBV[7:0]								00h

Description

This command returns the brightness value of the display.

It should be checked what the relationship between this returned value and output brightness of the display.

This relationship is defined on the display module specification.

In principle the relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness.

DBV[11:0] is reset when display is in Sleep In mode.

DBV[11:0] is '0', when bit BCTRL of Write CTRL Display Value command (53h) is '0'.

DBV[11:0] is manual set brightness specified with Write CTRL Display Value command (53h), when bit BCTRL of Write CTRL Display Value command (53h) is '1'.

When bit BCTRL of Write CTRL Display command (53h) is '1' and the setting value of Write Power Save command (55h) is '0', DBV[11:0] output is the brightness value specified with Write Display Brightness Value command (51h).

Restriction

None

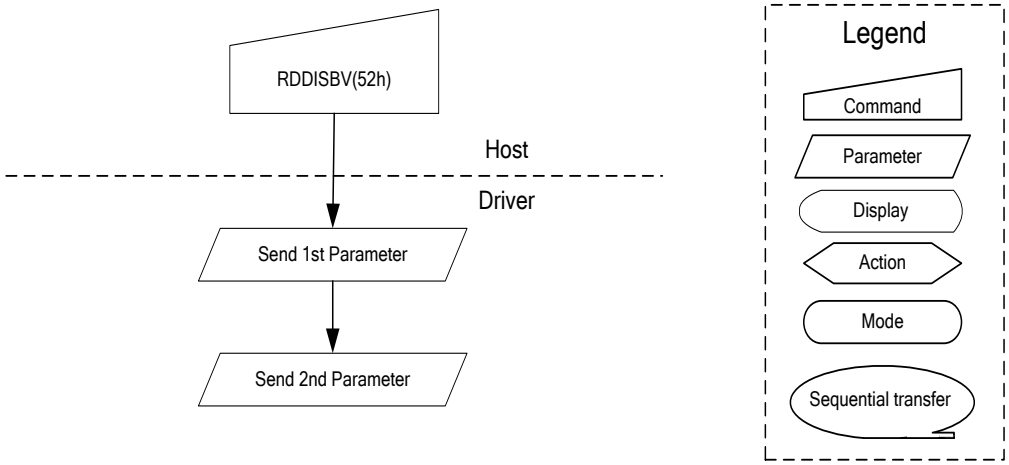
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



5.6.27. Write CTRL Display Value (53h)

Page 0 Command Set		53h : WRCTRLD (Write Control Display)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	1	53h
1st Parameter	Write	HBM[1:0]		BCTRL	0	DD	BL	0	0	00h

Description

This command is used to control the display brightness.

HBM: High Brightness Mode

HBM[1]	HBM[0]	Description
0	0	High brightness mode is off
0	1	High brightness mode is on. LCD: LED boost signal is ON. CABC_PWM_OUT= 100% PWM.
1	0	High brightness mode is on. LCD: LED boost signal is ON. CABC_PWM_OUT= 100% PWM.
1	1	High brightness mode is on. LCD: LED boost signal is ON. CABC_PWM_OUT= 100% PWM.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness ControlBlock Off (DBV[11:0]=00h)
1	Brightness Control Block On (DBV[11:0] is active)

DD: Display Dimming Control. This function is only for manual brightness setting.

DD	Description
0	Display Dimming Off
1	Display Dimming On

BL: Backlight Control On/Off

BL	Description
0	Backlight Control Off
1	Backlight Control On

Dimming function is adapted to the brightness registers for display, when bit BCTRL of Write CTRL Display Value command (53h) is changed at bit DD=1, e.g. bit BCTRL: 0 -> 1 or 1-> 0.

When bit BL changes from “On” to “Off”, backlight is turned off without gradual dimming, even if Display Dimming On (bit DD=1) is selected.

Restriction

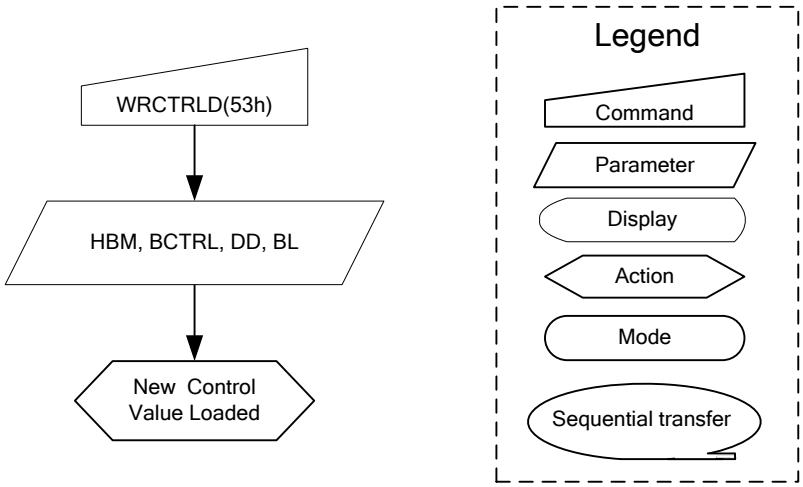
None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

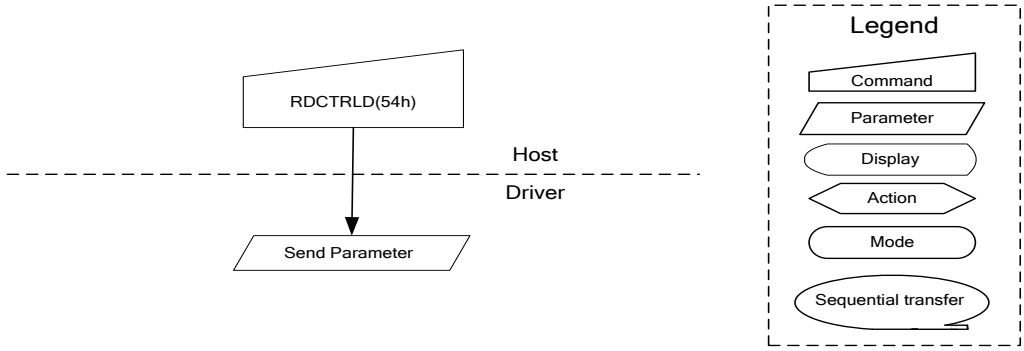
Flow Chart	

5.6.28. Read CTRL Display Value (54h)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">54h : RDCTRLD (Read Control Display Value)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>54h</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="2">HBM[1:0]</td><td>BCTRL</td><td>0</td><td>DD</td><td>BL</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">
This command returns the display brightness control values.

HBM: High Brightness Mode
<table>
<tr><th>HBM[1]</th><th>HBM[0]</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>High brightness mode is off</td></tr>
<tr><td>0</td><td>1</td><td>High brightness mode is on. LCD: LED boost signal is ON. CABC_PWM_OUT= 100% PWM.</td></tr>
<tr><td>1</td><td>0</td><td>High brightness mode is on. LCD: LED boost signal is ON. CABC_PWM_OUT= 100% PWM.</td></tr>
<tr><td>1</td><td>1</td><td>High brightness mode is on. LCD: LED boost signal is ON. CABC_PWM_OUT= 100% PWM.</td></tr>
</table>
BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.
<table>
<tr><th>BCTRL</th><th>Description</th></tr>
<tr><td>0</td><td>Brightness Control Block Off (DBV[11:0]=00h)</td></tr>
<tr><td>1</td><td>Brightness Control Block On (DBV[11:0] is active)</td></tr>
</table>
DD: Display Dimming Control. This function is only for manual brightness setting.
<table>
<tr><th>DD</th><th>Description</th></tr>
<tr><td>0</td><td>Display Dimming Off</td></tr>
<tr><td>1</td><td>Display Dimming On</td></tr>
</table>
BL: Backlight Control On/Off
<table>
<tr><th>BL</th><th>Description</th></tr>
<tr><td>0</td><td>Backlight Control Off</td></tr>
<tr><td>1</td><td>Backlight Control On</td></tr>
</table>
Dimming function is adapted to the brightness registers for display, when bit BCTRL of Write CTRL Display Value command (53h) is changed at bit DD=1, e.g. bit BCTRL: 0 -> 1 or 1-> 0.

When bit BL changes from “On” to “Off”, backlight is turned off without gradual dimming, even if Display Dimming On (bit DD=1) is selected.
</td></tr>
<tr><td>Restriction</td><td colspan="10">None</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

5.6.29. Write Power Save (55h)

Page 0 Command Set		55h : PWRSAVE (Write Power Save)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	0	1	55h
1st Parameter	Write	PWRSAVE[7:0]								00h

Description

This command is used to write the setting for power save control functionalities.

D7	D6	D5	D4	D3	D2	D1	D0	Function	Note
0	0	0	0	0	0	0	0	Power Save Off	-
0	0	0	0	0	0	0	1	Power Save Low	Conservative Setting of CABC/DBLC
0	0	0	0	0	0	1	0	Power Save Medium	Medium Setting of CABC/DBLC
0	0	0	0	0	0	1	1	Power Save High	Aggressive Setting of CABC/DBLC
1	0	0	0	X	X	X	X	IE On - Low	Low Enhancement of LCD
1	0	0	1	X	X	X	X	IE On – Medium	Medium Enhancement of LCD
1	0	1	1	X	X	X	X	IE On – High	High Enhancement of LCD
0	1	0	0	X	X	X	X	SRE – Low	Sunlight readability enhancement
0	1	0	1	X	X	X	X	SRE –Medium	Sunlight readability enhancement
0	1	1	0	X	X	X	X	SRE - High	Sunlight readability enhancement
Other Setting								-	Prohibited

CABC = Content Adaptive Brightness Control

DBLC = Dynamic Backlight Control (RGBW pixel structure, where is 2 sub pixels per pixel, is used on the display panel or a similar solution)

IE = Image Enhancement

X = 0 or 1

Restriction: None

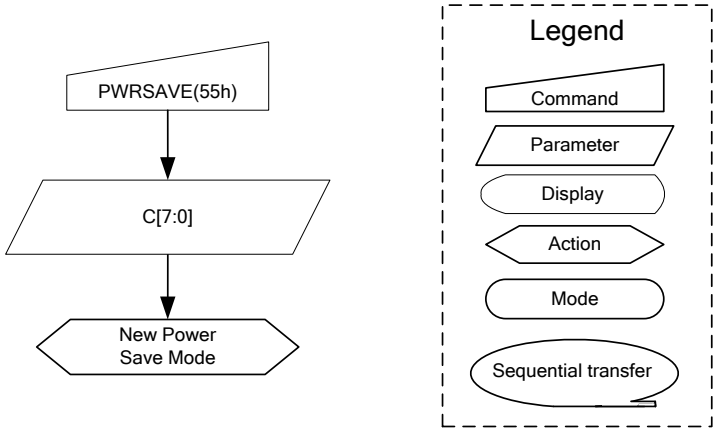
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

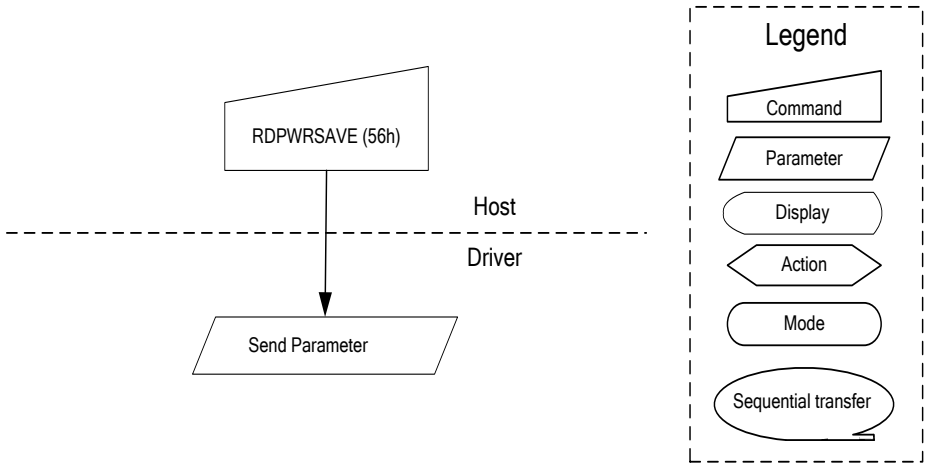
Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.6.30. Read Power Save (56h)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">56h : RDPWRSAVE (Read Power Save)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>56h</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="8">PWRSAVE[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to read the setting for power save control functionalities.
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Function</th><th>Note</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Power Save Off</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Power Save Low</td><td>Conservative Setting of CABC/DBLC</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Power Save Medium</td><td>Medium Setting of CABC/DBLC</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Power Save High</td><td>Aggressive Setting of CABC/DBLC</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>IE On - Low</td><td>Low Enhancement of LCD</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>IE On – Medium</td><td>Medium Enhancement of LCD</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>IE On – High</td><td>High Enhancement of LCD</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>SRE – Low</td><td>Sunlight readability enhancement</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>SRE –Medium</td><td>Sunlight readability enhancement</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>SRE - High</td><td>Sunlight readability enhancement</td></tr>
<tr><td colspan="8">Other Setting</td><td>-</td><td>Prohibited</td></tr>
</table>
CABC = Content Adaptive Brightness Control
DBLC = Dynamic Backlight Control (RGBW pixel structure, where is 2 sub pixels per pixel, is used on the display panel or a similar solution)
IE = Image Enhancement
X = 0 or 1</td></tr>
<tr><td>Restriction</td><td colspan="10">None</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

5.6.31. Write CABC Minimum Brightness (5Eh)

Page 0 Command Set		5Eh : WRCABCMB (Write CABC Minimum Brightness)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	1	1	1	0	5Eh
1st Parameter	Write	0	0	0	0	CMB[11:8]				00h
2nd Parameter	Write	CMB[7:0]								00h
Description	This command is used to set the minimum brightness value of the display for CABC function. CMB[11:0]: CABC minimum brightness control, this parameter is used to set a limit to the amount of brightness reduction allowed. When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function works as normal, even if the brightness can not be changed. This function does not affect manual brightness setting. Manual brightness setting does not have a limit on allowable brightness reduction; display brightness can be set less than CABC minimum brightness. Smooth transition and dimming function work as normal. When display brightness is turned off (bit BCTRL of Write CTRL Display Value command (53h) is '0'), CABC minimum brightness setting is ignored. The principle relationship is such that 0000h value means the lowest brightness for CABC and 0FFFh value means the highest brightness for CABC.									
Restriction	None									

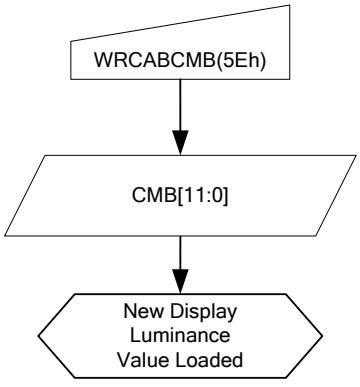
Register Availability

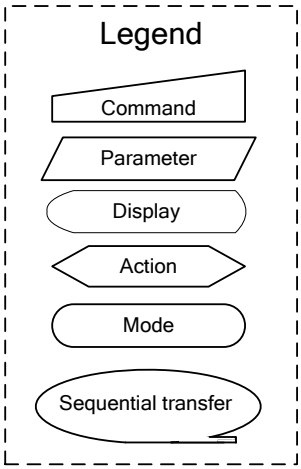
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart





5.6.32. Read CABC Minimum Brightness (5Fh)

Page 0 Command Set		5Fh : RDCABCMB (Read CABC Minimum Brightness)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	1	1	1	1	5Fh
1st Parameter	Read	0	0	0	0	CMB[11:8]				00h
2nd Parameter	Read	CMB[7:0]								00h

Description

This command returns the minimum brightness value of CABC function.

The principle relationship is such that 0000h value means the lowest brightness and 0FFFh value means the highest brightness.

CMB[11:0] is CABC minimum brightness specified with Write CABC minimum brightness command (5Eh).

Restriction

None

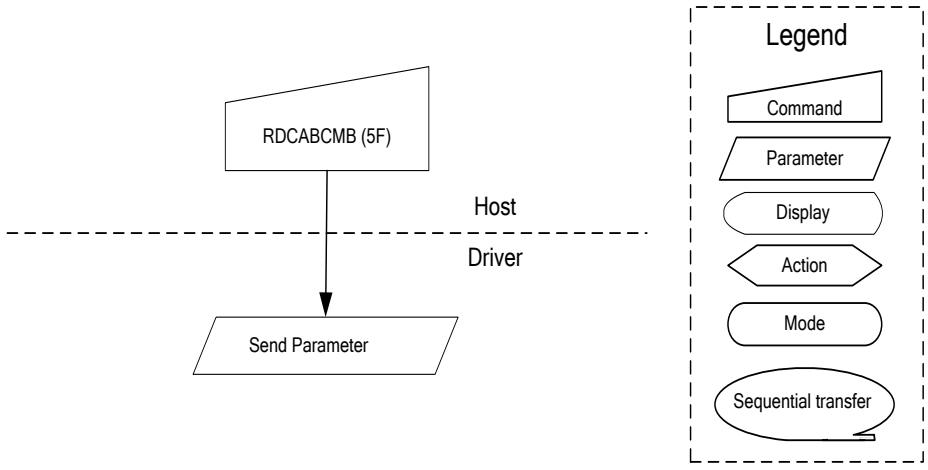
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



5.6.33. Set Transition Time (68h)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">68h : SET_TT (Set Transition Time)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>68h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">TT_STP[7:0]</td><td>00h</td></tr>
<tr><td>2nd Parameter</td><td>Write</td><td colspan="8">ST_TIM[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">
This command controls the total transition time of Display Dimming function.

Transition time is adjusted with two parameters, defining as follows:

1st Parameter TT_STP [7:0] defines the number of dimming steps for transition.
<table>
<tr><th>TT_STP[7:0]</th><th>Description</th></tr>
<tr><td>00h</td><td>1 step</td></tr>
<tr><td>01h</td><td>2 step</td></tr>
<tr><td>02h</td><td>4 step</td></tr>
<tr><td>03h</td><td>8 step</td></tr>
<tr><td>04h</td><td>16 step</td></tr>
<tr><td>05h</td><td>32 step</td></tr>
<tr><td>06h</td><td>64 step</td></tr>
<tr><td>07h</td><td>128 step</td></tr>
<tr><td>08h</td><td>256 step</td></tr>
<tr><td>09h</td><td>512 step</td></tr>
<tr><td>0Ah</td><td>1024 step</td></tr>
<tr><td>0Bh</td><td>2048 step</td></tr>
<tr><td>0Ch</td><td>4096 step</td></tr>
<tr><td>Others</td><td>Reserved</td></tr>
</table>
2nd Parameter ST_TIM [7:0] defines the step time as frame units for each dimming step.
<table>
<tr><th>ST_TIM[7:0]</th><th>Description</th></tr>
<tr><td>00h</td><td>1 frame</td></tr>
<tr><td>01h</td><td>1 frame</td></tr>
<tr><td>02h</td><td>2 frame</td></tr>
<tr><td>03h</td><td>3 frame</td></tr>
<tr><td>04h</td><td>4 frame</td></tr>
<tr><td>05h</td><td>5 frame</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>FBh</td><td>251 frame</td></tr>
<tr><td>FCh</td><td>252 frame</td></tr>
<tr><td>FDh</td><td>253 frame</td></tr>
<tr><td>FEh</td><td>254 frame</td></tr>
<tr><td>FFh</td><td>255 frame</td></tr>
</table>
Thereby, total transition time for dimming can be calculated as follows:

TT_STP [7:0] * ST_TIM [7:0] = TT, where TT unit is frame. Value 0000h means the transition is instant.

However, concerning relation with Display Brightness block, implementation should allow step selection between range from 0 to 4096.

When bit DD of Write CTRL Display Value command (53h) is ‘1’, the transition time of dimming shall be the same when display brightness is increased or decreased.
</td></tr>
<tr><td>Restriction</td><td colspan="10">None</td></tr>
</table>

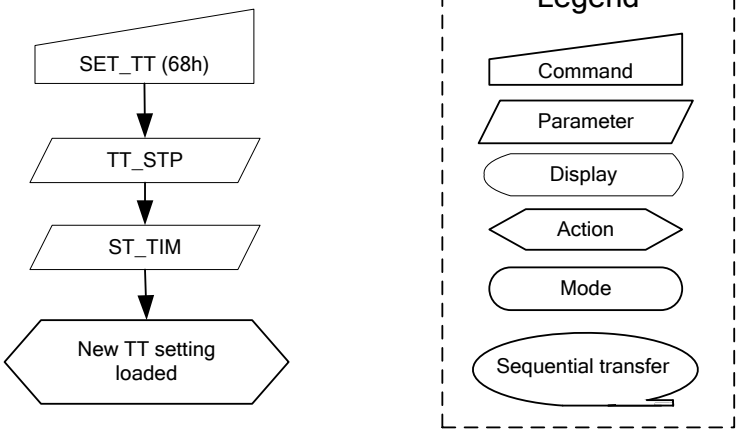
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



5.6.34. Get Transition Time (69h)

Page 0 Command Set		69h : GET_TT (Get Transition Time Value)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	1	0	1	0	0	1	69h
1st Parameter	Read	TT_STP[7:0]								00h
2nd Parameter	Read	ST_TIM[7:0]								00h

Description

This readout returns the Transition Time value of Display Dimming function, described in Set Transition Time command (68h).

Transition time is adjusted with two parameters, defining as follows:

1st Parameter TT_STP [7:0] defines the number of dimming steps for transition.

TT_STP[7:0]	Description
00h	1 step
01h	2 step
02h	4 step
03h	8 step
04h	16 step
05h	32 step
06h	64 step
07h	128 step
08h	256 step
09h	512 step
0Ah	1024 step
0Bh	2048 step
0Ch	4096 step
Others	Reserved

2nd Parameter ST_TIM [7:0] defines the step time as frame units for each dimming step.

ST_TIM[7:0]	Description
00h	1 frame
01h	1 frame
02h	2 frame
03h	3 frame
04h	4 frame
05h	5 frame
:	:
:	:
FBh	251 frame
FCh	252 frame
FDh	253 frame
FEh	254 frame
FFh	255 frame

Restriction: None

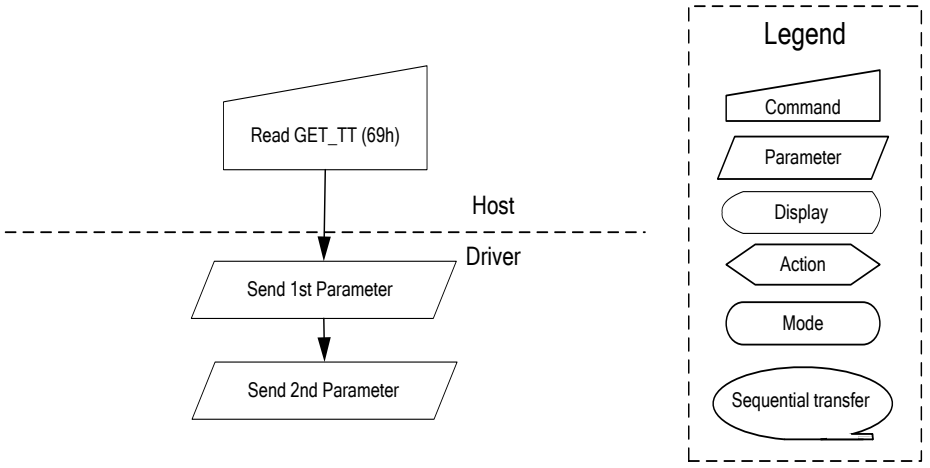
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



5.6.35. Read DDB Start (A1h)

Page 0 Command Set		A1h : RDDDBS (Read DDB Start)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	1	0	0	0	0	1	A1h
1st Parameter	Read	SID[7:0]								00h
2nd Parameter	Read	SID[15:8]								00h
3rd Parameter	Read	MID[7:0]								00h
4th Parameter	Read	MID[15:8]								00h
5th Parameter	Read	RID[7:0]								00h
6th Parameter	Read	RID[15:8]								00h
7th Parameter	Read	1	1	1	1	1	1	1	1	FFh

Description

This command returns supplier identification and display module model/revision information.

Note: This information is not the same what "Read ID1 (DAh)", "Read ID2 (DBh)" and "Read ID3 (DCh)" commands are returning.

Parameter 1：SID[7:0] LCD module's manufacturer ID.

Parameter 2：SID[15:8] LCD module/driver version ID.

Parameter 3：MID[7:0] LCD module/driver ID.

Parameter 4：MID[15:8] IC version code.

Parameter 5：RID[7:0] Customer ID

Parameter 6：RID[15:8] Customer ID

Parameter 7：FFh - Exit code – there is no more data in the Descriptor Block

This read sequence can be interrupted by any command and it can be continued by "Read DDB Continue (A8h)" command. For example, RDDDBS (A1h) => 1st parameter has been sent => 2nd parameter has been sent => interrupt => RDDDBC (A1h) => 3rd parameter of the RDDDBS has been sent.

Note:

These ID informations are not the same what "Read ID1 (DAh)", "Read ID2 (DBh)" and "Read ID3 (DCh)" commands are returned value.

Maximum DDB data length is 6 bytes with NVM program.

Restriction

None

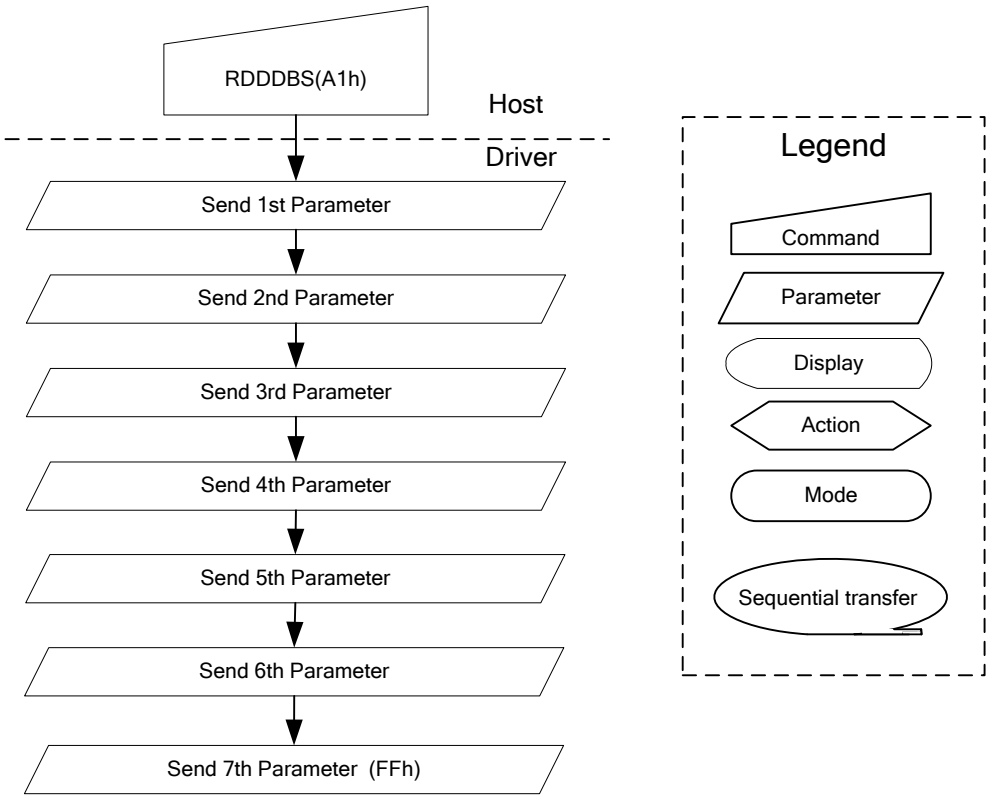
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before NVM program)	Default Value (After NVM program)
Power On Sequence	00h_00h_00h_00h_00h_00h_FFh	NVM value
S/W Reset	00h_00h_00h_00h_00h_00h_FFh	NVM value
H/W Reset	00h_00h_00h_00h_00h_00h_FFh	NVM value

Note: default value of 7th paramer of RDDDBS (A1h) always FFh before/after NVM program.

Flow Chart	

5.6.36. Read DDB Continue (A8h)

Page 0 Command Set		A8h : RDDDBC (Read DDB Continue)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	1	0	1	0	0	0	A8h
1st Parameter	Read	D1[7:0]								00h
2nd Parameter	Read	D2[7:0]								00h
:	Read	Dx[7:0]								00h
Nth Parameter	Read	Dn[7:0]								00h

Description

This command is used to return the supplier's identification and revision information from the point where RDDDBS (A1h) was interrupted by another command.

A Read DDB Start command (A1h) should be executed at least once before a Read DDB Continue command (A8h) to define the read location.

Restriction

None

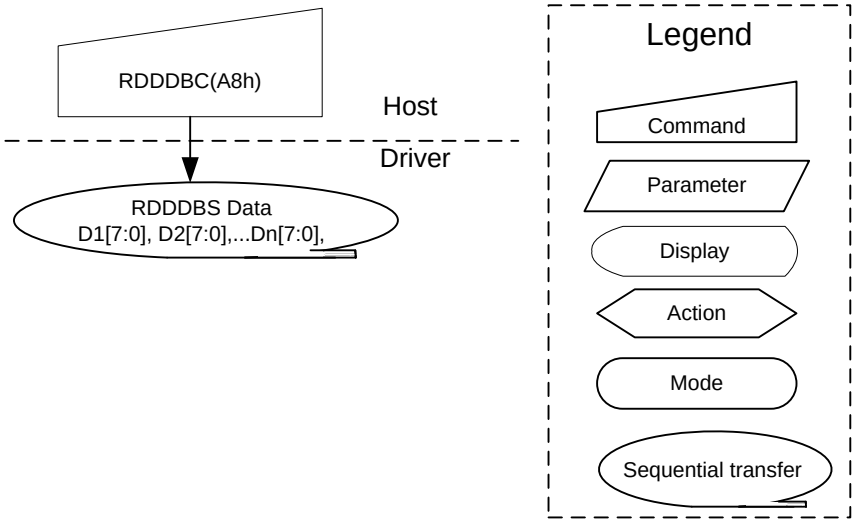
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.6.37. Read First Checksum (AAh)

Page 0 Command Set		AAh : RDFCS (Read First Checksum)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	1	0	1	0	1	0	AAh
1st Parameter	Read	FCS[7:0]								00h
Description	This command returns the first checksum calculated from Page 0 area registers after the write access to those registers has been done.									
Restriction	It will be necessary to wait 150ms after there is the last write access on Page 0 area registers before there can read this checksum value.									

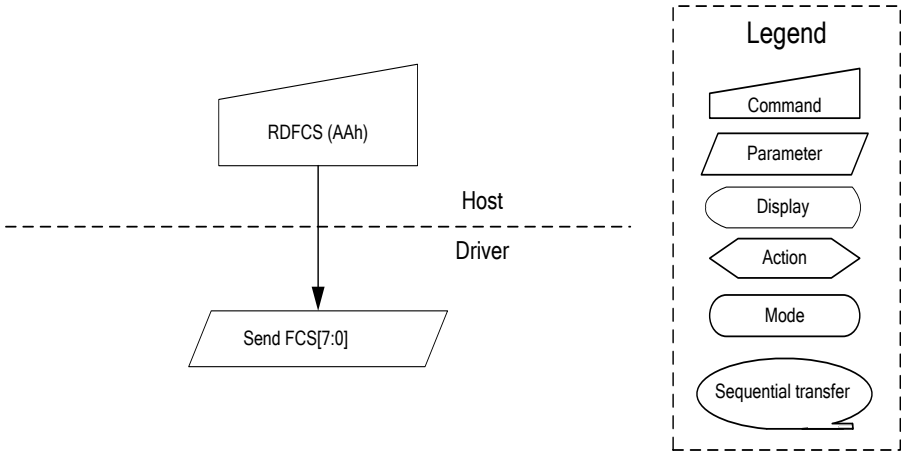
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.6.38. Read Continue Checksum (AFh)

Page 0 Command Set		AFh : RDCFCS (Read Continue Checksum)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	1	0	1	1	1	1	AFh
1st Parameter	Read	CCS[7:0]								00h
Description	This command returns the continue checksum that has been calculated continuously after the first checksum has calculated from Page 0 area registers after the write access to those registers has been done.									
Restriction	It will be necessary to wait 300ms after there is the last write access on Page 0 area registers before there can read this checksum value in the first time.									

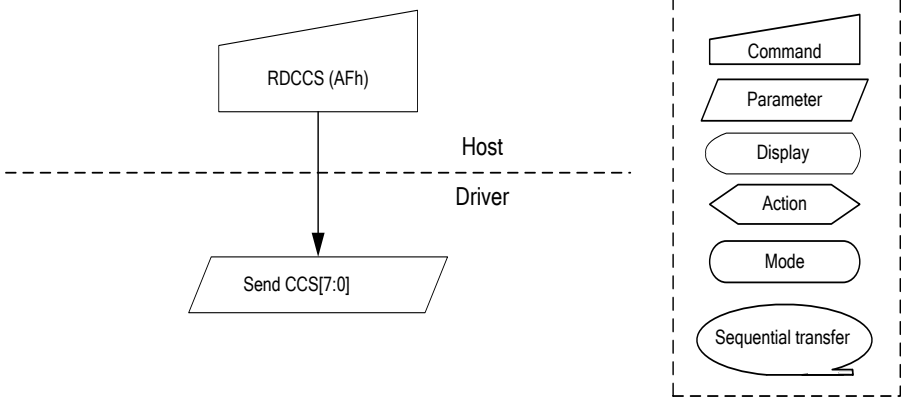
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.6.39. Read ID1 (DAh)

Page 0 Command Set		DAh : RDID1 (Read ID1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	0	1	0	DAh
1st Parameter	Read	ID1[7:0]								00h
Description	This read byte is used to track the LCD module/driver version. It is defined by the display supplier and changes each time a revision is made to the display, material or construction specifications. The ID1 is programmed by NVM function.									
Restriction	None									

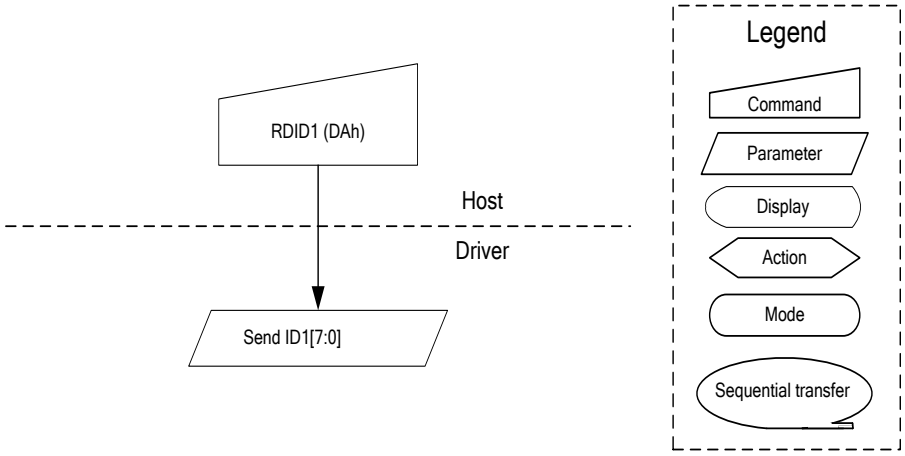
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before NVM program)	Default Value (After NVM program)
Power On Sequence	00h	NVM value
S/W Reset	00h	NVM value
H/W Reset	00h	NVM value

Flow Chart



5.6.40. Read ID2 (DBh)

Page 0 Command Set		DBh : RDID2 (Read ID2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	0	1	1	DBh
1st Parameter	Read	ID2[7:0]								80h
Description	This read byte is used to track the LCD module/driver version. It is defined by the display supplier and changes each time a revision is made to the display, material or construction specifications. This ID parameter range is from 80h to FFh. The ID2 is programmed by NVM function.									
Restriction	None									

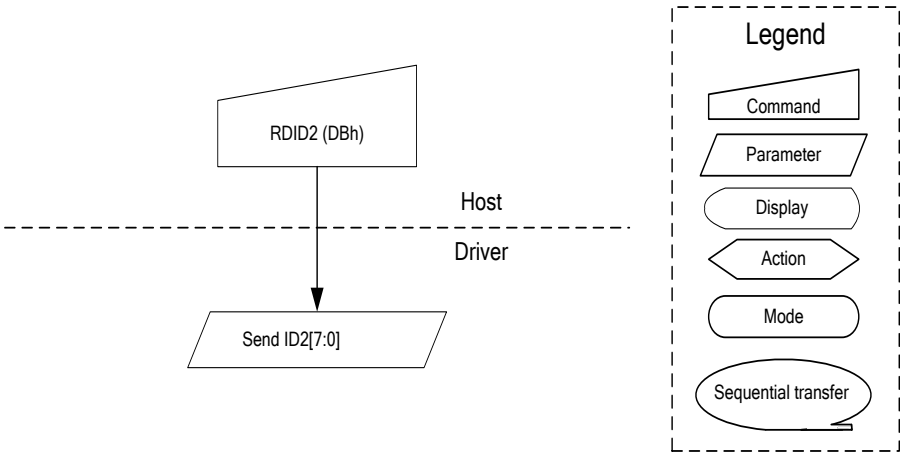
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before NVM program)	Default Value (After NVM program)
Power On Sequence	80h	NVM value
S/W Reset	80h	NVM value
H/W Reset	80h	NVM value

Flow Chart



5.6.41. Read ID3 (DCh)

Page 0 Command Set		DCh : RDID3 (Read ID3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	1	0	0	DCh
1st Parameter	Read	ID3[7:0]								00h

Description

This read byte identifies the LCD module/driver. It is specified by User.

The ID3 is programmed by NVM function.

Restriction

None

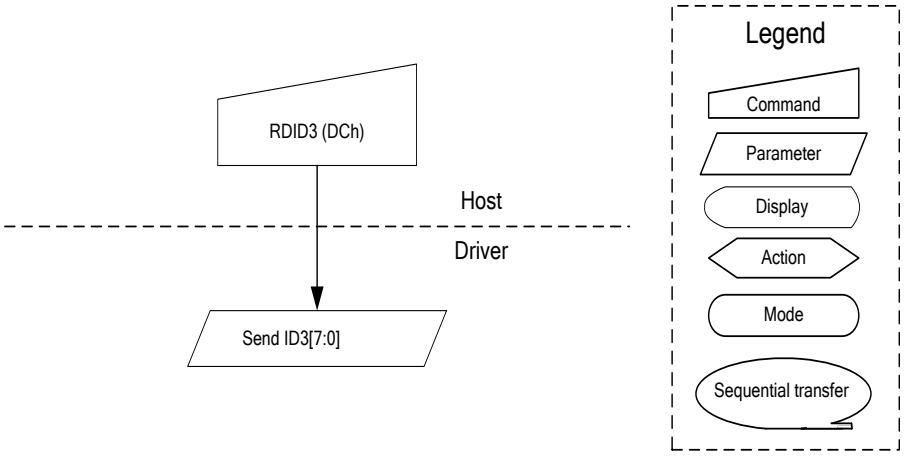
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before NVM program)	Default Value (After NVM program)
Power On Sequence	00h	NVM value
S/W Reset	00h	NVM value
H/W Reset	00h	NVM value

Flow Chart



5.6.42. EXTC Command Set Enable (FFh)

Page 0 Command Set		FFh : EXTC Command Set Enable								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	1	1	1	1	1	FFh
1st Parameter	Write	0	1	1	1	1	0	0	0	78h
2nd Parameter	Write	0	0	0	0	0	1	1	1	07h
3rd Parameter	Write	PAGE[7:0]								00h

Description

PAGE[7:0]**:** Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
0Bh	Page 11
0Ch	Page 12
0Dh	Page 13
0Eh	Page 14
Others	Reserved

Set the register, 1st Parameter = 78h, 2nd Parameter = 07h, 3rd Parameter = Page value to enable “page command set” available.

See chapter “5.1. Command Flow”.

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	78h_07h_00h
S/W Reset	78h_07h_00h
H/W Reset	78h_07h_00h

6. TE Pad Output Signal

Tearing Effect Line signal can be output from TE pad as synchronous signal. TE signal is trigger for MCU monitor display model normally working or not. Tearing Effect Output signal is turned on/off by Tearing Effect Line Off command (34h) and Tearing Effect Line On command (35h).

Table 38. TE Pad Output

TEON (represents status of 35h command)	M (35h 1st parameter)	TE pad output
0	X	VSS
1	0	TE Mode 1
1	1	TE Mode 2

Tearing Effect signal mode is defined by bit "M" of 1st parameter of Tearing Effect Line On command (35h). Write M=0 when using DSI TE reporting function.

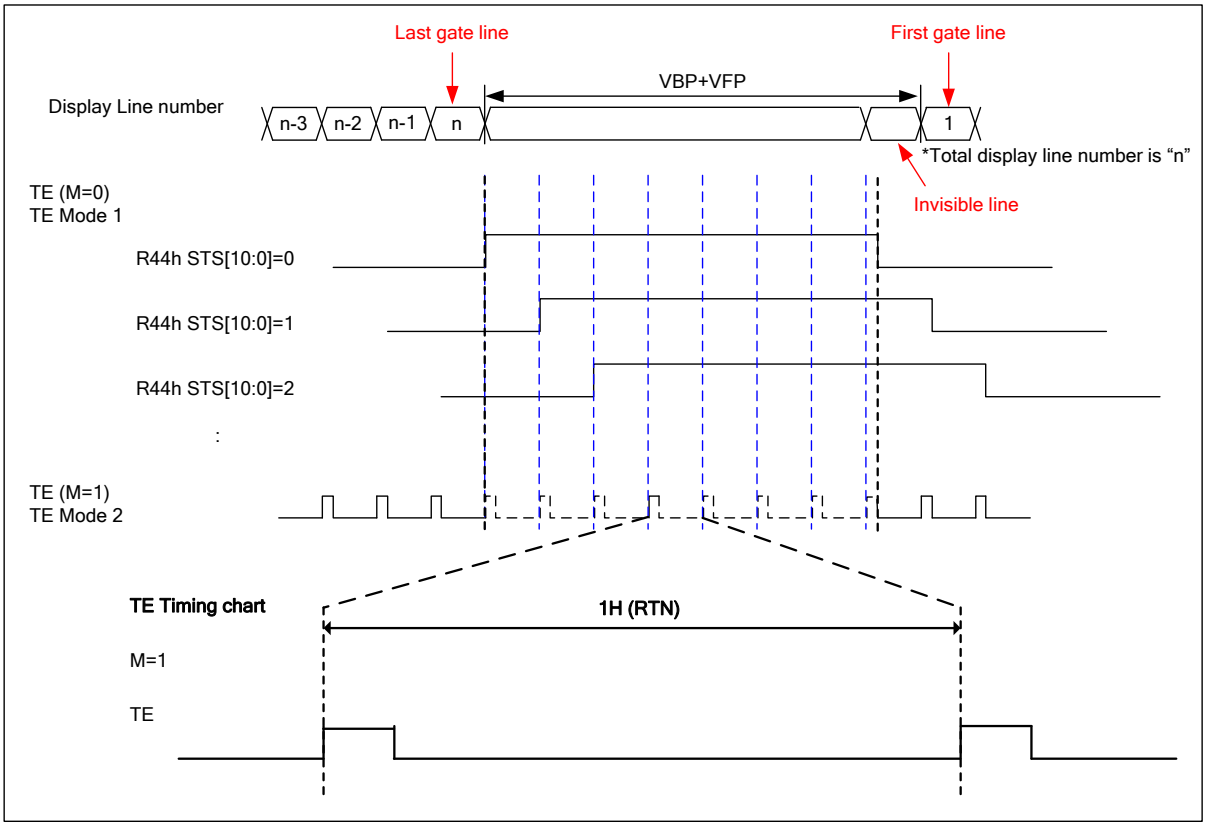


Figure 85. TE Pad Output Signal & Set Tear Scan Line command (44h)

7. CABC (Content Adaptive Brightness Control) Function

The CABC, a dynamic backlight control function, drastically reduces power consumption of the luminance source. The ILI7807S will refer the gray scale content of the display image to output the CABC_PWM_OUT pulse to the LED driver. The content of gray scale can be increased while simultaneously lowering the brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and the power consumption reduction depend on the content of the image.

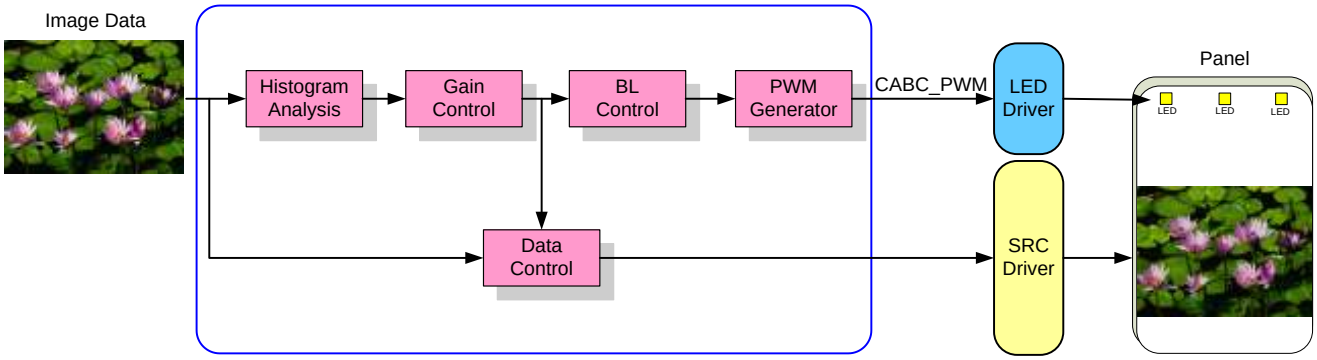


Figure 86. CABC Block Diagram

The ILI7807S can calculate the backlight brightness level and send a CABC_PWM_OUT pulse to the LED driver via CABC_PWM_OUT pad for backlight brightness control purposes. The PWM frequency can be adjusted by PWM_DIV parameters, and the calculating equation is shown below.

$$f_{LEDPWM} = \frac{32MHz}{(PWM\_DIV[7:0]+1)} \text{ X PWM\_DUTY\_PRECISOIN}$$

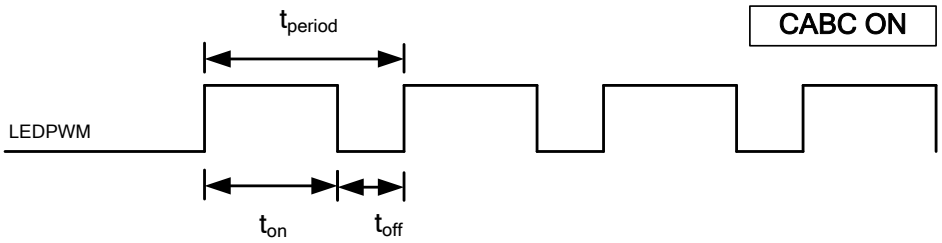


Figure 87. CABC_PWM_OUT on/off period

8. AWB (Auto White Balance) Adjust Function

The color temperature of a light source is the temperature of an ideal black body radiator that radiates light of comparable hue to that of the light source. In LCD, color temperature is mainly determined by backlight LED. ILI7807S uses AWB function to change prefered white balance within a specific range.

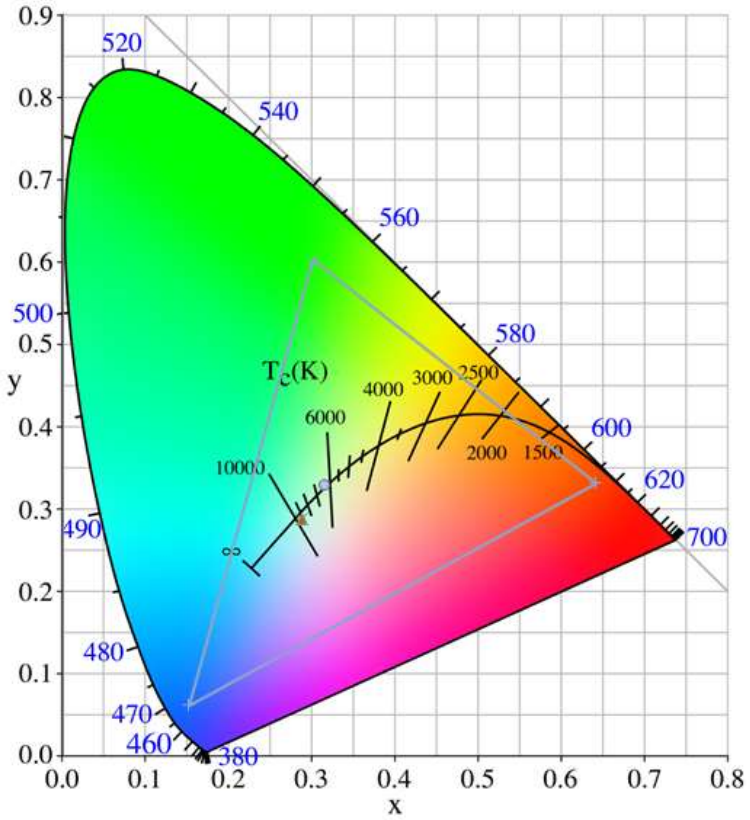
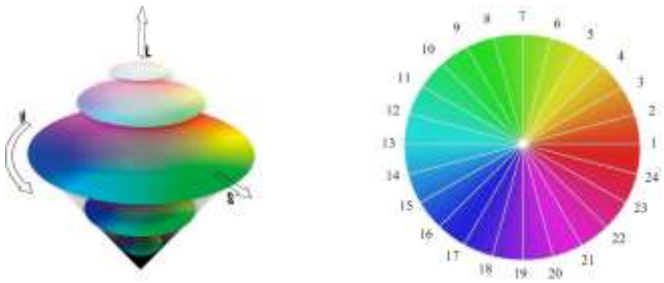


Figure 88. Adjust Color Temperature of White Point

9. Impressive Image Enhancement (IIE) Function

9.1. Saturation (Color Enhancement)

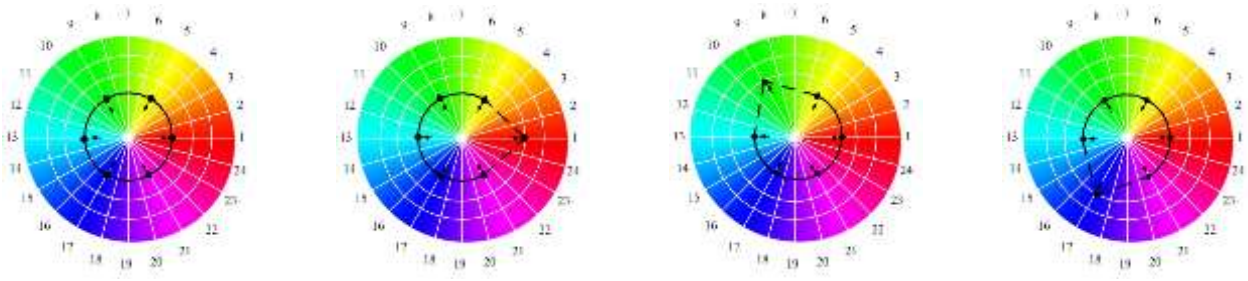
In this design, it provides the saturation enhancement to make the image content more vivid. The main concept in this feature is to enhance the color information on HSL domain, which includes the saturation information of each different color, show as Figure 89 (a) The user can simply adjust the saturation enhancement level by setting Write Power Save command (55h). In this design, it also provides the saturation enhancement for each different color-axis, show as Figure 89 (b).



(a) HSL model (b) the definition of 24 color-axis

Figure 89. HSL model and the definition of 24 color-axis.

The user can define the saturation enhancement level for each color-axis through the CMD command, such as red, yellow, green, cyan, blue and magenta (24 color-axis), the example of enhancement application shows in Figure 90. (Reserved Description)



(a) All color-axis with same level (b) higher level in red-axis (c) higher level in green-axis (d) higher level in blue-axis

Figure 90. Example of saturation enhancement application (24 color-axis). (Reserved)

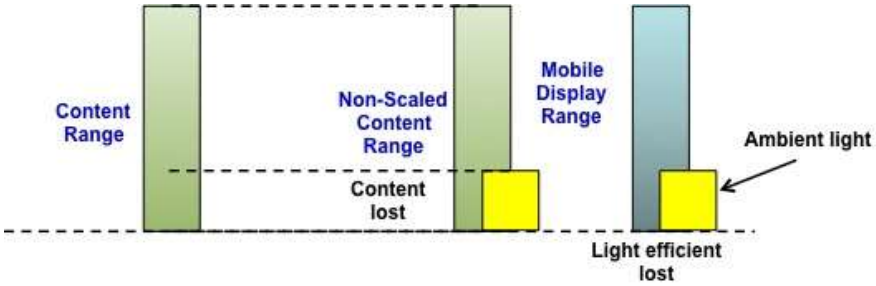
In Figure 91, there is an example for saturation enhancement. Different enhancement levels being applied in this example.

(a)Original (b) Low Level (c) Medium Level (d) High Level

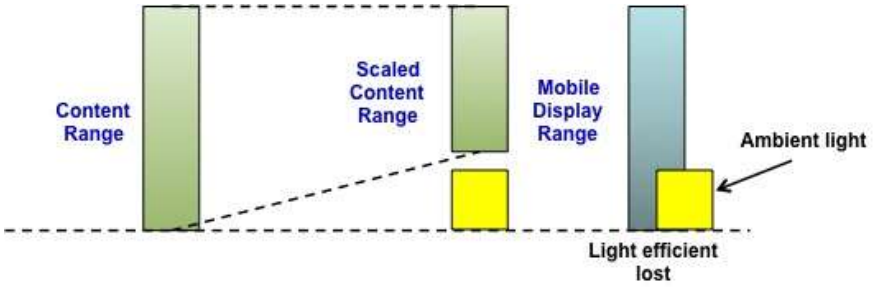
Figure 91. Example of saturation enhancement application (Picture).

9.2. Sunlight Readability Enhancement (SRE)

The sunlight readability enhancement is in order to achieve high visibility in daylight or other bright light condition. Figure 92 (a) shows the main concept of the influence of ambient light to the LCD displayer and the solution in the high ambient light condition. In this design, it changes the image content to achieve the high visibility in the ambient light condition as shows in Figure 92 (b).



(a) Backlight efficiency is consumed by ambient light



(b) Enhance the image content to avoid the influence

Figure 92. Main concept of Sunlight Readability Enhancement

9.3. Contrast Enhancement

The contrast between the dark and light, indicate the clarity of the image content. In this design, it provides contrast enhancement to increase the difference between dark and light to achieve the high contrast image. The user can select the enhancement level by setting command, the example shows below.

Figure 93. Original & After contrast enhancement.

9.4. Hue Adjustment

Hue means a color that can be described, like red, blue or green. In this design, it provides the hue adjustment to change color from one to another. The user can select the adjustment level by setting command, the example shows below.

Figure 94. Original & After Hue Adjustment.

9.5. Sharpness Enhancement

The sharpness indicates the clarity at the edge of the image content. In this design, it provides sharpness enhancement to increase the difference between the content of the edge to achieve the high sharpness image. The user can select the enhancement level by setting command, the example shows below.

Figure 95. Original & After sharpness enhancement.

10. Source Driver

The source driver uses 1080 channels (S1~S1080) which are used for driving the source line of the TFT LCD panel. The source driver converts the digital data into the analog voltage and generates the corresponding gray scale voltage output, enabling up to 16.7M colors to be displayed simultaneously. The output circuit of this source driver incorporates with an operational amplifier, so that a positive and a negative voltage can be alternately outputted from each channel.

11. Sleep Out Command and Self-diagnostic Functions

11.1. Register loading Detection

Sleep Out command (11h) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from NVM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the NVM and register values of the display controller by the display controller (1st step: Compares register and NVM values, 2nd step: Loads NVM value to register). If both values (NVM and register values) are the same, there is inverted bit (increased by 1), which is defined in the bit D[7] of Read Display Self-Diagnostic Result command (0Fh). If these values are not the same, the bit D[7] of Cmd. 0Fh is not inverted.

The flow chart for this internal function is following:

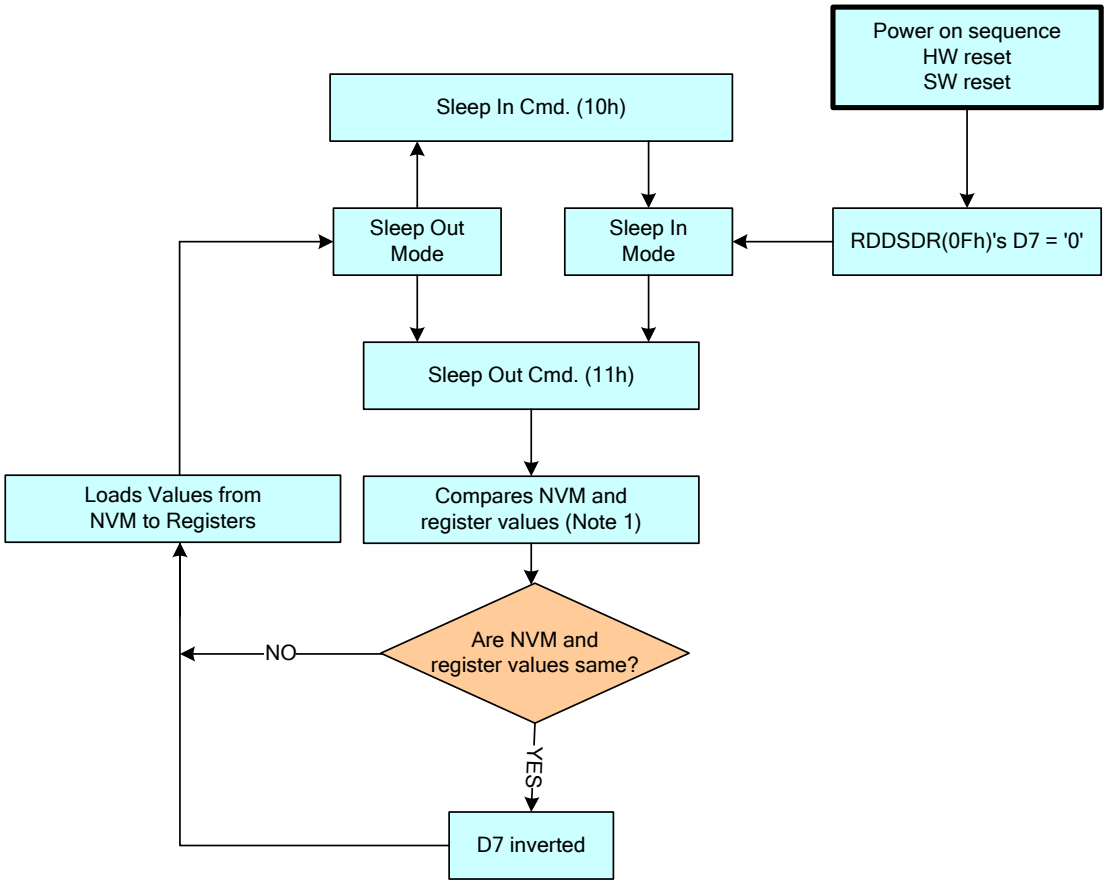


Figure 96. Register loading Detection

Note:

1. If the NVM and register values are not compared and loaded, they can be changed by 00h to AFh commands and DAh to DCh commands.
2. TE line state is ont affected by register loading detection of RDDSDR (0Fh).

11.2. Functionality Detection

The Sleep Out command (11h) is a trigger for an internal function of the display module. It indicates if the display module is still running and meets functionality requirements.

The internal function (display controller) is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirements are met, a bit is inverted (increased by 1), which defined in the bit D[6] of Read Display Self-Diagnostic Result command (0Fh). If functionality requirement is not the same, the bit D[6] of Cmd. 0Fh is not inverted (not increased by 1). The flow chart for this internal function is following:

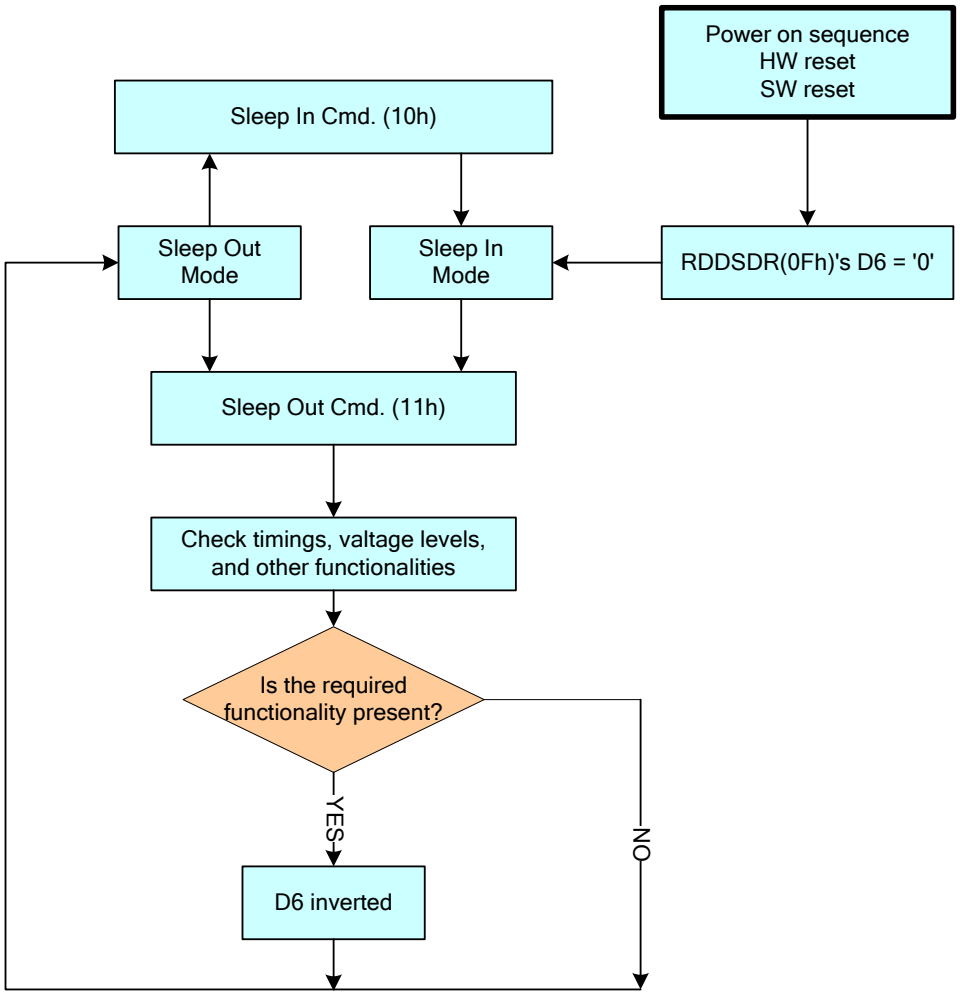


Figure 97. Functionality Detection

Note:

1. When changing from Sleep In mode to Sleep Out mode, 120msec waiting time is needed after the Sleep Out command (11h) before it is able to check if functionality requirements are met and a value of RDDSDR(0Fh)'s D6 is valid. Otherwise, there will be 5msec delay for the D6's value to be valid when the Sleep Out command (11h) is sent in the Sleep Out mode.
2. TE line state is ont affected by functionality detection of RDDSDR (0Fh).

11.3. Abnormal Power Off

The abnormal power off means a situation when e.g. there is removed a battery without the normal power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abnormal power off event, ILI7807S will force the display to blank and will not be any abnormal visible effects with in 1 second time on the display and remains blank until “Power On Sequence” powers it up.

12. Characteristics of I/O

12.1. Output or Bi-directional (I/O) Pads

Table 39. Characteristics of Output or Bi-directional (I/O) Pads

Pad/Line	Normal operating	After Hardware Reset
DATA0P	Hi-Z (Inactive)	Hi-Z (Inactive)
DATA0N	Hi-Z (Inactive)	Hi-Z (Inactive)
CABC_PWM_OUT	Low	Low
TE	Low	Low
TE1	Low	Low
TP_I2C_SCL	High/Low	High
TP_I2C _SDA	High/Low	High
TP_INT	High/Low	High
TP_SPI_MISO	High/Low	Low
TP_FLASH_CS	High/Low	High
TP_FLASH_SCK	High/Low	Low
TP_FLASH_MISO	High/Low	High
TP_FLASH_MOSI	High/Low	Low
TP_SPI_MISO	High/Low	Low

Note:

There will be no output from DATA0P, DATA0N and TE during power on/off sequence and hardware reset.

12.2. Input Pads

Table 40. Characteristics of Input Pins

Pad/Line	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Chapter 3.10	Input valid	Input valid	Input valid	See Chapter 3.10
TP_RESX	See Chapter 3.10	Input valid	Input valid	Input valid	See Chapter 3.10
IM[1:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
DSWAP[1:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
PNSWAP	Input invalid	Input valid	Input valid	Input valid	Input invalid
FRM	Input invalid	Input valid	Input valid	Input valid	Input invalid
CLKP	Input invalid	Input valid	Input valid	Input valid	Input invalid
CLKN	Input invalid	Input valid	Input valid	Input valid	Input invalid
DATA0P	Input invalid	Input valid	Input valid	Input valid	Input invalid
DATA0N	Input invalid	Input valid	Input valid	Input valid	Input invalid
DATA1P	Input invalid	Input valid	Input valid	Input valid	Input invalid
DATA1N	Input invalid	Input valid	Input valid	Input valid	Input invalid
DATA2P	Input invalid	Input valid	Input valid	Input valid	Input invalid
DATA2N	Input invalid	Input valid	Input valid	Input valid	Input invalid
DATA3P	Input invalid	Input valid	Input valid	Input valid	Input invalid
DATA3N	Input invalid	Input valid	Input valid	Input valid	Input invalid
TP_FLASH_MISO	Input invalid	Input valid	Input valid	Input valid	Input invalid
TP_SPI_CS	Input invalid	Input valid	Input valid	Input valid	Input invalid
TP_SPI_MOSI	Input invalid	Input valid	Input valid	Input valid	Input invalid
TP_SPI_SCLK	Input invalid	Input valid	Input valid	Input valid	Input invalid

12.3. Reset Timing

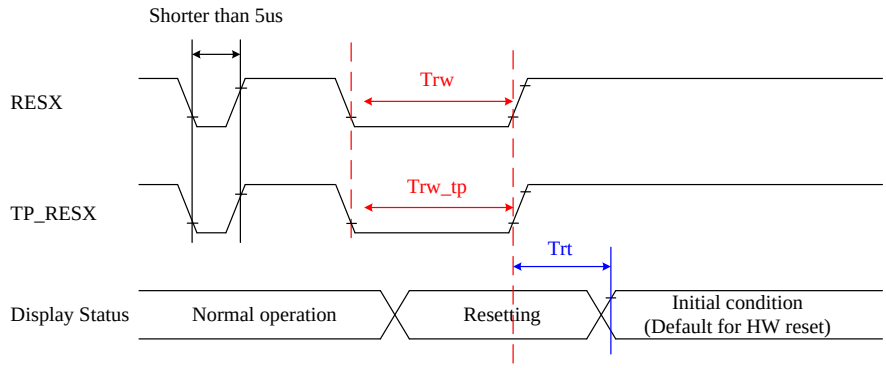


Figure 98. Reset Timing

Table 41. Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	Trw	Reset pulse duration	10	-	us
	Trt	Reset cancel	35 (Note 1,5)	-	ms
			150 (Note 1,6,7)	-	ms
TP_RESX	Trw_tp	Reset pulse duration	1	-	us

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM to registers. This loading is done every time when there is H/W reset cancel time (Trt) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the following table.

Table 42. Reset Description

RESX	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and return to default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown in following figure.

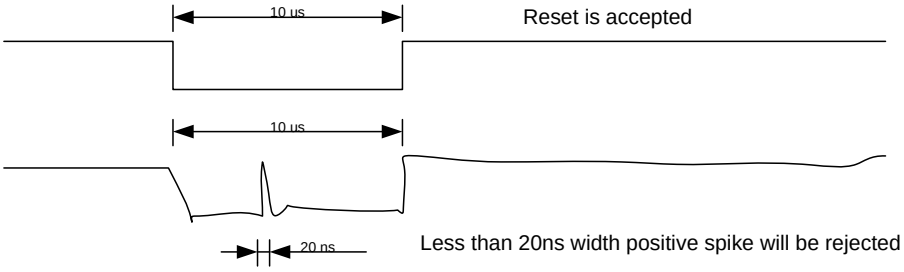


Figure 99. Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending other commands. Also Sleep Out command (11h) cannot be sent for 120msec.

13. Gamma Function

The Gamma structure of grayscale amplifier is shown as below. There are 23 voltage levels between GVDDP/GVDDN and VGS. It can be determined by the 23 adjustable registers.

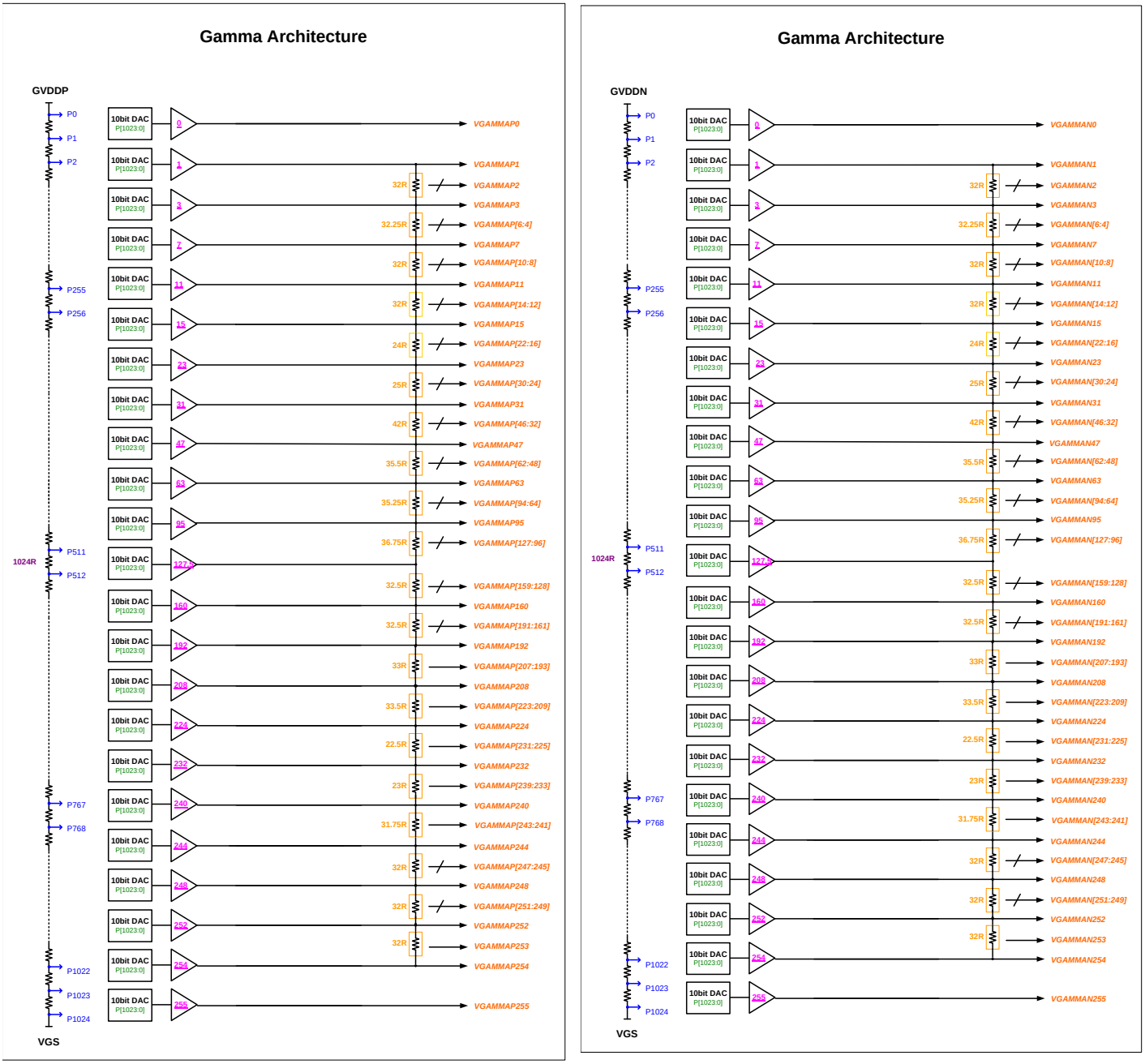


Figure 100. Gamma Architecture

14. NV Memory Programming Flow

- Auto Program
- One Byte Program
- Only Internal Program

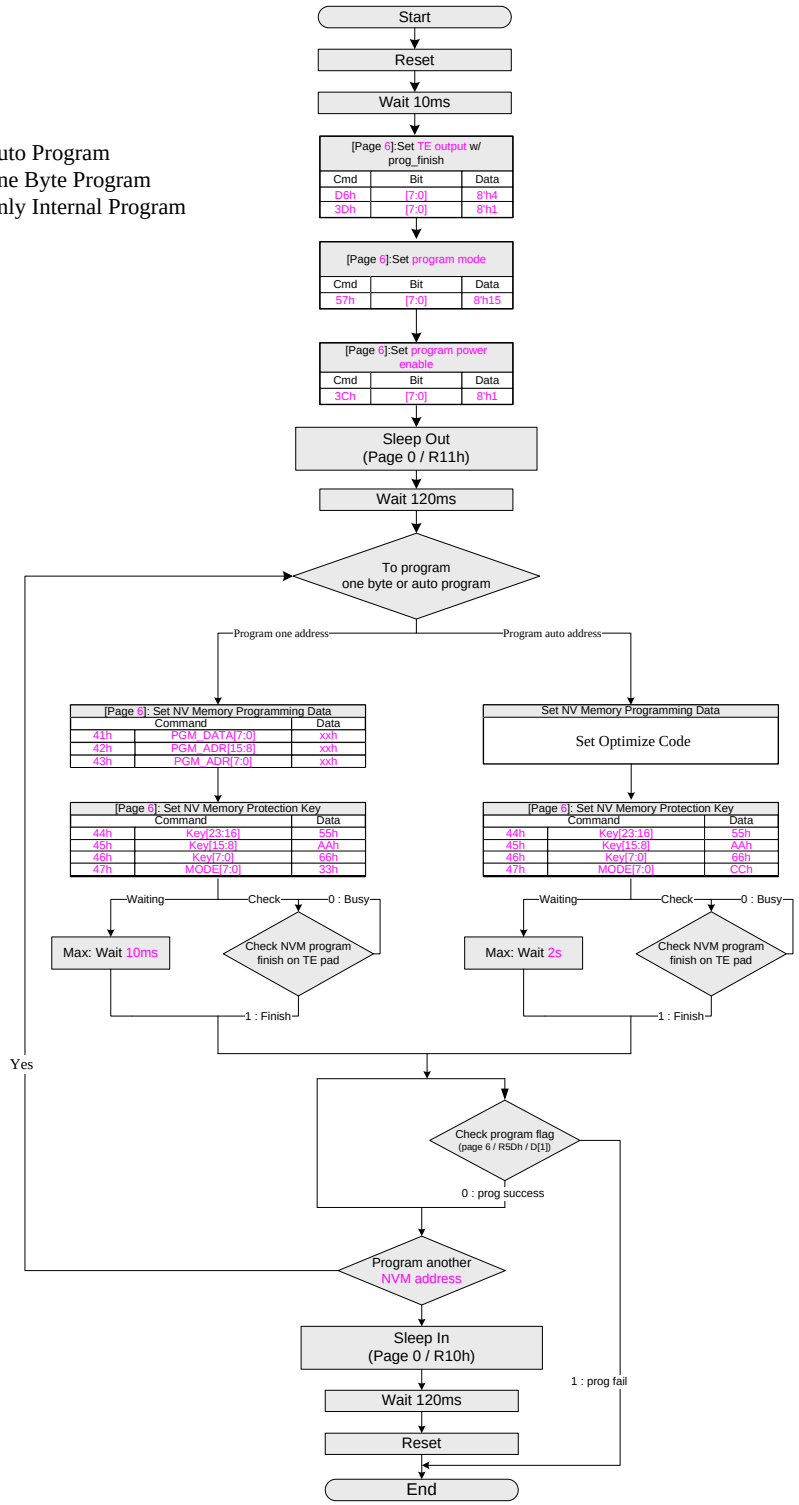


Figure 101. NVM Programming Flow (Internal power mode)

15. Electrical Characteristics

15.1. Absolute Maximum Ratings

The absolute maximum rating is listed on the following table. When the IL7807S is used out of the absolute maximum ratings, it may be permanently damaged. To use the ILI7807S within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI7807S will malfunction and cause poor reliability.

Table 43. Absolute Maximum Ratings

Item	Symbol	Unit	Value
Supply voltage (I/O)	VDDI ~ VSS	V	-0.3 ~ +1.95
Supply voltage (DSI I/O)	VDDAM ~ VSS	V	-0.3 ~ +1.95
Supply voltage	AVDD ~ AVSS	V	-0.3 ~ +6.3
Supply voltage	AVEE ~ AVSS	V	0.3 ~ -6.3
Driver Supply voltage	VGH ~ AVSS	V	-0.3 ~ +15
Driver Supply voltage	VGL ~ AVSS	V	0.3 ~ -13
Driver supply voltage	AVDD – AVEE	V	≦13V
Driver supply voltage	VGH – VGL	V	≦ 32V
Driver supply voltage	VDDI – VCL	V	≦ 5.3V
Input voltage	V_{IN}	V	-0.3 ~ VDDI + 0.3
HS Input voltage	V_{HSIN}	V	-0.3 ~ + 1.3
Operating temperature	Topr	℃	-30 ~ +70
Storage temperature	Tstg	℃	-55 ~ +110

Note:

If one of the above parameters is exceeded the absolute maximum rating even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

15.2. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Logic operating voltage	VDDI	-	1.65	1.8	1.95	V	
Operating Voltage	AVDD	-	4.5	5.5	6.3	V	
Operating Voltage	AVEE	-	-6.3	-5.5	-4.5	V	
Logic operating voltage	VDDAM	-	1.65	1.8	1.95	V	
Logic High level input voltage	V_{IH}	-	0.7*VDDI	-	VDDI	V	Note1
Logic Low level input voltage	V_{IL}	-	0	-	0.3*VDDI	V	Note1
Logic High level output voltage TE, CABC_PWM_OUT	V_{OH}	I_{OH} = -1.0mA	0.8*VDDI	-	VDDI	V	Note1
Logic Low level output voltage TE, CABC_PWM_OUT	V_{OL}	I_{OL} = +1.0mA	0	-	0.2*VDDI	V	Note1
Driver Supply Voltage	-	|VGH-VGL|	9	-	32	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-2.0	-	1	V	
Source Driver							
Positive Source Output Range	V_{SOUT}	-	0.2	-	GVDDP	V	Note2
Negative Source Output Range	V_{SOUT}	-	GVDDN	-	-0.2	V	Note2
Positive Gamma Reference Voltage	GVDDP	-	3	-	6	V	Note3
Negative Gamma Reference Voltage	GVDDN	-	-6	-	-3	V	Note3
Source Output Setting Time	Tr	Below with 99% precision	-	TBD		us	Note2
Source Output Deviation Voltage	V_{DEV}	Sout>=4.2V Sout<=0.8V	-	TBD		mV	
		4.2V>Sout>0.8V	-	TBD		mV	-
Source Output Offset Voltage	V_{OFFSET}	-	-	TBD		mV	
Booster Operation							
VCL Voltage	VCL	-	-3.3	-	-2.5	V	
Gate Driver High Voltage	VGH	-	6	-	15	V	
Gate Driver Low Voltage	VGL	-	-6	-	--13	V	

Note:

1. Ta = -30 to 70 °C, VDDI=1.65V ~ 1.95V.
2. The Max. Value is between with Note-2 measure point and Gamma setting value
3. GVDDP $\leqq$ AVDD-0.3V and GVDDN $\geqq$ AVEE+0.3V.

15.2.1. DSI DC characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	High (LP)

15.2.2. DC characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Digital power supply voltage	VDDI	Power supply voltage	1.65	1.8	1.95	V
Analog power supply voltage	AVDD	Operating voltage	4.5	5.5	6.3	V
Analog power supply voltage	AVEE	Operating voltage	-4.5	-5.5	-6.3	V
VDDI noise	V_{VDDI_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV

Note:

1. Ta = -30℃ to 70℃
2. These values are not symmetric amplitude, which centre points are VDDI. See examples as reference purposes, when V_{VDDI_NOISE} are maximums.

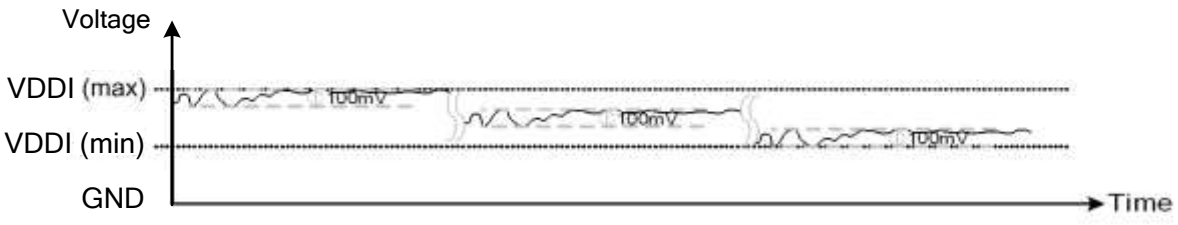


Figure 102. Noise on Power Supply Lines

15.2.3. DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below. DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic High level output voltage	V_{OHLP}	I_{OUT} = -1mA	0.8*VDDAM	-	VDDAM	V
Logic Low level output voltage	V_{OLLP}	I_{OUT} = 1mA	0.0	-	0.2*VDDAM	V
Logic High level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1, D2, D3)	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1, D2, D3)	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA

Note:

1. Ta=-30℃ to 70℃
2. This table only uses for DSI LP mode (DSI High Speed mode is off).

15.2.4. Spike / Glitch Rejection

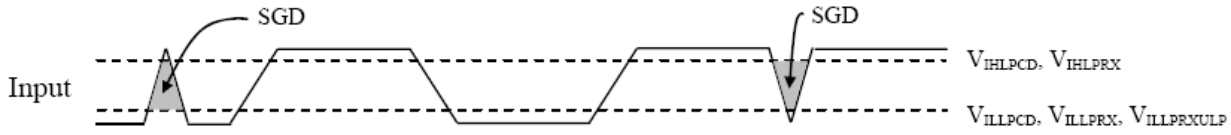


Figure 103. Spike / Glitch Rejection

Note:

1. A spike/glitch can be rejected when the Peak Interference Amplitude is 200mV (at maximum) and the Interference Frequency is 450 MHz (at the very least).
2. n = 0,1,2,3

Table 44. Spike / Glitch Rejection

Spike / Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min.	Max.	Unit
DSI-CLK+/-, DSI-Dn+/-	SGD	Input pulse rejection for DSI	-	300	Vps

15.2.5. DC Characteristics for DSI HS mode

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLK+/- Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-Dn+/- Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLK+/- Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DSI-Dn+/- Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLK+/-	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-Dn+/- Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLK+/-	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-Dn+/- Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLK+/-	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-Dn+/- Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/- Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5, Note 6	-	-	60	pF

Note:

1. Ta = -30 to 70°C, VDDI=1.65V ~ 1.95V, AVDD=4.5V ~ 6.3V, AVEE=-4.5V ~ -6.3V, VSS=AVSS=0V.
2. Includes 50mV (-50mV to 50mV) ground difference.
3. Without VCMRCLKM450/VCMRDATAM450.
4. Without 50mV (-50mV to 50mV) ground difference.
5. n = 0,1,2,3
6. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

The DSI receiver (HS mode) is understanding that there is logical '1' (HS-1) when a differential voltage is more than V_{THH} (CLK+/DATA+) and the DSI receiver (HS mode) is understanding that there is logical '0' (HS-0) when a differential voltage is more than V_{THL} (CLK-/DATA-). There is undefined state if the differential voltage is less than V_{THH} (CLK+/DATA+) and less than V_{THL} (CLK-/DATA-). A reference figure is below.

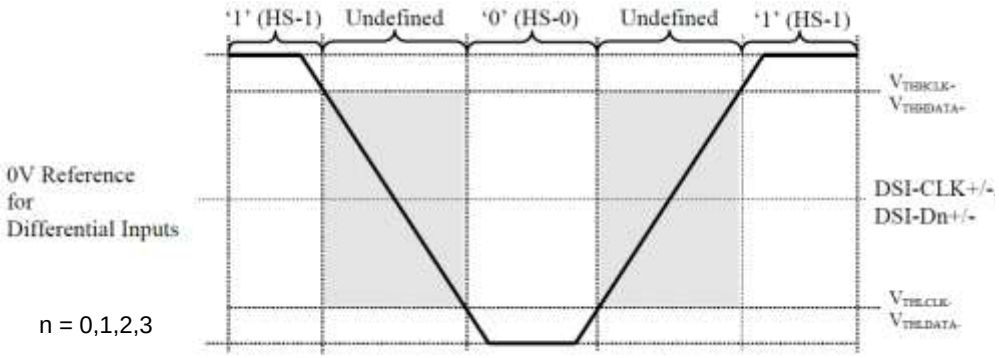


Figure 104. Differential Inputs Logical '0's and '1's, Threshold High/Low, Differential Voltage Range

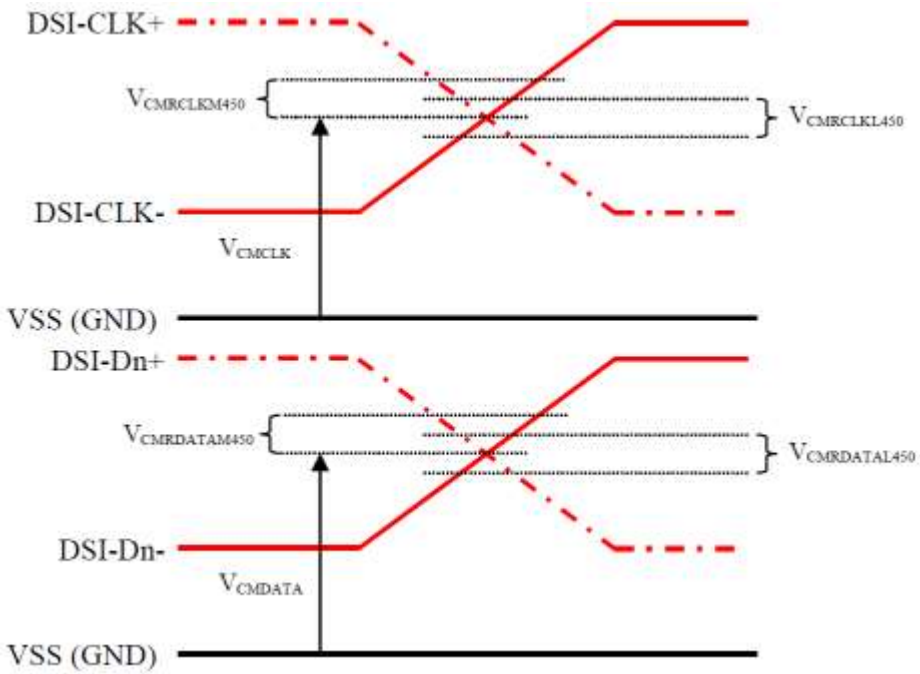


Figure 105. Common Mode Voltage on Clock and Data Channels

The termination resistor (R_{TERM}) of the differential DSI receiver can be driven two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs (DSI-CLK+ ⇔ DSI-CLK- or DSI-D0+ ⇔ DSI-D0- or DSI-D1+ ⇔ DSI-D1-)
- High Speed (HS) mode when the termination resistor is connected between differential inputs (DSI-CLK+ ⇔ DSI-CLK- or DSI-D0+ ⇔ DSI-D0- or DSI-D1+ ⇔ DSI-D1-)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

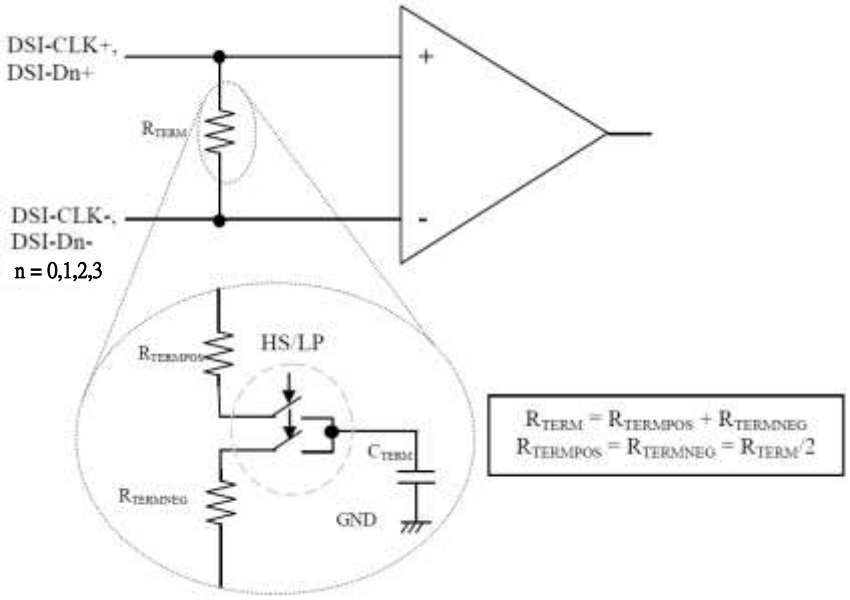


Figure 106. Differential Pair Termination Resistor on the Receiver Side

15.3. AC Characteristics

15.3.1. DSI Timing Characteristics

15.3.1.1. High Speed Mode – Clock Channel Timing

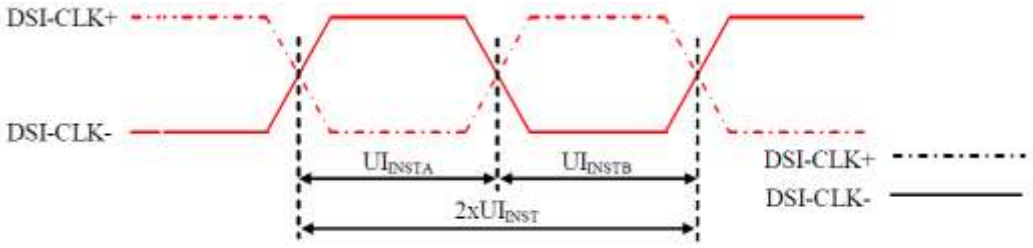


Figure 107. DSI Clock Channel Timing

Table 45. DSI Clock Channel Timing

Signal	Symbol	Parameter	Min.	Max.	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	2	25	ns
DSI-CLK+/-	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	1	12.5	ns

Note: $UI_{INST} = UI_{INSTA} = UI_{INSTB}$

15.3.1.2. High Speed Mode – Data Clock Channel Timing

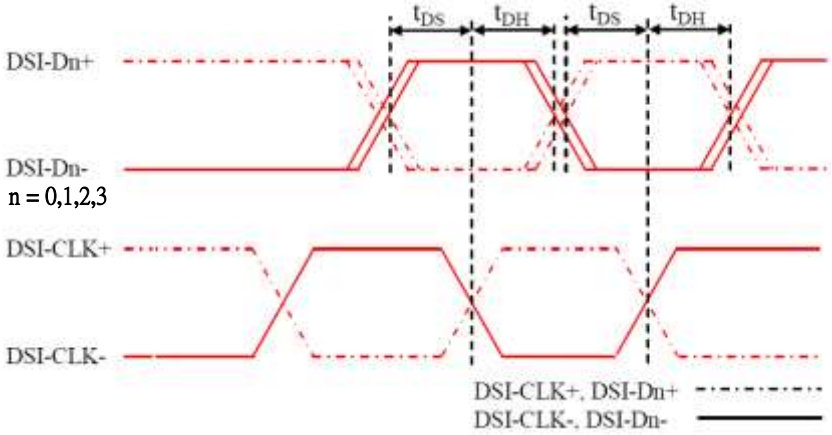


Figure 108. DSI Data to Clock Channel Timings

Table 46. DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min.	Max.
DSI-Dn+/- (n=0,1,2,3)	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

15.3.1.3. High Speed Mode – Rise and Fall Timings

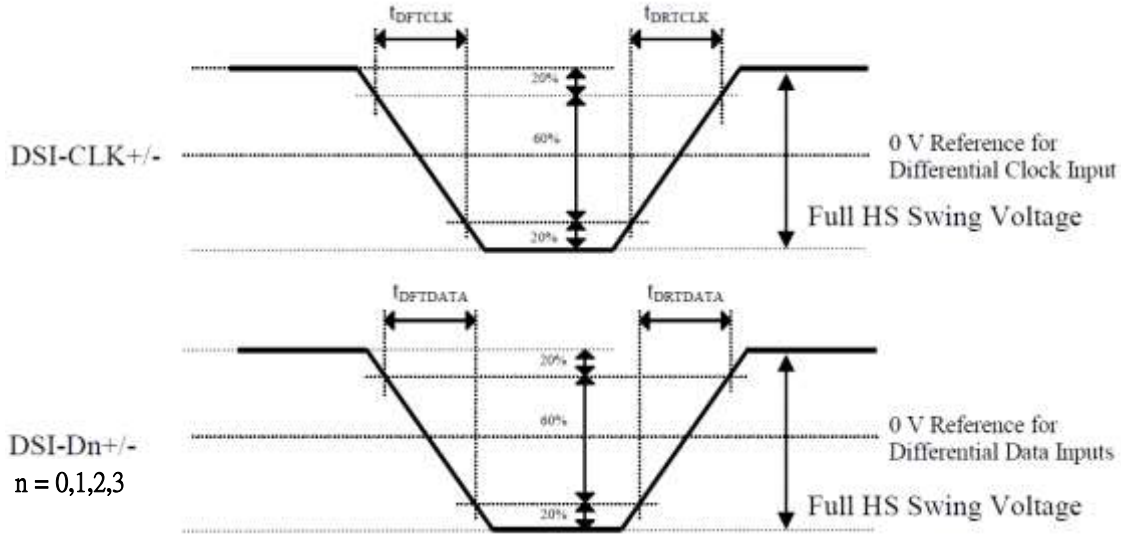


Figure 109. Rise and Fall Timings on Clock and Data Channels

Table 47. Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min.	Typ.	Max.
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	150 ps	-	0.3UI
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- (n=0,1,2,3)	150 ps	-	0.3UI
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	150 ps	-	0.3UI
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- (n=0,1,2,3)	150 ps	-	0.3UI

Note:

The display module has to meet timing requirements, what are defined for the transmitter (MCU) on MIPI D-Phy standard.

15.3.1.4. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MCU to the Display Module sequence below.

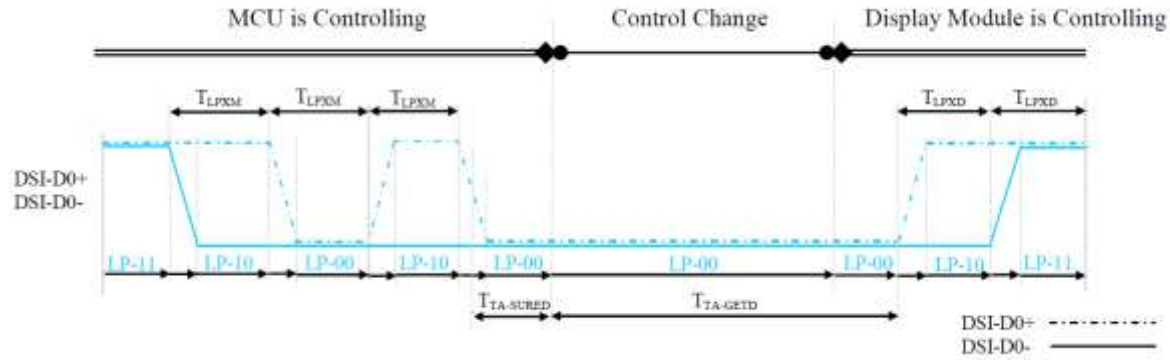


Figure 110. BTA from the MCU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module to the MCU sequence below.

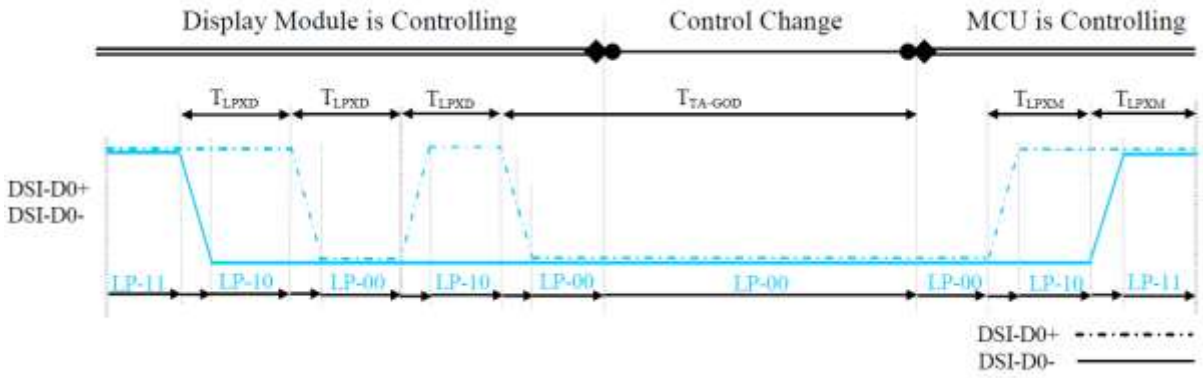


Figure 111. BTA from the Display Module to the MCU

Table 48. Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module ➔ MCU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module starts driving	T_{LPXD}	$2*T_{LPXD}$	ns

Table 49. Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module	$5*T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MCU	$4*T_{LPXD}$	ns

15.3.1.5. Data Lanes from Low Power Mode to High Speed Mode

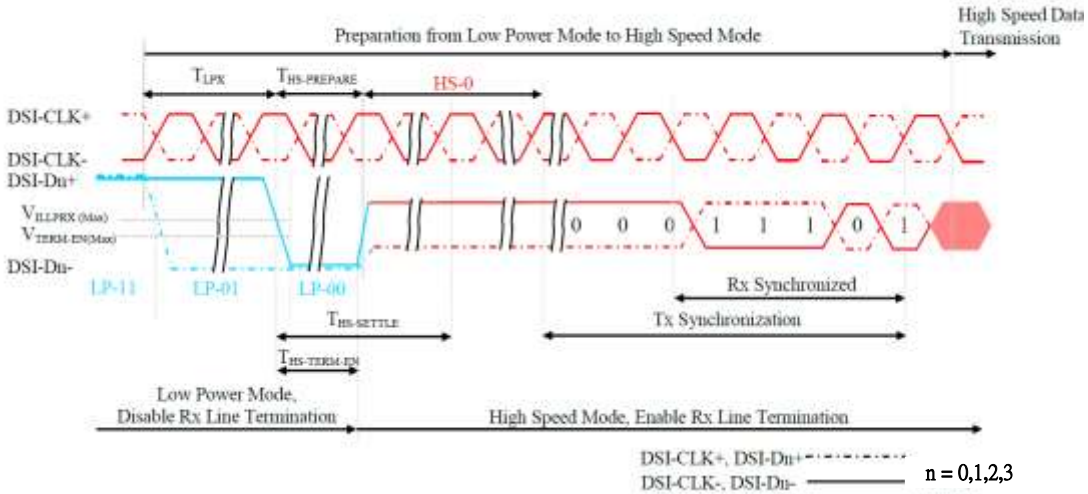


Figure 112. Data Lanes – Low Power Mode to High Speed Mode Timings

Table 50. Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/- (n=0,1,2,3)	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

15.3.1.6. Data Lanes from High Speed Mode to Low Power Mode

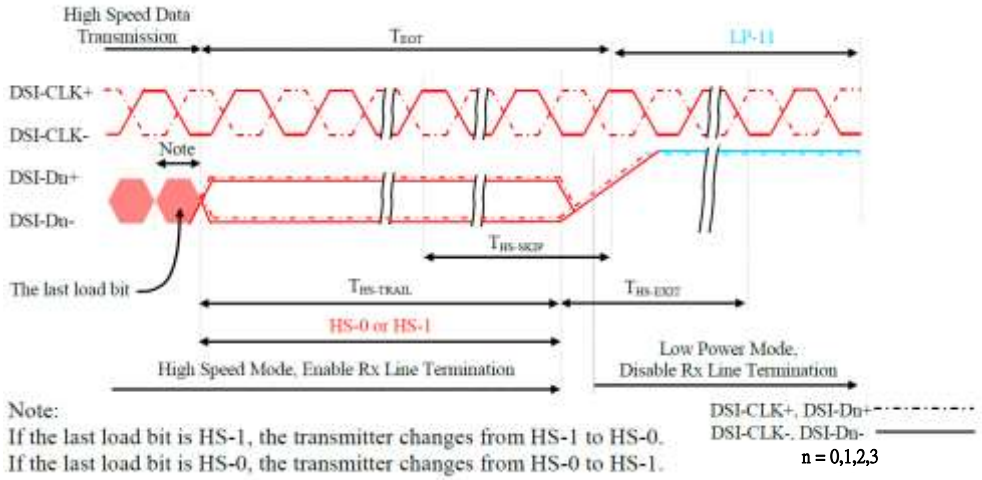


Figure 113. Data Lanes – High Speed Mode to Low Power Mode Timings

Table 51. Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-SKIP}$	Time-Out at Display Module to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(8*UI, 60ns+ 4*UI)	-	ns

15.3.1.7. DSI Clock Burst – High Speed Mode to/from Low Power Mode

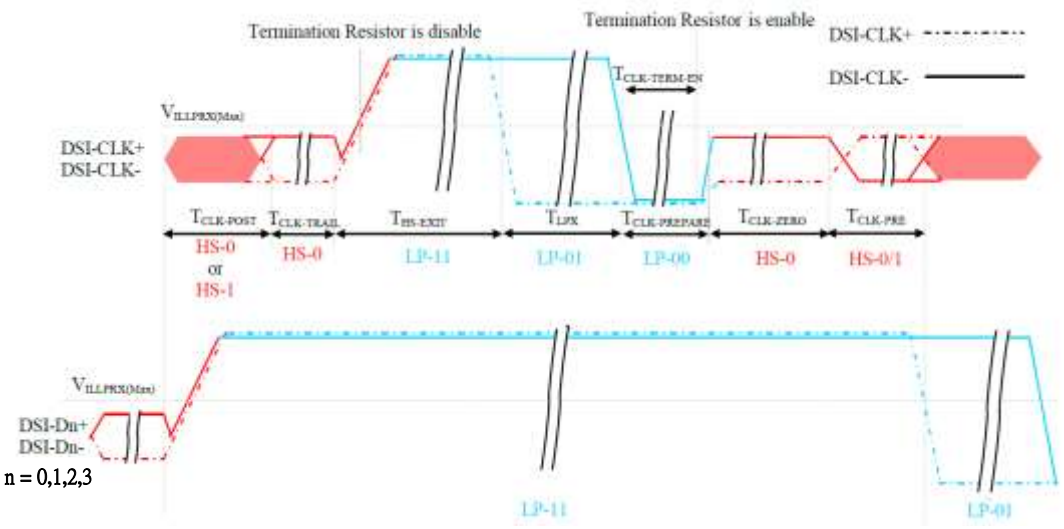
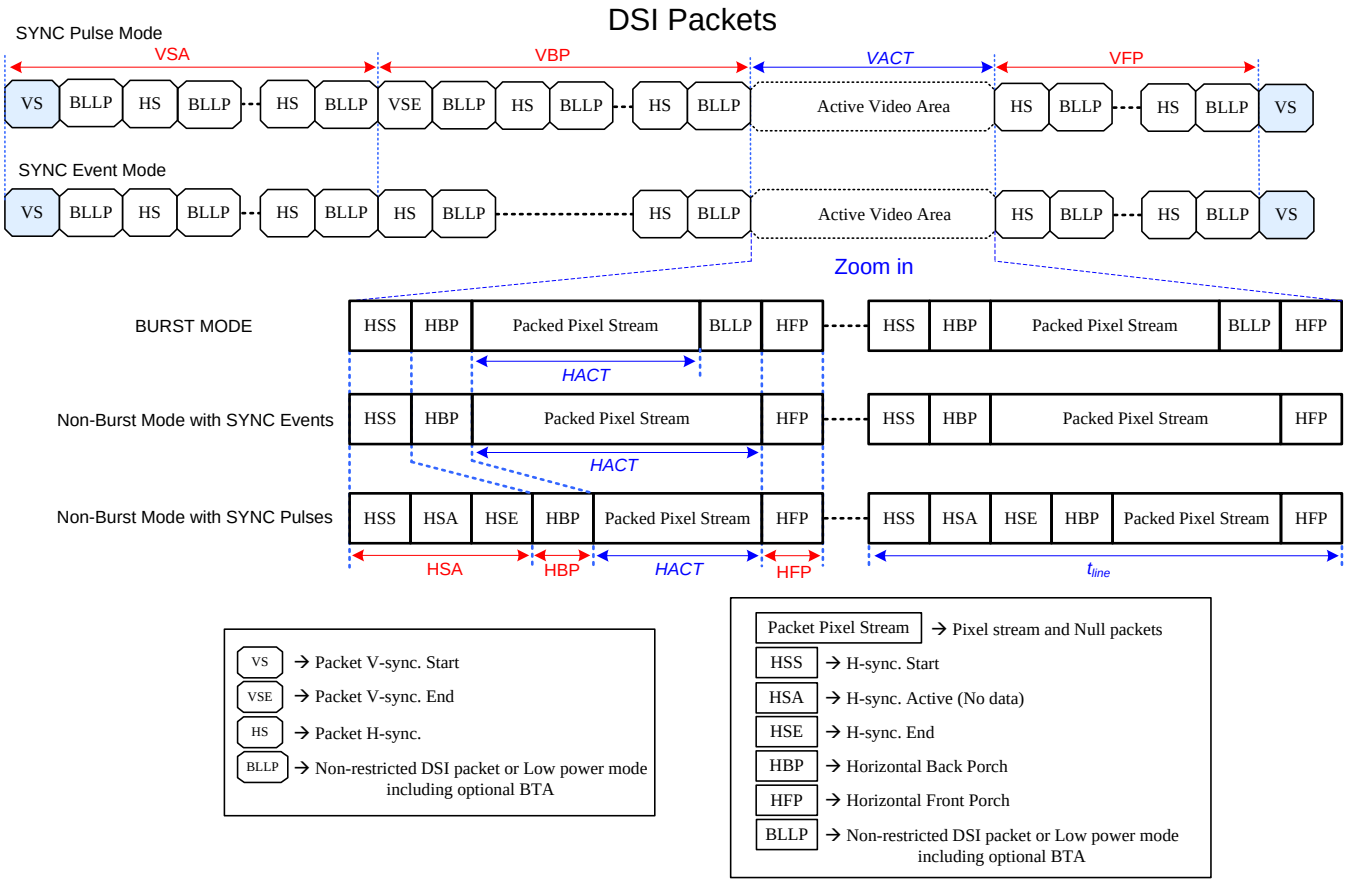


Figure 114. Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 52. Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

15.3.1.8. Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. Active	VSA Note 6, 7	2	-	-	Line
Vertical Back Porch	VBP Note 6, 7	6	-	-	Line
Vertical Front Porch	VFP Note 6, 7	30	-	-	Line
Active lines per frame	VACT	1280	1920	2520	Line
Horizontal sync. Active	HSA	2	-	-	Pixel
Horizontal Porch	HSA + HBP+ HFP	0.9	-		us
Active pixels per line	HACT	720	1080	1080	Pixel
Bit Rate	BRbps	TBD	-	TBD	Mbps/lane

Note6. The minimum values of this table mean the limitation of IC without considering the panel GIP.

Note7. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

1 UI = 1/Bit rate

HAS(pixel) = (tHSA*lane number) / (UI* pixel format)

HBP(pixel) = (tHBP*lane number) / (UI* pixel format)

HFP(pixel) = (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example：BR_{bps} = 880Mbps/lane, 1UI=1.13ns, Frame rate=60.2Hz, VACT=1280, VSA=4, VBP=4, VFP=4, HACT=720, HSA=20, HBP=70, HFP=90, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.3 DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting is 60 Hz.
5. Please reference to the following table.
6. The minimum values of this table mean the limitation of IC without considering the panel GIP.
7. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

Table 53. Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	1100MHz(Note)	733MHz	733MHz
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	1100MHz(Note)	1100MHz	733MHz
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	1100MHz(Note)	X	733MHz
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	1100MHz(Note)	X	1100MHz

Note. Only support HD+ (1680*720) resolution or below at MIPI 2 lanes.

15.4. Max series resistance table

Name	Type	Max Series Resistance	Unit
VDD	Power supply	1	Ω
AVDD, AVDD_DC, AVEE, AVEE_DC, VDDI, VDDI_DC, VDDAM, AVSS, AVSS_DC, VGS, VSS, HS_VSS, CVSS	Power supply	3	Ω
DATA2_P/N, DATA3_P/N, DATA1_P/N, DATA0_P/N, CLK_P/N	Input/Output	3	Ω
VGHO, VGLO, TPLDO_OUT, , VGH, C21P, C21M, VGL, C31P, C31M, VCL, HS_LDO, VCOM, VCOM_L*, VCOM_R,* HS_LDO, VDD_TP	Capacitance connection	3	Ω
VMD, VCOM_OPT	Output	3	Ω
TP_I2C_SDA, TP_I2C_SCL, TP_SPI_CS, TP_SPI_MISO, TP_SPI_MOSI, TP_SPI_SCLK, TP_FLASH_CS, TP_FLASH_MISO, TP_FLASH_MOSI, TP_FLASH_SCK	Input/Output	20	Ω
CGOUTR[24:1], CGOUTL[24:1]	Output	20	Ω
RESX, TP_RESX, TEST[2:0], IM[1:0], SCL, CSX, DCX, DSWAP[1:0], PNSWAP, TE, TE1, POWER_SEL, OSC, SDI, FRM	Input	30	Ω
GVDDP, GVDDN, SDO, TP_PWR_TEST, CABC_PWM_OUT,	Output	30	Ω
TP_TEST_EN, TP_TEST_L[3:0], TP_TEST_R[3:0], TP_GPIO[6:0], TP_INT, TP_EXTCLK, TP_FLASH_HOLD, TP_FLASH_WP, TCKC, TMSC, TP_UART_TX, PCLK, DE, VSYNC, HSYNC, TS[7:0],	Input/Output	30	Ω
COGTESTL[2:1], COGTESTR[2:1]	Output	100	Ω

Suggestion.

The resistance difference between VCOM_L and VCOM_R should be less than < 0.5 ohm.

16. Revision History

Version No.	Date	Page	Description
V001	2019/12/24	All	New created.