CONFIDENTIAL B



MT6765_62 ETT test & stress test reference for LP4X V1.6



Agenda

- ETT test step by step
- MTK Eye-Scan Function
- DRAM Stress Test step by step
- Nenamark2 + DVFS for Fast-K
- Suspend/Resume
- Reboot(DDR Reserve mode, Full-K, Fast-k)
- pass

Chang list

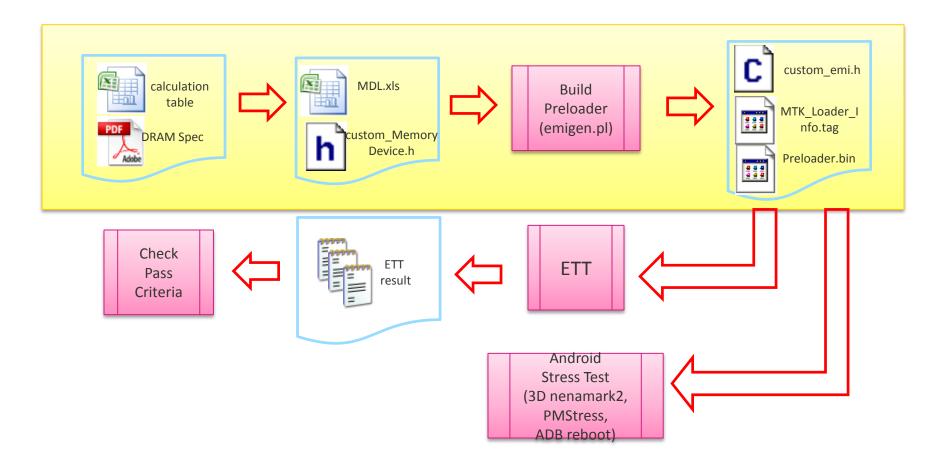
Vison	changlist	date		
1	Original version	2018 4 11		
1.1	pass	2018 4 20		
1.2	LP4X ETT	2018 7 9		
1.3	Fix script device id	2018/09/12		
1.4	Page 49 note Log	2018/12/10		
1.5	Page42 note	2018/12/20		
1.6	Page7 Page26 change VM(LV) from 1.09 to 1.06	2018/12/25		



ETT TEST STEP BY STEP

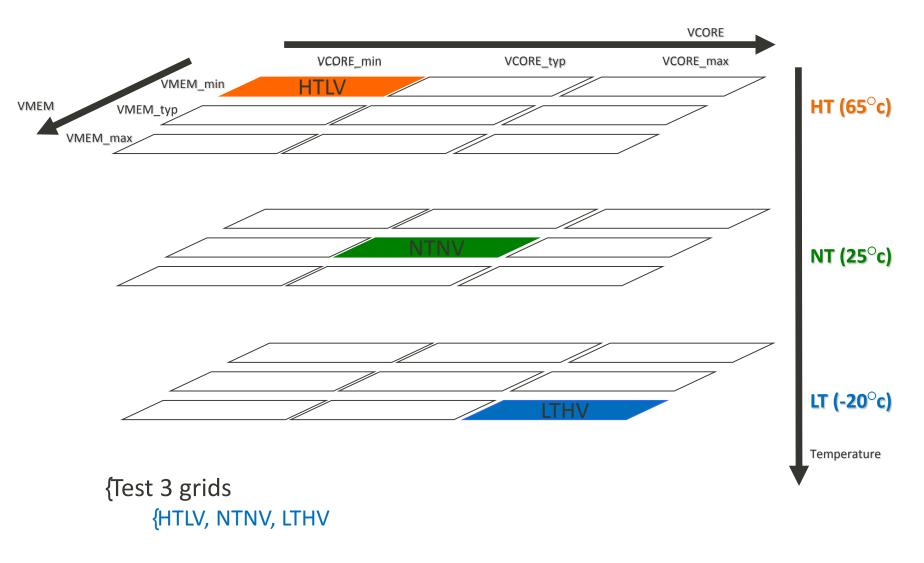


MT6765_62 DRAM Validation Flow





ETT Test Environment Setup (1/2)





ETT Test Environment Setup (2/2)

For LPDDR4X 3200MHz

Condition	Temperature (°C)	Vcore (V)	Vm (V)	Vddq(V)
HTLV	65	0.75625	1.06	0.58
NTNV	25	0.80	1.12	0.6
LTHV	-20	0.84375	1.17	0.65



ETT (1/12)

: MT6765_62 Flash tool(W1748).

• 不 Format whole flash;

ETT BIN :
 https://online.mediatek.com/qvl/_layouts/15/mol/qvl/ext/QVLHomeExternal.as
 px不 memory ETT bin

- Note1. VBAT 不
- Note2. NTC 不 10K GND, NTC!

ETT

(2/12)

• Step1. UART Cable PC uart0

• Step2.



ETT

(3/12)

• Step3: UARTO COM port MT6765_62 ETT log uart0 ok



ETT (4/12)

- Step4: 921600_U -





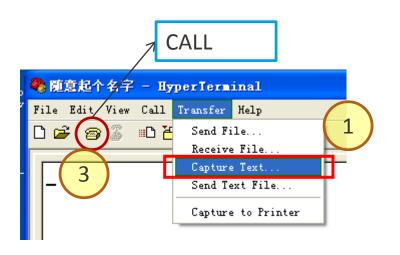
ETT

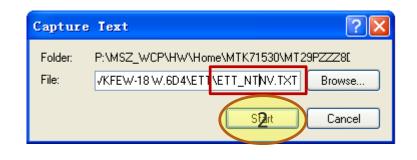
(5/12)

Step5:

ETT raw data

→ 不Start→ 不CALL





Note1:

Note2:

停

停.

:

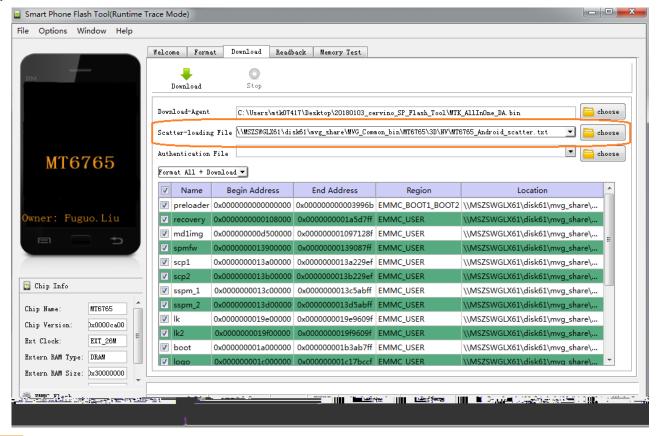
ETT LOG

$ETT \qquad (6/12)$

Step6: Flash tool download scatter file

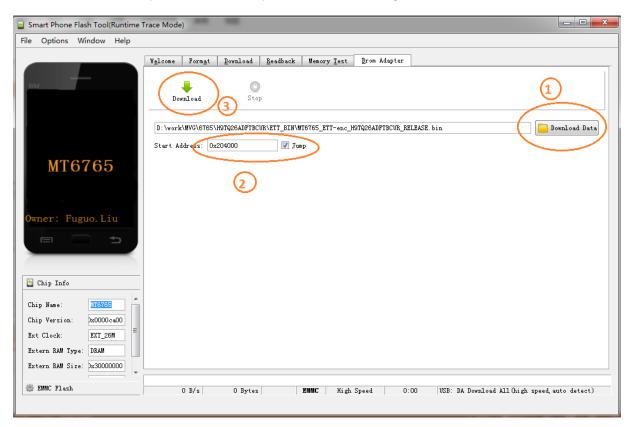
- 不

Format whole flash



ETT (7/12)

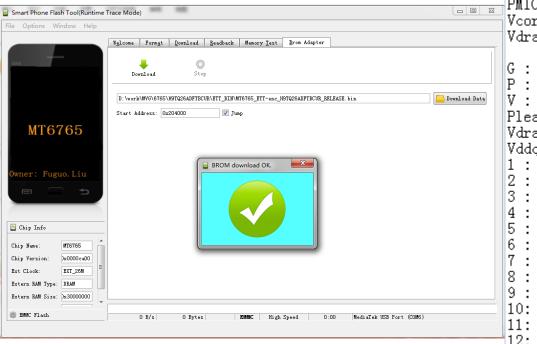
Step7: Ctrl+Alt+A flash tool brom Adapter→ ETT bin→ start address(0x204000)→ Jump→ download





$ETT \qquad (8/12)$

■ **Step8:** USB ETT bin 不 →



```
[MT6765] Welcome to ETT's world ... LPDDR3
PMIC TRAP GET DDR TYPE: 0x3
Vcore = 800000
Vdram = 1220000
G : Start the ETT test.
P : Print voltage settings
V : Voltage adjustment.
Please enter selection(v.)
Vdram (HV, NV, LV)=(1.17, 1.1, 1.06)
Vddq (HV, NV, LV)=(0.65, 0.6, 0.57)
1 : (Vcore HV, Vdram HV, Vddq HV)
2 : (Vcore NV, Vdram NV, Vddq NV)
3 : (Vcore LV, Vdram LV, Vddq LV)
4 : (Vcore HV, Vdram LV, Vddq LV)
5 : (Vcore LV, Vdram HV, Vddq HV)
6 : (Vcore) ++ ...
7 : (Vcore) -- ...
8 : (Vdram) ++ ...
9 : (Vdram) -- ...
10: (Vddq) ++ ...
11: (Vdda) -- ...
12: Max Vdram for heavy load test
```

ETT

(9/12)

Step9. (HV, NV, LV)

```
\equiv
```

```
G : Start the ETT test.
P : Print voltage settings
V : Voltage adjustment.
Please enter selection 🗞
Vdram (HV, NV, LV)=(1.17, 1.1, 1.06)
Vddq (HV, NV, LV)=(0.65, 0.6, 0.57)
1 : (Vcore HV Vdram HV. Vdda HV)
C: (Vcore NV, Vdram NV, Vddq NV)
3 : (Vcore LV, Vdram LV, Vddq LV)
4 : (Vcore HV, Vdram LV, Vddq LV)
5 : (Vcore LV, Vdram HV, Vddq HV)
6 : (Vcore) ++ ...
7 : (Vcore) -- ...
8 : (Vdram) ++ ...
9 : (Vdram) -- ...
10: (Vddq) ++ ...
11: (Vdda) -- ...
12: Max Vdram for heavy load test
13: Min Vdram for heavy load test
Please enter pattern selection: 200 VDDQ for LP3, return
```

ETT (10/12)

• **Step10:** G ETT





(11/12)

Step11:ETT

不 三

20mV

ETT log

log Vcore,Vmem, Vddq

For LPDDR4X 3200MHz

Condition	Temperature (°C)	Vcore (V)	Vm (V)	Vddq(V)
HTLV	65	0.75625	1.09	0.58
NTNV	25	0.80	1.12	0.6
LTHV	-20	0.84375	1.17	0.65

ETT

ETT out

(12/12)

```
Step12
                ETT
                                                  3200
                                                                fail
                                                                         pass ETT
                          pass
            [HQA] information for measurement,
                                                   Dram Data rate 🗐 3200
            [Read Voltage]
            [HQALOG] 3200 Vcore HQA = 756250
            [HQALOG] 3200 Vdram HQA = 1060000
            [HQALOG] 3200 Vddq HQA = 570000
            [Cmd Bus Training window]
            VrefCA Range: 1
            VrefCA
                [HQALOG] 3200 CA_Window ChannelO RankO 46 (bit 3)
                [HQALOG] 3200 CA_Window Channel0 Rank1 47 (bit 2)
                [HQALOG] 3200 CA_Window Channell Rank0 49 (bit 4)
                [HQALOG] 3200 CA_Window Channell Rank1 50 (bit 3)
                CA Min Window(%)
                [HQALOG] 3200 CA Window(%) ChannelO RankO 72% (PASS)
                [HQALOG] 3200 CA_Window(%) Channel0 Rank1 74% (PASS)
                [HQALOG] 3200 CA_Window(%) Channell Rank0 77% (PASS)
                [HQALOG] 3200 CA Window(%) Channell Rank1 79% (PASS)
   ETT log
                                        pass
   停NTNV HTLV LTHV下
                                                       log
```



parsetool

MTK EYE-SCAN FUNCTION



ETT

务

(1/2)

MTK Eye-Scan for each bit MT6765 62 ETT LP4X 55.70% 54.50% LPDDR4X memory 52.70% 52.10% 51.50% 50.90% LPDDR3 50.30% 49.70% 49.10% 48.50% 47.90% Vref 47.30% 46.10% 45.50% 44.90% 别pass DQ 住 44.30% 43.70% 43.10% **VREF Setting** 42.50% 41.90% 41.30% 40.70% 40.10% 39.50%000000000000.....125ps 38.90% 38.30%000000000000.......133ps 37.70% 37.10% 36.50% 35.90% 35.30% 34.70% 34.10%00000000000000....159ps000000000000000....167ps 33.50% 32.30% 31.70% 31.10% 30.50%0000000000000000....175ps000000000000000000....184ps 29.90% 29.30%0000000000000000....175ps0000000000000000...175ps 28.10% 27.50% 26.90%0000000000000......150ps 26.30% 25.10% 24.60% 24.00% 23.40%00000000000.......125ps 22.80% 22.20% 21.00% 20.40% PASS timing window • 19.20% 18.60%

CONFIDENTIAL B

dram SI Eye Scan

Debug Eye

bit/byte 后

10.

Vref Vref

pass window Vref JEDEC

Step : 0.6%

(1/167)

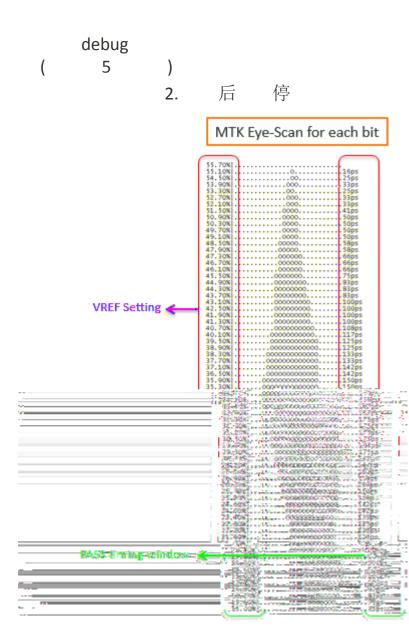
JEDEC Vref Setting table for LP4X

Table 2 Vacr Settings for Range[0] and Range[1]

Function	Operand	Range	[0] Values (% of	V _{DDQ})	Range	[1] Value	s (% of V	(ppg)	Notes
		0000000	15.0% 011010 _n :	30.5%	0000006:	32.9%	011010 _B :	48.5%	1,2,3
		000001 _a :	15.6% 011011 ₀ :	31.1%	000001 _n :	33.5%	011011 ₈ :	49.1%	
		000010 _B :	16.2% 011100 _a :	31.7%	0000108:	34.1%	011100 _a :	49.7%	
		000011 ₈ :	16.8% 011101 _a :	32.3%	000011 _a :	34,7%	011101 _n : default	50.3%	
		000100 _a :	17.4%011110 _n :	32.9%	000100 _a :	35.3%	011110 _n :	50.9%	
	1	000101 _n :	18.0% 011111 _n :	33.5%	0001018	35.9%	0111111	51.5%	
	3	000110 _n :	18.6% 100000 _n :	34.1%	000110 _n :	36.5%	100000 _n :	52,1%	
	1 3	000111 _n :	19.2% 100001 ₀ :	34.7%	000111 _a :	37,1%	100001 _a :	52.7%	
	3	001000 _s :	19.8% 100010 _m :	35.3%	001000	37,7%	100010 _a :	53.3%	
	1	001001 _a :	20.4% 100011 ₀ :	35.9%	001001 _a :	38.3%	100011 _a :	53.9%	
	1 8	001010 _a :	21.0% 100100 _m :	36.5%	0010108	38.9%	100100 _n :	54.5%	
VREF	OP [5:0]	001011 ₈ :	21.6% 100101 _n :	37.1%	001011 _n :	39.5%	100101 _a :	55.1%	
Settings		001100 _n :	22.2% 100110 _n :	37,7%	001100 _n :	40.1%	100110 _n :	55.7%	
for		001101 _n :	22.8% 100111 _a :	38.3%	001101 _m :	40.7%	100111 _n :	56.3%	
MR12		001110 _a :	23.4% 101000 _n :	38.9%	001110 _n :	41.3%	101000 _n :	56.9%	
		001111 ₀ :	24.0% 101001 _n :	39.5%	001111 _n :	41.9%	101001 _a :	57.5%	
		010000 ₀ :	24.6% 101010 ₀ :	40.1%	010000012	42.5%	101010 _n :	58.1%	
		010001 _n :	25.1% 101011 _a :	40.7%	010001,:	43.1%	101011 _n :	58.7%	
		010010 _m :	25.7% 101100 ₀ :	41.3%	010010,:	43.7%	101100 _n :	59.3%	
		010011 ₈ :	26.3% 101101 _m :	41.9%	010011 _n :	44.3%	101101 ₈ :	59.9%	
		010100 _a :	26.9% 101110 _n :	42.5%	010100 _n :	44.9%	101110 _a :	60.5%	
		010101 _n :	27.5% 101111 _n :	43.1%	010101 _n :	45.5%	101111 _n :	61.1%	
		010110 _n :	28.1% 110000 _n :	43.7%	010110 _n :	46.1%	110000 _n :	61.7%	
		010111 _n :	28.7%110001 _a :	44.3%	010111 _a :	46.7%	110001 _n :	62.3%	
		011000 _n :	29.3% 110010 _a :	44.9%	011000 _n :	47.3%	110010 _a :	62.9%	
		011001 _n :	29.9% All Others Reserved		011001 _m :	47.9%		Others: eserved	

1. These values may be used for MR12 OP[5:0] to set the V_{REP}(CA) levels in the LPDDR4-SDRAM.

2. The range may be selected in the MR12 register by setting OP[6] appropriately.



^{3.} The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

DRAM STRESS TEST STEP BY STEP



MT6765_62 DRAM Stress Test

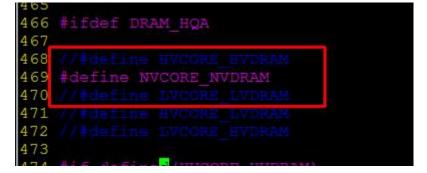
Stress Test **PMIC** NTNV HTIV ITHV preloader bin preloader bin preloder code Linux kernel code VDD2 VDDQ preloader linux kernel Linux kernel Vcore (Vcore DVFS) 1.停Memory 2. root MTK_BUILD_ROOT=yes build Note **ENG** userdebug user



MT6765_62 DRAM Stress Test SW Configuration Android preloader

- 2. Select voltage condition
 - HVCORE_HVDRAM / NVCORE_NVDRAM / LVCORE_LVDRAM
 - The 3 macros are exclusive for each other, please enable just one macro for each

voltage condition.



1/3

DRAM 不 停Stress test.

For LPDDR4X:

LP4X	DRAM Data Rate	HV	NV	LV
	3200(opp1)	0.84375	0.8	0.75625
	2400(opp3)	0.84375	0.8	0.75625
Vcore	2400(opp8)	0.7375	0.7	0.6625
	1534(opp10)	0.7375	0.7	0.6625
	1534(opp15)	0.6875	0.65	0.6125
VDRAM	1.17	1.12	1.06	
VD	0.65	0.6	0.58	



```
后 PMIC
                                                           run ETT
                                后
      Stress test
 Note1: Vcore DVFS
                                         Vcore
                                                                script
 Note2:
                                         Vcore
                                                                                      Vcore
 Note3: VDD2
                           preloader
                                                Vcore 住
                                    download HV / NV / LV preloader bin
 Note4:
                                 份
 Note5:
                                                        1ms
                                                                          Vcore
                  Vcore
1.
          dvfs
adb shell cat /sys/devices/platform/10012000.dvfsrc/helio-dvfsrc/dvfsrc enable---
                                                                            dvfs
adb shell "echo 1 > /sys/devices/platform/10012000.dvfsrc/helio-dvfsrc/dvfsrc enable"
         dvfs
```

```
C: Wsers\mtk07417\adb shell cat /sys/devices/platform/10012000.dvfsrc/helio-dvfs
rc/dvfsrc_enable

C: Wsers\mtk07417\adb shell "echo 1 > /sys/devices/platform/10012000.dvfsrc/heli
o-dvfsrc/dvfsrc_enable"

C: Wsers\mtk07417\adb shell cat /sys/devices/platform/10012000.dvfsrc/helio-dvfs
rc/dvfsrc_enable
```





```
2. vcore DVFS OPP table \overline{\Lambda} NV cat OPP13 OPP14 0.675V 0.65V cat
```

cat /sys/devices/platform/10012000.dvfsrc/helio-dvfsrc/dvfsrc_opp_table

```
C:\Users\mtk07417>adb shell
1 > /sys/devices/platform/10012000.dvfsrc/helio-dvfsrc/dvfsrc_enabl
s/platform/10012000.dvfsrc/helio-dvfsrc/dvfsrc_enable
sys/devices/platform/10012000.dvfsrc/helio-dvfsrc/dvfsrc_opp_table
[OPP0 1: 0
                               khz
                  uv Ø
[OPP1 ]: 800000
                  uv 3200000
                              khz
[OPP2 1: 800000
                  uv 3200000
                              khz
[OPP3 1: 800000
                  uv 2400000
                              khz
[OPP4 ]: 800000
                  uv 3200000
                              khz
COPPS 1: 800000
                  uv 2400000
                              khz
[OPP6 1: 800000
                  uv 3200000
                              khz
[OPP7 1: 800000
                  uv 2400000
                              khz
[OPP8 1: 700000
                  uv 2400000
                              khz
[OPP9 ]: 700000
                  uv 2400000
                              khz
[OPP10]: 700000
                  uv 1534000
                              khz
                  uv 2400000
[OPP11]: 700000
                              khz
[OPP12]: 700000
                  uv 1534000
                              khz
[OPP13]: 700000
                  uv 1534000
                              khz
[OPP14]: 700000
                  uv 1534000
                              khz
[OPP15]: 650000
                  uv 1534000
                              khz
```

```
3. HV DVFS_Nenamark_Memtester_Script set_opp_table_HV.bat device id LV set_opp_table_LV.bat opp table
```

```
[OPPØ ]: Ø
                   uv Ø
                                khz
|[OPP1 ]: 843750
                   uv 3200000
                                khz
|[OPP2 ]: 843750
                   uv 3200000
                                khz
[OPP3 1: 843750
                   uv 2400000
                                khz
|[OPP4 ]: 843750
                   uv 3200000
                                khz
[[OPP5 ]: 843750
                   uv 2400000
                                khz
|[OPP6 ]: 843750
                   uv 3200000
                                khz
|[OPP7 ]: 843750
                   uv 2400000
                                khz
|[OPP8 ]: 737500
                   uv 2400000
                                khz
[OPP9 ]: 737500
                   uv 2400000
                                khz
[OPP10]: 737500
                   uv 1534000
                                khz
[[OPP11]: 737500
                   uv 2400000
                                khz
[OPP12]: 737500
                   uv 1534000
                                khz
[OPP13]: 737500
                   uv 1534000
                                khz
[OPP141: 737500
                   uv 1534000
                                khz
[OPP15]: 687500
                   uv 1534000
                                khz
```



```
住
     adb
                                                            Vcore
4.
 5
                                                     Opp0 Vcore
                          3200,2400,1534 下
                                                    0.84375 0.7375,0.6875
             1866
                    0.84375
                                  OPP1
                                                OPP2
echo OPP ID > /sys/devices/platform/10012000.dvfsrc/helio-dvfsrc/dvfsrc_force_vcore_dvfs_opp
     不 HV preload
                      OPP8 0.7375V
                                                                      Vcore
     0.7375V VDD2 1.12V
 /sys/devices/platform/10012000.dvfsrc/helio-dvfsrc/dvfsrc_opp_table
             住
5.
                     cat /sys/devices/platform/10012000.dvfsrc/helio-dvfsrc/dvfsrc dump
  不
                       catch
```

```
sys/devices/platform/10012000.dvfsrc/helio-dvfsrc/dvfsrc_dump
Vcore : 843750 uv (PMIC: 0x34)
DDR : 1866000 khz
```



Step1: 1

Only need to do this for once on your PC

Download and install JAVA

http://www.java.com

Install Android SDK to have ADB.

- http://developer.android.com/sdk/index.html
- Remember to add ADB in your PATH.

取消

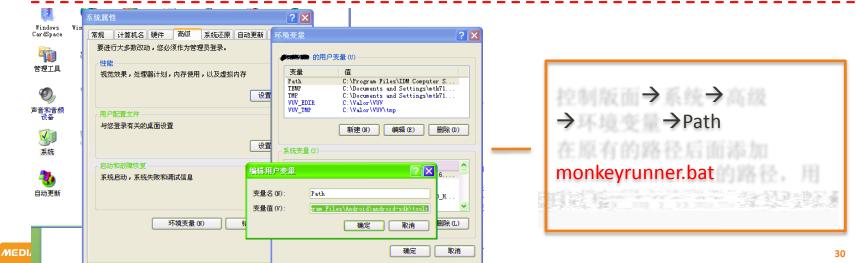
应用(A)

- EX: C:\ path = %path%; YOU ADB PATH
- 变ADB 住 tool 不 monkeyrunner.bat
 PATH EX ADB D:\Program Files monkeyrunner.bat住
 D:\Program Files\Android\android-sdk\tools

PC PATH

Install a python environment to be able to run python programs.

 For example, download Python 2.7.3 Windows Installer (Windows binary -- does not include source) from http://www.python.org/getit/



2/8

```
    Step2. 2
    Test_Tools.rar
    Test_Tools
    adb, SP_Driver_V2.0
    Note1. MOL不 MTK_MVG_TOOLs.rar,
    Note2. Test_Tools reboot_script DVFS_Nenamark_Memtester_Script suspend_and_DVFS script OA
    Stess Test UART log
```

3/8

(4/8)

Step5. device id

```
不
         eo
                       eo
c d gxkeg
                     gxkeg k
                                  不
                                         23456789 CDEF
             C:\Users\mtk07417>adb devices
             List of devices attached
             Ø123456789ABCDEF
                                   device
  UaPgpcoctmaogovg va etkrvaNRFFT6
                                                     vctvaF UaP4a goavg v dcv
 gv gxkegk
                                            gxkeg k. 不
             | 1_start_DVFS_N2_Mem_test.bat - 记事本
             文件(F) 编辑(E) 格式(O) 查看(V) 帮助(H)
             @echo off
             setlocal EnableDelayedExpansion
             set deviceid=-s 0123456789ABCDEF
             set memtester=/data/memtester
             set chk_status=/data/memtest_check_status.sh
             set test rank=no
             set test_num=6
```



Step6. Install_Nenamark2.bat

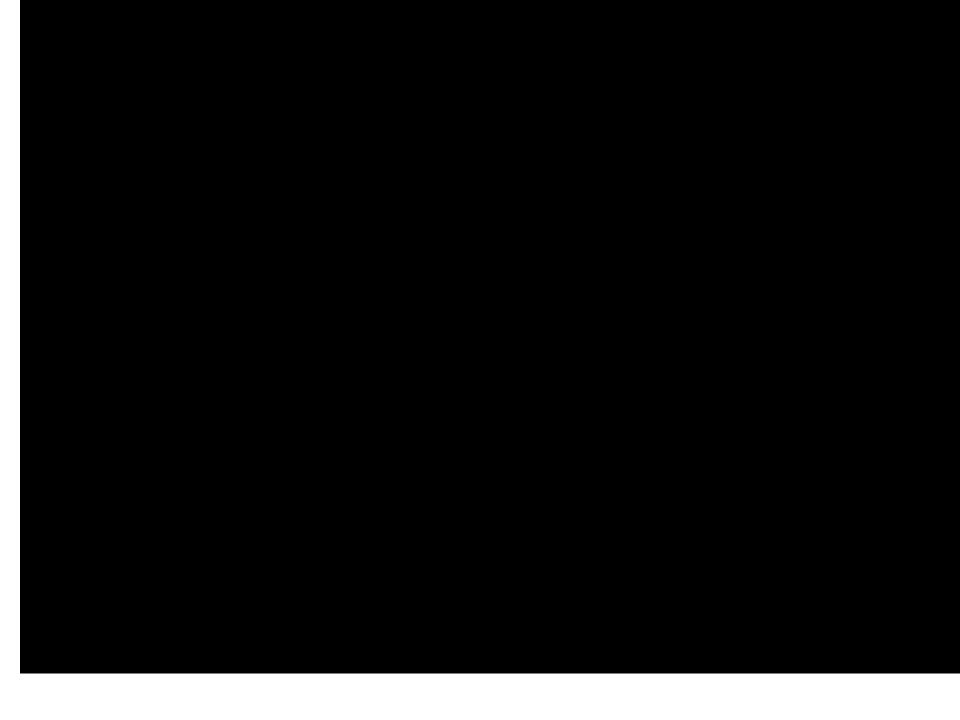
```
C:\Users\mtk07417\Desktop\DUFS_Nenamark_Memtester_Script>echo === install NenaMark ===
=== install NenaMark ===

C:\Users\mtk07417\Desktop\DUFS_Nenamark_Memtester_Script>adb install -r C:\Users\mtk07417\Desktop\DUFS_Nenamark_Memtester_Script\benchmark_apk\NenaMark2.apk
3607 KB/s (10200353 bytes in 2.761s)
Success

C:\Users\mtk07417\Desktop\DUFS_Nenamark_Memtester_Script>ping 127.0.0.1 -n 5 -w
1000 1>nul

C:\Users\mtk07417\Desktop\DUFS_Nenamark_Memtester_Script>adb install -r C:\Users\mtk07417\Desktop\DUFS_Nenamark_Memtester_Script\benchmark_apk\NenaMark2.apk
3628 KB/s (10200353 bytes in 2.745s)
Success
```

```
NenaMark2 , choose what to allow NenaMark2 to access 的 , continue Nenamark2 run 3D
```



(7/8)

mtester version 4.3.0 (64-bit)

HV OPP table

LV OPP table

Step9.

停HV

set_opp_table_HV.bat

Vindows\system32\cmd.exe

停LV

set_opp_table_LV.bat

· 停NV

OPP table

device id

- Step10: adb shell
- sh /data/run.sh &
- Step11: adb shell
- sh /data/vcorefs_cervino.sh &
- Step12:

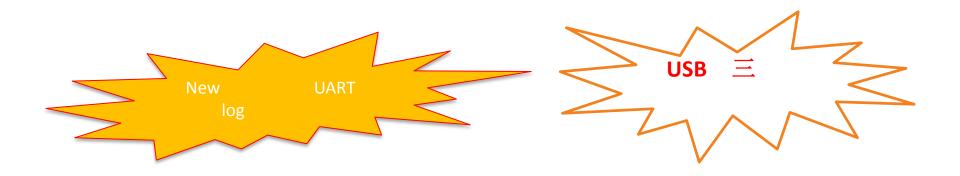
DVFS_Nenamark_memtest_script_LPDDR4
start_DVFS_N2_Mem_test.bat
n ,后 3D
, 3D run
display the x and y point.pdf

opyright (C) 2001-2012 Charles Cazabon. icensed under the GNU General Public License version 2 (only). ount succeeded ush memtester" 100x1 /data/mentest check status.sh emtester version 4.3.0 (64-bit) total " 402653184 Copyright (C) 2001-2012 Charles Cazabon. each "67108864 icensed under the GNU General Public License version 2 (only). == invoke mentester ===" CHECK SUME Copyright (C) 2001-2012 Charles Cazabon. version 2 (only). Licensed under the GNU General Public Licens C:\Windows\system32\cmd.exe emtester version 4.3.0 (64-bit) opyright (C) 2001-2012 Charles Cazabon. ersion 2 (only). icensed under the GNU General Public License C:\Windows\system32\cmd.exe mentester version 4.3.0 (64-bit) Copyright (C) 2001-2012 Charles Cazabon. version 2 (only). Licensed under the GNU General Public License _ 0 ■ Usrpub (\\Mediatek.inc\taiwan) mtester version 4.3.0 (64-bit) start DVFS N2 Mem test.bat puright (C) 2001-2012 Charles Cazabon. 👊 网络 (only). ensed under the GNU General Public License version **172.26.2.145** vcorefs cervino.sh MB0912312225 vcorefs cervino direct run gesize is 4096 gesizemask is Øxfffffffffffff000 ■ NB11090024 vcorefs_cervino_no_desense ant 32MB (33554432 bytes) 32MB (33554432 bytes), trying mlock ...

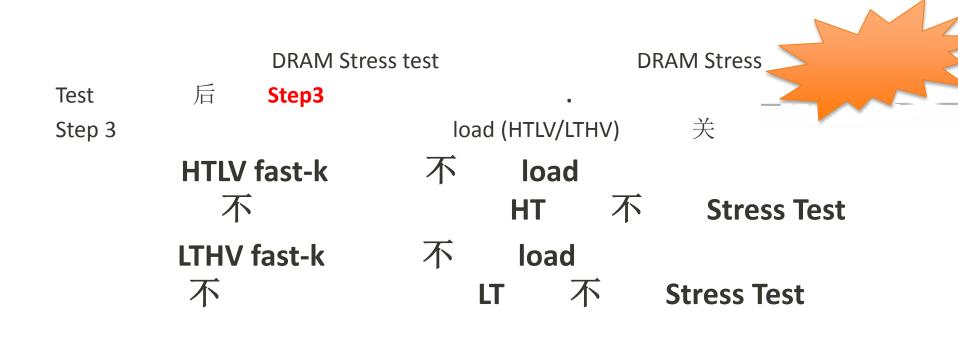
DRAM Stress test

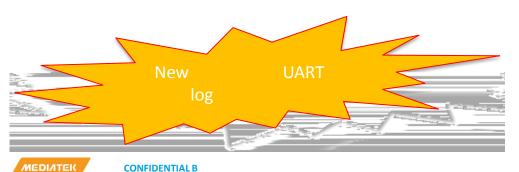
(8/8)

- Step13. 三 USB 8 Stress test
- Step14. " rc "
- Step15. >3 HTLV\LTHV\NTNV 不 Stress test
- preloader bin, preloader bin, preloader bin,
- download.



Nenamark2 + DVFS for Fast-K







SUSPEND/RESUME



Suspend/Resume

(1/3)

- Preloader bin
- always on
 MTK mobile log
- Step1. suspend_loop debug务
- Step2. _____suspend_loop_push.bat 份

```
_ 🗆 ×
C:\WINDOWS\system32\cmd.exe
b shell "chmod +rwx /data/suspend_loop.sh"
D:\$$8\Task\$ylvia\MUG\upload\Test_Tools\suspend_and_DUF$ sc<u>ript\suspend_loop>ad</u>
b shell "setprop log.tag S"
D:\$$8\Task\$ylvia\MUG\upload\Test_Tools\suspend_and_DUF$ script\suspend_loop>ad
b shell "echo 1 > /proc/mtprintk"
D:\S$8\Task\Sylvia\MUG\upload\Test_Tools\suspend_and_DUFS                    script\suspend_loop>ad
b shell "echo 8 8 8 8 > /proc/sys/kernel/printk"
D:\S$8\Task\Sylvia\MVG\upload\Test_Tools\suspend_and_DVFS script\suspend_loop>ec
ho === 300m DUFS script ===
=== 300m DVFS script ===
D:\SS8\Task\Sylvia\MUG\upload\Test_Tools\suspend_and_DUFS script\suspend_loop>ad
b push dvfs_300m.sh /data/dvfs_300m.sh
30 KB/s (1448 bytes in 0.046s)
D:\SS8\Task\Sylvia\MUG\upload\Test_Tools\suspend_and_DUFS script\suspend_loop>ad
b shell chmod 777 /data/dvfs_300m.sh
D:\$$8\Task\$ylvia\MUG\upload\Test_Tools\suspend_and_DUF$ script\suspend_loop>pa
```

Suspend/Resume

(2/3)

```
■ Step3. cmd

adb shell

sh /data/suspend_loop.sh &

D:\adb_1_031>adb shell

k71v1_64_bsp:/#_sh /data/suspend_loop.sh &

sh /data/suspend_loop.sh &

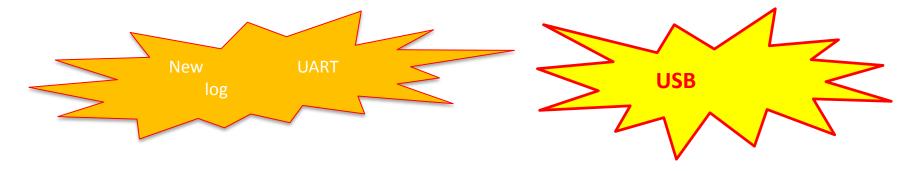
[11 3309

k71v1_64_bsp:/# !!![@@@]!!!!_wakeup_!!![@@@]!!!

Step4. usb, usb, usb,  

power monitor usb adapter
```

12



Suspend/Resume

(3/3)

停 Step5. adb shell cat /sys/kernel/debug/cpuidle/spm/spm_sleep_count 不 0 **USB USB** 662 1.USB C:\Users\mtk07417>adb shell cat /sys/kernel/debug/cpuidle/spm/spm_sleep_count 662 66 3 5" Step6. rc不 Step7. >3 **UART USB**

REBOOT (DDR RESERVE MODE, FULL-K FAST K)



DDR reserve mode Reboot

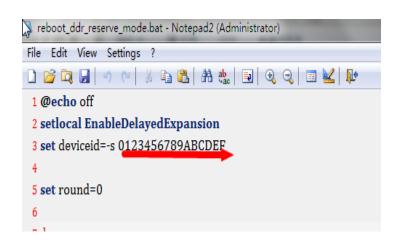
(1/2)

- DDR Reserve mode test
 reserve mode reboot DRAM
 reboot debug
- ${\sf DDR}$ reserve mode ${\it self}$ reboot ${\sf DDR}$ self refresh, reboot ${\sf DRAM}$,

Step1. Preloader bin

always on

Step2. reboot_scriptid 不reserve mode"Note:Opp table 16



MTK mobile log

reboot_ddr_reserve_mode.bat device id reboot "reboot with ddr

```
adbd is already running as root reboot ddr-reserve, opp table: 0 2018/04/09 周一 9:48:48.02 adbd is already running as root reboot ddr-reserve, opp table: 1 2018/04/09 周一 9:48:48.02 adbd is already running as root reboot ddr-reserve, opp table: 2 2018/04/09 周一 9:48:48.02 adbd is already running as root reboot ddr-reserve, opp table: 3
```

```
reboot ddr-reserve, opp table: 13
2018/04/09 周— 9:48:48.02
adbd is already running as root
reboot ddr-reserve, opp table: 14
2018/04/09 周— 9:48:48.02
adbd is already running as root
reboot ddr-reserve, opp table: 15
2018/04/09 周— 9:48:48.02
reboot ddr-reserve, round: 16, opp ta
adbd is already running as root
reboot ddr-reserve, opp table: 0
2018/04/09 周— 10:27:02.44
adbd is already running as root
reboot ddr-reserve, opp table: 1
```

DDR reserve mode Reboot

(2/2)

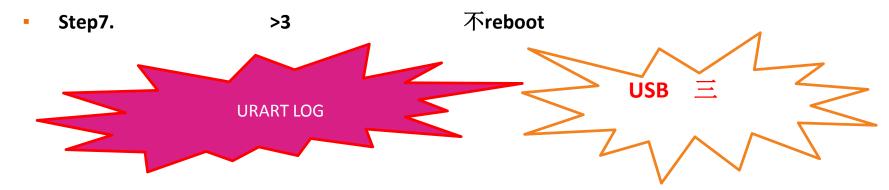
- Fail √RGU] WDT DDR reserve mode FAIL!
- PRCUU ADDR RESERVED A 不 log pass

 [RGU] WDT DDR reserve mode success! 1387F1

 [DDR Reserve] DCS/DVFSRC success! (dcs_en=0, dvfsrc_en=1)

 [RGU] WDT DDR reserve mode success! 1387F1

 [RGU] DDR RESERVE Success 1



[DDR Reserve] release dram from self-refresh PASS!

Full-K Reboot

(1/2)

```
    Si ep1 Preloader full k bin.
    Full k bin
    1 define DRAM_HQA
    2: dramc_pi_api.h
    Idefine SUPPORT_SAVE_TIME_FOR_CALIBRATION CFG_DRAM_CALIB_OPTIMIZATION
    define SUPPORT_SAVE_TIME_FOR_CALIBRATION 0
```

Step 2. always on MTK mobile log

Step3. reboot_full_k.bat device id

• id

- Note1: Full k 5
- Note2 device id

```
DR : 3
reboot full-k, opp table: 1
                         : 3200000
2018/09/12 周三 19:05:08.24
Ucore
                         : 800000
                                        (PMIC: 0x2d)
DDR
                         : 2400000
                                    khz
reboot full-k, opp table: 7
2018/09/12 周三 19:05:08.24
Vcore
                                        (PMIC: 0x1d)
                                    uν
                                    khz
reboot full-k, opp table: 8
2018/09/12 周三 19:05:08.24
                                        (PMIC: 0x1d)
Vcore
                         : 1534000
                                    khz
reboot full-k, opp table: 14
2018/09/12 周三 19:05:08.24
Vcore
                         : 650000
                                        (PMIC: 0x15)
                         : 1534000
                                    khz
reboot full-k, opp table: 15
2018/09/12 周三 19:05:08.24
reboot full-k, round: 5
Vcore
                         : 800000
                                        (PMIC: 0x2d)
                         : 3200000
reboot full-k, opp table: 1
2018/09/12 周三 19:07:41.00
```

Full-K Reboot

(2/2)

Step4. opp table

住

12

Step5.

rc

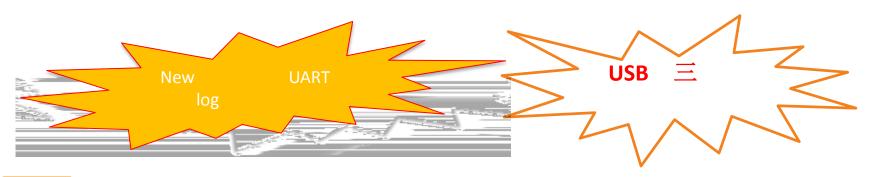
"

3 5"

Step6.

>3

不reboot



Fast-k Reboot

(1/2)

LPDDR4 LPDDR3



Preloader bin

LV bin

不

Fast-k Stress test



不

Step1. reboot_script reboot_fast_K.bat device id

id

Fast-k Reboot

(2/2)

Step2. reboot fast K.bat 12 C:\Windows\system32\cmd.exe reboot, round: 1, opp table: 1 2018/09/13 周四 12:15:11.59 reboot, round: 2, opp table: 2 2018/09/13 周四 12:16:28.62 reboot, round: 3, opp table: 3 2018/09/13 周四 12:17:44.05 reboot, round: 4, opp table: 0 2018/09/13 周四 12:18:59.11 reboot, round: 5, opp table: 1 Step3. pass Step4. **UART log UART log** n i kng Urnkvvgt 不 ni Save calibration result to emmc _ Fail Bypass saving calibration result to emmc ^ **PASS** 不reboot >3 NT Step5. Fail **PASS** code, **Note** log **USB URART LOG**

PASS



pass

(1/3)

1. N

2. memtester memtester memtester

不 fail

memtester Error detected 7

```
"wait for device.."
adbd is already running as root
remount succeeded
adbd is already running as root
"push memtester"
2169 KB/s (319856 bytes in 0.144s)
108 KB/s (555 bytes in 0.005s)
"total " 335544320
"each "67108864
check_sum=6
IDRAM_MEMTESTI Error detected, exit
Press any key to continue . . .
```

collect_memtest_log.bat log memtester fail log MTK

pass

(2/3)

```
3. 不 不 4 KE,HWT HW_reboot, MEMTEST,
不 份 fail, 3 pass
(1) /data/aee_exp (2) /data/vendor/mtklog/aee_exp
3 份 fail, log MTK
```

```
1 cmd
adb shell
cd data/aee_exp
ls
aee_exp
4
```

```
Microsoft Windows [版本 6.1.7601]
版权所有 (c) 2009 Microsoft Corporation。保留所有权利。

C:\Users\mtk07417\adb shell
evb6758_64:/ # cd data/aee_exp
cd data/aee_exp
evb6758_64:/data/aee_exp # 1s
ls
db_history
evb6758_64:/data/aee_exp #
```

pass

mtklog

log

mtklog

(3/3)

usb

mtklog

```
KE/HWT/HW_Reboot/
  /data/vendor/mtklog/aee_exp
                         db
                                  pull log.bat pull
                DB
                                                           MTK
  C:\Users\mtk10621\adb shell
  evb6765_64_emmc:/ # cd /data/vendor/mtklog/aee_exp
  evb6765_64_emmc:/data/vendor/mtklog/aee_exp # ls -al
  total 16
  ---- 1 root root
                     0 2010-01-01 04:04 aee.lck
  drwxrwxrwx 2 root root 4096 2010-01-01 04:04 db.00.KernelAPI
       -r-- 1 root root 103 2010-01-01 04:04 db_history
  evb6765_64_emmc:/data/vendor/mtklog/aee_exp #
              pull
                           MTK
aee exp
```

1.

2.

pull_log.bat

1

pull log.bat

MTK



CONFIDENTIAL B

54

ETT BIN 不

> 停Format whole flash \rightarrow

key.

 \rightarrow **UART** cable

1.8V,

log.

Jump, Address

UART cable

双

不Download

 \rightarrow **UART** RX, TX GND

ETT

 \rightarrow

adb

 \rightarrow ADB 双 务

APK

 \rightarrow APK

eMMC R/W

 \rightarrow 32bit 64bit,

Power KEY

 \rightarrow ->30 ->

	NTNV/LT Thermal	HV 3	BD		HTLV					1	Log
Therma	65 al	5	不停	停 NTC	PCB 停				PA 100	Therma	l ADC
况 1. 2.		N	ITC	10K							
3. 4.	Th LTE		Throttling mal Throttli	务 ing	不 不	3	1	2			
Mobile Log LTE Throttling LTE throttling Throttling AP Throttling (Log 3	נז	ΓE	

МЕДІЛТЕК

How To Modify Thermal Policy

thermal throttling (1)User sw load thermal throttling (a) Get root permission (b) adb shell "/system/bin/thermal manager /etc/.tp/.ht120.mtc" (for Android M) adb shell "/vendor/bin/thermal manager /vendor/etc/.tp/.ht120.mtc"(for Android N) (c) cat /data/.tp/.settings /vendor/etc/.tp/.ht120.mtc代表修改成功 /etc/.tp/.ht120.mtc thermal throttling (2)Eng sw load 不others-thermal (a) thermal policy high temp 120deg c, apply (b) adb shell "/system/bin/thermal manager /etc/.tp/.ht120.mtc" (for Android M) adb shell "/vendor/bin/thermal manager /vendor/etc/.tp/.ht120.mtc"(for Android N) (c) cat /data/.tp/.settings /etc/.tp/.ht120.mtc /vendor/etc/.tp/.ht120.mtc代表修改成功 (3)僅取消LTE throttling,保留其餘的thermal throttling功能 (a)adb shell "echo 1 120000 0 mtk-cl-shutdown02 0 0 no-cooler 0 0 no-cooler 0 0 no-cooler 0 0 nocooler 0 0 no-cooler 1000 > /proc/driver/thermal/tzbtspa ^ cat /proc/driver/thermal/tzbtspa. 如果 (b)

cooldev1=mtk-cl-mutt02,cooldev2=mtk-cl-mutt01,cooldev3=mtk-cl-mutt00,

cooler,cooldev2=no-cooler,cooldev3=no-cooler代表修改成功



成cooldev1=no-

How to check LTE throttling is triggered?

Thermal Mobile Log

 How to Check if LTE throttling is triggered from mobilelog searching keyword in kernel log

```
^ š Z Œ u o l } } o Œnhtk \( \text{LCE} \) is nutt_s\( \text{PCE} \) mutt_limit _ If the following log is found, LTE throttling is triggered.
```

```
[0) [481:kworker/0:2] [Auxadc] [AUXADC] ch=4 raw=1466 data=544
[0) [481:kworker/0:2] [Power/PA_Thermal] PA T=111000
[0) [481:kworker/0:2] [Power/BTSMDPA Thermal] T btsmdpa=61000
[0) [481:kworker/0:2] [thermal/cooler/mutt[mtk_cl_mutt_set_mutt_limit] ret 0 param 20101 bcnt 11
[0) [481:kworker/0:2] [Power/BTS_Thermal] T_AP=56000
[0) [55:cfinteractive] [Power/cpufreq] _mt_cpufreq_power_limited_verify(): idx = 10, limited_max_s
```

LTE Thermal Throttling Transceiver 之
Debug
SOP Eservice



MEDIATEK

everyday genius