MP2721

I²C Controlled 1-cell 5A NVDC Buck Charger

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP2721 is a highly-integrated 5A switching-mode battery management device for single-cell Li-ion or Li-polymer battery. The Narrow-VDC (NVDC) power management structure provides low impedance power path which optimizes charging efficiency, reduces battery charging time and extends battery life during discharging.

USB Battery Charging Specification 1.2 (BC1.2) and non-standard adaptor detection are supported by the input source type identification algorithm.

The I²C interface offers complete operating control, charging parameter programming and status/interrupt monitoring.

The MP2721 supports fully-customizable JEITA profile with programmable temperature windows and actions.

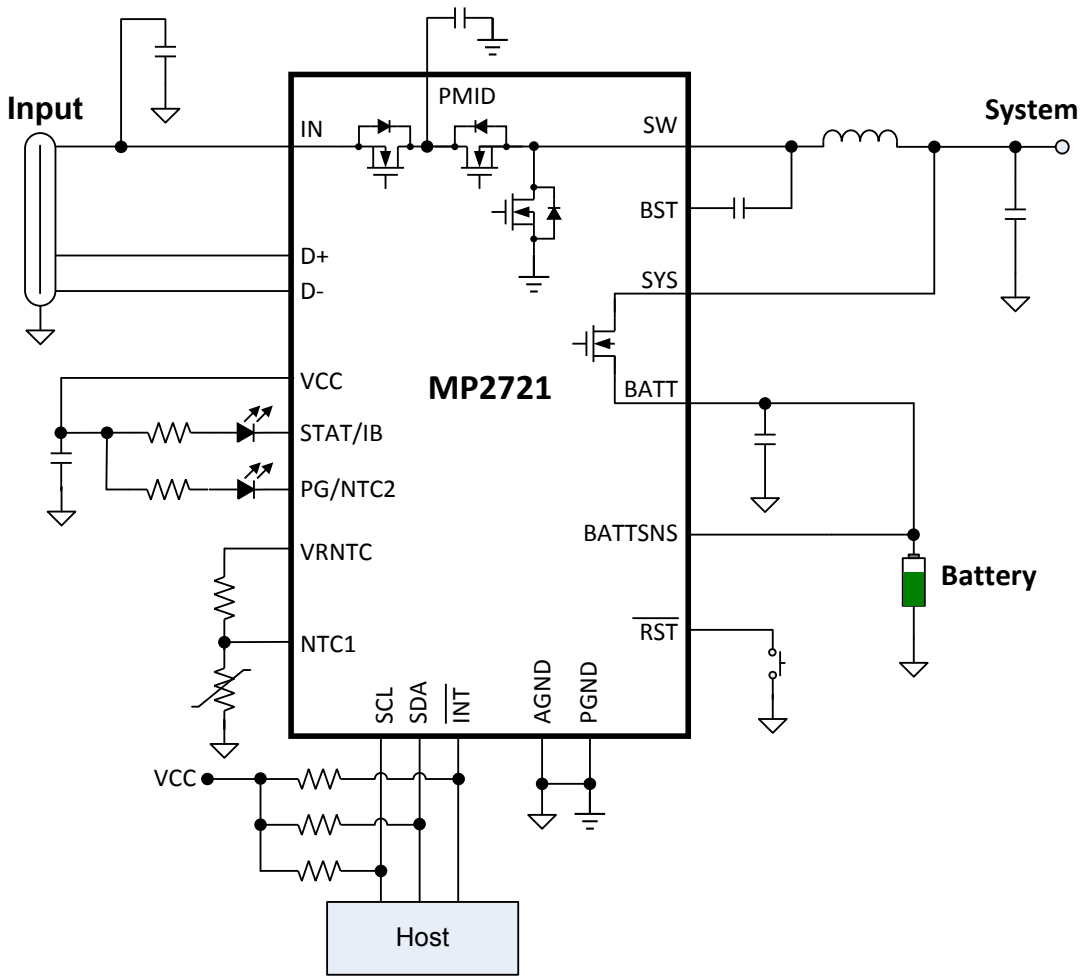
FEATURES

- 5A NVDC Switching Charger with Power Path
- Support USB BC1.2 and Non-Standard Adaptors
- 26V Sustainable Input Voltage
- 80mA to 5A I²C Programmable Charge Current
- 100mA to 3.2A I²C Programmable Input Current Limit
- Minimum Input Voltage Loop for Maximum Adaptor Power Tracking
- Comprehensive Safety Features
  - Fully-customizable JEITA Profile
  - Additional NTC Thermistor Input
  - Programmable Die Temperature Regulation from 60°C to 120°C
  - Complete Charge and Pre-Charge Safety Timers
  - Watchdog Safety Timer
  - Lockable Registers for Charging Parameters
- Programmable Switching Frequency from 750kHz to 1.5MHz
- Integrated 15mΩ Low-Rdson Battery FET with Shipping and Reset Modes
- Ultra-low 8.5μA Battery Discharge Current in Shipping Mode
- Down to 30mA Termination Current Settings for Wearable Applications
- I²C Port for Flexible System Parameter Setting and Status Reporting
- Programmable Boost-converter for Source Mode (OTG)
  - Programmable Output Current Limit Loop up to 3A
  - Output Over-current Protection
  - Ability to Power into Large Capacitive Loads up to 2mF
  - Programmable Output Voltage from 5.0V to 5.35V
- Accuracy
  - +/- 0.5% Battery Regulation Voltage
  - +/- 5% Charge Current
  - +/- 5% Input Current Limit
  - Remote Battery Sensing for Fast Charge
  - ±2% Output Regulation in Boost Mode
- Small QFN-22(2.5mm×3.5mm) Package

APPLICATIONS

- General <=15W USB Applications
- Bluetooth Headphones
- Bluetooth Speakers
- POS Terminals
- Portable Cameras

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2721GRH-xxxx**	QFN-22 (2.5mmx3.5mm)	*See Below*	1
EVKT-MP2721	Evaluation Kit		

* For Tape & Reel, add suffix –Z (e.g. MP2721GRH-xxxx–Z)
**"xxxx" is the register setting option. The factory default is "0000." This content can be viewed in the I²C register map. Contact an MPS FAE to obtain an "xxxx" value.

TOP MARKING

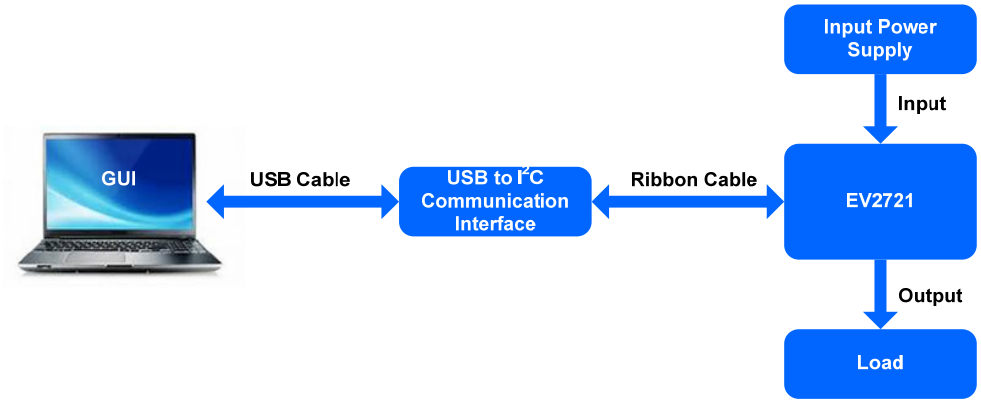
BNV: Product code of MP2721GRH
Y: Year code
WW: Week code
LLL: Lot number

EVALUATION KIT EVKT-MP2721

EVKT-MP2721 Kit contents: (Items below can be ordered separately).

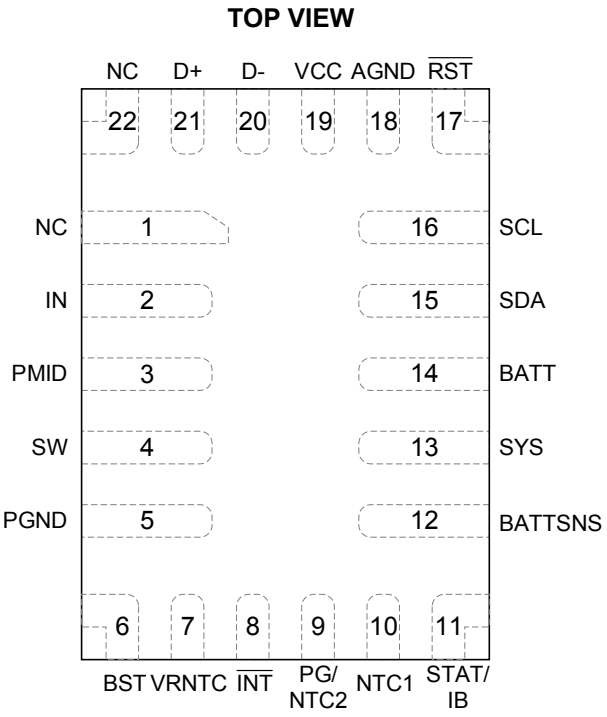
#	Part Number	Item	Quantity
1	EV2721-RH-00A	MP2721 evaluation board	1
2	EVKT-USBI2C-02-BAG	Includes one USB to I²C communication interface device, one USB cable, and one ribbon cable	1
3	Online resources	Include: Datasheet, User guide, Product brief, and GUI	1

Order directly from www.MonolithicPower.com or our distributors.



EVKT-MP2721 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-22 (2.5mm×3.5mm)

PIN FUNCTIONS

Package Pin #	Name	Type(1)	Description
2	IN	P	Power input. Place a 1µF ceramic capacitor from IN to PGND.
3	PMID	P	Decoupling node of power stage. Bypass it with minimum 10µF ceramic capacitor from PMID to PGND, placed as close to the IC as possible with shortest route.
4	SW	P	Switching node. Connect SW to the inductor.
6	BST	P	Bootstrap power. Connect a 100nF capacitor between BST and SW pin to form a floating supply for the high side power MOSFET driver.
13	SYS	P	System power output. Place minimum 20µF ceramic capacitor from SYS to PGND.
14	BATT	P	Battery positive terminal. The internal NVDC battery FET is connected between SYS and BATT pin. Place minimum 20µF ceramic capacitor from BATT to PGND.
5	PGND	P	Power ground. Short to AGND on PCB.
18	AGND	P	Analog ground. Short to PGND on PCB.
19	VCC	P	Internal circuit power supply. Connect a 4.7µF ceramic capacitor from VCC to AGND as close to the IC as possible.
12	BATTSNS	AI	Battery voltage sense pin for battery voltage regulation. Connect to the positive battery pack terminal as close as possible.
8	$\overline{\text{INT}}$	DO	Open-drain interrupt output. An active low 256us pulse is generated on this pin when the IC has status or fault report. Pull up this pin with a 10kΩ resistor to VCC or other logic rail.
16	SCL	DI	I²C interface clock. Pull up this pin with a 10kΩ resistor to VCC or other logic rail.
15	SDA	DIO	I²C interface data. Pull up this pin with a 10kΩ resistor to VCC or other logic rail.
1	NC	N/A	This pin can be short to AGND or left open.
22	NC	N/A	This pin can be short to AGND or left open.
21	D+	AIO	Positive line of the USB data line pair. USB charger type detection based on BC1.2 and non-stand adaptors is implemented.
20	D-	AIO	Negative line of the USB data line pair. USB charger type detection based on BC1.2 and non-stand adaptors is implemented.
17	$\overline{\text{RST}}$	DI	Battery FET reset input. During shipping mode, a logic low of $t_{SHIPMODE}$ wakes up the IC from shipping mode. When VIN is not present, a logic low of t_{RST} resets SYS power by turning battery FET off for t_{SYS_RST} and then re-enables battery FET. This pin has an internal 200kΩ pull-up.
7	VRNTC	AO	Voltage output for powering up the NTC. The VRNTC is powered to the same voltage as VCC when the buck or boost converter operates.
10	NTC1	AI	Temperature sense input #1. Connect to a negative temperature coefficient thermistor. Connect a resistor divider from VRNTC to NTC1 to AGND. JEITA profile is supported.
9	PG/NTC2	DO/AI	Open drain power good indicator. Pull up with a 10kΩ resistor. Active low when VIN_GD bit is 1. Can be configured as Temperature sense input #2.

PIN FUNCTIONS *(continued)*

Package Pin #	Name	Type(1)	Description
11	STAT/IB	DO/AO	Charge status open drain output. Pull up this pin with a 10kΩ resistor. LOW indicates charging in progress. HIGH indicates not in charging or charging completes. Blinking with 1Hz indicates fault happens. Can be configured as battery current indication. IB pin sources a current which is proportional to the charge or discharge current of the battery. Connect a resistor from IB to AGND to get the battery current information.

(1) AI = Analog Input, AO = Analog Output, AIO = Analog Input Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input Output, P = Power

ABSOLUTE MAXIMUM RATINGS (1)

IN to PGND ..... -0.3V to 26V
PMID to PGND..... -0.3V to 26V
SW to PGND .....-0.3V(-2V for 20ns) to 24V
PMID to IN..... -0.3V to 12V
BATT, SYS to PGND ..... -0.3V to 6.5V
BST to SW……..... -0.3V to 5V
All Other Pins to AGND ..... -0.3V to 5V
Continuous Power Dissipation (T_A=+25°C)(2) 2W
Junction Temperature..... 150°C
Lead Temperature (Solder) ..... 260°C
Storage Temperature…. .....-65°C to +150°C

ESD Ratings

Human Body Model (HBM) (3) 2000V
Charged Device Model (CDM) (4).....250V

Recommended Operating Conditions (5)

Supply Voltage (V_{IN})..... 3.9V to 16V
Input Current (I_{IN}) ..... Up to 3.2A
System Current (I_{SYS})..... Up to 5A
Charge Current (I_{CC}) ..... Up to 5A
Discharge Current (I_{DISCHG}) ..... Up to 8A
Battery Voltage (V_{BATT})..... Up to 4.6V
Operating Junction Temp. (T_J) -40°C to +125°C

Thermal Resistance (6)	θ_{JA}	θ_{JC}	
QFN-22(2.5mm×3.5mm)	50	12	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissip[ration will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per ANSI/ESDA/JEDEC JS-001, all pins.
4) Per ANSI/ESDA/JEDEC JS-002, all pins.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_A = -40℃ to 125℃, T_A=25°C and V_{BATT}=4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
QUIESCENT CURRENT						
Battery Discharge Current in Ship Mode	I_{BATT_SHIP}	V_{BATT}=4V, V_{IN}=0V, BATTFET disabled, T_A <85°C		8.5	12	μA
Battery Discharge Current in Idle Mode	I_{BATT_IDLE}	V_{BATT}=4V, V_{IN}=0V, BATTFET enabled, T_A <85°C		44	58	μA
USB Suspend Mode Current	I_{IN_SUSP}	V_{IN}=5V, EN_BUCK=0		0.8		mA
POWER ON/OFF						
Input Operating Range	V_{IN_OP}		3.9		16	V
Input Under-voltage Lock-out Threshold	V_{IN_UV}	V_{IN} falling, V_{BATT}=0V	3.1	3.25	3.45	V
Input Under-voltage Lock-out Threshold Hysteresis	$V_{IN\_UV\_HYS}$	V_{IN} rising, V_{BATT}=0V		250		mV
Input Debounce Time	t_{DEB}	V_{IN} debounce to set VIN_GD		15		ms
Hold-off Timer	t_{HOLD}	VIN_GD=1 to D+D- detection starts		250		ms
Input vs. Battery Voltage Headroom Threshold	V_{HDRM}	V_{IN}-V_{BATT}, V_{BATT}=4V, VIN rising	150	250	350	mV
		V_{IN}-V_{BATT}, V_{BATT}=4V, VIN falling		90		mV
Input Over-voltage Protection Threshold	V_{IN_OV}	V_{IN} rising, VIN_OVP = 6.3V	6.1	6.3	6.55	V
		V_{IN} rising, VIN_OVP = 11V	10.5	11	11.55	V
		V_{IN} rising, VIN_OVP = 14V	13.5	14	14.55	V
Input Over-voltage Protection Hysteresis	$V_{IN\_OV\_HYS}$	V_{IN} falling		250		mV
BATT Under-voltage Lock-out Threshold	V_{BATT_UV}	V_{IN}=0, V_{BATT} falling	2.4	2.5	2.6	V
BATT Under-voltage Lock-out Hysteresis	$V_{BATT\_UV\_HYS}$	V_{IN}=0, V_{BATT} rising		400		mV
POWER PATH						
System Regulation Voltage	V_{SYS_REG}	V_{BATT}<V_{SYS_MIN}, SYS_MIN=100	3.7	3.82	3.94	V
Blocking FET On Resistance	R_{ON_RBFET}	T_A=25°C		15		mΩ
High-side FET On Resistance	R_{ON_HS}	T_A=25°C		25		mΩ
Low-side FET On Resistance	R_{ON_LS}	T_A=25°C		25		mΩ
Battery FET On Resistance	R_{ON_BFET}	T_A=25°C		14		mΩ
Battery FET Forward Voltage in Supplement Mode	V_{FWD}			30		mV

ELECTRICAL CHARACTERISTICS *(continued)*

T_A = -40℃ to 125℃, T_A=25°C and V_{BATT}=4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
CHARGE (T_A = 0℃ to 70℃)						
Charge Voltage Program Range	V_{BATT_RANGE}		3.600		4.600	V
Charge Voltage Step	V_{BATT_STEP}			25		mV
Battery Charge Voltage Regulation	V_{BATT_REG}	V_{BATT}=4.2V	4.179	4.200	4.221	V
		V_{BATT}=4.35V	4.328	4.350	4.372	V
Charge Current Regulation Range	I_{CC_RANGE}		0		5000	mA
Charge Current Step	I_{CC_STEP}			80		mA
Fast Charge Current	I_{CC}	ICC=1040mA, V_{BATT}=3.8V	0.98	1.04	1.15	A
		ICC=2000mA, V_{BATT}=3.8V	1.90	2.00	2.10	A
Pre-charge to Fast Charge Threshold	V_{BATT_PRE}	V_{BATT} rising, VPRE = 3V	2.9	3	3.1	V
Pre-charge to Fast Charge Threshold Hysteresis		V_{BATT} falling, VPRE = 3V		250		mV
Pre-charge Current	I_{PRE}	IPRE=240mA, V_{BATT}=2.5V	210	240	275	mA
Charge Termination Current Threshold	I_{TERM}	ITERM=120mA	90	120	150	mA
		ITERM=30mA	18	30	42	mA
Trickle Charge to Pre-charge Threshold	V_{BATT_TC}	V_{BATT} rising	1.9	2.0	2.1	V
Trickle Charge to Pre-charge Threshold Hysteresis		V_{BATT} falling		200		mV
Trickle Charge Current	I_{TC}	V_{BATT}=1V, ITRICKLE=128mA	100	128	160	mA
Auto-recharge Battery Voltage Threshold	V_{RECH}	V_{BATT} falling, VRECHG=100mV	45	90	130	mV
		V_{BATT} falling, VRECHG=200mV	135	190	240	mV
INPUT REGULATION (T_A = 0℃ to 70℃)						
Input Minimum Voltage Regulation	V_{IN_LIM}	VIN_LIM=3.88V, V_{BATT}=3.3V	3.76	3.88	4.00	V
		VIN_LIM=4.36V, V_{BATT}=3.3V	4.24	4.36	4.48	V
Input Minimum Voltage Regulation Tracking Battery	$V_{IN\_LIM\_BATT}$	VIN_LIM=3.88V, V_{BATT}=4V	100	200	300	mV
Input Current Limit	I_{IN_LIM}	IIN_LIM=500mA	430	460	500	mA
		IIN_LIM=1.5A	1.34	1.41	1.5	A
		IIN_LIM=3A	2.7	2.84	3	A
BATT OVER VOLTAGE PROTECTION						
Battery Over-voltage Protection Threshold	V_{BATT_OVP}	V_{BATT} rising, percentage of V_{BATT_REG}	103	105	106.5	%
Battery Over-voltage Protection Hysteresis				1.7		%

ELECTRICAL CHARACTERISTICS *(continued)*

T_A = -40℃ to 125℃, T_A=25°C and V_{BATT}=4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
THERMAL						
Junction Temperature Regulation(7)	T_{J_REG}	TREG=80°C		80		°C
		TREG=120°C		120		°C
Thermal Shutdown Rising Junction Temperature(7)	T_{J_SHDN}	Temperature rising		150		°C
Thermal Shutdown Hysteresis(7)	T_{SHDN_HYS}			30		°C
JEITA NTC MONITOR (T_A = 0℃ to 70℃)						
NTC Cold Temp Rising Threshold	V_{COLD}	As percentage of V_{VRNTC} VCOLD=74.2% (0°C)	73.9	74.5	75.1	%
NTC Cold Temp Rising Threshold Hysteresis		As percentage of V_{VRNTC}		1.4		%
NTC Cool Temp Rising Threshold	V_{COOL}	As percentage of V_{VRNTC} VCOOL=64.8% (10°C)	64.3	64.9	65.5	%
NTC Cool Temp Rising Threshold Hysteresis		As percentage of V_{VRNTC}		1.4		%
NTC Warm Temp Falling Threshold	V_{WARM}	As percentage of V_{VRNTC} VWARM=32.6% (45°C)	31.9	32.5	33.1	%
NTC Warm Temp Falling Threshold Hysteresis		As percentage of V_{VRNTC}		1.4		%
NTC Hot Temp Falling Threshold	V_{HOT}	As percentage of V_{VRNTC} VHOT=23.0% (60°C)	22.7	23.3	23.9	%
NTC Hot Temp Falling Threshold Hysteresis		As percentage of V_{VRNTC}		1.4		%
BATTFET Over Current Protection						
BATTFET Over Current Threshold	I_{BATT_OCP}		7.0			A
PWM converter						
Switching Frequency	f_{SW}	SW_FREQ=750kHz	650	750	850	kHz
		SW_FREQ=1000kHz	900	1050	1200	kHz
		SW_FREQ=1250kHz	1080	1230	1380	kHz
		SW_FREQ=1500kHz	1300	1450	1600	kHz
BOOST						
Boost Regulation Voltage	V_{PMID_REG}	VBOOST= 5.15V, T_A <85°C	5.08	5.15	5.22	V
BATT_LOW Comparator Falling Threshold	V_{BATT_LOW}	BATT_LOW=3.0V	2.88	3.0	3.12	V
		BATT_LOW=3.3V	3.20	3.33	3.46	V
BATT_LOW Comparator Hysteresis				200		mV
Battery Low Comparator Debounce Time	$t_{D\_BATT\_LOW}$			10		ms
Boost Output Current Limit	I_{BST_LIM}	OLIM=500mA T_A = 0°C to 70°C	500		600	mA
		OLIM=1.5A T_A = 0°C to 70°C	1500		1700	mA
Boost Over Voltage Protection Threshold	V_{BST_OVP}	Boost mode, V_{IN} rising	5.5	5.8	6.1	V

Notes: 7) Guaranteed by design.

ELECTRICAL CHARACTERISTICS *(continued)*

T_A = -40℃ to 125℃, T_A=25°C and V_{BATT}=4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC LDO						
VCC Output Voltage	V_{VCC}	V_{IN}=5V, I_{VCC}=5mA		3.65		V
IB OUTPUT						
IB Current Output Gain	I_{IB}	I_{IB}, Charging, I_{BATT}=100mA	1	2	3.2	µA
		I_{IB}, Charging, I_{BATT}=1A	18	20	22.8	µA
		I_{IB}, Discharging, I_{BATT}=100mA	1	2	3.2	µA
		I_{IB}, Discharging, I_{BATT}=1A	18	20	22.8	µA
IMPEDANCE TEST						
Input Impedance Test Current	I_{VIN_SRC}	IVIN_SRC=10µA	7	10	13	µA
		IVIN_SRC=40µA	34	40	46	µA
		IVIN_SRC=320µA	280	320	365	µA
Input Impedance Test Voltage Threshold	V_{VIN_TEST}	VIN_TEST=0.5V	0.46	0.5	0.54	V
		VIN_TEST=1.5V	1.4	1.5	1.6	V
LOGIC I/O for SCL, SDA, INT, RST, STAT						
Logic Input Low Voltage	V_{IL}				0.4	V
Logic Input High Voltage	V_{IH}		1.3			V
Open Drain Output Low Voltage	V_{OL}	I_{SINK} = 10mA			0.2	V
Pull Up Resistor of RST	R_{PULL_UP}			200		kΩ
D+/D- DETECTION						
DCD D+ Pull Up Current	I_{DP_SRC}		7	10	13	µA
DCD D- Pull Low Resistance	R_{DM_DWN}		16	20	24	kΩ
D+D- Source Voltage Low	V_{SRC_L}		550	600	650	mV
D+D- Source Voltage High	V_{SRC_H}		3.1	3.3	3.5	V
D+D- Sink Current	I_{SNK}		50	100	150	µA
Data Detect Voltage	V_{DAT_REF}		300	350	400	mV
Non Standard 1.2V Window	V_{1P2_TH}	Low threshold	0.95	1	1.05	V
		High threshold	1.33	1.4	1.47	V
Non Standard 2.0V Window	V_{2P0_TH}	Low threshold	1.73	1.8	1.87	V
		High threshold	2.17	2.25	2.33	V
Non Standard 2.7V Window	V_{2P7_TH}	Low threshold	2.3	2.4	2.5	V
		High threshold	2.9	3.0	3.1	V

ELECTRICAL CHARACTERISTICS *(continued)*

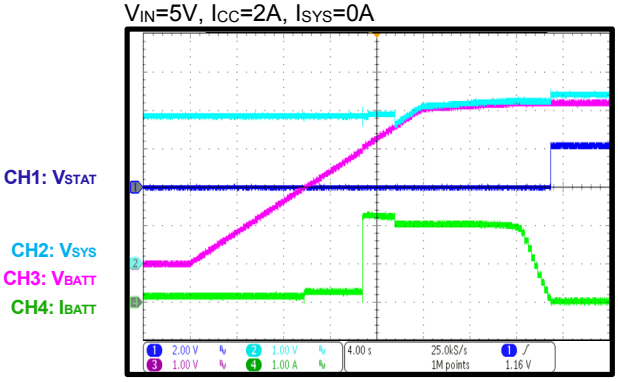
T_A = -40℃ to 125℃, T_A=25°C and V_{BATT}=4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
TIMING						
BATTERY CHARGER						
Charge Termination Deglitch Time	t_{TERM_DGL}			250		ms
Charge Timer	t_{CHG_TMR}	CHG_TIMER=10hrs	8	10	12	hr
Top-off Timer	t_{TOP_OFF}	TOPOFF_TIMER=30minus	24	30	36	min
Battery Auto-recharge Deglitch Time	t_{RECH_DGL}			100		ms
RST TIMING						
RST Low Time to Exit Ship Mode	$t_{SHIPMODE}$		0.9	1.1	1.3	s
RST Low Time to Reset BATTFET	t_{RST}		8	10	12	s
BATTFET Reset time	t_{SYS_RST}		250	330	400	ms
Enter Shipping Mode Delay	t_{SHIP_DLY}		10	12	15	s
WATCHDOG and CLOCK						
Watchdog Timer	t_{WDT}	WATCHDOG=40s		40		s
I²C Clock	F_{SCL}				400	kHz

TYPICAL PERFORMANCE CHARACTERISTICS

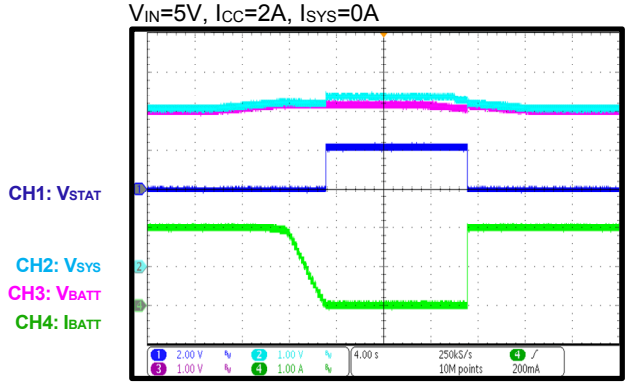
Battery Charge Profile

V_{IN}=5V, I_{CC}=2A, I_{SYS}=0A



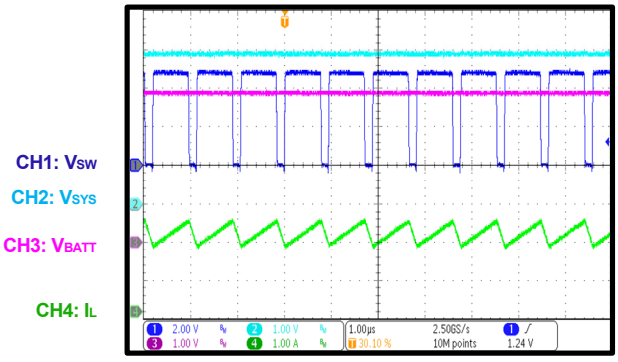
Auto Recharge

V_{IN}=5V, I_{CC}=2A, I_{SYS}=0A



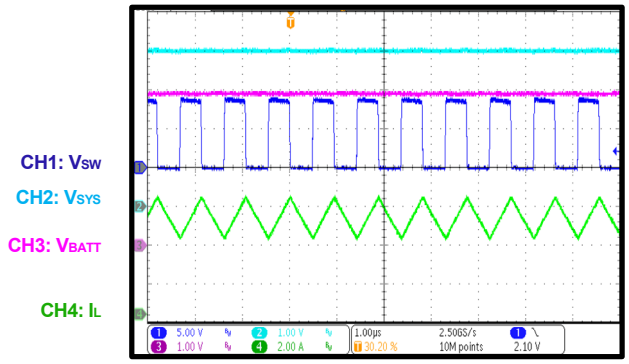
Charge Steady State

V_{IN}=5V, V_{BATT}=3.8V, I_{CC}=2A, I_{SYS}=0A



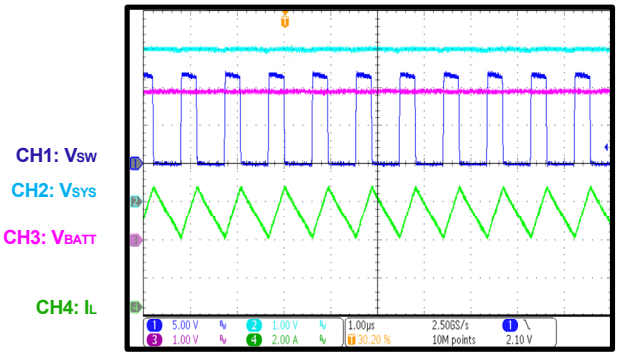
Charge Steady State

V_{IN}=9V, V_{BATT}=3.8V, I_{CC}=5A, I_{SYS}=0A



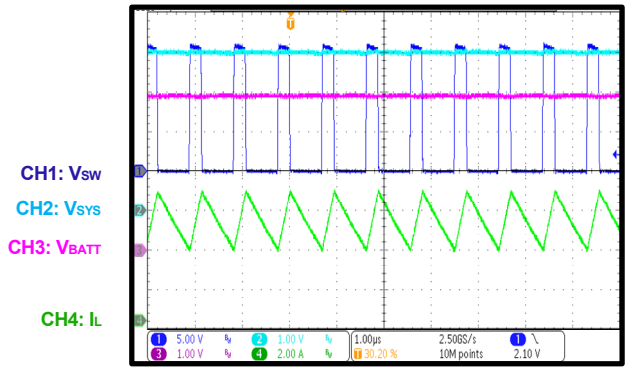
Charge Steady State

V_{IN}=12V, V_{BATT}=3.8V, I_{CC}=5A, I_{SYS}=0A



Charge Steady State

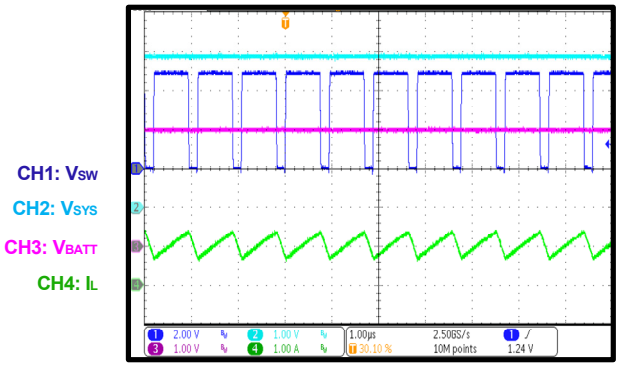
V_{IN}=16V, V_{BATT}=3.8V, I_{CC}=5A, I_{SYS}=0A



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

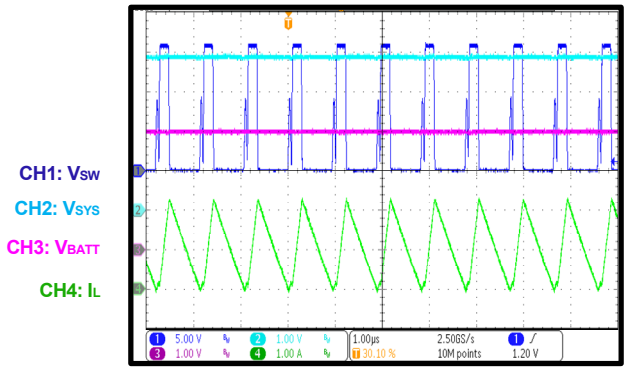
Charge Disable Steady State

V_{IN}=5V, V_{BATT}=3V, Charge disable, I_{SYS}=1A



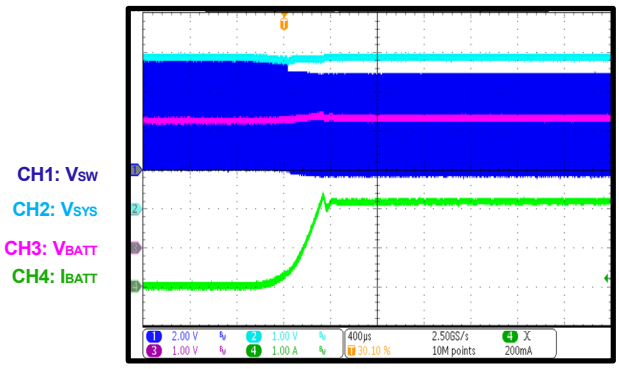
Charge Disable Steady State

V_{IN}=16V, V_{BATT}=3V, Charge disable, I_{SYS}=1A



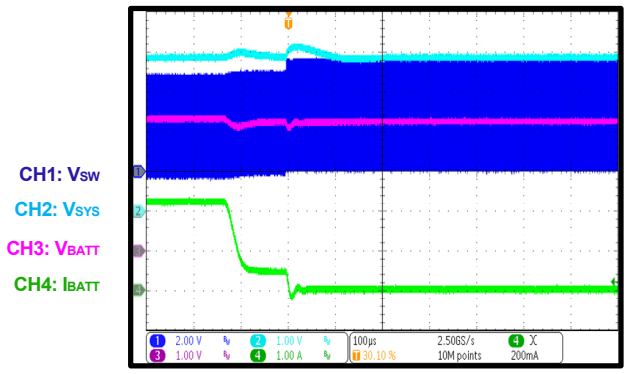
Charge Enable

V_{IN}=5V, V_{BATT}=3.3V, I_{CC}=2A, I_{SYS}=0A



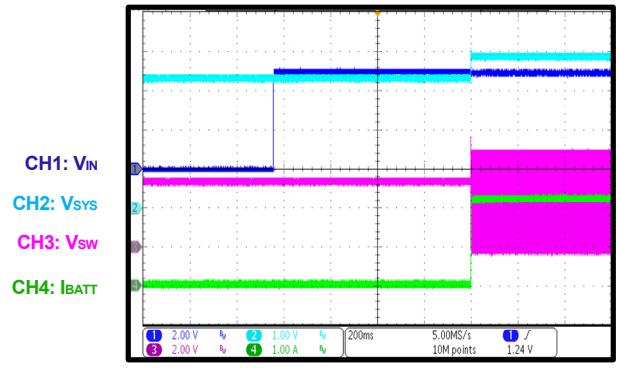
Charge Disable

V_{IN}=5V, V_{BATT}=3.3V, I_{CC}=2A, I_{SYS}=0A



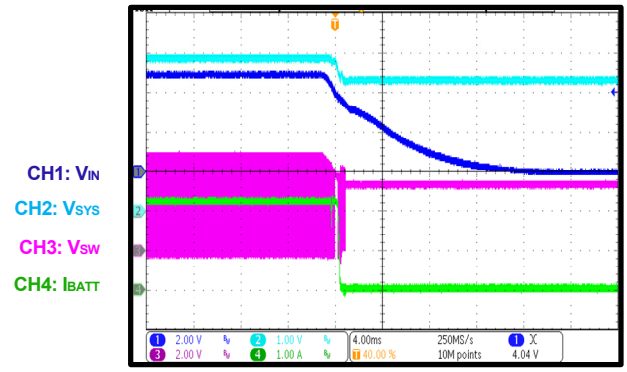
Power ON

V_{IN}=5V, V_{BATT}=3.3V, I_{CC}=2A, I_{SYS}=0A



Power OFF

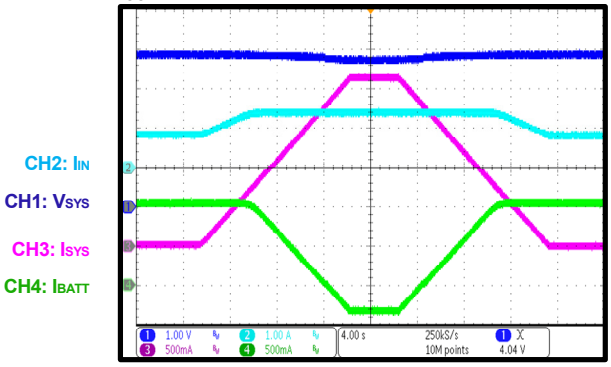
V_{IN}=5V, V_{BATT}=3.3V, I_{CC}=2A, I_{SYS}=0A



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

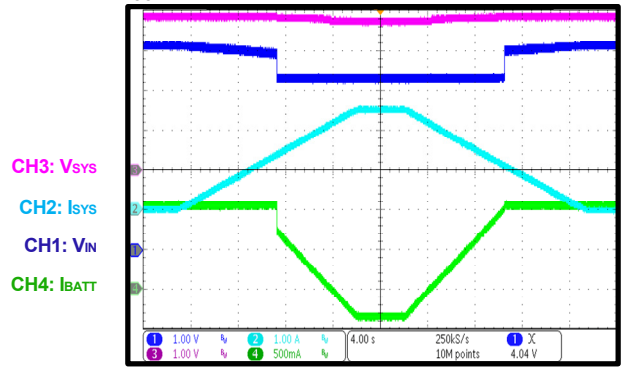
Input Current Limit

V_{IN}=5V, I_{IN_LIM}=1500mA, V_{BATT}=3.8V, I_{CC}=1040mA



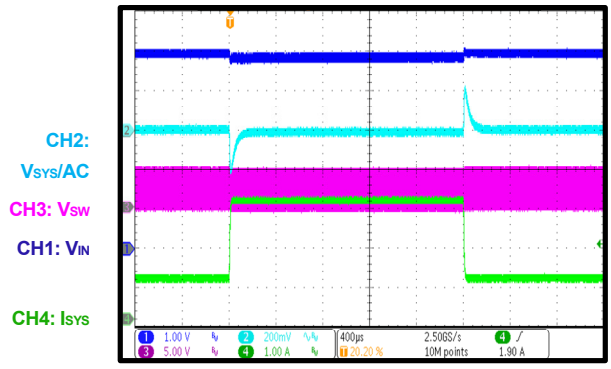
Input Voltage Limit

V_{IN}=5V(2A), I_{IN_LIM}=3000mA, V_{BATT}=3.8V, I_{CC}=1040mA



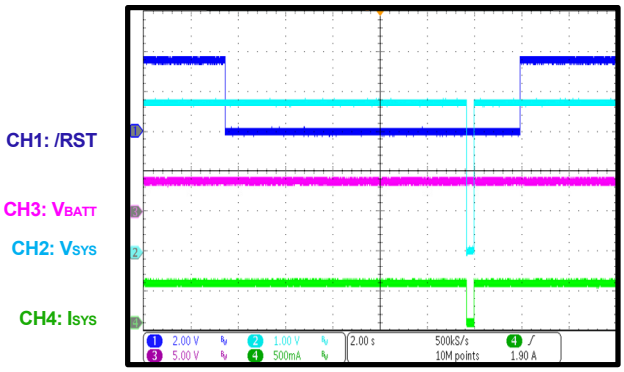
SYS Load Transient

V_{IN}=5V, V_{BATT}=3.3V, Charge disable, I_{SYS}=1-3A



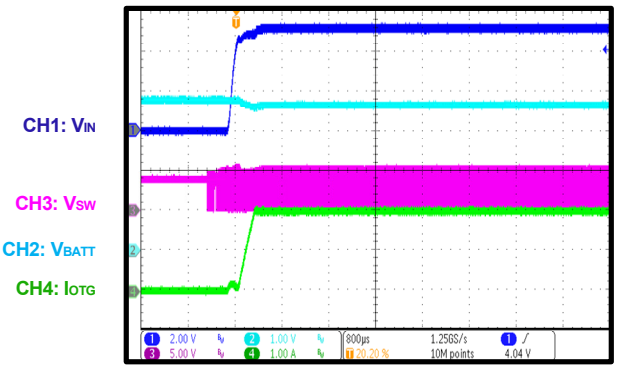
BATTFET Reset

V_{BATT}=3.8V, I_{SYS}=0.5A



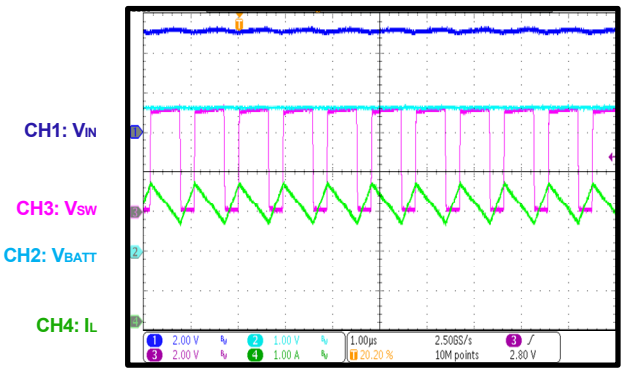
OTG Mode On

V_{BATT}=3.8V, V_{BOOST}=5.15V, I_{OTG}=2A



OTG Steady State Operation

V_{BATT}=3.8V, V_{BOOST}=5.15V, I_{OTG}=2A



FUNCTIONAL BLOCK DIAGRAM

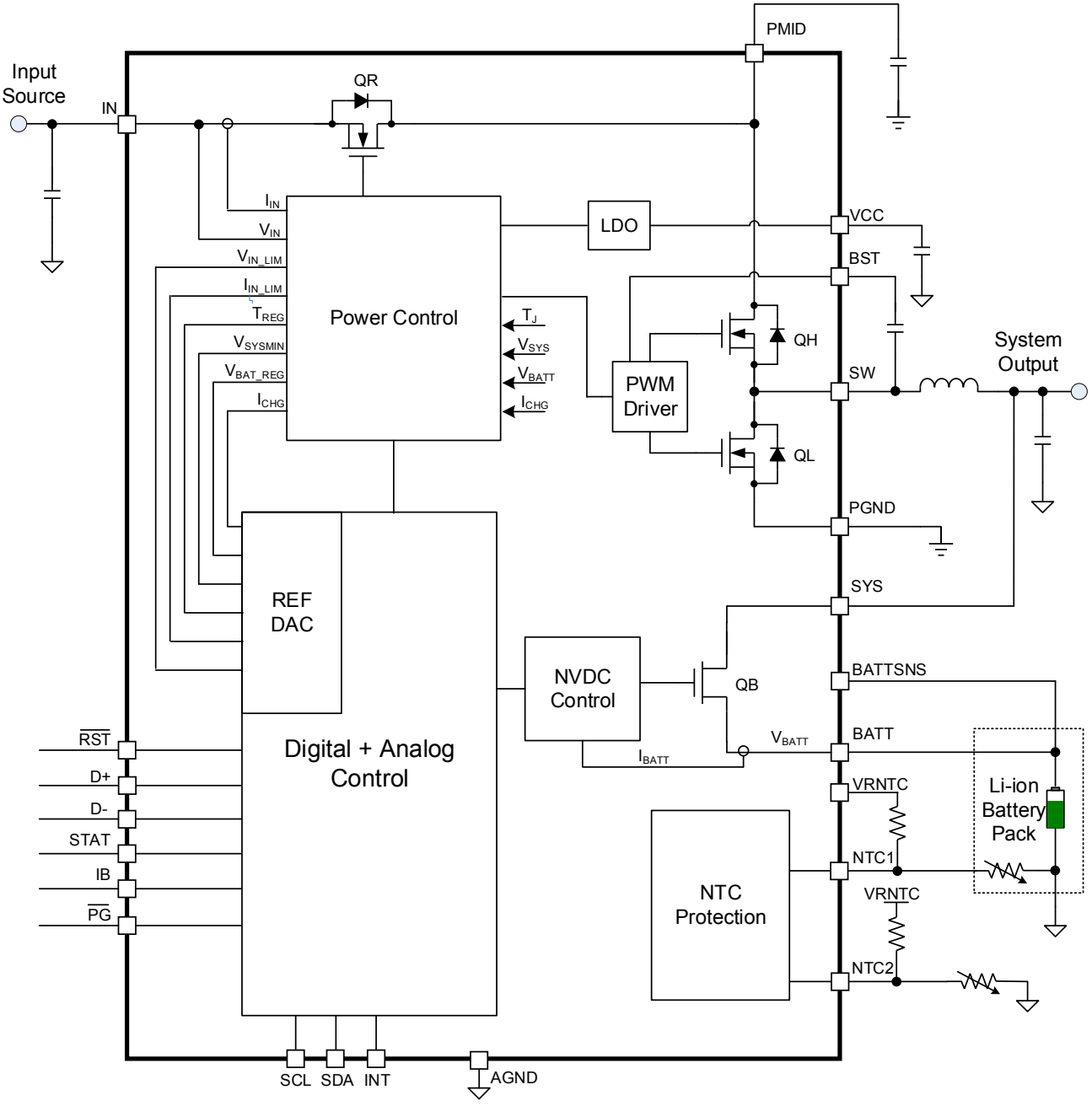


Figure 1: Functional Block Diagram

OPERATION

The MP2721 is a highly integrated I²C controlled switching-mode battery charger IC with NVDC power path management for the single-cell lithium-ion or lithium-polymer battery applications. The MP2721 integrates the reverse blocking FET (RBFET, QR), high-side switching FET (HSFET, QH), low-side switching FET (LSFET, QL), and battery FET (BATTFET, QB).

VCC REGULATOR

The VCC regulator is powered from the higher voltage of BATT and PMID pins. It requires an external 4.7μF bypass capacitor on VCC pin. The VCC pin provides power for the internal circuits and the gate drivers. When VCC pin voltage rises above the V_{VCC_UV} threshold, I²C interface is ready for communication and all the registers are reset to the default value. The VCC pin is suitable for external logic pull-ups but is not recommended for excess load.

BATTERY POWER ON

When input source is not available and battery is connected with V_{BATT}>V_{BATT_UV}, the BATTFET turns on and powers up the system. The low quiescent current and low voltage drop on BATTFET minimize the battery consumption and maximize the battery run time. The discharge current in the BATTFET is kept monitored. If the system is overloaded or shorted to ground (I_{BATT}>I_{BATT_OCP}), the device turns off BATTFET immediately and set BATTFET_DIS bit to 1. The BATTFET can be re-enabled with the methods described in Exit Shipping Mode.

INPUT POWER ON

When an input source is plugged in, the IC detects the input source type and sets the input current limit before the buck converter starts. The power up sequence from input source is as below:

1. V_{IN} detected
2. Hold-off timer (250ms)
3. Input source type detection
4. Set input current limit
5. Buck converter starts if EN_BUCK=1
6. Charging starts if EN_CHG=1

HOLD-OFF TIMER

When a valid input source is detected, the IC runs a hold-off timer (t_{HOLD}=250ms) before detecting the input source type. The hold-off timer can be bypassed by setting HOLDOFF_TMR bit to 0.

INPUT SOURCE TYPE DETECTION

The IC runs D+/D- detection when below conditions are met:

- VIN above VIN_UV
- VIN below VIN_OV
- VIN_GD=1
- Hold-off timer ends
- AUTODPDM=1 or FORCEDPDM is set

The D+/D- detection includes the USB Battery Charging Specification 1.2 (BC1.2), non-standard adaptors and adjustable high voltage adaptor handshake. The BC1.2 detection starts first with the Data Contact Detection (DCD). If the DCD detection is success, the Standard Downstream Port (SDP), Dedicated Charging Port (DCP) and Charging Downstream Port (CDP) can be distinguished by the following Primary Detection and Secondary Detection. If the DCD timer expires, the Non-standard adaptor detection is then applied.

Table 1: Non-standard Adaptor Detection

Adaptor Type	D+ Voltage	D- Voltage
Divider 1	V_{D+} within V_{2P0_TH}	V_{D-} within V_{2P7_TH}
Divider 2	V_{D+} within V_{2P7_TH}	V_{D-} within V_{2P0_TH}
Divider 3	V_{D+} within V_{2P7_TH}	V_{D-} within V_{2P7_TH}
Divider 4	V_{D+} within V_{1P2_TH}	V_{D-} within V_{1P2_TH}
Divider 5	V_{D+} within V_{2P7_TH}	V_{D-} > V_{2P7_TH}

When a DCP is detected, the device is ready to detect a high voltage adaptor. When high voltage adaptor is detected, DPDM_STAT is set to 1001 and an INT pulse is generated, the device is ready to configure the D+/D- pins according to host's setup in register 0Bh.

If AUTODPDM is set to 0, the D+/D- detection is bypassed and the DPDM_STAT bits keeps at 0000.

Table 2: Input Current Limit setting by D+/D- Detection

D+/D- Detection	Input Current Limit
Not started	500mA
USB SDP	500mA
USB DCP	2A
USB CDP	1.5A
Divider 1	1A
Divider 2	2.1A
Divider 3	2.4A
Divider 4	2A
Divider 5	3A
Unknown	500mA
High Voltage Adaptor	2A

INPUT CURRENT LIMIT SETTING

After input source type detection is finished, the following actions are proceeded:

- DPDM_STAT bits are updated
- Input current limit is updated
- VIN_RDY bit is set to 1

An INT pulse is asserted when VIN_RDY bit is set, and the input current limit is updated. The host can overwrite the IIN_LIM registers to modify the input current limit.
If FORCEDPDM bit is written to 1, the D+/D- detection restarts, after D+/D- detection finished, the DPDM_STAT bits and input current limit updates with an INT pulse followed.

INPUT VOLTAGE LIMIT SETTING

The IC supports programmable input voltage limit. When the IN pin voltage decreases to the programmed limit V_{IN_LIM} due to the input source capability or cable voltage drop, the duty-cycle is limited to prevent the input voltage from dropping further. This will reduce the total output current of the converter.

When EN_VIN_TRK bit is set to 0, the input voltage limit is the VIN_LIM register set absolute value. When EN_VIN_TRK bit is set to 1, the input voltage limit is the max value of VIN_LIM register setting and V_{BATT}+200mV.

BUCK CONVERTER AND CHARGER POWER UP

After the VIN_RDY bit is set to 1, the Buck converter soft starts if EN_BUCK=1. The Buck converter switching frequency can be selected from 750kHz to 1.5MHz. Peak current mode control is adopted for regulating the system voltage, battery charge current, battery regulation voltage, input current limit, input voltage limit and the device die temperature loops.

The device automatically starts charging if EN_CHG bit is set to 1.

NVDC BATTERY FET

With this Narrow VDC architecture (NVDC) structure, the BATTFET separates the system from battery and controls the battery charging and discharging. The device prioritizes the system (SYS) output by the power path function utilizing input source, battery, or both.

When the input source is absent, the BATTFET is turned fully on to pass the battery power to system with the ultra-low impedance path. When the input source is present and the buck converter has started up, the system output is related to the battery voltage:

1) When the battery is below minimum system voltage setting (V_{SYS_MIN}), the system voltage is regulated at V_{SYS_MIN}+V_{TRACK}, where V_{TRACK} is typically 150mV. And the battery FET works in linear mode to charge the battery with trickle-charge, pre-charge, or fast charge current through battery FET depending on the battery voltage.
2) As the battery voltage rises above V_{SYS_MIN}, BATTFET is turned fully on and the voltage difference between system and battery is the BATTFET resistive voltage drop.
3) When the charging is disabled or terminated, the system voltage is always regulated at Max(V_{SYS_MIN}, V_{BATT}) + V_{TRACK}. In this case the V_{TRACK} is typically 100mV.

The status register VSYS_STAT indicates whether the system is in V_{SYS_MIN} regulation.

Figure 2 illustrates system voltage regulation with changing battery voltage.

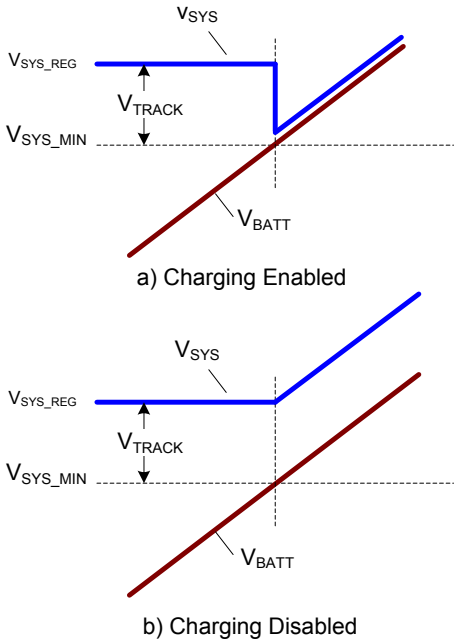


Figure 2: V_{SYS} Regulation with V_{BATT}

DYNAMIC POWER MANAGEMENT

During the buck converter operation, the device continuously monitors the input current and input voltage. When input current limit or input voltage limit is reached, the charge current is reduced to prevent the input source from being overloaded.

If the charge current is reduced to zero, the system voltage starts to drop due to input power limitation. Once the system voltage falls below the battery voltage, the IC automatically enters supplement mode.

When the converter operates in input current loop or input voltage limit loop, the IINDPM_STAT or VINDPM_STAT is set to 1 with an INT pulse followed (maskable).

SUPPLEMENT MODE

When the system voltage falls below the battery voltage, the BATTFET turns on to prevent the system voltage from dropping further. In this condition, the buck converter and the battery provide power for system together.

BATTERY CHARGING

The IC can autonomously run a charging cycle without host involvement. The host also can control the charge operations and parameters via the registers.

A new charge cycle starts with below conditions valid:

- Buck converter has started up
- NTC pins voltage in proper range
- BATTFET is on (BATTFET_DIS=0)
- Charging is enabled (EN_CHG=1)

CHARGE PROFILE

The IC detects the battery voltage to provide four main charging phases: trickle-charge, pre-charge, constant-current charge and constant-voltage charge.

Table 3: charge current setting

Battery Voltage	Charge Current	Default Value	CHG_STAT
<V_{BATT_TC}	$I_{TRICKLE}$	128mA	001
V_{BATT_TC} -- V_{BATT_PRE}	I_{PRE}	240mA	010
V_{BATT_PRE} -- V_{BATT_REG}	I_{CC}	2A	011
= V_{BATT_REG}	<I_{CC}		100

During the whole charging process, the actual charge current may be less than the register setting due to other regulation loops such as the input current loop, input voltage loop, or thermal regulation. In this case, charge termination is blocked and charge timer is counted as the half speed if EN_TMR2X=1.

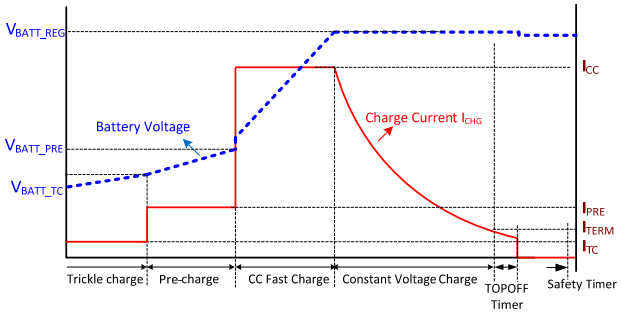


Figure 3: Battery Charging Profile

CHARGE TERMINATION

The charging is terminated if the below conditions are met:

- Termination enabled (EN_TERM=1)
- Charge current below termination threshold for t_{TERM_DGL}=250ms
- Charging in constant-voltage phase
- Not in input current or input voltage loop
- Not in thermal regulation

After termination, the status register CHG_STAT is set to 101, the STAT pin

indicator goes high, and an INT pulse is generated.

After the charging is terminated, input source re-plugging or toggling EN_CHG bit restarts a new charge cycle.

In order to further fully charge the battery, a top-off timer can be applied after termination is detected. The TOPOFF_TIMER bits set the top-off timer. The TOPOFF_ACTIVE bit is 1 when the top-off timer is active. An INT pulse is generated when entering and exiting the top-off timer (maskable). During the top-off timer operation, the charging will continue, while the CHG_STAT bits and the STAT pin both indicate the charging is done.

Top-off timer gets reset with any of the below conditions:

- Charging changes from disable to enable
- Recharge is launched.
- REG_RST bit is set

AUTOMATIC RECHARGE

When the battery is fully charged and the charging is terminated, the battery may be discharged because of the system supplement mode or self-discharge. When the battery voltage is discharged to the recharge threshold, the IC automatically starts another new charging cycle without the requirement of manually re-starting a charging cycle if the input power is valid. There are a deglitch timer t_{RECH_DGL}=100ms for detecting the battery voltage below the recharge threshold. When auto-recharge begins, an INT pulse is asserted.

JEITA THERMISTOR QUALIFICATION

The device supports JEITA profile for managing the charging parameters by continuously monitoring the NTC1/NTC2 pins voltages. Two independent negative temperature coefficient thermistor (NTC) temperature sensing with flexible configuration are provided. The NTC1 and NTC2 actions can be enabled/disabled by setting the NTC1_ACTION and NTC2_ACTION bit, respectively.

The EN_PG_NTC2 bit should be set to 1 to enable NTC2 channel. When EN_PG_NTC2 bit is set to 0, there will be one NTC monitor only.

If the corresponding NTC channel is enabled, to initiate a charge cycle, the voltage on NTC pin must be within the V_{HOT} to V_{COLD} range. If NTC pin voltage exceeds the V_{HOT} to V_{COLD} range, the IC suspends charging and waits NTC voltage to get back in the range.

At cool temperature range V_{COLD}-V_{COOL}, the charge current and/or charge voltage are reduced according to COOL_ACT, JEITA_ISET and JEITA_VSET settings.

At warm temperature range V_{WARM}-V_{HOT}, the charge voltage and/or charge current are reduced according to WARM_ACT, JEITA_ISET and JEITA_VSET settings.

The V_{COLD}, V_{COOL}, V_{WARM} and V_{HOT} thresholds all have 4 programmable percentage levels.

The temperature conditions can be read in NTC1_FAULT and/or NTC2_FAULT bits. An INT pulse is generated when NTC1 or NTC2 condition has any changes.

The NTC1 pin and NTC2 pin share same programmable thresholds. If the detection result is different from the two NTC input, refer to table 4 below for the detection priority.

Table 4: JEITA detection priority

NTC1 / NTC2	Hot	Warm	Normal	Cool	Cold
Hot	Hot	Hot	Hot	Hot	Hot
Warm	Hot	Warm	Warm	Warm	Cold
Normal	Hot	Warm	Normal	Cool	Cold
Cool	Hot	Warm	Cool	Cool	Cold
Cold	Hot	Cold	Cold	Cold	Cold

For battery temperaure protection during boost mode, if the NTC1_ACTION or NTC2_ACTION bit is set to 1, the device compares the NTC1 and/or NTC2 pin voltage with the V_{COLD} and V_{HOT} thresholds. If the NTC pin voltage is outside of V_{COLD} to V_{HOT} range, the boost is suspended. The NTC1_FAULT or NTC2_FAULT is also set to report the condition.

The preset Hot/Cold/Warm/Cool voltage threshold is defined for a β=3435 thermistor. A pull up resistor with value as same as the thermistor's 25°C resistance is recommended.

Figure 4 illustrates the JEITA voltage/current regulations with set up as: NTC1_ACTION = 1, NTC2_ACTION = 0, WARM_ACT = 01, COOL_ACT = 10, JEITA_VSET = 00, JEITA_ISET = 00.

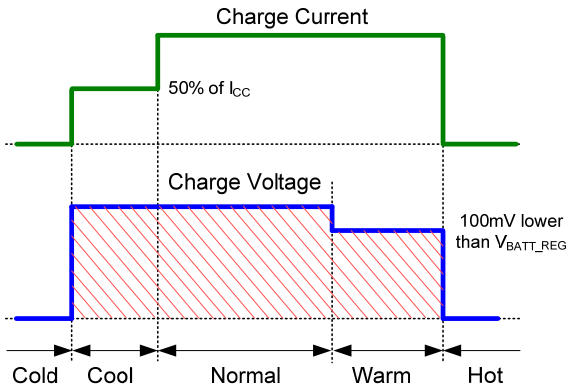


Figure 4: NTC Window under JEITA Control

CHARGING SAFETY TIMER

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. When battery voltage is lower than V_{BATT_PRE} threshold, the safety timer is fixed as 2 hours. When battery voltage is higher than V_{BATT_PRE} threshold, the safety timer is programmed by CHG_TIMER bits. When CHG_TIMER bits are set to 00, both the pre-charge timer and the fast-charge timer are disabled.

Charging is disabled after safety timer expiration, the fault register CHG_FAULT bit is set to 10 and an INT pulse is generated.

During input current, input voltage, thermal regulation or JEITA cool/warm condition (when charge current reduction is enabled), the charge timer counts at half of its rate. This half clock rate function can be disabled by setting EN_TMR2X bit to 0.

Charging safety timer gets reset with any of the below conditions:

- Input source unplugs
- EN_BUCK or EN_CHG toggles
- REG_RST bit is set

REMOTE BATTERY VOLTAGE SENSE

In order to minimize the parasitic trace resistance during charging, BATTSNS pin can be connected to the actual battery pack positive terminal. The remote sensing of battery voltage accelerates the charging speed by helping the charger stay longer in constant current charge mode.

SHIPPING MODE

Enter shipping mode:

When the host sets BATTFET_DIS bit to 1, the IC turn off BATTFET immediately or after a delay time t_{SHIP_DLY}, configured by the BATTFET_DLY bit. I²C communication is still alive in shipping mode.

Exiting shipping mode:
When the IC is in shipping mode (BATTFET_DIS=1), one of the below events can wake up the BATTFET:

- Input source is applied
- Host clears BATTFET_DIS bit
- REG_RST is set to restore default setups
- $\overline{RST}$ pin is pulled low for $t_{SHIPMODE}$

BATTFET RESET

When the input source is absent, the system is powered by the battery through the BATTFET. The system can be forced to have a hardware power-on-reset by changing the BATTFET status from on to off to on. The $\overline{RST}$ pin could be connected to the device's push-button for this function. The $\overline{RST}$ pin has internal pull up.

When the $\overline{RST}$ pin is driven low for t_{RST} while the input source is not plugged-in and BATTFET_DIS=0, the BATTFET is turned off for t_{SYS_RST} and then is enabled again.

This function can be disabled by setting BATTFET_RST_EN bit to 0.

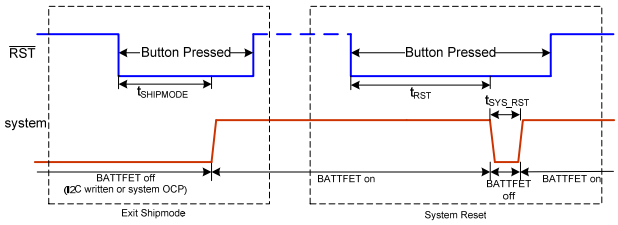


Figure 5: RST Timing

PG INDICATIONA

When EN_PG_NTC2 is set to 0, the PG/NTC2 pin acts as the power good indicator. This pin goes low to indicate a good input source when:

- IN voltage above V_{IN_UV}
- IN voltage below V_{IN_OV}
- 15ms debounce timer has passed

STAT AND IB INDICATION

When EN_STAT_IB bit is set to 0, the charging status is indicated on the open drain STAT/IB pin.

Table 5: STAT Indication

Charging State	STAT
In charging	LOW
Charging completes, top-off timer, boost mode, charging disabled	HIGH
Charging suspend: Battery OVP, Input OVP, Timer fault, NTC fault Boost suspend: NTC fault, OTP, BATT_LOW	Blinking at 1Hz

When EN_STAT_IB is set to 1, the STAT/IB pin act as an analog current source output to indicate the battery current flowing in or out of the battery. The current flowing direction can be read in BFET_STAT bit. A resistor load should be connected between STAT/IB pin and AGND to sense the IB current. When IB_EN is set to 1, the IB output is always on, when IB_EN is set to 0, the IB output is only on when the device is switching.

The IB output voltage range is 0V to V_{VCC}, host can measure the IB voltage which can be useful for either making a fuel gauge or for monitoring the peak discharge current.

INTERRUPTS

A 256us Interrupt pulse is generated on the open drain INT pin with any of the interrupt events. Please refer to the interrupt table.

BARK AND BITE WATCHDOG

After first power up by battery or VIN, the IC operates with default setup. The watchdog timer is default expired with WATCHDOG_FAULT=1. Writing 1 to WATCHDOG_RST starts the watchdog timer.

The watchdog timer has a bark function which generates an INT pulse at the 3/4 time of the watchdog timer setting. The host can distinguish this condition by reading WATCHDOG_BARK bit.

Once the watchdog timer started, The WATCHDOG_RST bit should be written to 1 before Watchdog timer expires to keep the customized settings. The registers will be reset according to the register table when watchdog timer expires. After the watchdog timer expires, an INT pulse is sent with WATCHDOG_FAULT bit set to 1.

The watchdog timer can be disabled by setting the WATCHDOG bit to 00, in this case the registers keep their values until power-on-reset.

BOOST MODE

Boosting from the battery, the device is able to supply a regulated output at the IN pin. Boost will start with below conditions are valid:

- IN voltage less than V_{IN_UV}
- EN_BOOST bit is set to 1 Voltage of the NTC pin in acceptable range
- Battery voltage above V_{BATT_UV}
- If BOOST_STP = 1, BATT voltage needs to be above V_{BATT_LOW}

The boost PWM switching frequency is as same as the buck converter setting.

The boost voltage loop regulates the PMID pin voltage at the setting of VBOOST bits.

The boost output current loop limits the output current at the value set by OLIM bits for V_{IN} >V_{BATT}+ V_{HDRM} range.

Boost start up sequence:

- Converter soft starts with regulation on PMID voltage.
- Blocking FET (QR) soft starts regulating the discharge current from PMID to IN.
- Once IN pin is started up successfully, boost is controlled to regulate PMID voltage and output current sensed through QR.

The soft start-up of the boost converter allows the device to power into large capacitive loads on IN pin.

FORCE INPUT CURRNET LIMIT

In Sink mode, when an input source is plugged in, the IC runs the startup sequence and input source type detection, after the detection is finished, the input current limit is auto-generated. The input current limit result is shown in IIN_LIM bits.

If the host doesn't want to use the auto-generated input current limit, there are 2 ways of setting the input current limit to different

values, by configuring IIN_MODE or IIN_LIM bits:

If IIN_MODE bits are set to 000, the IC runs with the auto-generated input current limit as shown in IIN_LIM bits. Host can over-ride the IIN_LIM bits to set the input current limit to any values after VIN_RDY bit is set. This needs host's involving every time after the charger starts.

If IIN_MODE bits are set to other values, the input current limit is forced and fixed. For example, if IIN_MODE bits are set to 101, the device always runs with a fixed 2000mA input current limit, ignoring the input source type detection.

INPUT IMPEDANCE TEST

The IC supports an input impedance testing function, by sourcing a current on IN pin, the device is able to detect the impedance on the connector receptacle (water detection).

Host writing 1 to VIN_SRC_EN bit can turn on the input impedance test by sourcing a current to IN pin. The testing current can be programmed by IVIN_SRC bits. If the IN pin voltage rise to the threshold programmed by VIN_TEST bit, VIN_TEST_HIGH is set to 1 and latches with an INT pulse followed.

Host writing 0 to VIN_SRC_EN bit turns off the test current source and clears VIN_TEST_HIGH bit.

The VIN_SRC_EN bit can only be effective when neither buck nor boost is operating, and the maximum pull up voltage of the current source is 2.5V. If $V_{IN}>V_{IN\_UV}$ is detected during test, the VIN_SRC_EN and VIN_TEST_HIGH bits are reset to 0 and the test ends immediately. If boost is enabled during test, the VIN_SRC_EN and VIN_TEST_HIGH bits are reset to 0 and the test ends immediately.

LOCK FUNCTION

The IC supports a lock function, which can limit the value of some key parameters (prevent I^2C mis-writing). Battery regulation voltage, constant-current charge current, pre-charge current and JEITA voltage/current settings are in the list.

To enable the lock function, host can set above parameters to a desired value, then write LOCK_CHG bit to 1. After those operations, the future writing of these parameters can only decrease their values.

Below events can unlock the parameters:

- Host writes LOCK_CHG bit to 0
- Host writes REG_RST bit to 0
- Device power off

PROTECTIONS

BATTERY UNDER-VOLTAGE PROTECTION

When the input source is absent, if battery is discharged to below V_{BATT_UV}, the BATTFET is turned off, and all the registers reset.

BATTFET OVER-CURRENT PROTECTION

The current in the BATTFET is kept monitored. When the SYS is overloaded or short, and the battery discharge current reach I_{BATT_OCP} threshold, the BATTFET turns off and latches up, the BATTFET_DIS bit is set to 1. To exit the latch-off, one of Exit Shipping Mode methods should be applied.

INPUT OVER VOLTAGE

The device has input over voltage protection with default OVP threshold of 6.3V. Once IN pin senses a voltage higher than V_{IN_OV} threshold, the buck converter stops. The CHG_FAULT bits are set to 01 and an INT pulse is generated.

When the IN pin voltage goes back to the normal range, the device runs the startup sequence again and resumes normal operation. The CHG_FAULT bits are also cleared.

BATTERY OVER VOLTAGE PROTECTION

The battery over voltage threshold is 4% above the battery regulation voltage V_{BATT_REG}. If the battery over voltage is detected, the charging is disabled. The fault register CHG_FAULT bits are set to 11 with an INT pulse asserted.

THERMAL REGULATION AND THERMAL SHUTDOWN

During battery charging, when the internal junction temperature reaches to the thermal regulation limit T_{J_REG} programmed by TREG bits (60°C to 120°C), the charge current is reduced, charge termination is blocked, the charge timer runs at half rate, and the status register THERM_STAT bit is set to 1 with an INT pulse followed (maskable).

For any time, if the internal junction temperature rises to shutdown threshold T_{J_SHDN} (150°C), both the converter and BATTFET are turned off. All the registers are reset. The IC resumes normal operation when the junction temperature is T_{SHDN_HYS} (30°C) below T_{J_SHDN}(150°C).

BOOST OVER VOLTAGE PROTECTION

During boost operation, when the IN voltage rises above regulation target and exceeds V_{BST_OVP}, the device stops switching immediately. The BOOST_FAULT bits are set to 010 with an INT pulse generated. Boost recovers when the IN voltage gets back to normal range.

BOOST OVER LOAD PROTECTION

During boost operation, once the IN voltage drops below the V_{BATT} + V_{HDRM} or V_{IN_UV} threshold due to heavy load or short, the blocking FET turns off and restarts after 500ms. If 8 restarts are not successful, the boost stops and latches up. BOOST_FAULT bits are set to 001 and an INT pulse is generated.

If the IN pin is short to GND before the boost starts, the blocking FET will also restarts for 8 times, and if it is not successful, the boost stops and latches up.

EN_BOOST bit changing to 0 clears the BOOST_FAULT bits.

BOOST BATTERY LOW PROTECTION

To protect the battery from over-drained and the shutdown of system during boost operation, if the BOOST_STP_EN bit is set to 1, the boost automatically turns off and latches up when battery voltage decreases to below the BATT_LOW setting. The BOOST_FAULT bits are set to 100 with an INT pulse generated (maskable). BATTFET is still alive in this condition to provide power to SYS.

The battery low comparator has 10ms de-bounce time. EN_BOOST bit changing to 0 clears the BOOST_FAULT bits.

BOOST OVER TEMPERATURE PROTECTION

To protect the IC from over temperature in boost mode, if the BOOST_OTP_EN bit is set to 1, the boost converter stops and latches up in case of the internal junction temperature rises to the thermal regulation limit T_{J_REG} (programmed by TREG bits). The BOOST_FAULT bits are set to 011 with an INT pulse followed. BATTFET is still alive in this condition to provide power to SYS.

EN_BOOST bit changing to 0 clears the BOOST_FAULT bits.

SERIES INTERFACE

The IC uses an I²C compatible interface for flexible charging parameter setting and instantaneous device status reporting. I²C is a 2-wire serial interface with two bus lines required: a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL lines are open-drain and need to be connected to the positive supply voltage via a pull-up resistor.

The IC operates as a slave device, receiving control inputs from the master device such as a micro-controller. The SCL line is always driven by the master device. The I²C interface supports both standard mode (up to 100 kbit/s), and fast mode (up to 400 kbit/s).

All transactions begin with a START (S) and are terminated by a STOP (P). START and STOP conditions are always generated by the master. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

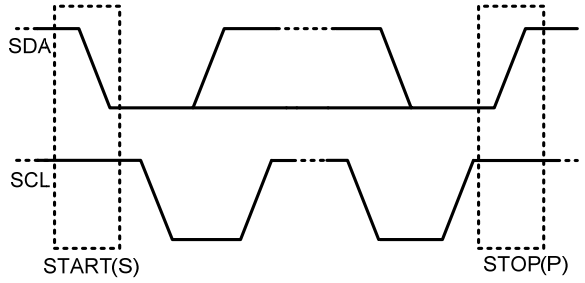


Figure 6: START and STOP Conditions

For data validity, the data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the SDA line can only change when the clock signal on the SCL line is LOW. Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) firstly.

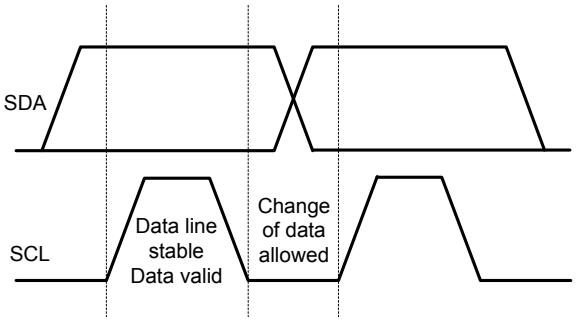


Figure 7: Bit Transfer on the I²C Bus

Each byte has to be followed by an Acknowledge (ACK) bit which is generated by the receiver, to signal the transmitter that the byte was successfully received.

The ACK signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains LOW during the HIGH period of the 9th clock.

If SDA line is HIGH during the 9th clock, this is defined as the Not Acknowledge (NACK) signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

After the START signal, a slave address is sent. This address is 7 bits long, followed by the 8th bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE), and a one indicates a request for data (READ). The address bit arrangement is shown below.

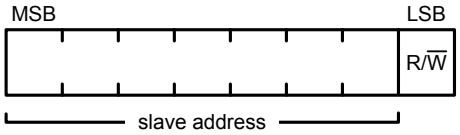


Figure 8: 7-Bit Addressing

Please refer to Figure 9-13 for detailed signal sequences.

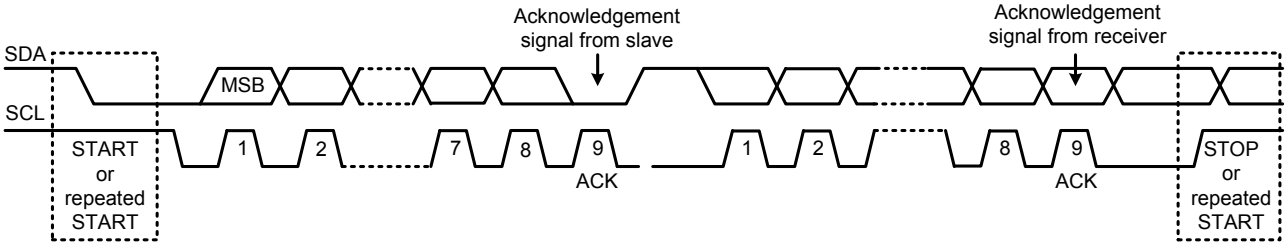


Figure 9: Data Transfer on the I²C Bus

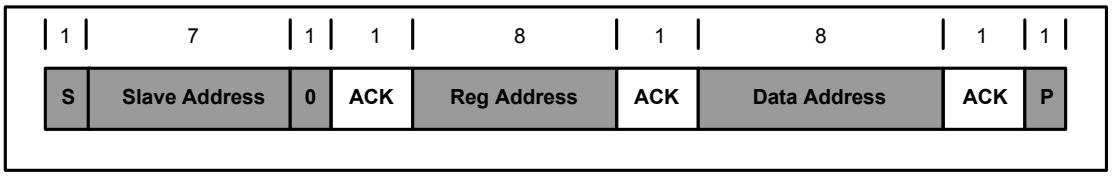


Figure 10: Single Write

Figure 11: Single Read

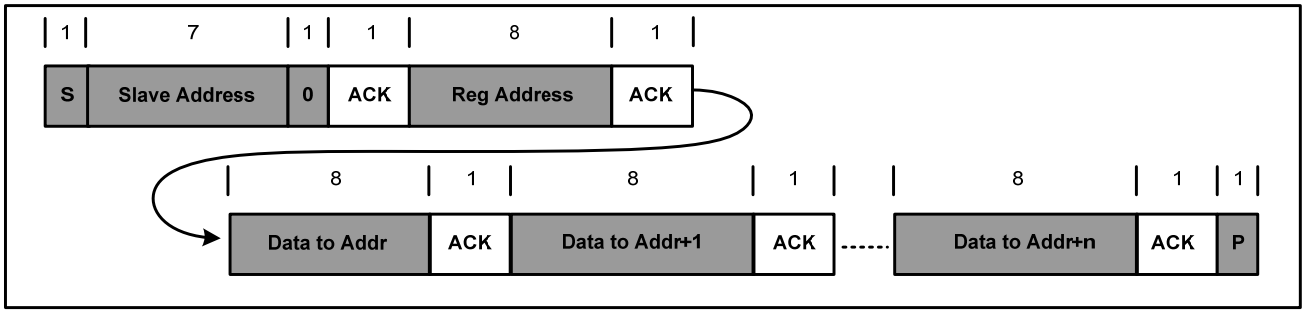


Figure 12: Multi Write

Figure 13: Multi Read

REGISTER MAP

I²C Slave Address: 3Fh
Configuration bytes: 00h-10h; Status bytes: 11h-16h
Legend: POR=Default value; WTD=Watchdog; R/W=Read/Write; R=Read only;
OTP: One time programmable (register default value is programmable)

REG00h:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	REG_RST	0	X	R/W	Register reset 0: Keep current setting 1: Reset registers to default	This bit returns to 0 after 1 written.
6	EN_STAT_IB	0	N	R/W	0: STAT/IB pin is configured as open drain status indicator 1: STAT/IB pin is configured as battery current indicator	OTP
5	EN_PG_NTC2	0	N	R/W	0: PG/NTC2 pin is configured as open drain power good indicator 1: PG/NTC2 pin is configured as second thermistor input	To enable NTC2 channel, this bit must be set to 1. OTP
4	LOCK_CHG	0	N	R/W	0: Not lock 1: VBATT[5:0], ICC[5:0], IPRE[3:0], JEITA_VSET[1:0] and JEITA_ISET[1:0] value is locked	After this bit is set to 1, the future writing of VBATT[5:0], ICC[5:0], IPRE[3:0], JEITA_VSET[1:0] and JEITA_ISET[1:0] can only decrease their values.
3	HOLDOFF_TMR	1	Y	R/W	0: Disable hold-off timer 1: Enable hold-off timer	OTP
2	SW_FREQ[1]	0	N	R/W	00: 750kHz 01: 1.0MHz 10: 1.25MHz 11: 1.5MHz	Programs both the buck and boost operating frequency. Default: 1.0MHz (01) OTP
1	SW_FREQ[0]	1	N	R/W		
0	EN_VIN_TRK	1	N	R/W	0: VIN_LIM is fixed 1: VIN_LIM also tracks V_{BATT}	When set to 0, the VIN_LIM is the register set absolute value. When set to 1, the VIN_LIM is the max value of VIN_LIM[3:0] and V_{BATT}+200mV.

REG01h:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	IIN_MODE[2]	0	N	R/W	000: Follow IIN_LIM setting 001: Force input current limit to 100mA 010: Force input current limit to 500mA 011: Force input current limit to 900mA 100: Force input current limit to 1500mA 101: Force input current limit to 2000mA 110: Force input current limit to 3000mA	When setting these bits to 000, the input current limit follows the auto-generated input current limit value in IIN_LIM[4:0]. When setting these bits to other values, the input current limit is fixed. Default: 000 OTP
6	IIN_MODE[1]	0	N	R/W		
5	IIN_MODE[0]	0	N	R/W		
4	IIN_LIM[4]	0	N	R/W	1600mA	Input current limit setting Range: 100mA to 3.2A Offset:100mA Default: 500mA (00100) Auto updated after input source type detection. Host can overwrite the IIN_LIM value
3	IIN_LIM[3]	0	N	R/W	800mA	
2	IIN_LIM[2]	1	N	R/W	400mA	
1	IIN_LIM[1]	0	N	R/W	200mA	
0	IIN_LIM[0]	0	N	R/W	100mA	

REG02h:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	VPRE[1]	1	N	R/W	00: 2.4V 01: 2.6V 10: 2.8V 11: 3V	Pre-charge to fast charge battery voltage threshold Default: 3V (11)
6	VPRE[0]	1	N	R/W		
5	ICC[5]	0	Y	R/W	2560mA	Fast charge current setting Default: 2A (011001) OTP
4	ICC[4]	1	Y	R/W	1280mA	
3	ICC[3]	1	Y	R/W	640mA	
2	ICC[2]	0	Y	R/W	320mA	
1	ICC[1]	0	Y	R/W	160mA	
0	ICC[0]	1	Y	R/W	80mA	

REG03h:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	IPRE[3]	0	Y	R/W	320mA	Pre-charge current setting Range: 80mA to 680mA Offset: 80mA Default: 240mA (0100) OTP
6	IPRE[2]	1	Y	R/W	160mA	
5	IPRE[1]	0	Y	R/W	80mA	
4	IPRE[0]	0	Y	R/W	40mA	
3	ITERM[3]	0	Y	R/W	240mA	Termination current setting Range: 30mA to 480mA Offset: 30mA Default: 120mA (0011) OTP
2	ITERM[2]	0	Y	R/W	120mA	
1	ITERM[1]	1	Y	R/W	60mA	
0	ITERM[0]	1	Y	R/W	30mA	

REG04h:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	VRECHG	0	Y	R/W	0: 100mV 1: 200mV	Recharge threshold Default: 100mV
6	ITRICKLE[2]	0	Y	R/W	128mA	Trickle charge current setting Range: 32mA to 256mA Offset: 32mA Default: 128mA (011) OTP
5	ITRICKLE[1]	1	Y	R/W	64mA	
4	ITRICKLE[0]	1	Y	R/W	32mA	
3	VIN_LIM[3]	0	N	R/W	640mV	Input voltage limit threshold Range: 3.88V to 5.08V Offset:3.88V Default:4.36V (0110)
2	VIN_LIM[2]	1	N	R/W	320mV	
1	VIN_LIM[1]	1	N	R/W	160mV	
0	VIN_LIM[0]	0	N	R/W	80mV	

REG05h:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	TOPOFF_TMR[1]	0	Y	R/W	00: Disabled 01: 15 minutes 10: 30 minutes 11: 45 minutes	Timer to stop charging after charge termination.
6	TOPOFF_TMR[0]	0	Y	R/W		
5	VBATT[5]	0	N	R/W	800mV	Battery Regulation Voltage Range:3.6V to 4.6V Offset: 3.6V Default: 4.2V (011000) Value above 101000 (4.6V) is clamped to 101000. OTP
4	VBATT[4]	1	N	R/W	400mV	
3	VBATT[3]	1	N	R/W	200mV	
2	VBATT[2]	0	N	R/W	100mV	
1	VBATT[1]	0	N	R/W	50mV	
0	VBATT[0]	0	N	R/W	25mV	

REG06h:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	VIN_OVP[1]	0	N	R/W	00: VIN OVP = 6.3V 01: VIN OVP = 11V 10: VIN OVP = 14V 11: VIN OVP disabled	Input over voltage protection threshold Default: 6.3V (00) OTP
6	VIN_OVP[0]	0	N	R/W		
5	SYS_MIN[2]	1	N	R/W	000: 2.975V 001: 3.15V 010: 3.325V 011: 3.5V 100: 3.588V 101: 3.675V 110: 3.763V	System minimum regulation voltage Default: 3.588V (100) The actual system regulation voltage is this value plus V_{TRACK}=150mV OTP
4	SYS_MIN[1]	0	N	R/W		
3	SYS_MIN[0]	0	N	R/W		
2	TREG[2]	1	Y	R/W	000: 60°C 001: 70°C 010: 80°C 011: 90°C 100: 100°C 101: 110°C 110: 120°C	Thermal regulation threshold for charge Thermal protection threshold for boost Default: 100°C (100)
1	TREG[1]	0	Y	R/W		
0	TREG[0]	0	Y	R/W		

REG07h:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	IB_EN	0	Y	R/W	0: IB outputs when switcher is on 1: IB outputs all the time	Enabling IB when only battery presents costs ~3uA battery current Default: 0
6	WATCHDOG_RST	0	X	R/W	Write 1 to this bit to reset the watchdog timer	After writing 1, the watchdog timer is reset and this bit goes back to 0.
5	WATCHDOG[1]	0	Y	R/W	00: Disable timer 01: 40s 10: 80s 11: 160s	Default:40s (01) OTP
4	WATCHDOG[0]	1	Y	R/W		
3	EN_TERM	1	Y	R/W	0: Disable termination 1: Enable termination	Default: Enable (1)
2	EN_TMR2X	1	Y	R/W	0: Disable 2X timer 1: Enable 2X timer	Default: Enable (1)
1	CHG_TIMER[1]	1	Y	R/W	00: Disable timer 01: 5hrs 10: 10hrs 11: 15hrs	Charge safety timer Default: 10hrs (10)
0	CHG_TIMER[0]	0	Y	R/W		

REG08h:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	BATTFET_DIS	0	N	R/W	0: Allow BATTFET on 1: Turn off BATTFET	Shipping mode or OCP The writing command to this bit controls the BATTFET on/off. The reading result of this bit indicates the BATTFET status.
6	BATTFET_DLY	1	N	R/W	0: Turn off BATTFET immediately 1: Turn off BATTFET after 10s delay	Delay after BATTFET_DIS is set to 1 Default: 1
5	BATTFET_RST_EN	1	Y	R/W	0: Disable BATTFET reset function 1: Enable BATTFET reset function	Default: Enable (1)
4	OLIM[1]	1	Y	R/W	00: 500mA 01: 1.5A 10: 2.1A 11: 3A	Boost output current limit Default: 3A (11)
3	OLIM[0]	1	Y	R/W		
2	VBOOST[2]	1	N	R/W	011: 5.35V 010: 5.30V 001: 5.25V 000: 5.2V 111: 5.15V 110: 5.1V 101: 5.05V 100: 5.0V	Boost output voltage Default: 5.15V (111) OTP
1	VBOOST[1]	1	N	R/W		
0	VBOOST[0]	1	N	R/W		

REG09h:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	Reserved	0	N	R		
6	Reserved	1	Y	R		
5	Reserved	0	Y	R		
4	Reserved	1	Y	R		
3	Reserved	0	Y	R		
2	EN_BOOST	0	Y	R/W	0: Boost disable 1: Boost enable	When AUTOOTG=1, this bit is automatically set/reset and boost is turned on/off accordingly, while writing 0 to this bit can also turn off boost. When AUTOOTG=0, the host can know the boost requirement from OTG_NEED bit, and writing this bit turns on/off the boost.
1	EN_BUCK	1	Y	R/W	0: Buck disable 1: Buck allowed	0 forces Buck converter off
0	EN_CHG	1	Y	R/W	0: Charge disable 1: Charge allowed	0 forces charge off

REG0Ah:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	Reserved	0	N	R		
6	Reserved	0	N	R		
5	AUTODPDM	1	Y	R/W	0: D+/D- detection starts manually 1: D+/D- detection automatically starts after VIN_GD=1 and hold-off timer ends	Default: 1 OTP
4	FORCEDPDM	0	X	R/W	0: Normal 1: Force D+/D- detection	This bit returns to 0 after 1 written This bit is only effective when input source is applied.
3	Reserved	0	Y	R		
2	Reserved	0	Y	R		
1	Reserved	1	Y	R		
0	Reserved	1	Y	R		

REG0Bh:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	Reserved	0	N	R		
6	Reserved	0	N	R		
5	Reserved	0	N	R		
4	HVEN	1	N	R/W	0: Disable HV adaptor detection 1: Enable HV adaptor detection	Default: 1 OTP
3	HVUP	0	X	R/W	0: DP DM unchanged 1: DP=DM=3.3V for 500μs	Only effective when DPDM_STAT=1001 and HVREQ[1:0]=11 This bit returns to 0 after 1 written
2	HVDOWN	0	X	R/W	0: DP DM unchanged 1: DP=DM=0.6V for 500μs	Only effective when DPDM_STAT=1001 and HVREQ[1:0]=11 This bit returns to 0 after 1 written
1	HVREQ[1]	0	Y	R/W	00: DP=0.6V, DM=HighZ 01: DP=3.3V, DM=0.6V 10: DP=0.6V, DM=0.6V 11: DP=0.6V, DM=3.3V	Only effective when DPDM_STAT=1001 Reset to 00 when VIN_GD=0
0	HVREQ[0]	0	Y	R/W		

REG0Ch:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	Reserved	0	N	R		
6	NTC1_ACTION	1	N	R/W	0: only generate INT when NTC1 status changes 1: NTC1 is full function active	Buck is not affected Default: 1 OTP
5	NTC2_ACTION	0	N	R/W	0: only generate INT when NTC2 status changes 1: NTC2 is full function active	Buck is not affected Default: 0 OTP
4	BATT_OVP_EN	1	Y	R/W	0: Battery OVP is neglected 1: Battery OVP is enabled	Default: 1
3	BATT_LOW[1]	0	N	R/W	00: 3.0V falling 01: 3.1V falling 10: 3.2V falling 11: 3.3V falling	When V_{BATT} falls below BATT_LOW, INT pulse is generated with 10ms debounce Default: 3.0V (00)
2	BATT_LOW[0]	0	N	R/W		
0	BOOST_STP_EN	0	Y	R/W	0: BATT_LOW comparator only generates INT 1: BATT_LOW comparator turns off boost and latch	Default: 0 OTP
1	BOOST_OTP_EN	1	Y	R/W	0: Boost OTP is neglected 1: Boost OTP at TREG	Default:1 OTP

REG0Dh:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	WARM_ACT[1]	0	N	R/W	00: No Action when NTC warm 01: Reduce V_{BATT_REG} when NTC warm 10: Reduce I_{CC} when NTC warm 11: Reduce both V_{BATT_REG} and I_{CC} when NTC warm	When both NTC1_ACTION and NTC2_ACTION bits are 1, refer to table 4 for WARM result. Default: 01
6	WARM_ACT[0]	1	N	R/W		
5	COOL_ACT[1]	1	N	R/W	00: No Action when NTC cool 01: Reduce V_{BATT_REG} when NTC cool 10: Reduce I_{CC} when NTC cool 11: Reduce both V_{BATT_REG} and I_{CC} when NTC cool	When both NTC1_ACTION and NTC2_ACTION bits are 1, refer to table 4 for COOL result. Default: 10
4	COOL_ACT[0]	0	N	R/W		
3	JEITA_VSET[1]	0	Y	R/W	00: V_{BATT_REG} minus 100mV 01: V_{BATT_REG} minus 150mV 10: V_{BATT_REG} minus 200mV 11: V_{BATT_REG} minus 250mV	Default: 00
2	JEITA_VSET[0]	0	Y	R/W		
1	JEITA_ISET[1]	0	Y	R/W	00: 50% of ICC 01: 33% of ICC 10: 20% of ICC	Default: 00
0	JEITA_ISET[0]	0	Y	R/W		

REG0Eh:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	VHOT[1]	1	Y	R/W	00: 29.1% (50°C) 01: 25.9% (55°C) 10: 23.0% (60°C) 11: 20.4% (65°C)	Hot falling threshold Setting Default: 23.0% (10)
6	VHOT[0]	0	Y	R/W		
5	VWARM[1]	0	Y	R/W	00: 36.5% (40°C) 01: 32.6% (45°C) 10: 29.1% (50°C) 11: 25.9% (55°C)	Warm falling threshold Setting Default: 32.6% (01)
4	VWARM[0]	1	Y	R/W		
3	VCOOL[1]	1	Y	R/W	00: 74.2% (0°C) 01: 69.6% (5°C) 10: 64.8% (10°C) 11: 59.9% (15°C)	Cool rising threshold Setting Default: 64.8% (10)
2	VCOOL[0]	0	Y	R/W		
1	VCOLD[1]	0	Y	R/W	00: 78.4% (-5°C) 01: 74.2% (0°C) 10: 69.6% (5°C) 11: 64.8% (10°C)	Cold rising threshold Setting Default: 74.2% (01)
0	VCOLD[0]	1	Y	R/W		

REG0Fh:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	Reserved	0	N	R		
6	VIN_SRC_EN	0	Y	R/W	0: normal 1: Source current to IN pin	Enabling the input impedance test.
5	IVIN_SRC[3]	0	Y	R/W	0000: 5uA 0001: 10uA 0010: 20uA 0011: 40uA 0100: 80uA 0101: 160uA 0110: 320uA 0111: 640uA 1000: 1280uA	Programs the input impedance test current source.
4	IVIN_SRC[2]	0	Y	R/W		
3	IVIN_SRC[1]	0	Y	R/W		
2	IVIN_SRC[0]	0	Y	R/W		
1	VIN_TEST[1]	0	Y	R/W	00: 0.3V 01: 0.5V 10: 1V 11: 1.5V	Programs the input impedance test comparator threshold.
0	VIN_TEST[0]	0	Y	R/W		

REG10h:

Bit	Name	POR	WTD Reset	Type	Description	Comment
7	Reserved	0	N	R		
6	Reserved	1	N	R		
5	MASK_THERM	0	N	R/W	0: Allow THERM_STAT INT pulse 1: Mask THERM_STAT INT pulse	OTP
4	MASK_DPM	0	N	R/W	0: Allow VINDPM and IINDPM INT pulse 1: Mask VINDPM and IINDPM INT pulse	
3	MASK_TOPOFF	0	N	R/W	0: Allow TOPOFF timer INT pulse 1: Mask TOPOFF timer INT pulse	
2	Reserved	1	N	R		
1	MASK_BATT_LOW	0	N	R/W	0: Allow BATT_LOW INT pulse 1: Mask BATT_LOW INT pulse	
0	Reserved	0	N	R		

Status bytes: REG11h--REG16h
Legend: POR=Default value; R/W=Read/Write; R=Read only; INT: Interrupt; YM=Interrupt maskable

REG11h:

Bit	Name	POR	R/W	INT	Description
7	DPDM_STAT[3]	X	R	N	Input Source D+/D- detection result 0000: Not started 500mA 0001: USB SDP 500mA 0010: USB DCP 2A 0011: USB CDP 1.5A 0100: Divider 1 1A 0101: Divider 2 2.1A 0110: Divider 3 2.4A 0111: Divider 4 2A 1000: Unknown 500mA 1001: High voltage adaptor 2A 1110: Divider 5 3A
6	DPDM_STAT[2]	X	R	N	
5	DPDM_STAT[1]	X	R	N	
4	DPDM_STAT[0]	X	R	N	
3	Reserved	X	R	N	
2	Reserved	X	R	N	
1	VINDPM_STAT	X	R	YM	0: Not in VINDPM 1: In VINDPM
0	IINDPM_STAT	X	R	YM	0: Not in IINDPM 1: In IINDPM

REG12h:

Bit	Name	POR	R/W	INT	Description
7	Reserved	X	R	N	
6	VIN_GD	X	R	Y	0: Input source is not valid 1: Input source is good In Buck mode, when V_{VIN_UV}<V_{IN}<V_{VIN_OV}, after 15ms debounce, this bit is set to 1, PG pin is driven low.
5	VIN_RDY	X	R	Y	0: VIN is not ready to charge 1: VIN is ready to charge Input source type detection is finished. IIN_LIM[4:0] is updated.
4	Reserved	X	R	N	
3	THERM_STAT	X	R	YM	0: Not in thermal regulation 1: In thermal regulation
2	VSYS_STAT	X	R	N	0: BATT<SYS_MIN 1: BATT>SYS_MIN
1	WATCHDOG_FAULT	X	R	Y	0: Normal 1: Watchdog timer expires
0	WATCHDOG_BARK	X	R	Y	0: Normal 1: 3/4 watchdog timer expires

REG13h:

Bit	Name	POR	R/W	INT	Description
7	CHG_STAT[2]	X	R	N	000: Not charging 001: Trickle charge 010: Pre-charge 011: Fast charge 100: Constant voltage charge 101: Charge done
6	CHG_STAT[1]	X	R	N	
5	CHG_STAT[0]	X	R	N	
4	BOOST_FAULT[2]	X	R	Y	000: Normal 001: IN overloaded or short (latch) 010: Boost OVP (not latch) 011: Boost Over-temperature protection (latch) 100: Boost stops due to BATT_LOW (latch)
3	BOOST_FAULT[1]	X	R	Y	
2	BOOST_FAULT[0]	X	R	Y	
1	CHG_FAULT[1]	X	R	Y	00: Normal 01: Input OVP 10: Charge timer expires 11: Battery OVP
0	CHG_FAULT[0]	X	R	Y	

REG14h:

Bit	Name	POR	R/W	INT	Description
7	NTC_MISSING	X	R	Y	0: Normal 1: NTC is missing (V_{NTC}>95%*V_{VRNTC}), not latch, do nothing but INT
6	BATT_MISSING	X	R	Y	0: Normal 1: Battery is missing (2 terminations detected within 3 seconds, not latch, do nothing but INT)
5	NTC1_FAULT[2]	X	R	Y	000: Normal 001: Warm 010: Cool 011: Cold 100: Hot
4	NTC1_FAULT[1]	X	R	Y	
3	NTC1_FAULT[0]	X	R	Y	
2	NTC2_FAULT[2]	X	R	Y	000: Normal 001: Warm 010: Cool 011: Cold 100: Hot
1	NTC2_FAULT[1]	X	R	Y	
0	NTC2_FAULT[0]	X	R	Y	

REG16h:

Bit	Name	POR	R/W	INT	Description
7	Reserved	X	R	N	
6	TOPOFF_ACTIVE	X	R	YM	0: Top-off timer is not counting 1: Top-off timer is counting
5	BFET_STAT	X	R	N	0: battery is charging or disabled 1: battery is discharging
4	BATT_LOW_STAT	X	R	YM	0: battery voltage is higher than BATT_LOW[1:0] 1: battery voltage is lower than BATT_LOW[1:0] Hysteresis=200mV
3	Reserved	X	R	N	
2	VIN_TEST_HIGH	X	R	Y	0: VIN voltage less than VIN_TEST threshold 1: VIN touched VIN_TEST threshold
1	Reserved	X	R	N	
0	Reserved	X	R	N	

Interrupt list:

INT Name	Related registers	Maskable	Event
VIN_GD	VIN_GD changes	N	Good input source is detected
DPDM_DET_DONE	DPDM_STAT[3:0] changes	N	DPDM detection is finished
VIN_RDY	VIN_RDY 0→1	N	Input current limit is updated, buck converter starts
CHG_DONE	CHG_STAT[2:0] any to 101	N	Charge terminates
RECHARGE	CHG_STAT[2:0] exits 101 and enter CC/CV charge	N	Recharge initiates
THERM_STAT	THERM_STAT 0→1	Y	IC enters charge thermal regulation
WATCHDOG_FAULT	WATCHDOG_FAULT 0→1	N	Watchdog timeout
WATCHDOG_BARK	WATCHDOG_BARK 0→1	N	Watchdog bark
CHG_FAULT	CHG_FAULT[1:0] 00→01, 00→10, 00→11	N	Charge faults: Input OVP, Charge timer expires, Battery OVP
NTC_MISSING	NTC_MISSING changes	N	NTC is missing: not latch, do nothing but INT
BATT_MISSING	BATT_MISSING changes	N	BATT is missing: not latch, do nothing but INT
BOOST_FAULT	BOOST_FAULT[2:0] 000→001 000→010, 010→000 000→011, 000→100	N	Boost faults: IN overloaded or short, Boost OVP, Boost OTP, Boost stops due to BATT_LOW
NTC_FAULT	NTC1_FAULT[2:0] or NTC2_FAULT[2:0] changes	N	NTC status changes
VINDPM_STAT	VINDPM_STAT 0→1	Y	Vin regulation loop enters
IINDPM_STAT	IINDPM_STAT 0→1		Iin regulation loop enters
TOPOFF_TMR	TOPOFF_ACTIVE changes	Y	TOPOFF timer starts and ends
BATT_LOW	BATT_LOW_STAT 0→1	Y	Battery voltage drops to BATT_LOW threshold
VIN_TEST_HIGH	VIN_TEST_HIGH 0→1	N	VIN rises up to VIN_TEST threshold during input impedance test
HVCHARGER	DPDM_STAT[3:0] Any → 1001	N	HV charger detected

OTP MAP

The MP2721 has one-time-programming (OTP) function to configure the default value of part of the registers. OTP Map below shows the configurable parameters.

#	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	N/A	EN_STAT_IB	EN_PG_NTC2	N/A	HOLDOFF_TMR	SW_FREQ[1:0]		N/A
01h	IIN_MODE			N/A	N/A	N/A	N/A	N/A
02h	N/A	N/A	ICC[5:0]					
03h	IPRE[3:0]				ITERM[3:0]			
04h	N/A	ITRICKLE[2:0]			N/A			
05h	N/A	N/A	VBATT[5:0]					
06h	VIN_OVP[1:0]		SYS_MIN[2:0]			N/A	N/A	N/A
07h	N/A	N/A	WATCHDOG[1:0]		N/A	N/A	N/A	N/A
08h	N/A	N/A	N/A	N/A	N/A	VBOOST[2:0]		
0Ah	N/A	N/A	AUTODPDM	N/A	N/A	N/A	N/A	N/A
0Bh	N/A	N/A	N/A	HVEN	N/A	N/A	N/A	N/A
0Ch	N/A	NTC1_ACTION	NTC2_ACTION	N/A	N/A	N/A	BOOST_STP_EN	BOOST_OTP_EN
10h	N/A	N/A	MASK_THERM	N/A	N/A	N/A	N/A	N/A

OTP DEFAULT

OTP Items	Default
EN_STAT_IB	0: STAT
EN_PG_NTC2	0: PG
HOLDOFF_TMR	1: Enable hold-off timer
SW_FREQ[1:0]	01: 1.0MHz
IIN_MODE[2:0]	000: Follow IIN_LIM setting
ICC[5:0]	011001: 2A
IPRE[3:0]	0100: 240mA
ITERM[3:0]	0011: 120mA
ITRICKLE[2:0]	011: 128mA
VBATT[5:0]	011000: 4.2V
VIN_OVP[1:0]	00: 6.3V
SYS_MIN[2:0]	100: 3.588V
WATCHDOG[1:0]	01: 40s
VBOOST[2:0]	111: 5.15V
AUTODPDM	1: D+/D- detection auto start
HVEN	1: Enable HV adaptor detection
NTC1_ACTION	1: Active
NTC2_ACTION	0: INT only
BOOST_STP_EN	0: BATT_LOW comparator only generates INT
BOOST_OTP_EN	1: Boost stops when TREG
MASK_THERM	0: Allow INT

TYPICAL APPLICATION CIRCUITS

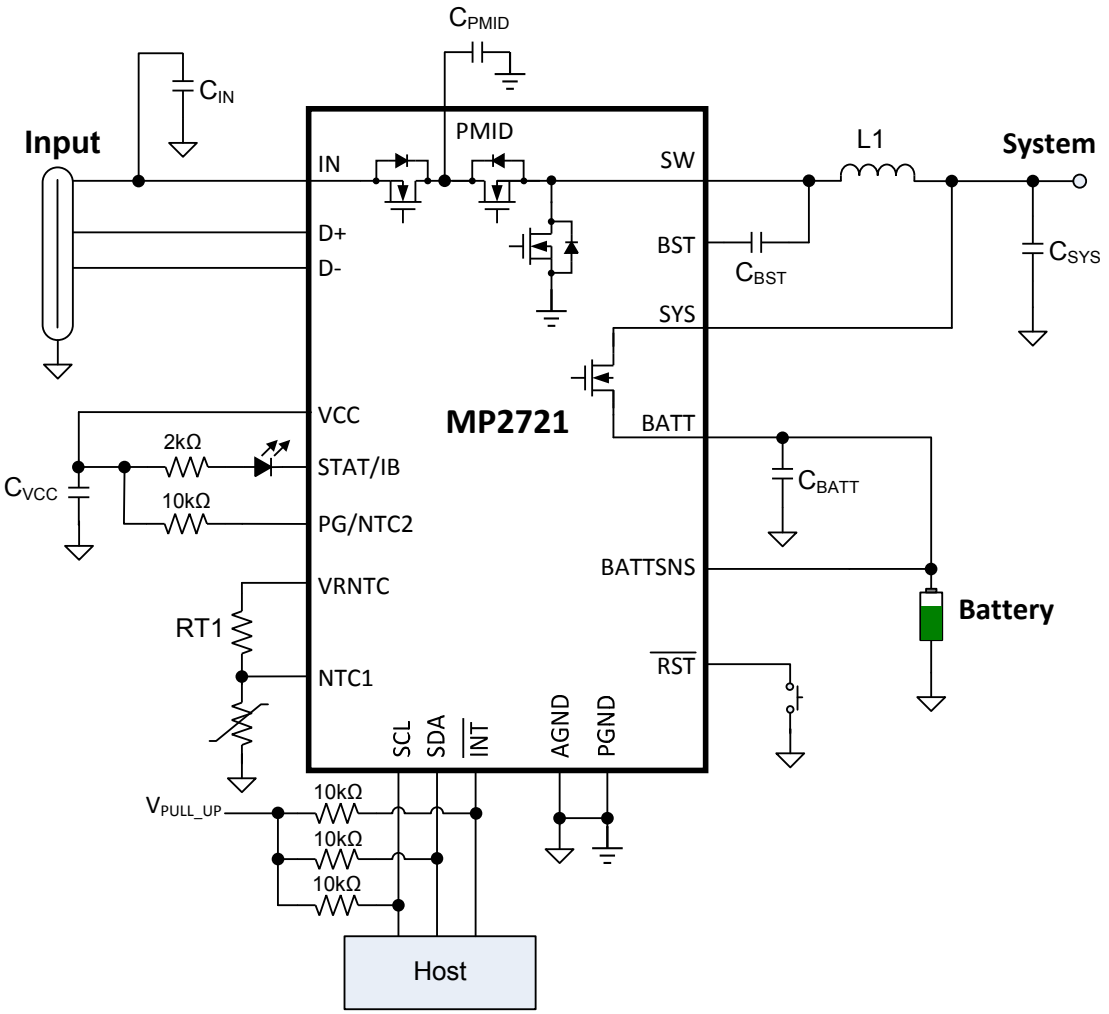


Figure 14: Typical Application Circuit

Table 6: The Key BOM of Figure 14

Qty	Ref	Value	Description	Package	Manufacture
1	C_{IN}	1μF	Ceramic Capacitor; 25V; X5R or X7R	0603	Any
1	C_{PMID}	10μF	Ceramic Capacitor; 25V; X5R or X7R	0805	Any
2	C_{SYS}	10μFx2	Ceramic Capacitor; 16V; X5R or X7R	0805	Any
1	C_{BATT}	10μF	Ceramic Capacitor; 16V; X5R or X7R	0805	Any
1	C_{VCC}	4.7μF	Ceramic Capacitor; 10V; X5R or X7R	0603	Any
1	C_{BST}	100nF	Ceramic Capacitor; 16V; X5R or X7R	0603	Any
1	L1	1μH	Inductor; 1μH; Low DCR	SMD	Any
1	RT1	10kΩ	Film Resistor; 1%, same value as the NTC resistance at 25°C	0603	Any

APPLICATION INFORMATION

Selecting the Inductor

Inductor selection requires a tradeoff between cost, size, and efficiency. A lower inductance value corresponds with a smaller size, but results in higher current ripple, higher magnetic hysteretic losses, and higher output capacitances. However, a higher inductance value benefits from lower ripple current and smaller output filter capacitors, but results in higher inductor DC resistance (DCR) loss.

Estimate the required inductance with Equation (1):

$$L = \frac{V_{IN} - V_{SYS}}{\Delta I_{L\_MAX}} \times \frac{V_{SYS}}{V_{IN} \times f_{SW}} \quad (1)$$

Where V_{IN} is the input voltage, V_{SYS} is the converter output voltage, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the maximum peak-to-peak inductor current, which is usually designed at 20% to 40% of the maximum load current.

Choose an inductor that does not saturate under the worst-case load condition.

$$I_{SAT} > I_{LOAD} + \frac{\Delta I_{L\_MAX}}{2} \quad (2)$$

Where I_{SAT} is the inductor saturation current, I_{LOAD} is the max load of the buck converter.

Selecting the PMID Capacitor C_{PMID}

The PMID capacitance decouples the switching buck converter and absorbs the switching ripple current. Select C_{PMID} based on the demand of the PMID current ripple. The input current ripple is calculated using equation (3):

$$I_{RMS\_MAX} = I_{LOAD} \times \frac{\sqrt{V_{SYS} \times (V_{IN} - V_{SYS})}}{V_{IN}} \quad (3)$$

Low ESR ceramic capacitor with X7R or X5R rating is required as the PMID capacitor, and the PMID capacitor should be placed to the PMID pin and PGND pin as close as possible. Voltage rating of the capacitor must be higher than the input voltage and considering plug-in overshoot voltage. A rating of 25V or higher capacitor is preferred for 15V input voltage. Capacitance of 10µF is generally considered as a starting value.

PCB Layout Guide

PCB layout is important to meet specified noise, efficiency and stability requirements. The following is a PCB layout priority list for proper layout.

1. Place the PMID capacitor as close as possible to the PMID and PGND pins using a short copper plane connection. Place the PMID capacitor on the same layer as the IC.
2. Minimize the high-frequency current path loop between the PMID capacitor and the buck converter power MOSFETs (PMID pin to capacitor, capacitor to PGND pin).
3. Place the inductor input terminal as close as possible to the SW pin.
4. Minimize the copper area of the inductor input terminal trace to reduce electrical and magnetic field radiation, but ensure the trace is wide enough to carry the charging current.
5. Minimize parasitic capacitance from the inductor input terminal to any other trace or plane.
6. Place decoupling capacitors (e.g. the VCC pin capacitor) as close as possible to the IC pins, and make the connection as short as possible.
7. Connect the IC's power pin to as many copper planes as possible to conduct heat away from the IC.
8. Ensure the number and physical size of the vias is sufficient for a current path.

Layout example: the high side FET, low side FET and the PMID capacitor forms the high frequency current path, which must be minimized.

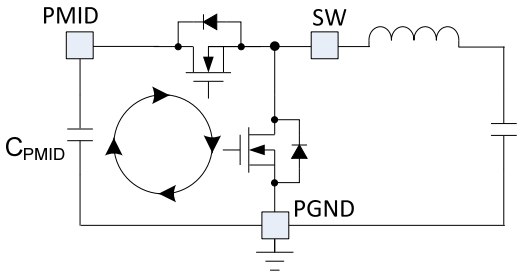
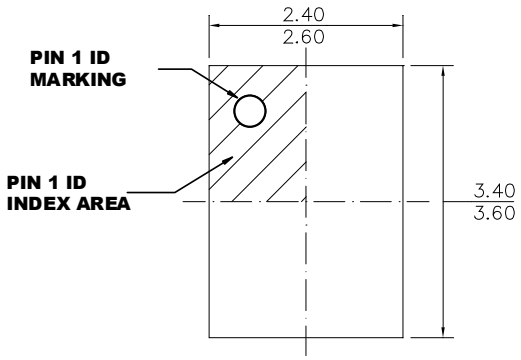


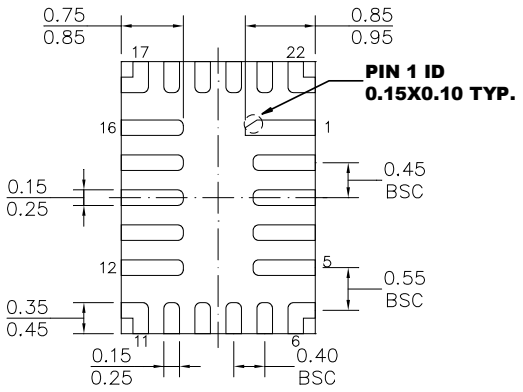
Figure 15: High frequency current path

PACKAGE INFORMATION

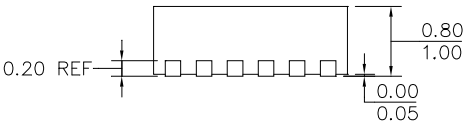
QFN-22 (2.5mm×3.5mm)



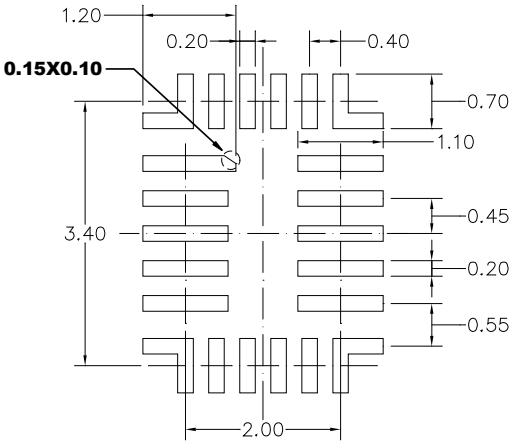
TOP VIEW



BOTTOM VIEW



SIDE VIEW

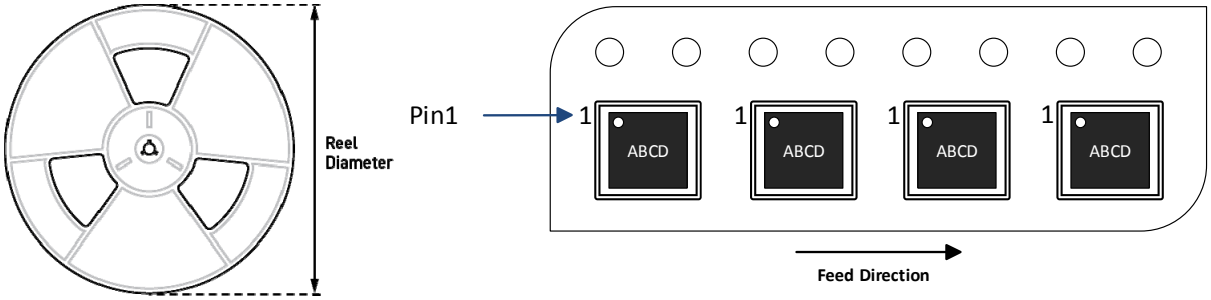


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Quantity/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2721GRH-xxxx–Z	QFN-22 (2.5mmx3.5mm)	5000	N/A	N/A	13 in.	12 mm	8 mm