Alarm Clock Project Development Report

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***Abstract*—An alarm clock system was successfully proposed, designed and developed utilizing previously developed Verilog HDL modules including sound generation, digital clock, and debounding circuit modules. These modules are integrated along with modules including alarm controller, storage elements and seven segment display controller and implemented on a Digilent Nexys A7 Development board.**

***Index Terms*—Verilog HDL, FPGA, Sound Generation, Sequential Circuit**

I. Introduction

This report documents the description, development process and result of the alarm clock project.

II. System Description

The alarm clock system will have the functionality of displaying time to end user. The user will be able to obtain the minutes and seconds passed since the clock was powered on, reset, or overflow. The user will also be able to input a certain value of time to be notified by sound when the clock matches the designated time.

III. System Development

A. Requirement

From the system description the following requirements are proposed.

1) The system shall display time passed, up to 59 minutes and 59 seconds, since last occurrence of any of the following events:
   - Power on of the system
   - Reset of the system
   - One hour passed since either of the two above event

   This value of time will be referred as ”clock time” in this document.
2) The system shall provide alarm functionality, i.e., when enabled, it shall notify user when clock time matches a value of time designated by user. This value of time will be referred as ”alarm time” in this document.
3) The system shall provide a mean for user to input alarm time.
4) The system shall display alarm time.
5) The system shall allow user to enable or disable the alarm functionality.
6) The system shall indicate to user if alarm functionality is enabled or disabled.
7) The system shall play sound when clock time matches alarm time for a maximum of one minutes.
8) The system shall provide a mean for user to stop the system from continuing to play sound.
9) The system shall allow user to reset the system.

B. Design

The system will utilize the Verilog modules developed in the Digital Clock and Sound Generation labs. The use of the digital clock module will satisfy requirement 1.

Satisfying requirement 3 to 8 will satisfy requirement 2.

To satisfy requirement 3, two sets of six switches will be used to allow user to input two 6-bits binary number representing minutes and seconds of alarm time respectively. The user will then be able to press a button to feed it into the registers that will hold the value.

To satisfy requirement 4, the alarm time will be converted to four BCD number, which will then be fed into seven segment decoders that will display it to seven segment display.

To satisfy requirement 5, a T flip flop will be used to store the status of alarm functionality, i.e., if it is enabled or disabled. The user will be able to toggle the flip flop by pressing a button. The signal from the button will be fed to a debouncing module and the debounced signal will be fed to both T input and clock to toggle the flip flop.

To satisfy requirement 6, an LED will be wired to the output of the T flip flop to provide an indicator to the status of alarm functionality.

To satisfy requirement 7, a one minute timer module will be used to control the sound generation module. It will receive alarm time from registers and clock time from digital clock module. If the alarm time matches the clock time, it will start the timer and it will output an enable signal to the enable input of the sound generation while the timer is running.

To satisfy requirement 8, a button will be wired to the reset input of the timer to disable the song generation module.

To satisfy requirement 9, a button will be wired to the reset input of all the modules.

Figure 1 show the block diagram of such a design.

C. Implementation

The Verilog code implementing the alarm clock system is attached at the end of report.

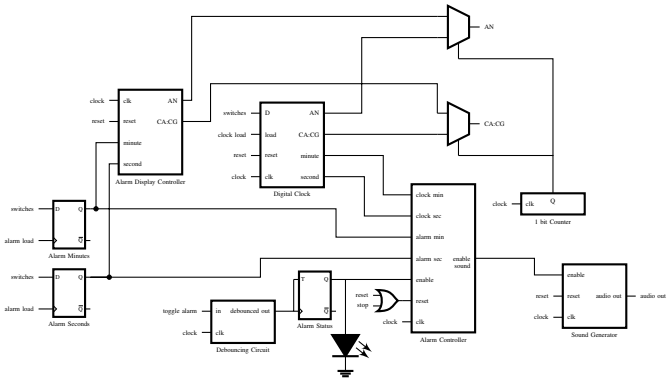

Fig. 1. Block Diagram of Alarm clock

D. Verification

A user manual is proposed below demonstrating the normal usage procedure of the alarm clock system.

1) Turn on the alarm clock by flipping the top left switch to the ON position
2) Enter the desired alarm time by putting the binary representation of the minute value to the left eight switches and the second value to the right eight switches, from left to right in decreasing significance
3) Press the bottom button to load alarm time into the alarm clock
4) Press the top button to enable alarm
5) When the alarm goes off, press the center button to stop the alarm if so desired

To verify the alarm clock system, a Digilent Nexys A7 development board was used to implement the alarm clock system and the user manual was followed to replicate normal usage of the system.

The video demonstrating the verification process of the alarm clock system is submitted separately.

IV. Result

Utilizing the previously developed sound generation, digital clock and debouncing circuit modules, in addition to the integration of new modules including alarm controller, storage elements and seven segment display controller, an alarm clock was successfully developed.

References

[1] Brown, A., 2020. Nexys A7 Reference Manual [Digilent Documentation]. [online] Reference.digilentinc.com. Available at: ¡https://reference.digilentinc.com/reference/programmable-logic/nexys-a7/reference-manual¿ [Accessed 20 October 2020].

[2] Brown, S. and Vranesic, Z., 2014. Fundamentals Of Digital Logic With Verilog Design. 3rd ed. New York: McGraw-Hill.