# ECE-4303　　Professor: Mohamed Aly　　03/10/2021

Time: Check gradescope

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- Write your name on every page.
- Read each question carefully and be sure that you answer all parts.
- This exam contains 5 questions. For a total 100 points.
- Show all your work! Answers without supporting work will not be given credit.
- Exams are closed-book and notes, you can use the calculator.

Grade Table (for instructor use only)

Question	Points	Score	Notes
1	20		
2	20		
3	20		
4	20		
5	20		
Total:	100		

1) (**20 Points**): Write the VHDL code equivalent of the following combinational circuit. Make sure to add a Flip-Flop after E stage and another after F stage. (Write a full testbench describing all possible corner cases).
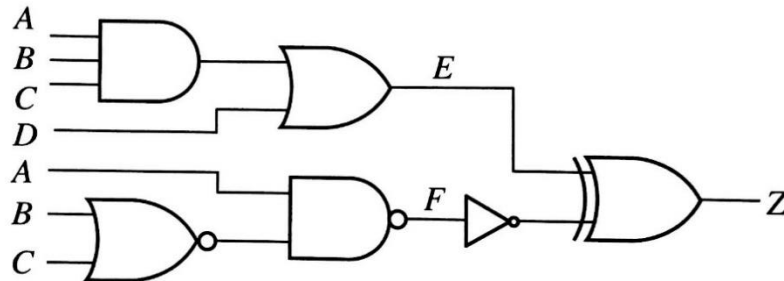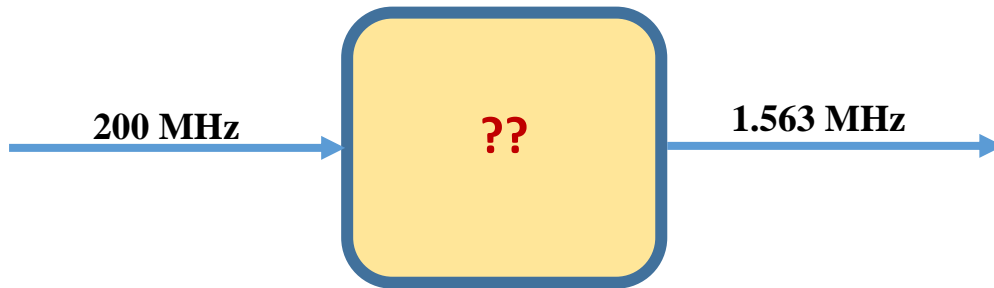
2) (20 Points):

Design two bits comparators using VHDL language (using structure modeling)

Note: Design means RTL code and Testbench covering all possible corner cases)

3) **(20 Points):** (**Show all your work! Answers without supporting work will not be given credit: Negotiation is refused**).

   Write the VHDL code, which describe the functionality of the following circuit. (**Testbench is important**)

200 MHz → [**??**] → **1.563 MHz**

4) (20 points): (Show all your work! Answers without supporting work will not be given credit: Negotiation is refused).

(Write/Design) both the RTL and Testbench using the VHDL language of the five-input majority using the structure modeling approach.

NOTE: Design means RTL code and Testbench covering all possible corner cases

5) **(20 Points):** Design and implement generic N-bit multiplier using VHDL language. Make sure to use the structural modeling and provide a testbench with all possible corner cases.
(**Show all your work! Answers without supporting work will not be given credit: Negotiation is refused).**