ECE 3300
Digital Circuit Design Using Verilog

Exercise 3

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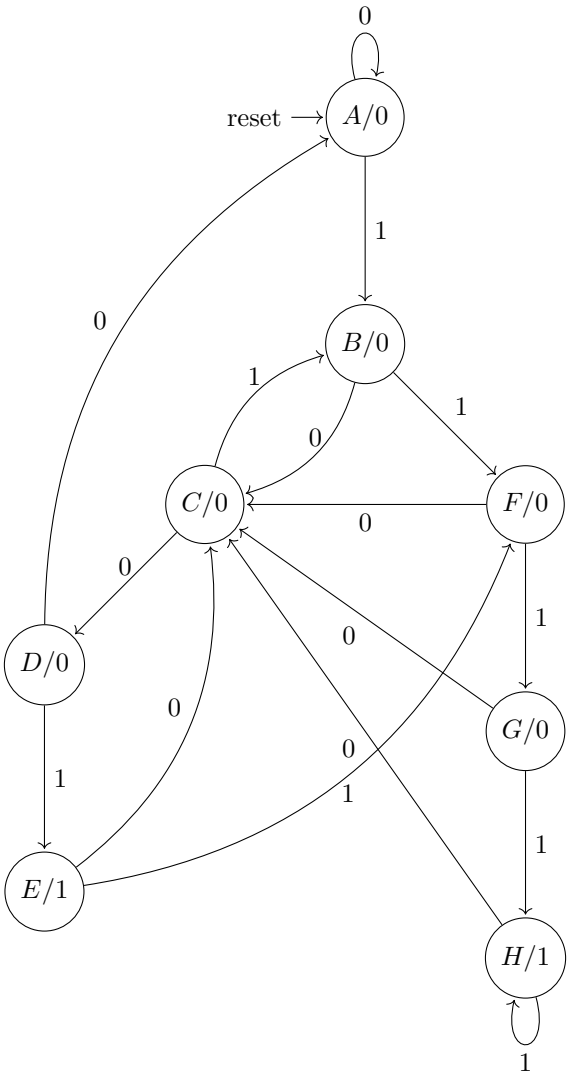
State Diagram



State Table

Present State	Next State $w=0$	Next State $w=1$	Output z
A	A	B	0
B	C	F	0
C	D	B	0
D	A	E	0
E	C	F	1
F	C	G	0
G	C	H	0
H	C	H	1

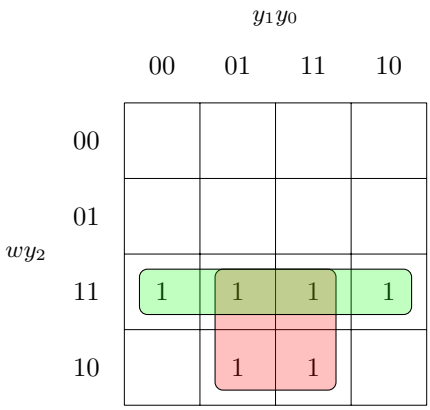
State-assigned Table

	Present State			Next State $w=0$			Next State $w=1$			Output
	y_2	y_1	y_0	Y_2	Y_1	Y_0	Y_2	Y_1	Y_0	z
A	0	0	0	0	0	0	0	0	1	0
B	0	0	1	0	1	0	1	0	1	0
C	0	1	0	0	1	1	0	0	1	0
D	0	1	1	0	0	0	1	0	0	0
E	1	0	0	0	1	0	1	0	1	1
F	1	0	1	0	1	0	1	1	0	0
G	1	1	0	0	1	0	1	1	1	0
H	1	1	1	0	1	0	1	1	1	1

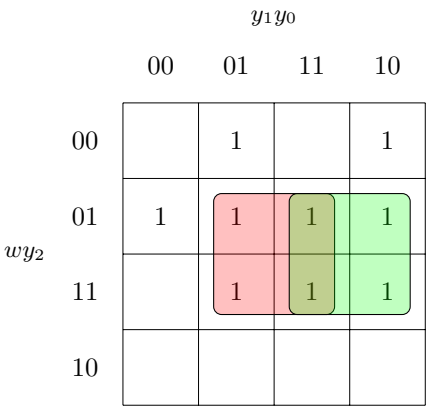
Truth Table

w	y_2	y_1	y_0	Y_2	Y_1	Y_0	z
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0
0	0	1	0	0	1	1	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	0	0	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	1	0
1	0	1	1	1	0	0	0
1	1	0	0	1	0	1	1
1	1	0	1	1	1	0	0
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

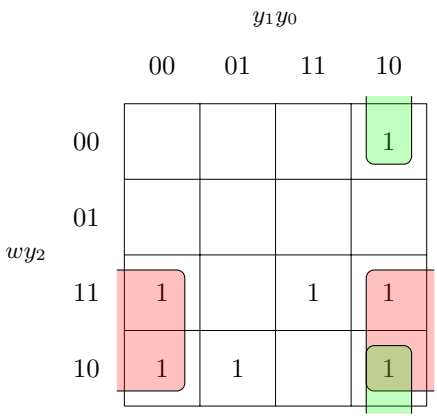
Karnaugh Maps



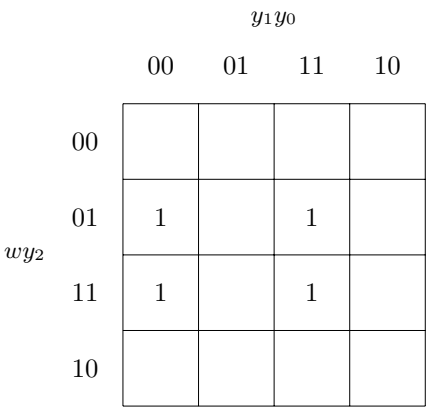
$$Y_2 = wy_0 + wy_2 = w(y_2 + y_0)$$



$$Y_1 = y_2y_0 + y_2y_1 + \overline{w}\,(y_2 \oplus y_1 \oplus y_0)$$

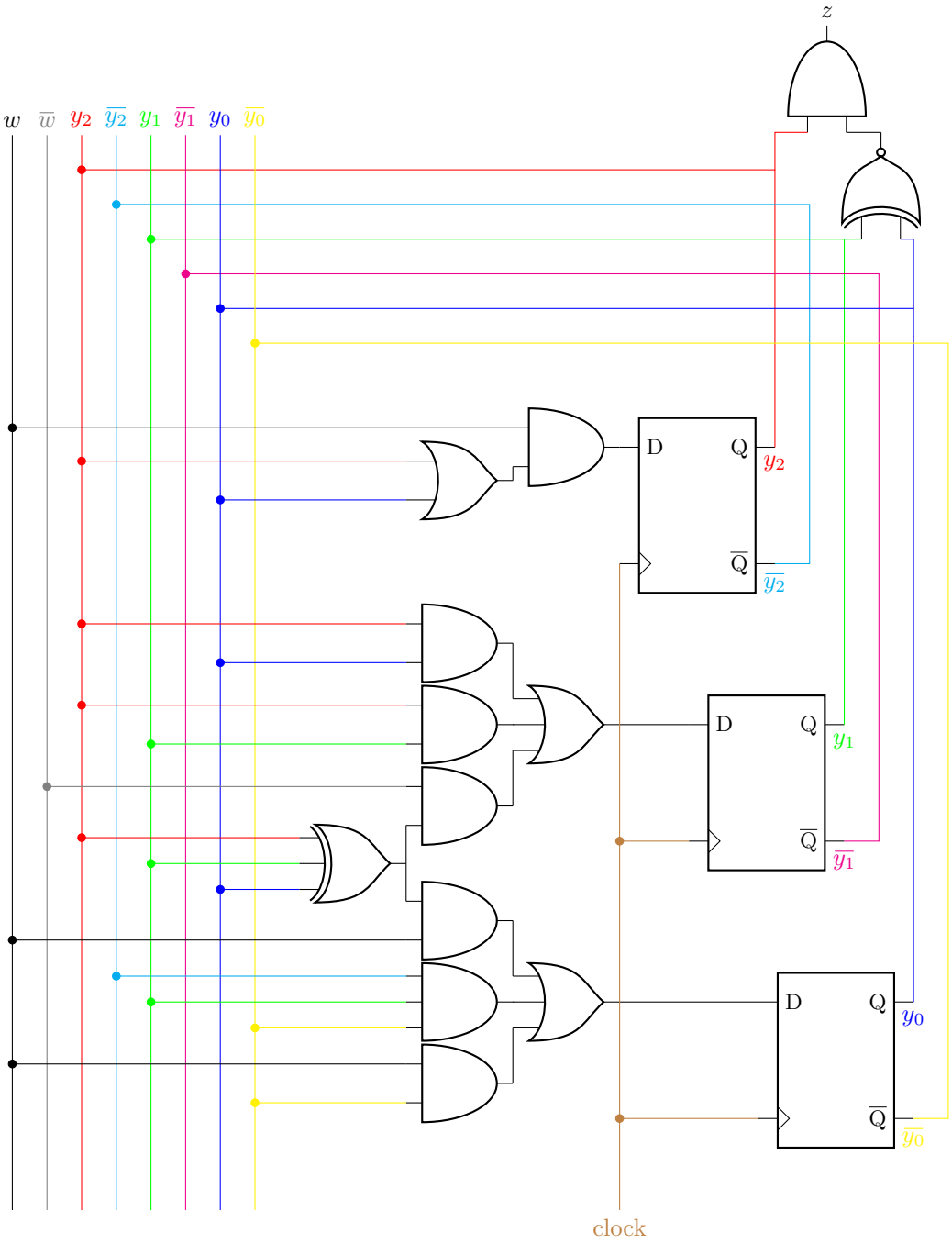


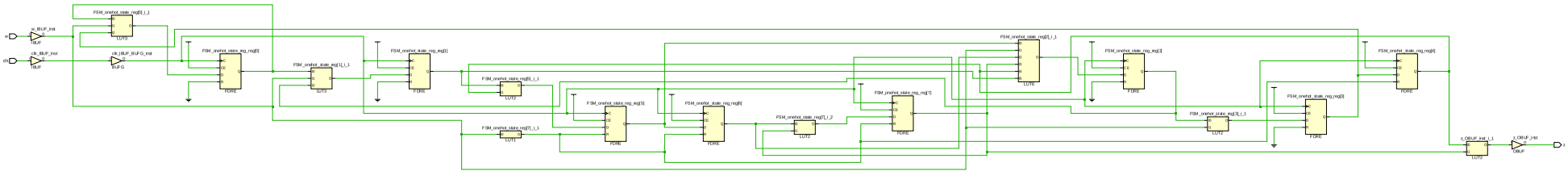
$$Y_0 = w\overline{y_0} + \overline{y_2}y_1\overline{y_0} + w\,(y_2 \oplus y_1 \oplus y_0)$$



$$z = y_2\,(y_1 \odot y_0)$$

Schematic


z
w
$\overline{w}$
y_2
$\overline{y_2}$
y_1
$\overline{y_1}$
y_0
$\overline{y_0}$
D
Q
$\overline{Q}$
clock


FSM_onehot_state_reg[0]_i_1
LUT3
FSM_onehot_state_reg_reg[0]
FDRE
FSM_onehot_state_reg[1]_i_1
LUT3
FSM_onehot_state_reg_reg[1]
FDRE
FSM_onehot_state_reg[1]_i_1
LUT2
FSM_onehot_state_reg[1]_i_1
LUT1
FSM_onehot_state_reg_reg[5]
FDRE
FSM_onehot_state_reg_reg[6]
FDRE
FSM_onehot_state_reg[7]_i_2
LUT2
FSM_onehot_state_reg_reg[7]
FDRE
FSM_onehot_state_reg[7]_i_1
LUT6
FSM_onehot_state_reg_reg[2]
FDRE
FSM_onehot_state_reg[2]_i_1
LUT2
FSM_onehot_state_reg_reg[3]
FDRE
FSM_onehot_state_reg_reg[4]
FDRE
z_OBUF_inst_i_1
LUT2
z_OBUF_inst
OBUF
w_IBUF_inst
IBUF
clk_IBUF_inst
IBUF
clk_IBUF_BUFG_inst
BUFG
w
clk
z

Conclusion

A significant difference between the two schematic is that the Vivado generated one use LUTs in contrast to logic gates. Also, the Vivado generated one have 8 flipflops instead of three.