ECE 2300L
Digital Logic Design Laboratory

Experiment 11

Report

Choi Tim Antony Yung

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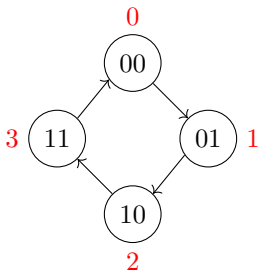
State Diagram



State Table

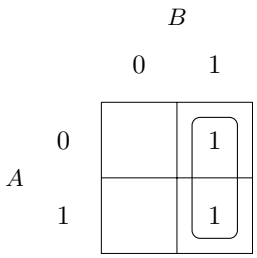
A	B	A^+	B^+	T_A	T_B
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

Truth Table

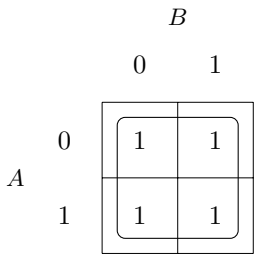
A	B	T_A
0	0	0
0	1	1
1	0	0
1	1	1

A	B	T_B
0	0	1
0	1	1
1	0	1
1	1	1

Karnaugh Maps

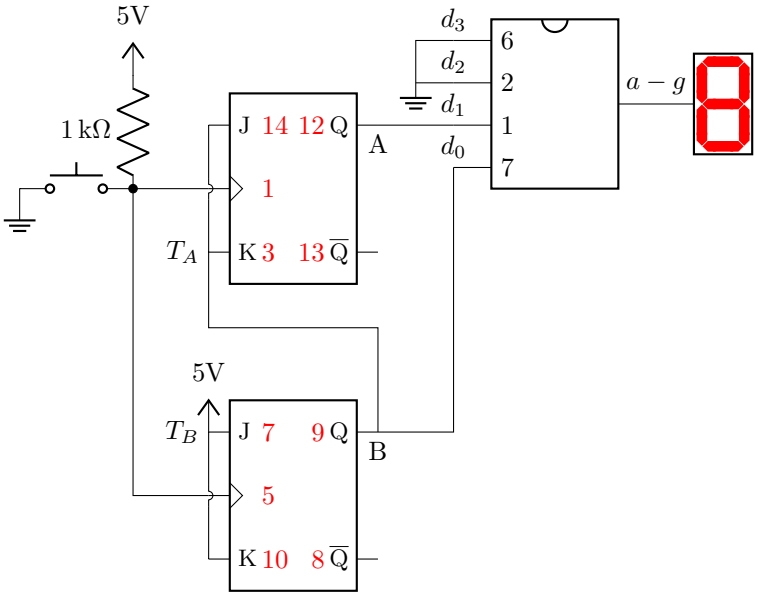


$T_A = B$



$T_B = 1$

Schematic



MOTOROLA

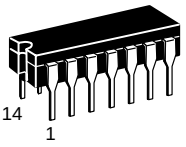
SN54/74LS73A

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

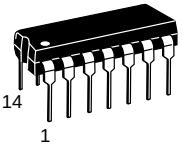
The SN54LS/74LS73A offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

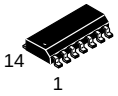
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08

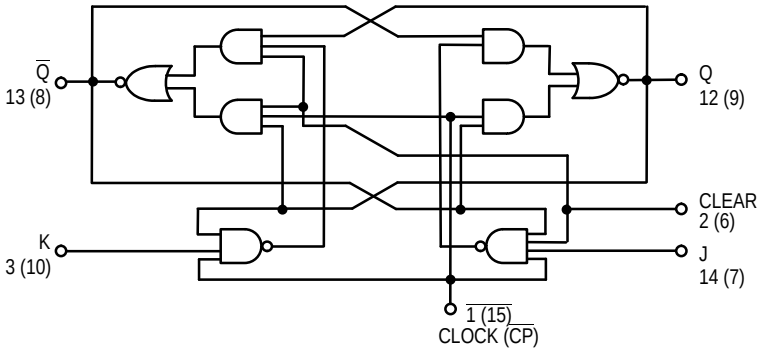


N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

LOGIC DIAGRAM (Each Flip-Flop)



ORDERING INFORMATION

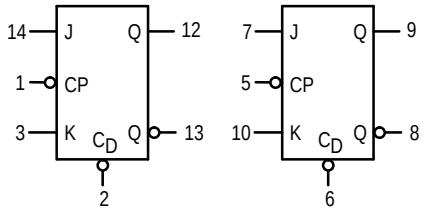
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Reset (Clear)	L	X	X	L	H
Toggle	H	h	h	$\overline{q}$	q
Load “0” (Reset)	H	l	h	L	H
Load “1” (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don’t Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

LOGIC SYMBOL



V_{CC} = PIN 4
GND = PIN 11

Demo

A video demonstration can be found here at https://photos.app.goo.gl/729cwgJ9mkX1yE7Z6