ECE 2300
Digital Logic Design

Homework 6

Choi Tim Antony Yung

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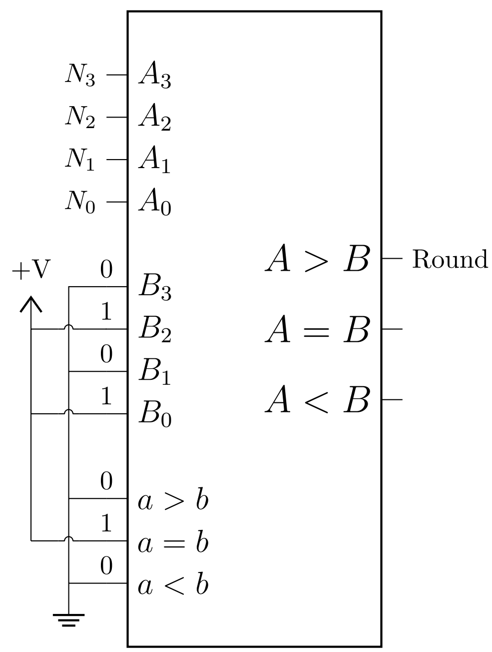
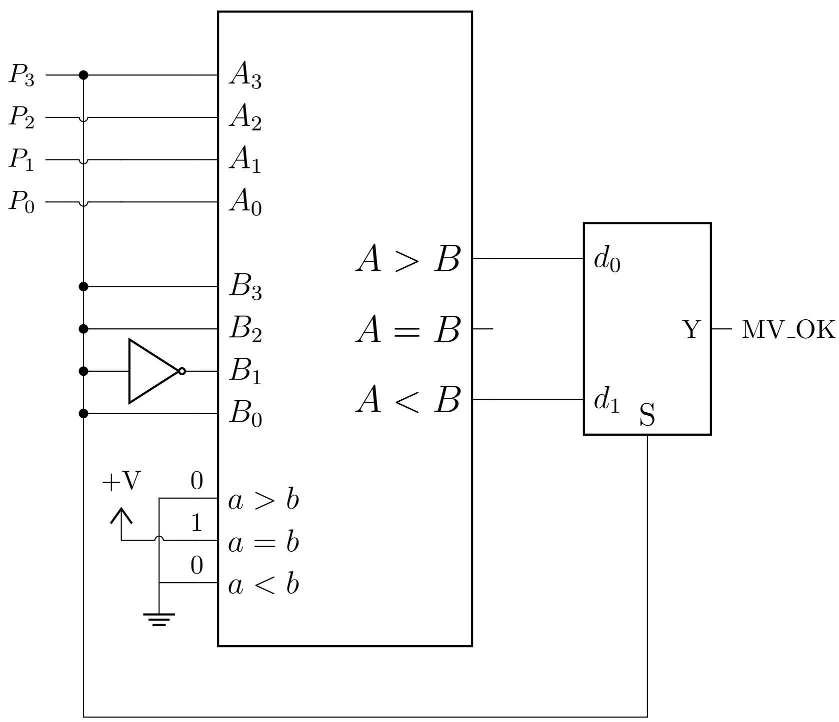
1 Using a magnitude comparator, generate a logic one “Round” signal (to rounda number up by one) if the base 12 input, $N = N_3, N_2, N_1, N_0$, is six or higher. Let N connect to the comparator’s A input.

$$Round = N > 5 = (N_3 N_2 N_1 N_0)_2 > (0101)_2$$

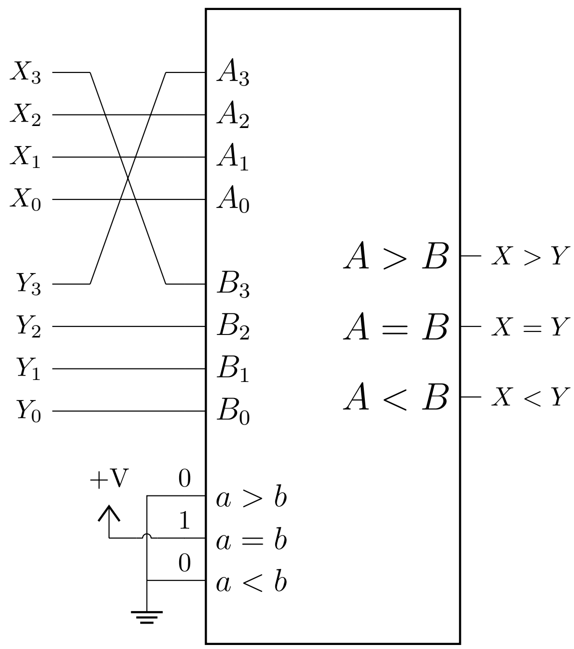


2 **A simple mechanism moves between positions $P = (0000)_2$ and $P = (1111)_2$. Using a magnitude comparator, generate an enable signal, MV_OK,that is one if the position, P, is 12 or lower or if it is three or higher.**

P_3	Threshold				Relationship
0	0	0	1	0	P valid if greater than threshold
1	1	1	0	1	P valid if less than threshold
	P_3	P_3	$\overline{P_3}$	P_3	



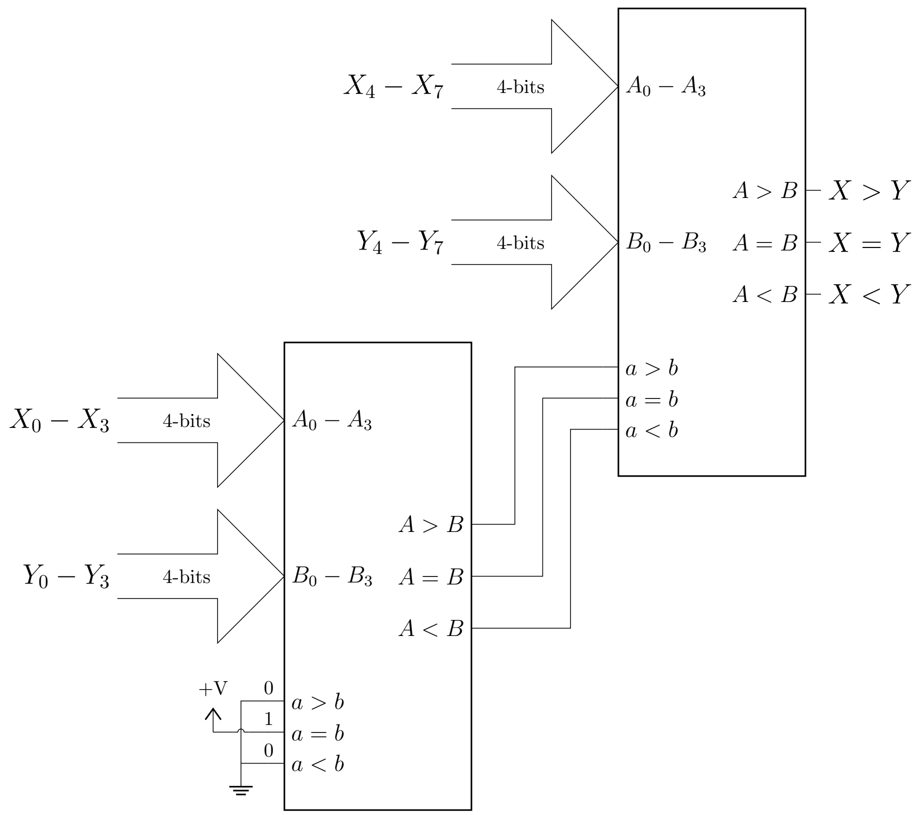
3.a Design a magnitude comparator to compare two 4-bit two's complement numbers, X and Y.



3.b Complete the following chartgiving the outputs for the corresponding inputs (the leftmost X and Y bits are the MSBs). Indicate whether the output is correct (i.e."OK") and give the true relationship of the-signedinputs.

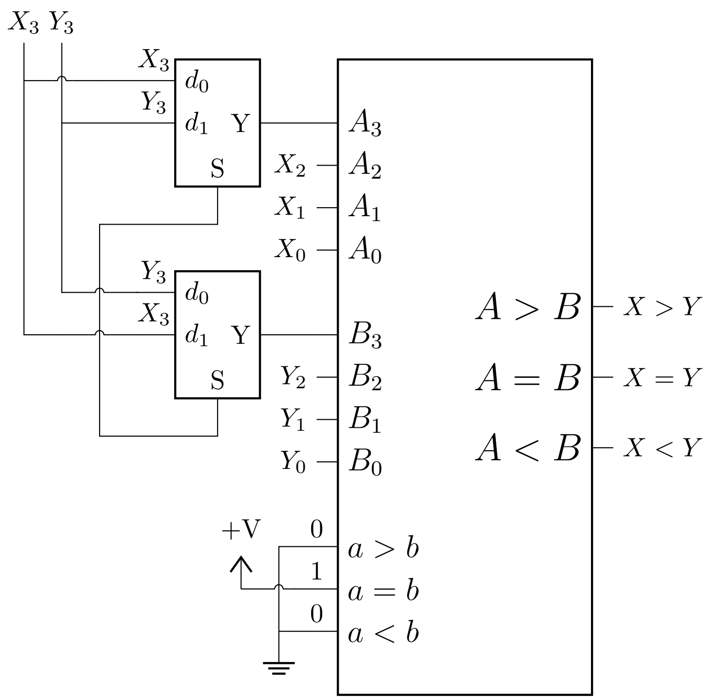
X (in) signed				Y (in) signed				A unsigned				B unsigned				$X > Y$	$X = Y$	$X < Y$	OK (Signed Result)
1	1	0	0	0	1	0	1	0	1	0	0	1	1	0	1	0	0	1	OK ($-4 < +5$)
1	0	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0	0	OK ($-6 > -7$)
1	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	0	0	1	OK ($-8 < +5$)
1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0	1	0	OK ($-3 = -3$)
0	0	1	1	1	1	0	1	1	0	1	1	0	1	0	1	1	0	0	OK ($+3 > -5$)
1	1	0	1	1	1	0	0	1	1	0	1	1	1	0	0	1	0	0	OK ($-3 > -4$)
0	1	1	1	0	1	0	1	0	1	1	1	0	1	0	1	1	0	0	OK ($+7 > +5$)
0	0	1	1	0	1	0	0	0	1	0	0	1	1	0	1	0	0	1	OK ($+3 < +4$)

4 Using magnitude comparators, create a circuit to compare two 8-bit unsigned numbers, X and Y. Let X connect to the comparator A inputs.

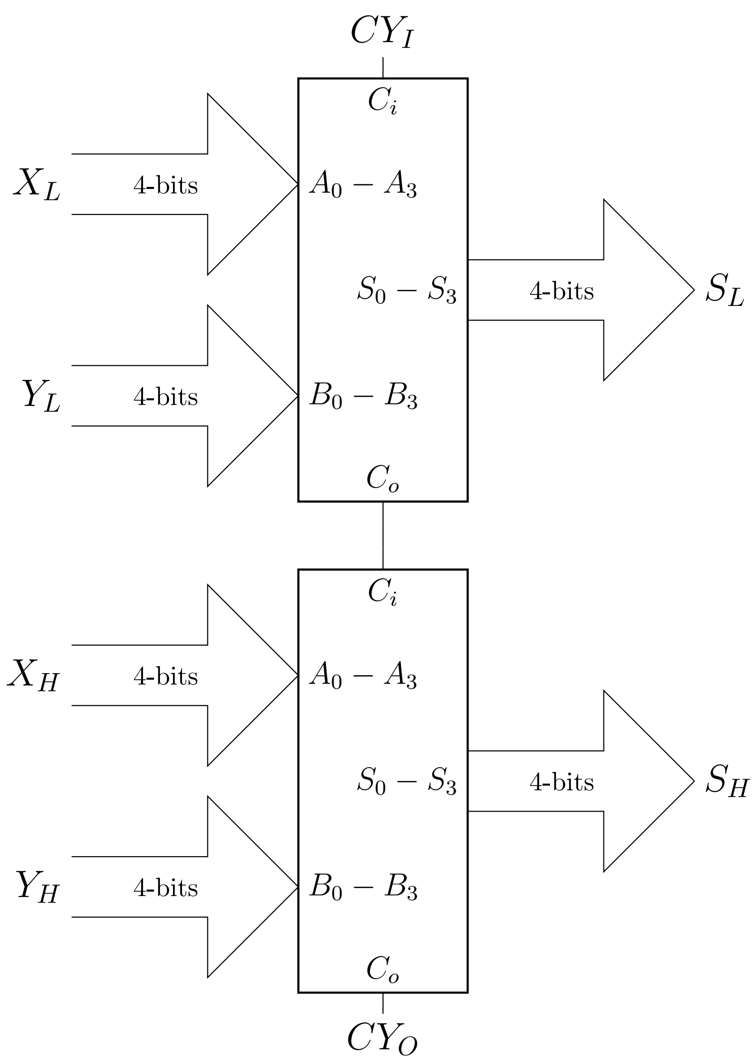


5 Using two 2:1 muxes and a magnitude comparator, design a circuit to compare 4-bit inputs X and Y as unsigned numbers when S=0 or as two's complement numbers when S=1.

S	A_3	B_3
0	X_3	Y_3
1	Y_3	X_3

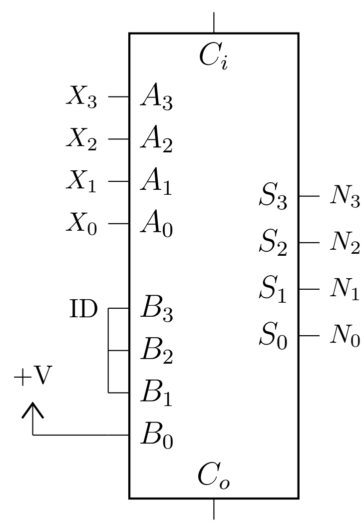


6 Draw a circuit to add two 8-bit unsigned binary numbers, X and Y. Include acarry-in, CY_I, and carry-out, CY_O. Let X connect to the adder A inputs and Y to the adder B inputs. The sum is S. Hint: Use fat arrows for each nybble with subscript "L" or "H" for the low and high nybbles respectively.



7 **Using an adder, draw a circuit to increment or decrement an unsigned 4-bit number, $X = \{X_3X_2X_1X_0\}$. Let X connect to the adder A inputs and let the result be $N = \{N_3N_2N_1N_0\}$. Ignore the carry-out. Let ID be the increment or decrement signal (0 = increment, 1 = decrement). Hint: Do not use the carry-in input.**

	ID	B	B_3	B_2	B_1	B_0
Increment	0	1	0	0	0	1
Decrement	1	-1	1	1	1	1



8 Using an adder, draw a circuit to subtract Y from X where X connects to the A input. The format is two's complement. Let the result be $N = \{N_3 N_2 N_1 N_0\}$. Ignore the carry-out. Hint: This is only a subtractor so complements can be done with inverters.