### ECE 2300 Digital Logic Design

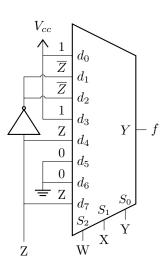
Homework 5

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### 1 Using an 8:1 mux, create a circuit to generate

$$f(WXYZ) = \overline{W} \cdot \overline{Z} + \overline{X} \cdot \overline{Y} \cdot Z + X \cdot Y \cdot Z$$

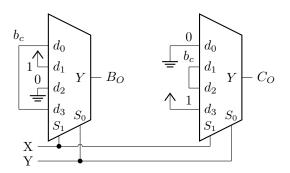
W	X	Y	Z	f	W	X	Y	$\mid \mathbf{Z} \mid f$
0	0	0	0	1	1	0	0	0   0
0	0	0	1	1	1	0	0	$\left \begin{array}{c c}0&0\\1&1\end{array}\right $
0	0	1	0	1	1	0	1	$\left  \begin{array}{c c} 0 & 0 \\ 1 & 0 \end{array} \right $
0	0	1	1	0	1	0	1	1   0
0	1	0	0	1	1	1	0	$\left  \begin{array}{c c} 0 & 0 \\ 1 & 0 \end{array} \right $
0	1	0	1	0	1	1	0	1 0
0	1	1	0	1	1	1	1	0   0
0	1	1	1	1	1	1	1	1   1



Using two 4:1 muxes, generate the  $B_O$  (Borrow-Out) and  $C_O$  (Carry-Out) outputs for a 1-bit full subtractor and 1-bit full adder respectively where X is the minuend, Y is the subtrahend or Y and Y are the addends and be is the borrow-in or carry-in.

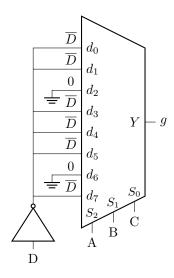
$$B_O = \overline{X} \cdot b_c + \overline{X} \cdot Y + Y \cdot b_c$$
 
$$C_O = X \cdot Y + X \cdot b_c + Y \cdot b_c$$

X	Y	$b_c$	$B_O$	$C_O$	X	Y	$b_c$	$B_O$	$C_O$
0	0	0	0	0	1	0	0	0 0	0
0	0	1	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1
0	1	1	1	1	1	1	1	1	1



3 Using an 8:1 mux, create a circuit to generate the segment g outputs for a 7-segment display where  $g = \overline{B} \cdot \overline{D} + C \cdot \overline{D}$ .

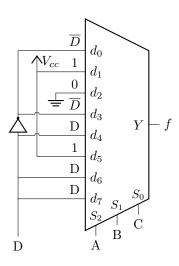
A	В	С	D	$\mid g \mid$	A	В	С	D	$\mid g \mid$
0	0	0	0	1	1	0	0	0	1
0	0	0	1	0					
		1	0	1	1	0	1	0	1
0	0	1	1	0	1	0	1	1	0
0	1	0	0	0	1	1	0	1 0	0
0	1	0	1	0	1	1	0	0	0
0	1	1	0	1	1	1	1	0	1
0	1	1	1	0	1	1	1	1	0



### 4 Using an 8:1 mux, create a circuit to generate

 $f(ABCD) = A \cdot D + \overline{A} \cdot \overline{B} \cdot \overline{D} + \overline{B} \cdot C + \overline{A} \cdot C \cdot \overline{D}$ 

A	В	$\mathbf{C}$	D	$\mid f \mid$	A	В	$\mathbf{C}$	D	$\mid f \mid$
0	0	0	0	1	1	0	0	0	0
			$\begin{vmatrix} 0 \\ 1 \end{vmatrix}$		1	0	0	1	1
0	0	1	0	1	1	0	1 1	0	1
0	0	1	1	1	1	0	1	1	1
0	1	0	0	0	1	1	0	0	0
0	1	0	$\begin{vmatrix} 0 \\ 1 \end{vmatrix}$	0	1	1	0	1	1
0	1	1	0	1	1	1	1	0	0
0	1	1	1	0	1	1	1	1	1

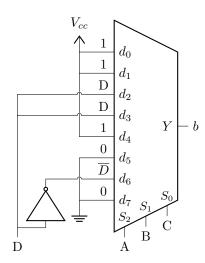


## 5 Using an 8:1 mux, create a circuit to generate the segment b outputs for a 7-segment display.

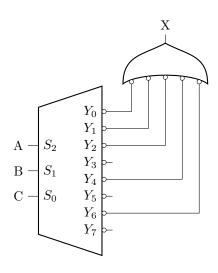
Given ABCD = 0, 1, 2, ..., F, the segment b outputs are  $(F9C8)_{16}$  (e.g. the MSB of  $(F)_{16}$  = output for ABCD =  $(0000)_2$  and the LSB of  $(8)_{16}$  = output for ABCD =  $(1111)_2$ ).

 $(F9C8)_{16} = (1111010111001000)_2$ 

A	В	С	D	b	A	В	С	D	b
0	0		0		1	0	0	0	1
0	0	0	1	1	1	0	0	1	1
0	0	1	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1	1	0
0	1	0	0	0	1	1	0	0	1
0	1	0	0 1	1	1	1	0	$\begin{vmatrix} 0 \\ 1 \end{vmatrix}$	0
0	1	1	0		1	1	1	0	0
0	1	1	1	1	1	1	1	$\begin{vmatrix} 0 \\ 1 \end{vmatrix}$	0



6 Given inputs A, B, and C where A is the MSB, use a 3:8 demux to generate  $X = \sum (m_0, m_1, m_2, m_4, m_6)$ 

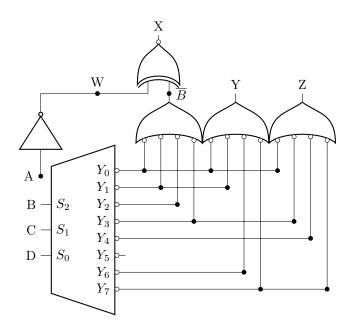


# 7 Using a 3:8 demux, generate a complemented Gray code

A	В	С	D	W	X	Y	Z	,	A	В	С	D	W	X	Y	Z
0	0	0	0	1	1	1	1		1	0	0	0	0	0	1	1
0	0	0	1	1	1	1	0		1	0	0	1	0	0	1	0
0	0	1	0	1	1	0	0		1	0	1	0	0	0	0	0
0	0	1	1	1	1	0	1		1	0	1	1	0	0	0	1
0	1	0	0	1	0	0	1		1	1	0	0	0	1	0	1
0	1	0	1	1	0	0	0		1	1	0	1	0	1	0	0
0	1	1	0	1	0	1	0		1	1	1	0	0	1	1	0
0	1	1	1	1	0	1	1		1	1	1	1	0	1	1	1

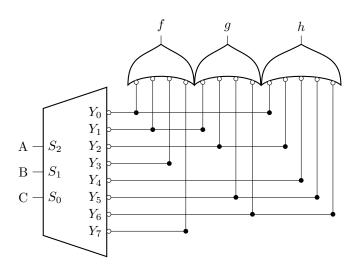
Observe that  $\sum (m_0, m_1, m_2, m_3) = \overline{B}$ , it can be decuced that  $X = \overline{B} \otimes W$ 

$\overline{B}$	W	X
0	0	1
0	1	0
1	0	0
1	1	1



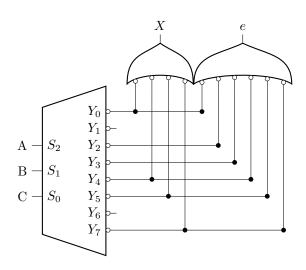
# 8 Using a 3:8 demux, generate these functions of A, B and C:

$$f = \sum (m_0, m_1, m_3, m_7)$$
$$g = \sum (m_1, m_2, m_5, m_6)$$
$$h = \sum (m_0, m_2, m_4, m_5, m_6)$$



# 9 Using a 3:8 demux generate the following truth table:

A	В	С	X	e				X	1
0	0	0	$\left \begin{array}{c}1\\0\\0\\0\end{array}\right $	1	1	0	0	1 1 0 1	1
0	0	1	0	0	1	0	1	1	1
0	1	0	0	1	1	1	0	0	0
0	1	1	0	1	1	1	1	1	1

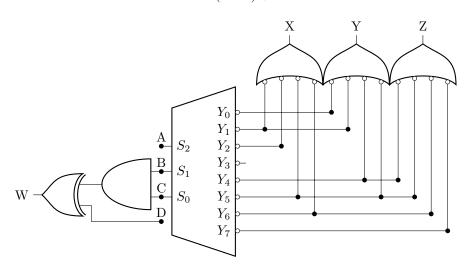


10.a Using a 3:8 demux, transpose input ABCD then add two, modulo 16 to created output WXYZ.
(i.e. WXYZ = (DCBA + 2)mod 16).

A	В	С	D	W	X	Y	Z	A	В	С	D	W	X	Y	Z
0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1
0	0	0	1	1	0	1	0	1	0	0	1	1	0	1	1
0	0	1	0	0	1	1	0	1	0	1	0	0	1	1	1
0	0	1	1	1	1	1	0	1	0	1	1	1	1	1	1
0	1	0	0	0	1	0	0	1	1	0	0	0	1	0	1
0	1	0	1	1	1	0	0	1	1	0	1	1	1	0	1
0	1	1	0	1	0	0	0	1	1	1	0	1	0	0	1
0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	1

Observing the truth table:

$$W = (B \cdot C) \oplus D$$



10.b This circuit can be simplified to remove the 3:8 demux. Draw the schematic for each output (W, X, Y and Z) using only the six basic Gates:

A	В	С	D	W	X	Y	Z	A	В	С	D	W	X	Y	Z
0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1
0	0	0	1	1	0	1	0	1	0	0	1	1	0	1	1
0	0	1	0	0	1	1	0	1	0	1	0	0	1	1	1
0	0	1	1	1	1	1	0	1	0	1	1	1	1	1	1
0	1	0	0	0	1	0	0	1	1	0	0	0	1	0	1
0	1	0	1	1	1	0	0	1	1	0	1	1	1	0	1
0	1	1	0	1	0	0	0	1	1	1	0	1	0	0	1
0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	1

Observing the truth table:

$$W = (B \cdot C) \oplus D$$
 
$$X = B \oplus C$$
 
$$Y = \overline{B}$$
 
$$Z = A$$

