

ECE 2300
Digital Logic Design

Homework 5

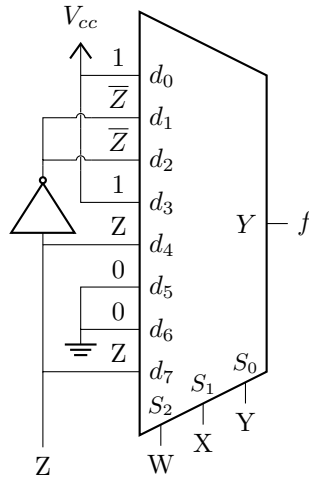
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1 Using an 8:1 mux, create a circuit to generate

$$f(ABCD) = \overline{W} \cdot \overline{Z} + \overline{X} \cdot \overline{Y} \cdot Z + X \cdot Y \cdot Z$$

W	X	Y	Z	f	W	X	Y	Z	f
0	0	0	0	1	1	0	0	0	0
0	0	0	1	1	1	0	0	1	1
0	0	1	0	1	1	0	1	0	0
0	0	1	1	0	1	0	1	1	0
0	1	0	0	1	1	1	0	0	0
0	1	0	1	0	1	1	0	1	0
0	1	1	0	1	1	1	1	0	0
0	1	1	1	1	1	1	1	1	1

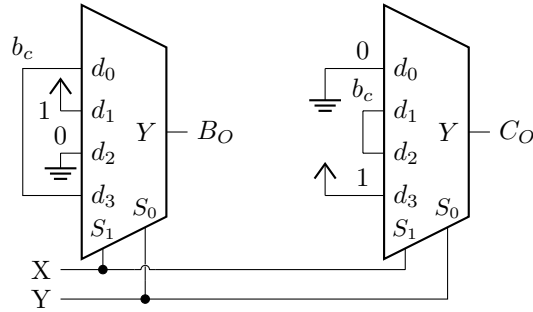


- 2 Using two 4:1 muxes, generate the B_O (Borrow-Out) and C_O (Carry-Out) outputs for a 1-bit full subtractor and 1-bit full adder respectively where X is the minuend, Y is the subtrahend or Y and Y are the addends and bc is the borrow-in or carry-in.

$$B_O = \overline{X} \cdot b_c + \overline{X} \cdot Y + Y \cdot b_c$$

$$C_O = X \cdot Y + X \cdot b_c + Y \cdot b_c$$

X	Y	b_c	B_O	C_O	X	Y	b_c	B_O	C_O
0	0	0	0	0	1	0	0	0	0
0	0	1	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1
0	1	1	1	1	1	1	1	1	1



- 3 Using an 8:1 mux, create a circuit to generate the segment g outputs for a 7-segment display where $g = \overline{B} \cdot \overline{D} + C \cdot \overline{D}$.

A	B	C	D	g
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0

A	B	C	D	g
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	1	0
1	1	0	0	0
1	1	1	0	1
1	1	1	1	0

