MPLAB X IDE v4.20 - ECE3301_Assg8_1 : default

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default | PC: 0x114 | n ov Z DC C : W:0 | How do I? Keyword(

Start Page | ftdiv.c | ftmul.c | float.c | ftadd.c | main.c

Source | History

```
1  #include <math.h>
2  #include <xc.h>
3  #include <p18f4321.h>
4
5  char high_byte, low_byte;
6  int last = 0;   // hold last CCPR value
7  int temp = 0;
8  int result = 0;
9
10 void interrupt high_priority isr()
11 {
12     if (PIR1bits.TMR1IF)
13     {   // TMR1 overflow, add 0x10000 to get correct result
14         PIR1bits.TMR1IF = 0;
15         temp = 0x10000;
16     }
17     if (PIR1bits.CCP1IF)
18     {   // rising edge at CCP1, compute period
19         PIR1bits.CCP1IF = 0;
20         high_byte = CCPR1H;
21         low_byte = CCPR1L;
22         temp += high_byte*0x100 + low_byte;
23         result = temp - last;
24         last = high_byte*0x100 + low_byte;
25         temp = 0;
26     }
27
28 }
29 void main(void) {
30
31     CCP1CON = 0x05;          // capture mode, every rising edge
32     TRISCbits.TRISC2 = 1;    // CCP1 as input
33     T1CON = 0x01;            // two 8-bits pair, Timer1 osc off, 1:1 prescale, internal clk, enable tmr1
34     CCPR1H = 0;
35     CCPR1L = 0;
36     PIR1bits.CCP1IF = 0;     // clear flag
37     PIR1bits.TMR1IF = 0;     // clear flag
38     INTCONbits.GIE = 1;      // enable interrupt
39     INTCONbits.PEIE = 1;     // enable peripheral interrupt
40     IPR1bits.CCP1IP = 1;     // set high priority interrupt
41     IPR1bits.TMR1IP = 1;     // set high priority interrupt
42     RCONbits.IPEN = 0;       // disable priority
43     PIE1bits.CCP1IE = 1;     // enable interrupt
44     PIE1bits.TMR1IE = 1;
45
46     while (1)
47     {
48
49     }
50 }
```

main > while (1) >

Ser... | Files | Cla...

- ECE3301_Assg8_1
  - Header Files
  - Important Files
  - Linker Files
  - main.c
  - Source Files
  - Libraries
  - Loadables

Navigator | ECE3301_Ass...

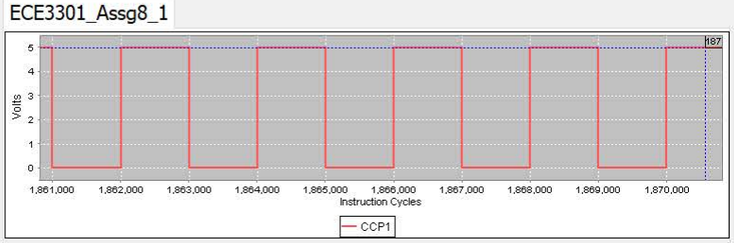
- ECE3301_Assg8_1
  - Project Type: Application - C
  - Device
    - PIC18F4321
    - Checksum: Debug Image
  - Compiler Toolchain
    - XC8 (v1.34) [C:\Program F
    - Debug Image: ELF: Optim
  - Memory
    - Data 512 (0x200) bytes
      - 5%
      - Data Used: 24 (0x18) Fr
    - Program 8,192 (0x2000) b
      - 4%
      - Program Used: 296 (0x1
  - Debug Tool
    - Simulator
    - Click for Simulated Periphe
  - Debug Resources
    - Program BP Used: 0 Free
    - Data BP Used: 0 Free: 10
    - Data Capture BP: No Supp
    - Unlimited BP (S/W): Simu

...ts | I/O Pins | RegisterTrace | Output | Watches

Name	Type	Address	Value
PORTC	SFR	0xF82	0x04
PORTD	SFR	0xF83	0
result	int	0x13	2000
<Enter new v			

Logic Analyzer

ECE3301_Assg8_1



ECE3301_Assg8_1 (Build, Load, ...) | debugger halted | 49:1 | INS

```
1         ; master program
2
3         INCLUDE <P18F4321.INC>
4
5         ORG     0x100
6
7         ; init config
8         ; ADCON
9         MOVLW   0x0F            ; Vref = Vdd - Vss, all digital
10        MOVWF   ADCON1
11        ; TRISC
12        MOVLW   0x00            ; SCK, SDO, all digital output
13        MOVWF   TRISC
14        ; TRISD
15        MOVLW   0xFF            ; switches, all digital  input
16        MOVWF   TRISB
17        ; SSPSTAT
18        MOVLW   0x40            ; high to low clock
19        MOVWF   SSPSTAT
20        ; SSPCON
21        MOVLW   0x20            ; enable SPI, set as master
22        MOVWF   SSPCON1
23
24        ; main loop
25  LOOP  MOVF    PORTB, SSPBUF   ; move PORTB to SSPBUF to be transmitted
26  RUNNIN BTFSS  SSPSTAT, BF     ; if transmisison completed branch back to loop
27        BRA     RUNNIN          ; transmission in progress
28        BRA     LOOP
29
30        END
```

```
1         ; slave program
2
3         INCLUDE <P18F4321.INC>
4
5         ORG     0x100
6
7         ; init config
8         ; ADCON
9         MOVLW   0x0F            ; Vref = Vdd - Vss, all digital
10        MOVWF   ADCON1
11        ; TRISC
12        MOVLW   0xFF            ; SCK, SDI, all digital  input
13        MOVWF   TRISC
14        ; TRISD
15        MOVLW   0x00            ;     LEDs, all digital output
16        MOVWF   TRISD
17        ; SSPSTAT
18        MOVLW   0x40            ; high to low clock
19        MOVWF   SSPSTAT
20        ; SSPCON
21        MOVLW   0x25            ; enable SPI, set as slave
22        MOVWF   SSPCON1
23
24        ; main loop
25  LOOP  BTFSC   SSPSTAT, BF     ; if transmission not completed branch here
26        MOVFF   SSPBUF, PORTD   ; transmission completed, move SSPBUF to PORTD
27        BRA     LOOP
28
29        END
```