1 (20) What is the size of the program counter in the PIC18F? What is the maximum size of the PIC18F program memory? Justify your answer.

The size of the program ccounter in the PIC18F is 21 bits. The maximum size of the PIC18F program memory is then the maximum memory the program counter can address, which is (address size) $\times$ (word size) $= 2^{21} \times 8$ bits $=$ 2MBytes

2 (15) If the last address of an on-chip memory is 0x7FF, determine its size.

Since the last address is (111 1111 1111), the address size of the memory is 11 bits, which make the size of the memory (address size) $\times$ (word size) = $2^{11} \times$ 8 bits = 2KBytes

3 (15) Assume that the PIC18F is currently executing a 16-bit instruction addressed by 4000H. What are the current contents of the program counter?

The program counter is incremented to point to the next instruction to be executed. If the PIC18F is currently executing a 16-bit instruction addressed ny 4000H, the PC will point to the next 16-bit instruction, which is located in 4002H.

4 (20) What is the largest hex value that can be moved into an 8-bit register? What is the decimal equivalent of that hex value?

The largest hex value that can be moved into an 8-bit register is $(1111\ 1111)_2$ = 0xFF = $15 \times 16^1 + 15 \times 16^0 = 255$

5 (30)

5.a How many address and data lines are required for a 1M $\times$ 16 memory chip?

The 1M indicated that the memory chip have 1M = 2^{10} locations, which needs 10 address bits to be addressed, thus the memory chip require 10 address lines. 16 indicates that each address is occupied by 16 bits of data, which indicates that 16 data lines is needed to transfer the data.

5.b What is the size of a decoder with one chip enable (CE) to obtain a 64k × 32 memory from 4k × 8 chips? Where are the inputs and outputs of the decoder connected?

A 4 to 16 decoder is needed.

Suppose the product 64k × 32 memory is meant to be connected to address lines A_{15} to A_0 and to data lines A_{31} to A_0. Four 4k × 8 can be used to compose a 4k × 32 module by connecting the enable pin of the 4 chip to the same output of the decoder,the lower 12 address lines (A_{11} to A_0) to each memory chip, and splitting 8 of the 32 data line to each memory chip. Since $\frac{64k \times 32}{4k \times 32}$ = sixteen 4k × 32 module is needed to compose a 64k × 32 memory, 16 decoder output is needed to enable each of the sixteen 4k × 32 module i.e. sixteen group of four 4k × 8 memory chip, 16 output of the decoder is connected to the enable pin of the chips. To select which group of memory is being accessed, the higher 4 address line A_{15} to A_{12} is conneccted as the inputs to the decoder. To decode from 4 address line inputs to 16 enable outputs, a 4 to 16 decoder is needed.

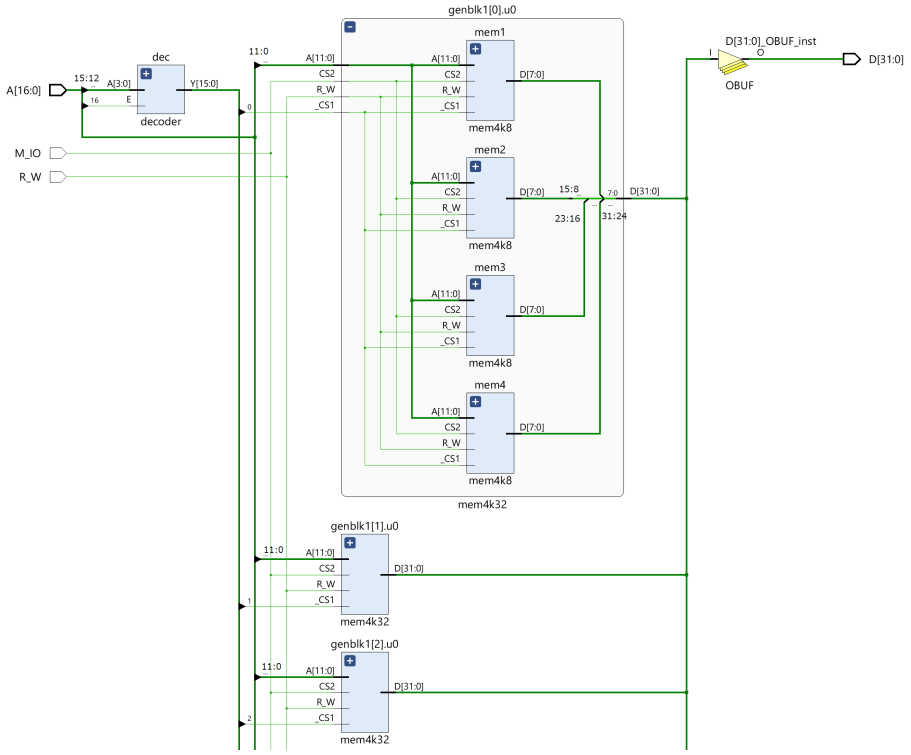
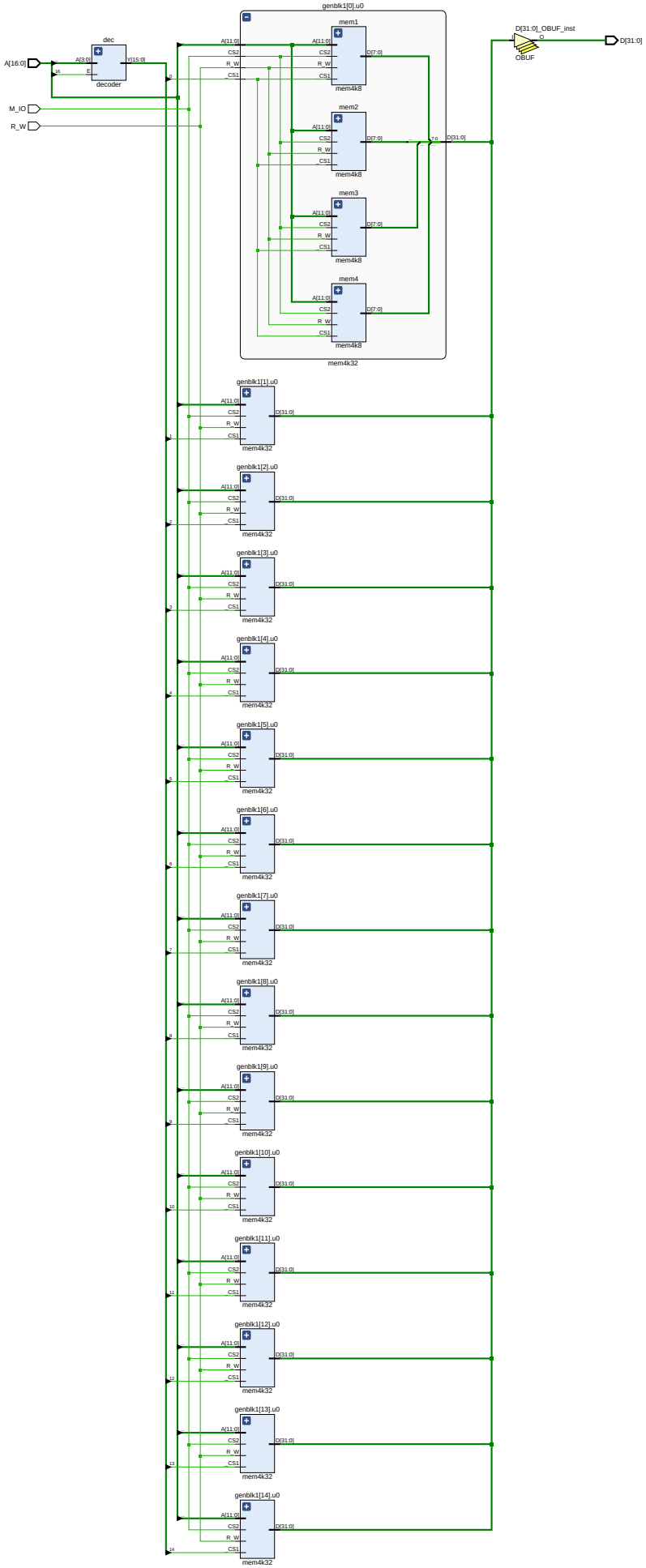


Figure 1: A portion of the below schematic denoting the distribution of split bus line omitted in original schematic generated by Xilinx Vivado


A[16:0]
M_IO
R_W
dec
A[3:0]
E
Y[15:0]
decoder
genblk1[0].u0
mem1
mem2
mem3
mem4
A[11:0]
CS2
R_W
CS1
D[7:0]
mem4k8
mem4k32
D[31:0]_OBUF_inst
I
O
OBUF
D[31:0]
genblk1[1].u0
genblk1[2].u0
genblk1[3].u0
genblk1[4].u0
genblk1[5].u0
genblk1[6].u0
genblk1[7].u0
genblk1[8].u0
genblk1[9].u0
genblk1[10].u0
genblk1[11].u0
genblk1[12].u0
genblk1[13].u0
genblk1[14].u0