**QUESTIONS & ANSWERS**

***An example of a self complementing code is :***

(A) 8421 code (B) Gray code (C) Excess-3 code(yes) (D) 7421 code

***The Excess-3 decimal code is a self-complementing code because***

(A) The binary sum of a code and its 9’s complement is equal to 9.(yes)

(B) It is a weighted code.

(C) Complement can be generated by inverting each bit pattern.(yes)

(D) The binary sum of a code and its 10’s complement is equal to 9.

***The size of the ROM required to build an 8-bit adder/subtractor with mode control, carry input, carry output and two’s complement overflow output is given as***

(A) 216 × 8 (B) 218 × 10(YES) (C) 216 × 10 (D) 218 × 8

**Explanation:-**total input to the rom decoder will be (8+8 ( two 8 bit number ) +1( mode ) +1( carry in))

so total number of words out of decoder will be 2^18 . result will be 8 bit so 8 vertical lines +( 1 for carry ) +1 ( for saying underflow).

***8-bit 1’s complement form of –77.25 is***

(A) 01001101.0100 (B) 01001101.0010 (C) 10110010.1011(yes) (D) 10110010.1101

Explanation: convert 77 into binary . i.e.. 01001101

convert 0.25 into binary. i.e.. 0100

binary equivalent of 77.25 = 01001101.0100

make 1's into 0's and 0's into 1's = 10110010.1011

***A latch is constructed using two cross-coupled***

(A) AND and OR gates (B) AND gates

(C) NAND and NOR gates (D) NAND gates(yes)

**Explanation:-**Latch can be designed either Nand or Nor gates. But not both nand and nor gates.

***multiplexer is a logic circuit that***

(A) accepts one input and gives several output

(B) accepts many inputs and gives many output

(C) accepts many inputs and gives one output(yes)

(D) accepts one input and gives one output

**Explanation:-** Multiplexer means many to one. Encoder means one to many

***The hexadecimal number equivalent to (1762.46)8 is***

(A) 3F2.89 (B) 3F2.98 (C) 2F3.89 (D) 2F3.98

**Explanation:-** convert octal into binary form. convert each digit into triplet form (1762.46) = 001111110010.100110

0011 1111 0010.1001 1000 = 3F2.98

***Negative numbers cannot be represented in***

(A) signed magnitude form (B) 1’s complement form

(C) 2’s complement form (D) none of the above(yes)

**Explanation:-** All of the options has both positive and negative representations

***How many 64 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?***

Assuming that 64 x 8 RAM chips means 64 x 8 bit RAM chips,Since 8 bits = 1 byte,

Each RAM chip has 64 x 1 byte = 64 bytes.

Thus the number of chips to address a memory capacity of 2048 bytes will be,

2048/64 = 32 chips.

***How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?***

A chip size is 128 x 8bit = 128 byte

For 2048 byte = 2014 / 128 = 16 chip

**How many 128×8 bit RAMs are required to design 32K×32 bit RAM?**

a) 512 b) 1024(Ans) c) 128 d) 32

Number of RAM = (32 \* K \* 32) / 128 \* 8

= 2^5 \* 2^10 \* 2^5 / 2^7 \* 2^3

= 2^20 / 2^10 = 1024

***A combinational logic circuit which is used to send data coming from a single source to two or more separate destinations is called a***

(A) decoder (B) encoder (C) multiplexer (D) demultiplexer(yes)

***If each address space represents one byte of storage space, how many address lines are needed to access RAM chips arranged in a 4 x 6 array, where each chip is 8K x 4 bits***

A. 13 B. 14 C. 16 D. 17(yes)

**Explanation1 :-**

As there are 4\*6 = 24 chips so (as 25>= 24 ) 5 bits are required to address them.

in each RAM number of bytes=(8k\*4)/8 = 4k

So to represent 4k we need(as 212=4096) 12 bits

Therefore to represent total structure we need 12+5=17 bits.

**Explanation2 :-**

Number of chips = 4 \* 6 = 24 =>To address chips need 5 bits

Chip is byte addressable and number of bytes in a chip = (8K x 4) / 8 = 210+2 = 212

=> To address bytes of chips needs 12 bits

=> So total 17 address lines need in corresponding to 17 bits.

Reference: <http://gateoverflow.in/15027/how-many-address-lines-are-needed-to-access-ram-chips>

***The opcode itself specifies all the required addresses is***

(A) indirect addressing (B) implied addressing

(C) inclined addressing (D) immediate addressing(yes)

***If F and G are Boolean functions of degree n. Then, which of the following is true ?***

(A) F ≤ F + G and F G ≤ F

(B) G ≤ F + G and F G ≥ G

(C) F ≥ F + G and F G ≤ F

(D) G ≥ F + G and F G ≤ F

**Explanation:-**

let the F & G be two boolean function of degree 1:

with degree n =2^2^n total boolean function

with degree n= 2^2^1=4 boolean function

F^1-->F & G^1-->G

F=( 4 boolean function)

G= (4 boolean function)

F+G=( 8 boolean function)

F\*G= (16 boolean function)

so answer is B

***Which one of the following is decimal value of a signed binary number 1101010, if it is in 2’s complement form ?***

(A) – 42 (B) – 22(yes) (C) – 21 (D) – 106

***If X is a binary number which is the power of 2, then the value of X&(X-1) is:***

A)11….11 B)00…..00 C)100…..0 D)000…..1

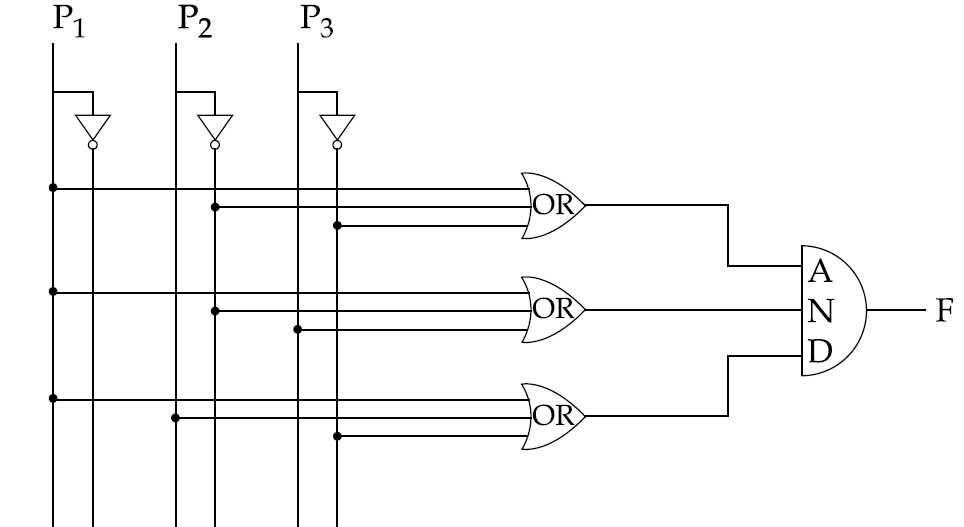
Explanation:-

let X=2^3=8=1000 then X-1=7=0111 now X&(X-1)=0000

(here & is bitwise AND= If both bits in the compared position of the bit patterns are 1, the bit in the resulting bit pattern is 1, otherwise 0)

so ans is B

***The output of the following combinational circuit is F.***



The value of F is :

(A) P +P P

(B) P +P P

(C) P +P P

(D) P +P P

Answer: (B)

Explanation: We know that (A+B)(A+C) = A + BC

ON the basis of Given question OR gates will produce output:

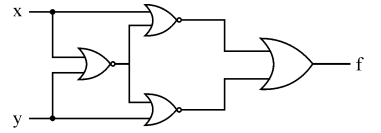
(P +P’ +P’ )

(P +P’ +P )

(P +P +P )

AND gate will take all three input produced by OR gate and generate (P + P’ P’ ) as output.

***Which logic operations is performed by the following given combinational of the following circuit ?***



A) EXCLUSIVE-OR B) EXCLUSIVE-NOR C) NAND D) NOR

**Explanation:-**

(X+(X+Y)')' + (Y+(X+Y)')'  
  
NOW USING DEMORGAN  LAW HERE   
  
X'(X+Y)+Y'(X+Y)  
  
XX'+X'Y+Y'X+Y'Y  
  
0+X'Y+Y'X+0  
  
X ex-or Y

***The simplified form of a boolean equation (AB'+AB'C+AC)(A'C'+B') is :***  
  
(1) AB'                      (2) AB'C (3) A'B                     (4) ABC  
  
**Explanation:**  
  
 =( AB' + AB'C + AC ) ( A'C' + B' )  
  
 =( AB'( 1 + C ) + AC ) ( A'C' + B' )                       [ x + 1 = 1 ]  
  
 =( AB' + AC ) ( A'C' + B' )  
  
 =( AA'B'C' + AB'B' + AA'CC' + AB'C )  
  
 =( 0 + AB' + 0 + AB'C )                                         [ x . x' = 0 ]  
  
 = AB'( 1 + C )  
  
 = AB'

**A non-pipelined system takes 30ns to process a task. The same task can be processed in a four-segment pipeline with a clock evcle of 10ns. Determine the speed up of the pipeline for 100 tasks. (2019 – Dec)**

**a)1. 5 b)2. 4 c). 3.91 d) 2.91**

**Explanation**

Speed up ratio (S):  
It is defined as the speedup of a pipeline processing with respect to the equivalent non-pipeline processing.  
  
Formula for calculating Speed up ratio is : ntn/(n+k-1)tp  
Number of tasks, n = 100  
  
For Nonpipeline:  
Time taken by nonpipeline to process a task, tn = 30 ns  
  
Total time taken by nonpipeline to process 100 task = ntn  
= 100 \* 30  
= 3000 ns  
  
For Pipeline:  
Number of segment pipeline k = 4  
Time period of 1 clock cycle, tp = 10 ns  
  
Total time requires to complete n tasks in k segment pipeline with tp clock cycle time:  
= (n + k - 1)tp  
= (100 + 4 -1)10  
= 1030  
  
Speed up Ratio:  
When total time taken by the pipeline to process 100 tasks is divided by the total time requires to complete n tasks in k segment pipeline with tp clock cycle time then speed up ratio is obtained.  
= 3000/1030  
= 2.9161  
  
So, option 4 is correct answer

Ref https://geekscompete.blogspot.com/2020/06/ugc-net-cs-2019-4-december-question-59.html

***A non pipeline system takes 50 ns to process a task. The same task can be processed in a 6 segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved. (UGC-2020-july)***

***a. 3.76 b. 4.76 c. 5.76 d. 2.76***

Explanation:

Total Number of tasks "n" = 100

Time taken by non pipeline "Tn" = 50 ns

Time period of 100 tasks = ntn

= 100 x 50 = 5000 ns

Number of segment pipeline "K" = 6

Time period of 1 clock cycle = 10 ns

Total time required = ( k + n - 1)tp

= ( 6 + 100 - 1)10

= 1050 ns

Speed up ratio " S" = 5000/1050

= 4.76

***ALTERNATE METHOD***

S= ntn/(n+k-1)tp = 100\*50/(100+6-1)\*10 = 4.76

***A non-pipeline system takes 50ns to process a task. The same task can be processed in six-segment pipeline with a clockcycle of 10ns. Determine approximately the speedup ratio of the pipeline for 500 tasks.***

a)6 b)4.95 c)5.7 d)5.5

***Explanation:-***

time for non pipeline system 1 task =50 ns 500 tasks =500x50 =25000 ns

time with k(=6) segment pipeline

first task 6x10 ns subsequent task =10 ns so 499x10 =4990

total =60+4990=5050

Speedup ratio = time taken without pipeline / time with pipeline

=25000/5050 =4.95

hence option 2) is the right ans

***The simplified SOP (Sum Of Product) form of the boolean expression (P+Q’+R’).(P+Q’+R).(P+Q+R’) is***

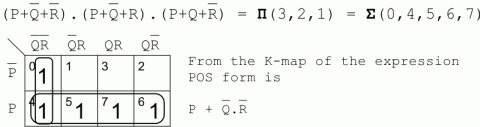
\_ \_ \_ \_

(A) (P.Q + R) (B) (P + Q.R)

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(C) (P.Q + R) (D) (P.Q + R)

Explanation:



***Consider the following boolean equations:***

***1) wx+w(x+y)+x(x+y)=x+wy***

***2) wx'(y+xz')+w'x')y=x'y***

***What can you say about the above equations ? (ugc – Dec 2018)***

(i) is true and (ii) is false

(i) is false and (ii) is true

Both (i) and (ii) are true(yes)

Both (i) and (ii) are false

***Which of the following is/are true of the auto-increment addressing mode?***

***(NET – 2018 – DEC)***

I. It is useful in creating self-relocating code.

II. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation.

III.The amount of increment depends on the size of the data item accessed.

(A) I only (B) II only (C) III Only (yes) (D) II and III only

**Explanation:** In auto-increment addressing mode the address where next data block to be stored is generated automatically depending upon the size of single data item required to store.

Self relocating code takes always some address in memory and statement says that this mode is used for self relocating code so option 1 is incorrect and no additional ALU is required So option (C) is correct option.

***Which of the following statements are true ? (NET - 2018 - DEC)***

(i) Every logic network is equivalent to one using just NAND gates or just NOR gates.

(ii) Boolean expressions and logic networks correspond to labelled acyclic digraphs.

(iii) No two Boolean algebras with n atoms are isomorphic.

(iv) Non-zero elements of finite Boolean algebras are not uniquely expressible as joins of atoms.

(A) (i) and (iv) only (B) (i) and (ii) only (yes)

(C) (i), (ii) and (iii) only (D) (ii), (iii) and (iv) only

***A computing architecture, which allows the user to use computers from multiple administrative domains to reach a common goal is called as (ISRO - 2014 )***

a)Grid Computing b)Neutral Networks c)Parallel Processing d)Cluster Computing

**Explanation:-**

Grid computing is the collection of computer resources from multiple locations to reach a common goal.

**The register that stores all interrupt requests is:**

(A) Interrupt mask register (B) Interrupt service register

(C) Interrupt request register(yes) (D) Status register

**Explanation:**

The register that stores all interrupt requests is Interrupt request register.

Interrupt mask register is a read and write register. This register enables or masks interrupts from being triggered on the external pins of the Cache Controller.

Interrupt service register handle the interrupt and service them according to priority and other condition.

Status register is a hardware register that contains information about the state of the processor