

Proteus Lab

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Section: 02

Program33

The image displays the Proteus 8 Professional interface, showing a schematic capture and the corresponding assembly source code for an ATMEGA328P microcontroller.

Schematic Capture:

- The microcontroller (U1) is an ATMEGA328P.
- It is connected to a 7-segment display (R1) via a resistor (R1).
- A DIP switch (DSW1) is connected to the microcontroller's I/O pins.
- The microcontroller's pins are configured as follows:
 - PD0/RXD/PCINT16, PD1/TXD/PCINT17, PD2/INT0/PCINT18, PD3/INT1/OC2B/PCINT19, PD4/T0/XCK/PCINT20, PD5/T1/OC0B/PCINT21, PD6/AN0/OC0A/PCINT22, PD7/AIN1/PCINT23, AREF, AVCC, ADC6, ADC7, PB0/CP1/CLKO/PCINT0, PB1/OC1A/PCINT1, PB2/SS/OC1B/PCINT2, PB3/MOSI/OC2A/PCINT3, PB4/MISO/PCINT4, PB5/SCK/PCINT5, PB6/TOSC1/XTAL1/PCINT6, PB7/TOSC2/XTAL2/PCINT7, PC0/ADC0/PCINT8, PC1/ADC1/PCINT9, PC2/ADC2/PCINT10, PC3/ADC3/PCINT11, PC4/ADC4/SDA/PCINT12, PC5/ADC5/SCL/PCINT13, PC6/RESET/PCINT14.

Source Code (main.asm):

```
.INCLUDE "m328Pdef.inc"
.DEF var_a = R16
.DEF tmp = R17

.CSEG
.ORG 0x0000
ldi var_a, 0xFF
out DDRB, var_a
ldi var_a, 0x00
out DDRC, var_a
ldi tmp, 0x00

MAIN: in var_a, PINC
andi var_a, 0x0F ; 0000 1111
ldi ZL, low(TB7SEG*2)
ldi ZH, high(TB7SEG*2)
add ZL, var_a
add ZH, tmp
lpm
com R0
out PORTB, R0
rjmp MAIN

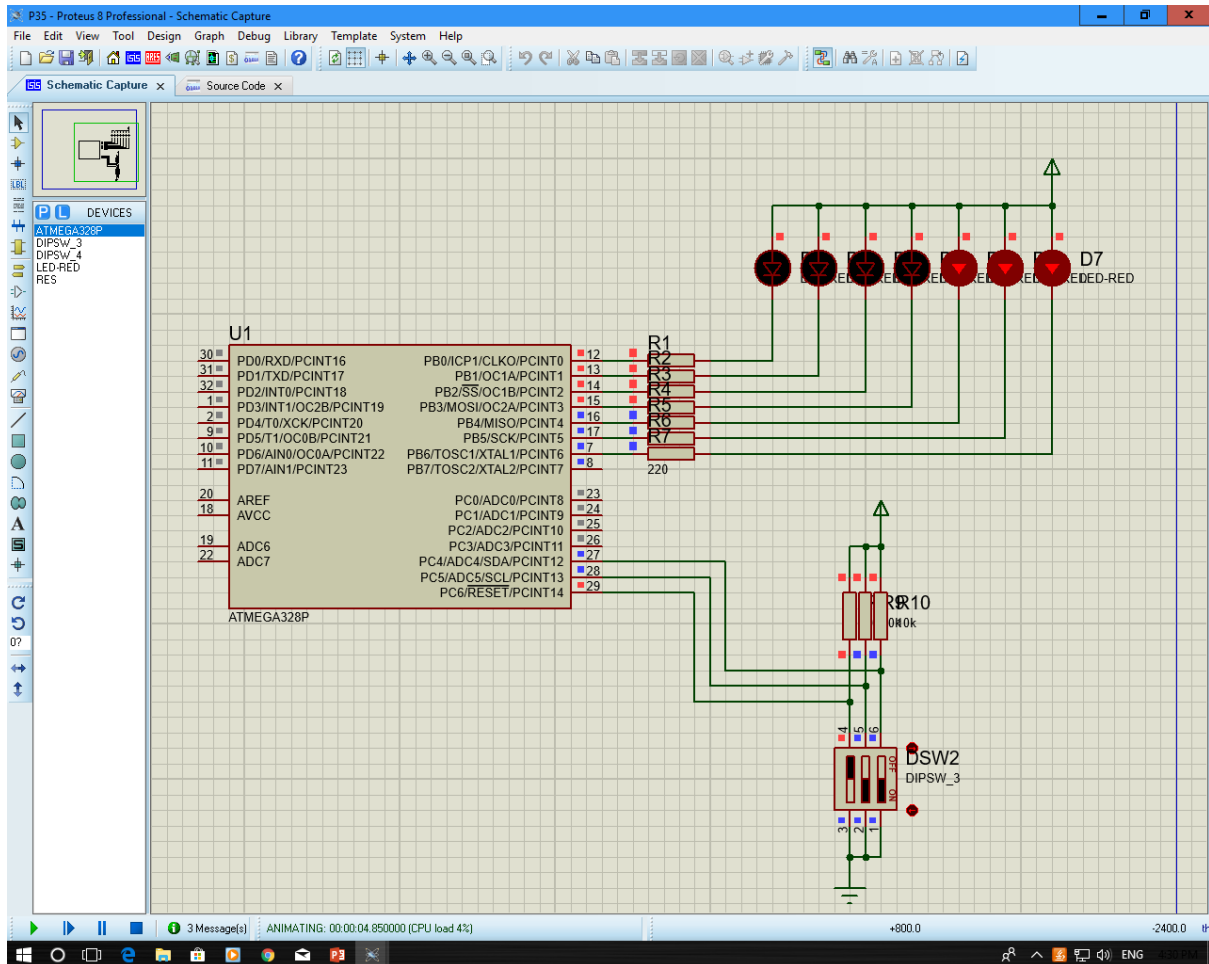
TB7SEG: .db 0b00111111, 0b00000110, 0b01011011, 0b01001111
        .db 0b01100110, 0b01101101, 0b01111101, 0b00000111
        .db 0b01111111, 0b01101111, 0b01110111, 0b01111100
        .db 0b00111001, 0b01011110, 0b01111001, 0b01110001

.DSEG
.ENDSEG
```

VSM Studio Output:

Already compiled, target is up to date.
Compiled successfully.

Program35



```

1  .include "m328Pdef.inc"
2
3  .DEF    VAR_A = R16
4  .DEF    TEMP = R17
5
6  .CSEG
7  .ORG    0x00
8
9      ldi    VAR_A, 0xFF
10     out    DDRB, VAR_A
11     ldi    VAR_A, 0x00
12     out    DDRC, VAR_A
13     ldi    TEMP, 0x00
14
15 MAIN:  in     VAR_A, PINC
16        andi  VAR_A, 0x70 ; 0111 0000
17        swap  VAR_A       ; 0000 0111
18        ldi   ZL, low(TB_LOGIC*2)
19        ldi   ZH, high(TB_LOGIC*2)
20        add   ZL, VAR_A
21        adc   ZH, TEMP
22        lpm   R10, Z
23
24        out   PORTB, R10
25        rjmp  MAIN
26
27 TB_LOGIC: .DB 0b00000000, 0b00000001
28           .DB 0b00000011, 0b00000111
29           .DB 0b00001111, 0b00011111
30           .DB 0b00111111, 0b01111111
31
32 .DSEG
33 .ESEG
  
```

VSM Studio Output

Already compiled, target is up to date.
Compiled successfully.