Folded Cascode Amplifier Design

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I. Introduction

This report details the design of a folded cascode amplifier meeting the following specifications: supply of 1.2V, load capacitance of 2pF, gain greater than 70dB, slew rate greater than 30V/µs, phase margin greater than 60, and power consumption less than 200µW. The amplifier schematic is shown in Fig. 7 at the end of this report.

II. Amplifier Design

A. Initial Calculations

The minimum value for the tail current (current through M9) can be found from the specified slew rate.

$$SR = \frac{I_{d9}}{C_L} > 30\frac{V}{\mu s}$$

$$I_{d9} > \left(30\frac{V}{\mu s}\right)(2pF) = 60\mu A$$

The maximum total current allowed by the power specification is:

$$I = \frac{P}{V} = \frac{200\mu W}{1.2V} = 167\mu A$$

This current is allocated such that approximately 70µA flows through each PMOS source transistor (M10 and M11) and 10µA flows through each of two biasing branches. The tail transistor will also be biased to carry about 70µA of current and so each input transistor will carry about 35µA. The minimum transconductance of the input transistors can be calculated based upon this current, the gain specification, and the 3dB bandwidth specification.

$$\omega_{3dB} > 2\pi \cdot 10kHz = 62.8x10^3$$

$$20\log(A_v) > 70dB \Rightarrow A_v > 3162$$

$$\omega_u = A_v\omega_{3dB} \Rightarrow \omega_u > 1.986x10^8$$

$$g_{m1} = \omega_u C_L \Rightarrow g_{m1} > 397\mu S$$

The minimum aspect ratio for the input transistors can then be calculated. Since there are no specifications for low noise, NMOS input transistors will be used in order to obtain higher gain with lower area. The value of $\mu_n C_{ox}$ was found to be $265\mu A/V^2$ in a previous lab.

$$\left(\frac{W}{L}\right)_1 = \frac{g_{m1}^2}{2\mu_n C_{ox} I_{d1}}$$

$$\left(\frac{W}{L}\right)_1 > \frac{(397x10^{-6})^2}{2(265x10^{-6})(35x10^{-6})} = 8.5$$

An approach similar to Example 9.6 in the Razavi textbook was used to calculate the aspect ratios of the remaining transistors. Overdrive voltages were guessed and used to calculate the aspect ratio. Assumed overdrive voltages were 0.15V for M3, M4, M5, M6, M7, M8, and M9, and 0.3V for M10 and M11. Given these values, the aspect ratios are as follows.

$$\left(\frac{W}{L}\right) = \frac{2I_d}{\mu C_{ox} V_{ov}^2}$$

$$\left(\frac{W}{L}\right)_{3,4,5,6} = \frac{2(35x10^{-6})}{(265x10^{-6})(0.15)^2} \approx 12$$

$$\left(\frac{W}{L}\right)_{7,8} = \frac{2(35x10^{-6})}{(126x10^{-6})(0.15)^2} \approx 25$$

$$\left(\frac{W}{L}\right)_{9} = \frac{2(70x10^{-6})}{(265x10^{-6})(0.15)^2} \approx 23$$

$$\left(\frac{W}{L}\right)_{10,11} = \frac{2(70x10^{-6})}{(126x10^{-6})(0.3)^2} \approx 12$$

Using these initial values, the amplifier was then implemented and simulated in Cadence. Based upon these simulations, transistor sizes were fine-tuned in order to achieve a gain slightly above the specification with a reasonable area.

The biasing branches were designed through experiments in Cadence. The sizes were kept as small as possible while maintaining the desired operating points. The final total widths, lengths, and number of fingers for all transistors are shown in Table 1.

B. Layout

The goals in the layout were to minimize area, keep current flow in one general direction, have as much symmetry as possible, and use as few metal layers as possible.

The current flow direction is from top to bottom. The PMOS source transistors (M10 and M11) are at the top of the layout. Below them, the input transistors are in the center with the remaining transistors to their sides. The biasing transistors are on the left side of the amplifier.

The layout passes both DRC and LVS checks. The total layout width is 4.7µm and height is 4.215µm, giving an area of $19.81\mu m^2$. Two metal layers were required to complete the layout.

The amplifier layout is shown in Fig. 8.

TABLE 1. TRANSISTOR SIZES.

Transistor	Width (µm)	Length (µm)	Fingers
M1,2	5.5	0.1	11
M3,4	2	0.25	2
M5,6	2.4	0.25	3
M7,8	3	0.25	3
M9	1.75	0.05	2
M10,11	3.7	0.1	2
M12,13	0.25	0.05	2
M14,15	0.51	0.05	3
M16	0.51	0.1	3
M17	0.5	0.1	2

III. RESULTS

All simulated design metrics are shown in Table 2.

A. *AC Analysis*

AC analysis was used to find the gain and phase margin of the amplifier. The inputs of the amplifier were both connected to a DC common mode source set at 700mV. Each input was also connected to a sinusoidal AC source of opposite phase to produce a differential input. The AC sources were set up with AC magnitude of 1V, amplitude of 10mV, and frequency of 5kHz.

The simulation was run over frequencies from 1Hz to 10GHz. The simulation showed a gain of 75.069dB, 3dB bandwidth of 19.6kHz, and phase margin of 87°. The AC analysis simulation results are shown in Fig. 1.

TABLE 2. DESIGN METRICS.

Gain	75.069dB
3dB Bandwidth	19.6kHz
Slew rate (rising)	35.5V/µs
Slew rate (falling)	33.3V/µs
Phase margin	87°
Power consumption	193.2µW
Area	19.81µm^2

B. *Transient Analysis*

A transient analysis was performed to observe the input and output waveforms as well as measure the slew rate. To observe the input and output waveforms, the same setup from the AC analysis was used. The results of this simulation are shown in Fig. 2.

To measure the slew rate, input 2 was connected to a common mode source with no AC component. Input 1 was connected to a pulse source to generate a square wave input. The square wave varied from 0V to 1.2V (V_{DD}) with a rise and fall time of 10ps. The results of this simulation are shown in Fig. 3.

The slew rate is the slope of the output curve in Fig. 3. The Cadence calculator was used to take the derivative of this curve. This result is shown in Fig. 4. This output shows that the slew rate is about 35.5V/µs for the rising transition and 33.3V/µs for the falling transition.

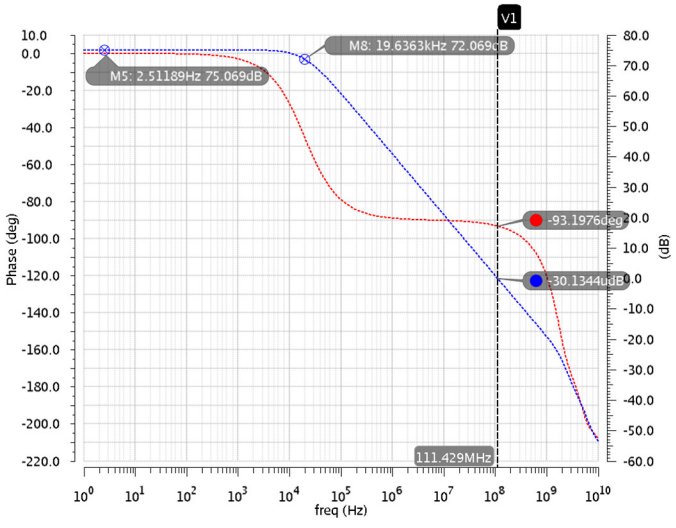

Fig. 1. AC analysis results showing gain, 3dB bandwidth, and phase margin. Gain is shown in blue and phase is shown in red.

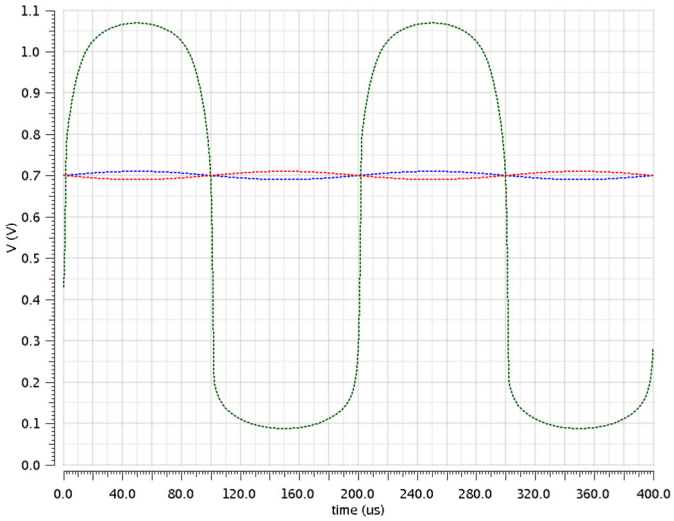

Fig. 2. Transient analysis showing input and output waveforms.

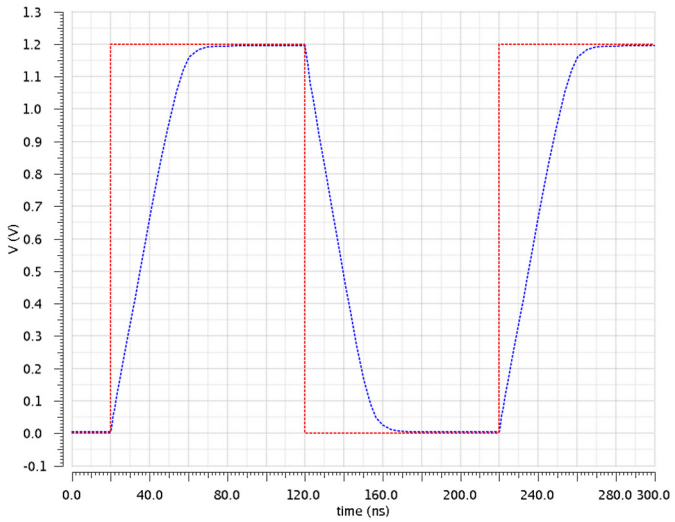

Fig. 3. Transient simulation used to measure slew rate. Input 1 is shown in red and the output is shown in blue.

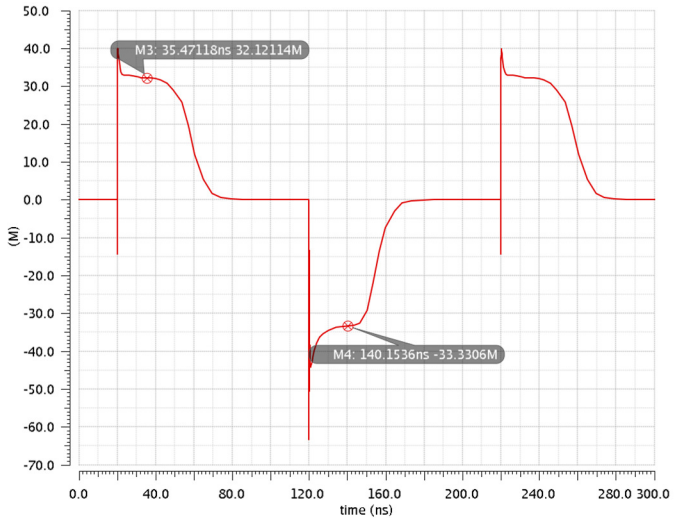

Fig. 4. Derivative of output curve from transient simulation for slew rate measurement.

C. *Power Analysis*

The circuit setup for power and noise analysis were identical to that used for AC analysis. The power was measured by running a DC simulation to find the current leaving the V_{DD} source and multiplying by the value of V_{DD}. The simulated current was 161µA. Multiplied by V_{DD} of 1.2V, this gives a power consumption of 193.2µW.

D. *Noise Analysis*

The results of the noise analysis are shown in Fig. 5 and Fig. 6. MOSFET flicker noise is of the form:

$$V_n^2 = K\left(\frac{1}{f}\right)$$

The coefficient K can be found from the value of the noise at a frequency of 1Hz. From the left marker in Fig. 5, the flicker noise coefficient is 181.3pV^2. From the right marker in Fig. 5, the thermal noise level is 113.4aV^2/Hz. The corner frequency

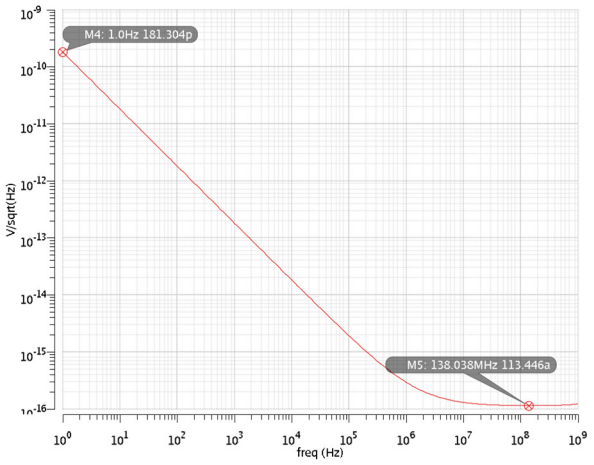

Fig. 5. Squared input noise.

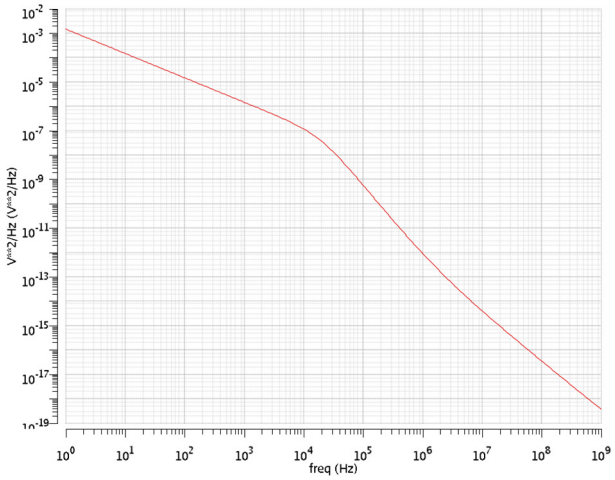

Fig. 6. Squared output noise.

can be calculated from the intersection of the flicker noise and thermal noise.

$$113.4x10^{-18} = 181.3x10^{-12}\left(\frac{1}{f_c}\right)$$

$$f_c = \frac{181.3x10^{-12}}{113.4x10^{-18}} \approx 1.6MHz$$

This value appears to match well with the corner of the input squared noise plot.

IV. Conclusion

This report has described the design and layout of a folded cascode amplifier meeting various specifications. Hand calculations were performed to find starting values for currents and transistor sizes. Cadence Virtuoso was used to fine tune the amplifier and simulate its operation.

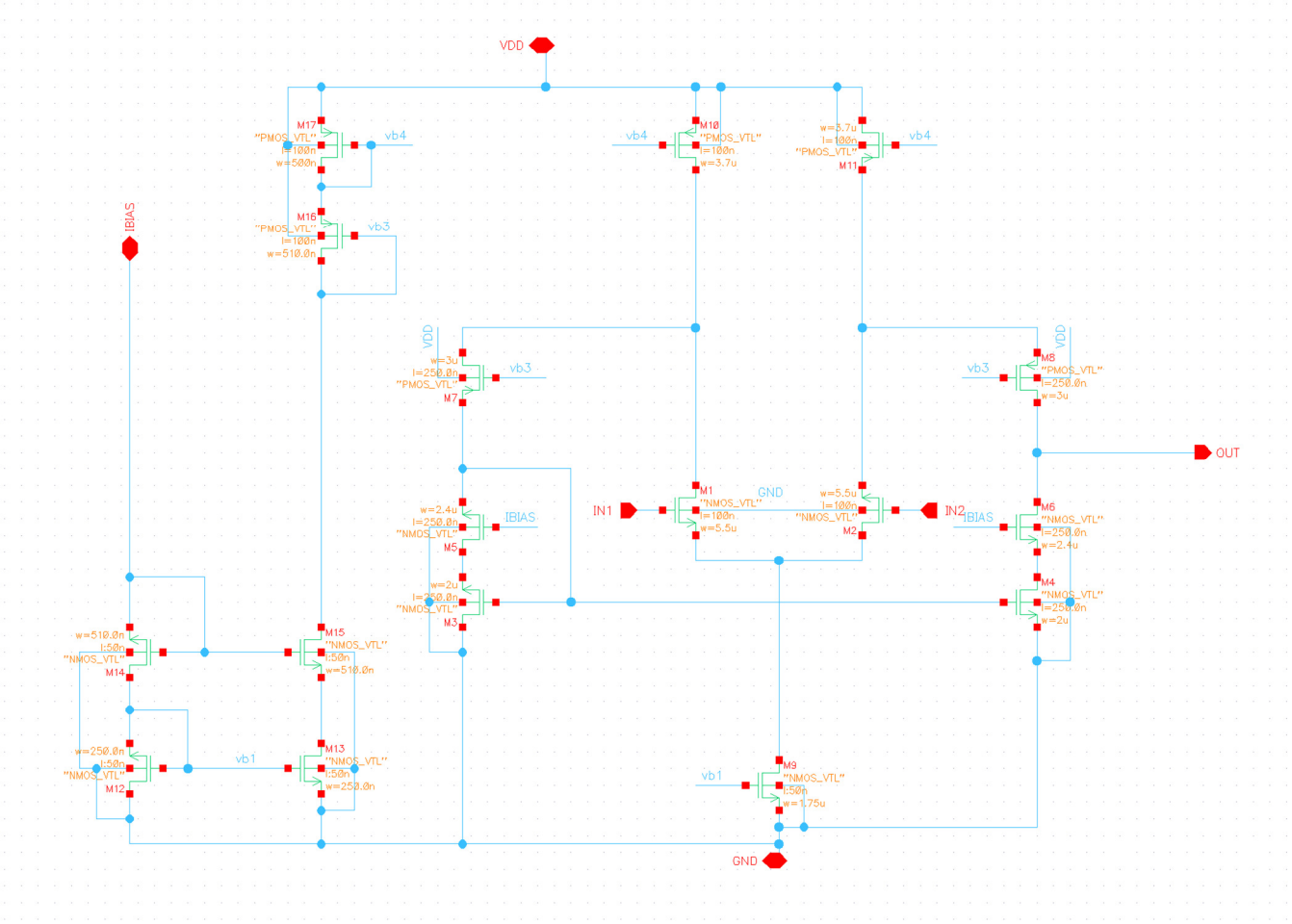

Fig. 7. Schematic of folded cascode amplifier.

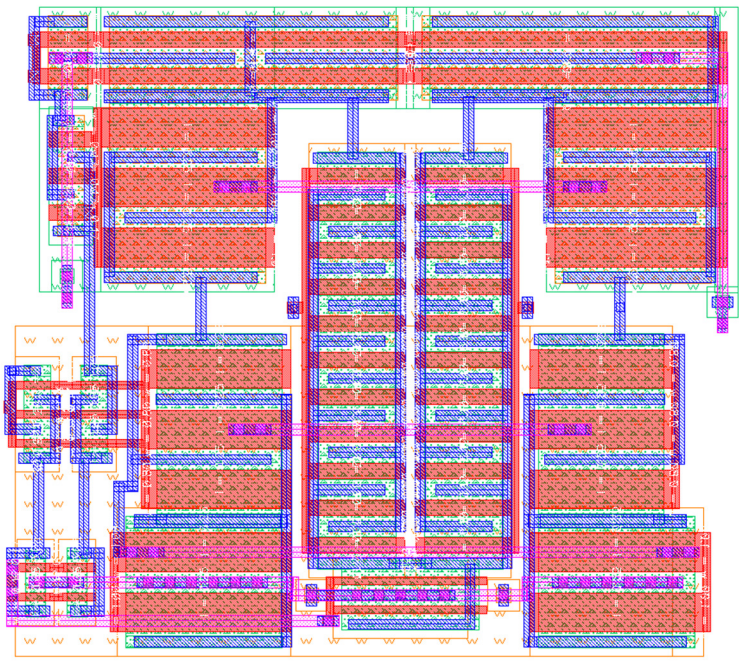

Fig. 8. Amplifier layout.