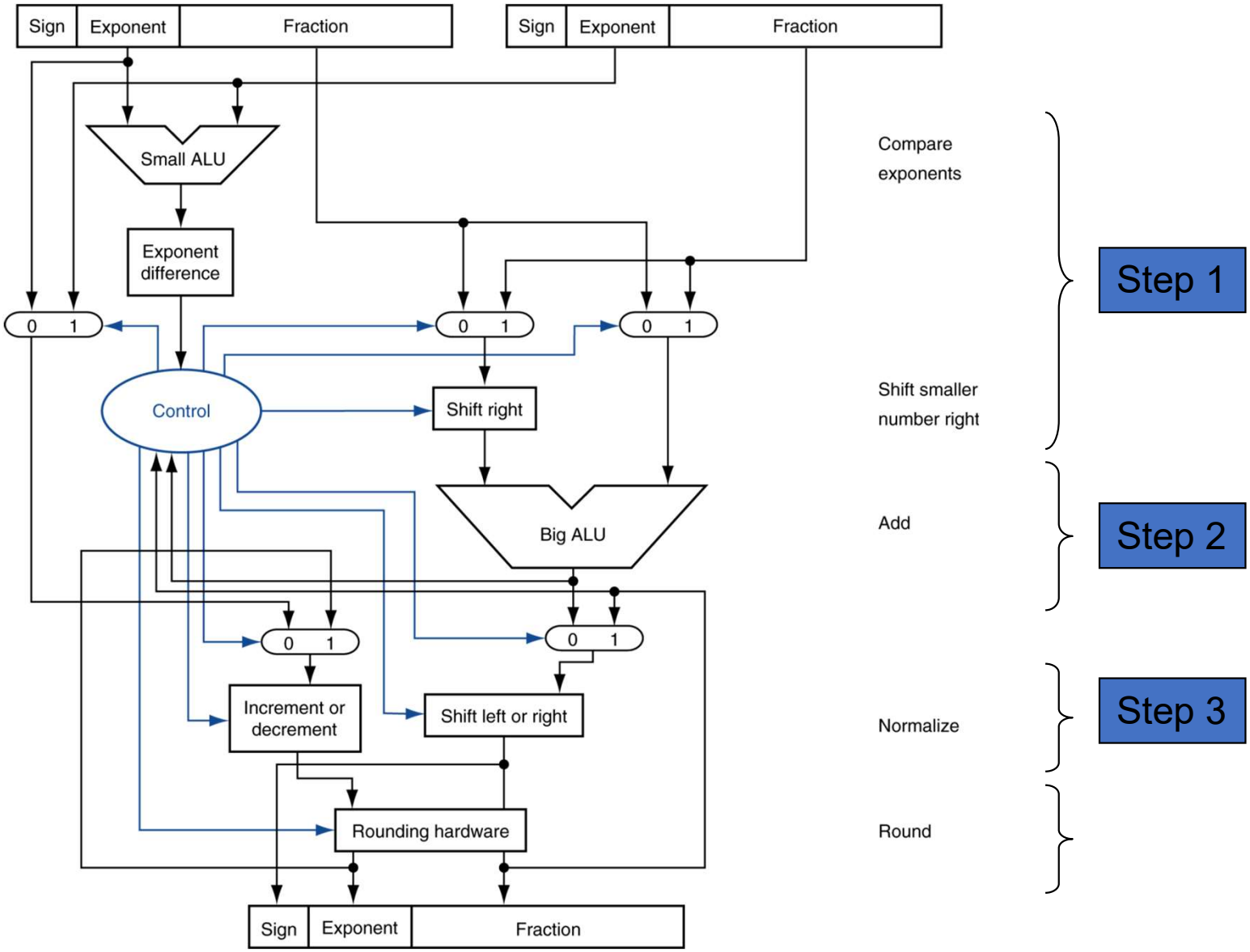
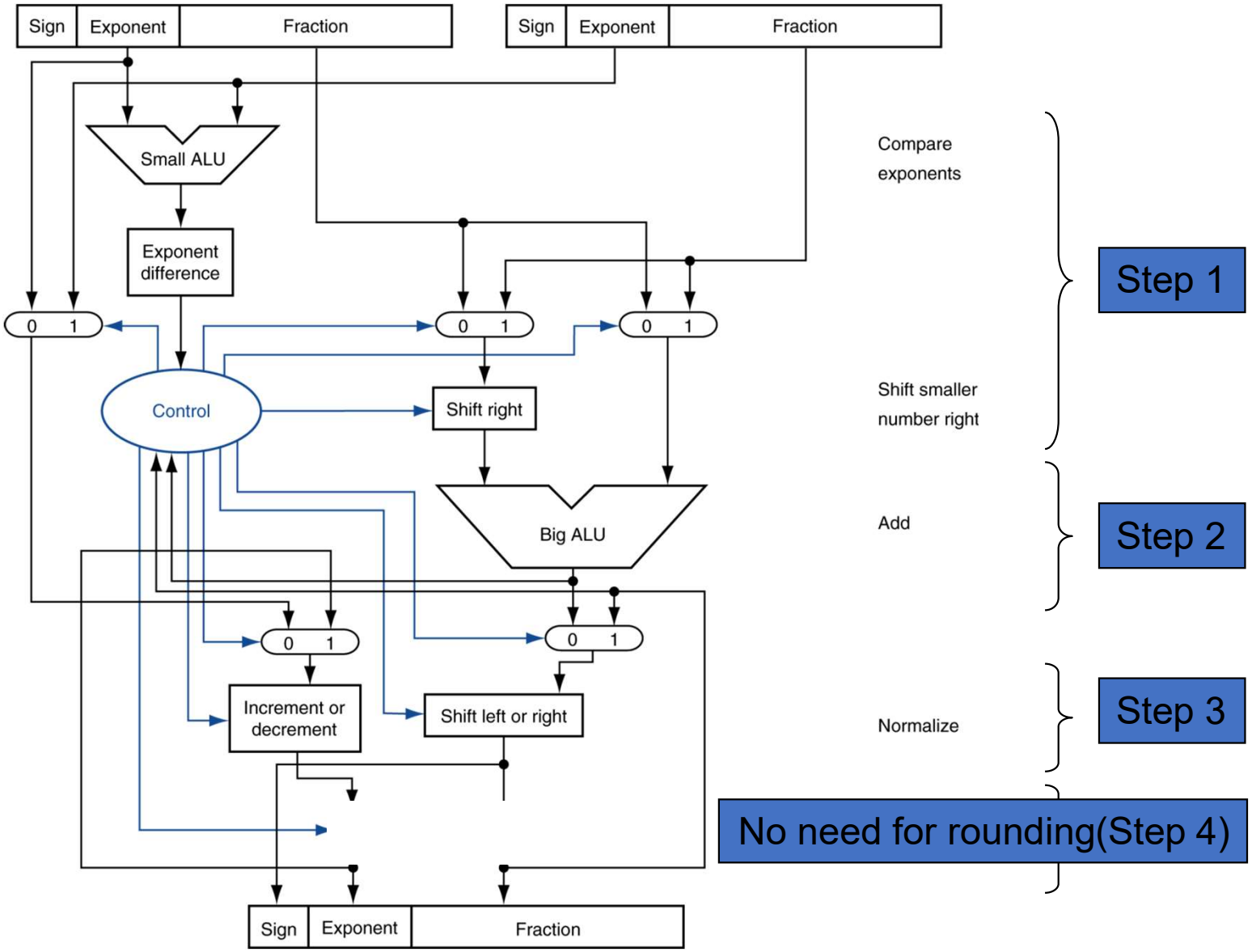
Final Project

2/3-stage Pipelined Single Precision Floating Point Adder without Rounding in VHDL/Verilog

Original Design (Chapter 3 - Slide 30)



What You Implement



Description

- Design and implement a 2/3-stage Pipelined Single Precision Floating Point Adder without Rounding in VHDL/Verilog
- The design should enable consecutive execution of floating-point addition for single precision numbers, so that it offers the speed-up of 2 or 3
- You can work in a team of 2.
- You submission should include
  - Your VHDL/Verilog code. The implementation should be in the Structural Modeling style, not the behavioral modeling style. Each part of code needs to be explained.
  - A testbench engaging the adder for 100 different input values.
    - Input values should be numbers with various combination of negative and positive numbers with different non-zero exponents and fractions
    - A new set of inputs is fed to the adder per clock cycle
  - Waveform showing the correct operation of the adder
  - Speed-up analysis by measuring the number of completed addition over time against non-pipelined implementation.
    - You don’t need to realize the non-pipelined implementation.