

~~Latches & Shuts~~

~~Interfacing~~

~~Microprocessor~~

Ex →

1)

2)

3)

Number

Complement are used in the digital computers in order to simplify the subtraction operation and for the logical manipulation.

21/08/19

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Digital Electronics/ System → It is combination

of devices that are designed to manipulate physical quantity of logical information that are in the form of digital or discrete. Digital computer, Digital Audio & video fields.

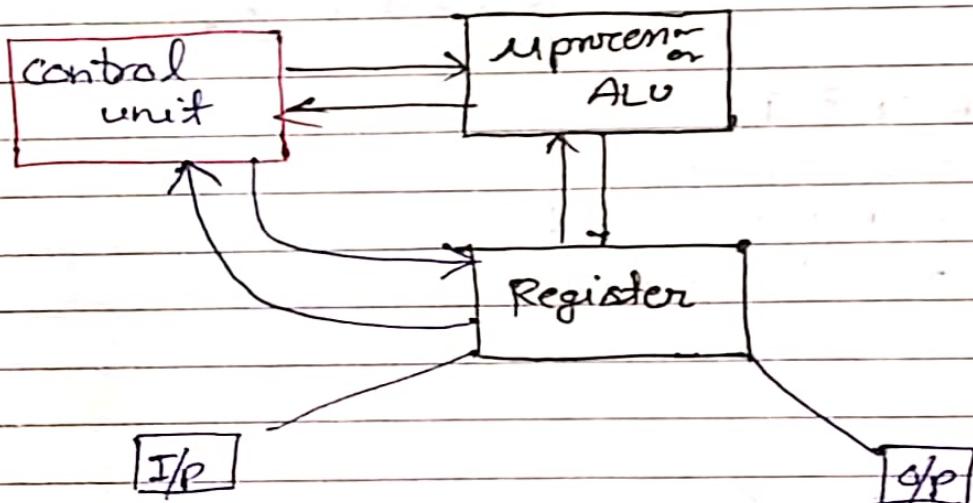
Advantage of Digital system

Packaging density is high

Easy to design

D.S takes less memory

{ Microprocessor is the key part of D.S.



Number System → Positional & Non-positional Number System

What is the significant of the complement?

Codes → Weighted code

→ Non weighted code

BCD
Gray

~~Weighted → 7421, 5421, 5211, 4211, 2421, 7421~~

Non weighted code → Excess-3 code

→ Gray

→ Alphanumeric

→ ASCII

→ EBCDIC

→ Hollerith code

→ Error detecting code (Parity)

→ Error detecting and correcting code
(Hamming code)

→ Self complementary & reflective code
↳ $5211 = 9$ effecting

Sum = 9 must

Ex-

8421.

0000 → 0

0111 → 1

0110 → 2

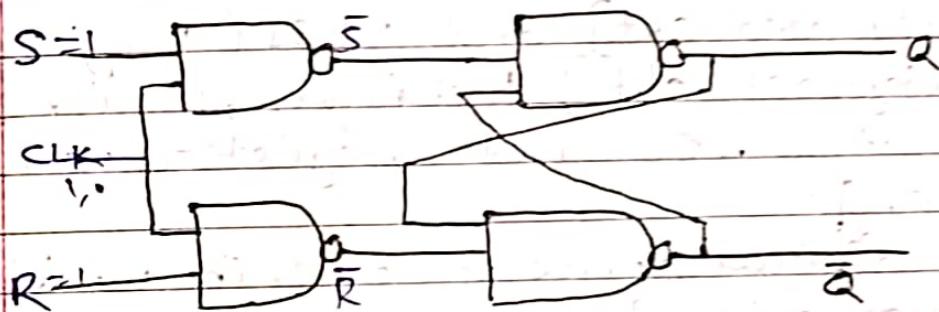
1000 → 8

1111 → 9

FF → Flip Flop → It is a memory element which is capable of storing one bit of information. It is used in clocked sequential ckt.

→ A FF is also known as bistable multivibrator.

To make FF NAND or NOR Gate are used.
Type of Flip-Flop → SR, JK, D, T



Microprocessor

A Microprocessor is an important part of a computer architecture without which you be able to perform anything on your computer system.

- It is a programmable device.
- MP is the semiconductor (Digital) device, that is manufactured by the LSI [large scale integrated ckt] and VLSI (Very Large Scale Integrated ckt) techniques, which includes ALU., CU and register on a single chip.
- It is a digital device on a chip which can fetch instruction from memory, decode and execute them and give results.

Basic of MP → A MP takes a bunch of instruction in machine language and executes them, telling the processor what it has to do.

Microcontroller - MC is a semiconductor device that can be manufactured by LSI & VLSI technique that includes MP along with external peripheral such as Input & o/p on a single chip.

Historical Development of MP

MP	year	word length	memory capacity
----	------	-------------	-----------------

MP	year	word length	memory capacity
Intel(Pmos) 4004	1971	4 bits	640 B
Intel 8008	1972	8 bits	16 Kb
8080 n-mos	1973	8 bits	64 Kb
8085 (n-mos)	1976	8 bits	64 Kb
Intel 8086(H-mos)	1978	16 bits	1 MB
Intel (8088)	1980	8/16 bits	1 MB
Intel (80186)	1982	16 bits	1 MB
Intel 80286	1983	16 bits	16 MB (real) 4 GB (virtual)
Intel 80386	1983	32 bits	4 GB real 4 GB virtual
INTEL 80486	1989	32 bits	4 GB (real) 64 Tb (virtual)
Pentium-1	1993	64 bits	64 GB real
Pentium-2	1997	64 bits	64 GB real
Pentium-3	1999	64 bits	64 GB real
Pentium-4	2000	64 bits	4
Pentium M	2001	64 bits	64 GB Real.

Word Length → The number of bits that can be processed by a MP is termed as word length of the MP. Word length of 8085 is —8 bits

Basic Terminology in MP

- Nimonic → (ADD)
- Programming
- Machine Language
- Assembly Language
- Low Level "
- High Level "
- Compiler, "

Processor 8085

It is 8-bit MP designed by INTEL using NMOS Technology.

- It has following configuration
 - .) 8 bit Data bus
 - *) 16-bit address bus, which can address upto 64 KB
 - .) A 16 bit program counter.
 - .)

Address Bus → It is a group of 16-lines i.e. $A_0 - A_{15}$. It is unidirectional i.e. bits flow in one direction from the MP unit to the peripheral devices and uses the high order address bus.

Control Line:- (Bidirectional)

Control line or unit is the bidirectional which basically generated timing and controlling signal.

Opcode & operand → An opcode is a single instruction that can be executed by the CPU. The opcode is the Mov instruction. The other parts are called the 'operands'. Operands are manipulated by the opcode.

Possible operand types in MP:

- i) Byte and short → 8 bit variable
- ii) Word and Integer → 16 bit variable.
- iii) Double word, long integer → 32 bit variable.
- iv) String - series of bytes or series of word which is generally stored in memory location.
- v) Nibble: 4 bit unit.
- vi) byte word or double word - these are unsigned operands.
- vii) Integer, short & long → Signed operands.
- viii) Compiler → Assembler → The compiler is a simple program which converts the source code written by the humans to a machine language. While the assembler has a little different work, it converts the assembly

(3c) ALU → Harvard latch enable

Used to 8 bit address of line AD₁-AD₇ into
an external latch.

Date: / /

language to the machine language.
Compiler works more directly than the
assemblers.

Control & Timing Unit → The control and timing
unit coordinates with all
the actions of the MP by the clock and
gives control signals which are required
for communication among the MP as
well as peripherals.

8085 PIN Description.

- 1) Von Neumann Architecture:
- 2) Harvard Architecture

The difference is that Von neumann Architecture
has common memory space for data and
instruction while in Harvard it has
separate memory for data and instructions.

→ Program & Data can stored in same
memory location ex- 8085, 8086

Von-Neumann

⇒ 2) 8085

⇒ 8085 has 40 pins

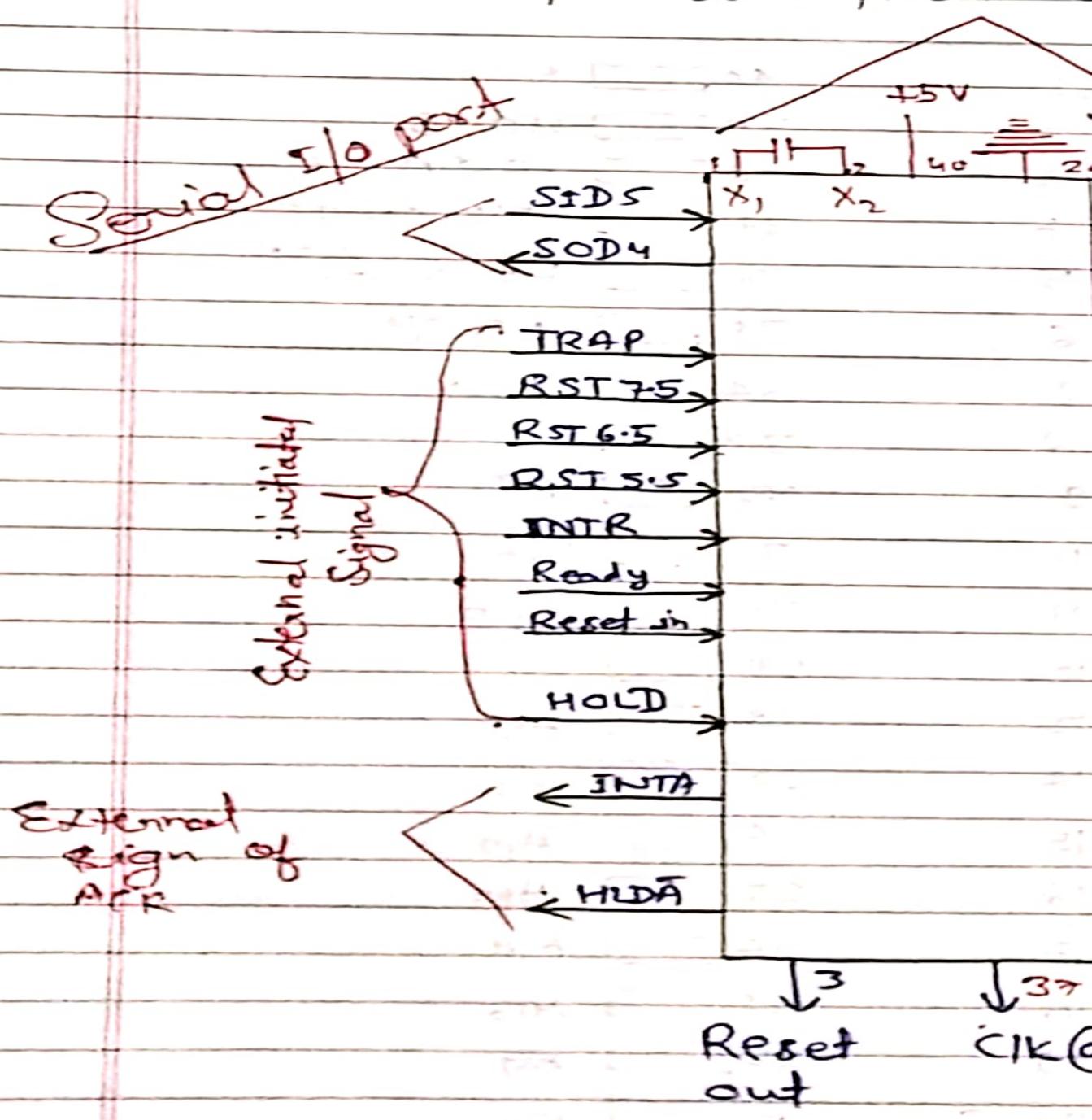
Pin Diagram of 8085 μP

X_1	1	40	Vcc
X_2	2	39	HOLD
RESET OUT	3	38	HLDA
SOD	4	37	CLK (COUT)
SIO	5	36	RESET IN
TRAP	6	35	READY
RST 7.5	7	34	IO/M'
RST 6.5	8	33	S
RST 5.5	9	32	RD
INTR	10	31	WR
INTA	11	30	ALE
AD ₀	12	29	S ₀
AD ₁	13	28	A ₁₅
AD ₂	14	27	A ₁₄
AD ₃	15	26	A ₁₃
AD ₄	16	25	A ₁₂
AD ₅	17	24	A ₁₁
AD ₆	18	23	A ₁₀
AD ₇	19	22	A ₉
V _{SS}	20	21	A ₈

Exact Pin Description of 8085 μP -

The O/P pins are $A_8 - A_{15}$ (8 pins), $AD_0 - A_7$, RD, WR, HLD \bar{A} , INTA, RESET OUT, CLK.

General Pin description



Key feature of 8085

- (1) It is a 8 bit processor
- (2) It has 8 data bus line

8085

AD7 (8 pins), ALE, S₀, S₁, RD_Y,
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of 8085

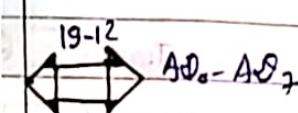
powersupply

V_{SS}

20

28-21

A₀ to A₁₅



30

29 → S₀

33 → S₁ Control & Status
34 → IO/m Signal

32 → RD

31 → WR

(out)

- bit capacity of M.P.
- It has total 16th address line which addressing capacity is 64K.
- The crystal frequency of processor is 6 MHz and the clock frequency is $3.07 \approx (3 \text{ MHz})$ which is the half of the crystal frequency.
- $\boxed{\text{Clock frequency} = \frac{1}{2} \text{crystal frequency}}$
- lower order address bus is multiplexed with data bus in order to reduce the number of pin.
- To Demultiplex address bus from Data, ALE (address Latch Enable) signal is used if ALE=1 that means address will transfer to bus.
ALE=0 Data transfer to bus.
- Disadvantage of multiplexing is that speed will be reduced.

Serial number	Signal	Pins
1)	Power supply	V _{cc} , V _{SS}
2)	Clock signal	X ₁ , X ₂ , CLK out
3)	Reset Signal	Reset in, Reset out
4)	Interrupt Signal	TRAP, Restart, INTR, INTX (Interrupt RST, 7.5, 6.5, 5.5)

c, which is the

~~Microprocessor~~

Pins

5)	Address bus & Data Bus	A ₀ -A ₁₅ and AD ₀ -AD ₇ ,
6)	Status signal & Control signal	ALE, I _O /memory S ₀ , S ₁ , Read (RD), WR, Ready.
7)	Serial I/O Signal	SIO, SAS
8)	DMA Request Signal	HOLD & HLDA

- 1) Address Bus
- 2) Data Bus
- 3) Control Bus
- 4) System Bus

i) Bus is a group of wires or conductor that is used for communication b/w MP, memory, I/O device, peripheral.

A) Address Bus: Group of conducting wires which carries address only. Address bus is unidirectional because data flow in one direction, from MP to memory or from MP to I/O devices.

Length of address Bus of 8085 MP is 16 Bit
 → It is defined as maximum no. of memory that can be connected with MP.

$$2^n = N$$

ii) Data bus: It carries Data only. It is used to transfer data b/w MP, memory, peripheral. Bidirectional. Data flow in both direction

DMA allows data transfer between source and destination thus bypassing the MP.

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from MP to memory or I/O devices and from memory or I/O devices to MP.

Control Bus :- It is a group of control signal required for various operation of the MP. It is used to generate timing and control signals to control all the associated peripherals, MP uses control bus to process data that is what to do with selected memory location. Some control signals are:

- Memory Read
- Memory write
- I/O read
- I/O write
- Opcode fetch.

Control and Status Signal

RD (Read) → When the signal is low on this pin the MP performs memory or I/O read operation.

WR (write) → When the signal is low on this pin MP performs writing operation with either memory or I/O.

I/O IO/M : This stat signal is used to give information of operation to be perform with memory or I/O devices

<u>I/O/R</u>	<u>R/W</u>	<u>I/O</u>	<u>WR</u>	<u>operation</u>
0	0	1	1	memory read (mR)
0	1	0	0	memory write (mW)
1	0	0	1	I/O read I/oR
1	1	1	0	I/O write I/oR

Status Signal \rightarrow (S_1, S_0)

<u>S_1</u>	<u>S_0</u>	<u>operation</u>
0	0	Halt (No operation)
0	1	write operation
1	0	Read operation
1	1	opcode fetch (Reading Instruction)

Power Supply $V_{cc} : +5V$, $V_{ss} \rightarrow$ It indicates ground signal

Frequency Signals $\rightarrow X_1, X_2$:

X_1, X_2 - clock out.

X_1, X_2 - A crystal (RC, LC M/H) is connected at these two pins is used to set frequency of the internal clock generator. This frequency is internally divided by 2.

Clock Out \rightarrow This signal is used as the system clock for devices connected with the microprocessor.

→ provide synchronization between CPU & peripheral

Serial I/O port → There are 2 serial signals, SIO & SOO

- i) SIO → (Serial Input Data) This pin is used for receiving the data into microprocessor by serially.
- ii) SOO → (Serial Output Data) → This pin is used for sending the data from MP by serially.

Hardware and Software Interrupts

When MP receive interrupt signals through pins (hardware) of MP, they are known as hardware interrupt.

There are 5 hardware interrupt in 8085 MP → INTR, RST 7.5, RST 6.5, RST 5.5, TRAP.

Priority order
 $4.5 > 7.5 > 6.5 > 5.5 > \text{INTR}$

Software interrupts are those which are inserted in between the program which means these are mnemonics of microprocessor. There are 8 software interrupt in 8085 MP RST0, RST1, RST2, RST3, RST4, RST5, RST6, RST7

RST0 RST1 ... RST7
 ↓ ↓ ↓ ↓
 more more more more → order

- Ans: ⇒ * Trap is edge as well as level triggered.
 - RST 7.5 is a +ve edge triggered interrupt.
 - RST 6.5 and RST 5.5 are level triggered interrupt

Vectorized and Non vectorized Interrupts

Vector Interrupts are those which have fixed vector address (starting address of subroutine) and after executing these, program control is transferred to that address.

Vector addresses are calculated by the formula

(Type

Interrupt

TRAP (RST 4.5)

RST 4.5

RST 6.5

RST 7.5

vector Address

0024 H

002CH

0034H

003CH

for software interrupts vector addresses are given by:

Interrupt

RST 0

vector Address

00H

RST 1

08H

RST 2

10H

RST 3

18H

RST 4

20H

RST 5

28H

RST 6

30H

RST 7

38H

Note: INTR is the only one non-vectorized interrupt in 8085 up

⇒ Maskable and Non-Maskable Interrupts :-
Maskable Interrupts are those which can be

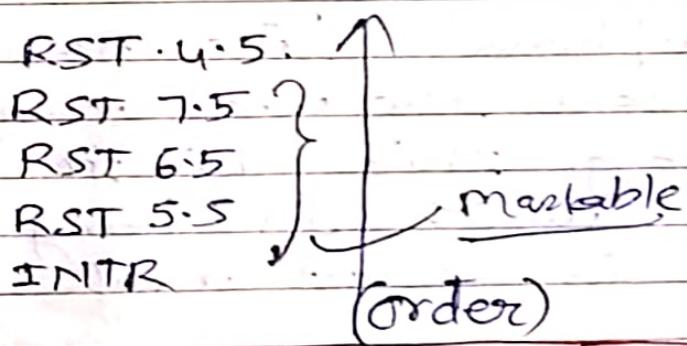
disabled or ignored by the MP. These interrupt are either edge-triggered or level triggered. So they can ~~be~~ be disabled.

INTR, RST 7.5, RST 6.5, RST 5.5 are maskable interrupts in 8085MP.

Non maskable interrupts are those which cannot be disabled or ignored by MP.

~~TRAP~~ is non maskable interrupt.

It consists of both level as well as edge triggering and is used in critical power failure conditions.



Hardware interrupt \rightarrow Software interrupt
(priority order)

RESET IN \rightarrow Reset in Low signal. When the signal on this pin is low (0), the program counter is set to zero, the buses are ~~tied~~ triated and the MP unit is reset.

RESET OUT \rightarrow It is used to reset the other peripheral devices.

Ready Signal It is used to interface to the few peripheral devices (Memory) to the MP.

It senses whether a peripheral is ready to transfer data or not.

If ready is high (1) the peripheral is ready. If it is low (0) the MP waits till it goes high. It is useful for interfacing low speed devices.

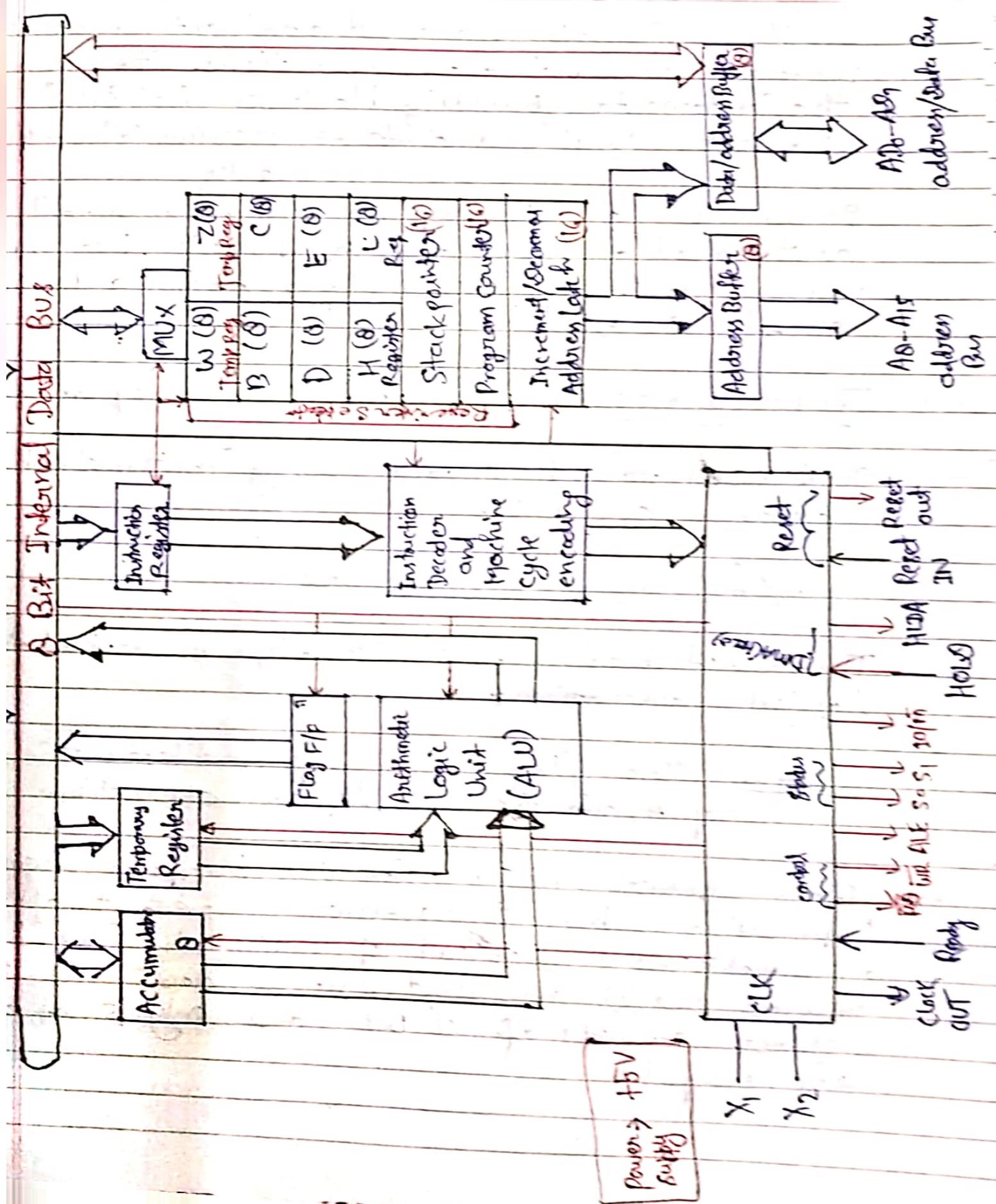
HOLD AND HLDA

Hold in a peripheral like Direct Memory Access DMA controller sends the whole request to the MP through this bus to leave the data bus which is being used by MP. It is faster method of Data transfer.

HLDA → Hold acknowledgement, by MP to peripheral.

It is a signal which indicates that the hold request has been received after the removal of a HOLD request, the HLDA goes low.

Internal Architecture of 8085 MP



ALU → An ALU is a digital ckt used to perform arithmetic & logic operations. It represents the fundamental building block of the CPU of a computer which includes → Accumulator - Program register

It is an 8 bit programmable register. All arithmetical & logical operation perform with contents of Accumulator (Acc) and results stored in Acc.

→ Temporary Register: 8-bit Non-programmable register

It is used to hold data using arithmetical & logical operation.

Arithmetic and logic Unit

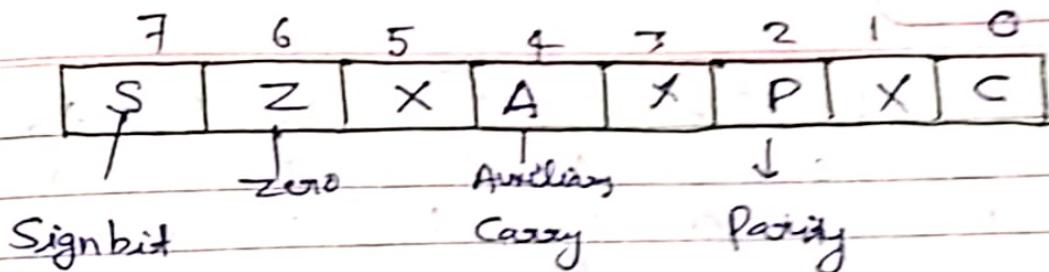
This unit perform the actually numerical & logical operations.

Flag → The flag generally reflects the status of Arithmetic and logical operation

→ Flag register is a Special purpose register. Depending upon the value of result after any arithmetic and logical operation the flag bits become Set(1) or reset(0). In 8085 CPU, Flag register consists of 8 bits and only 5 of them are useful.

Flag register (8 bits)

Date: / / Page: / /



1) D₇- Sign Flag -

D₇ - MSB = 1 \Rightarrow -ve (Set)

D₇ - LSB = 0 \Rightarrow +ve (Reset)

Ex- MVI A 30 (Load 30H in register A)

MVI B 40 (Load 40H in register B)

SUB B (A = A - B)

These set of instructions will set the sign flag to 1 as 30 - 40 is a -ve number

2) Zero Flag :- After any arithmetical or logical operation if the result is 0(00)H

the zero flag becomes set i.e 1, otherwise it becomes reset 0.

D₆ = 0 (Reset)

D₆ = 1 (Set)

3) Auxiliary Carry \Rightarrow This flag is used in BCD number system (0-9).

If after any arithmetic or logical operation D(3) generates any carry and passes it to D(4) this flag becomes Set '1', otherwise reset (0).

This is the only flag register which is not accessible by the programmer.

ALU → An ALU is a digital ckt used to perform arithmetic logic operations. It represents the fundamental building block of the CPU of a computer which includes → Accumulator + Program register.) D7

It is an 8-bit programmable register. All arithmetical & logical operation perform with contents of Accumulator (Acc) and results stored in ACC.

→ Temporary Register: 8-bit Non-programmable regit

It is used to hold data using arithmetical & logical operation.

Arithmetic and logic Unit) 2)

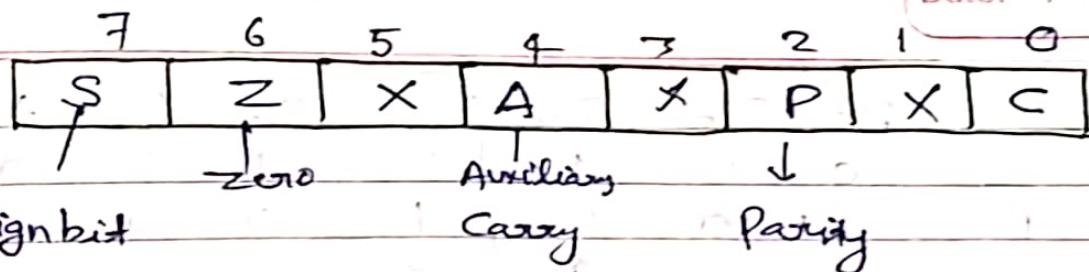
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Flag register (8 bits)

Date: / / Page: / /



7- Sign Flag

$D_7 - \text{MSB} = 1 \Rightarrow \text{-ve (Set)}$

$D_7 - \text{LSB} = 0 \Rightarrow \text{+ve (Reset)}$

Ex- MVI A 30 (Load 30H in register A)

MVI B 40 (Load 40H in register B)

SUB B (A = A - B)

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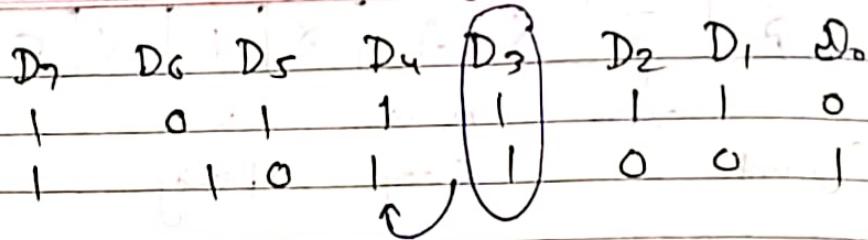
$D_6 = 0$ (Reset)

$D_6 = 1$ (Set)

Auxiliary Carry \rightarrow This flag is used in BCD number system (0-9).

If after any arithmetic or logical operation D(3) generates any carry and passes it to D(4) this flag becomes Set '1', otherwise reset (0).

This is the only flag register which is not accessible by the programmer.



Import

Imp-2

Ex- MOV A 2B (load 2BH in register A)

MOV B 39 (load 39H in register B)

ADD B (A = A + B)

⇒ Parity Flag → If after any Arithmetic or logical operation the result has even parity, an even number of 1 bits, the flag is Set, otherwise Reset.

→ Carry Flag (Cy) → Carry is generated when performing n bit operations and the result is more than n bits, then this flag becomes Set 1, otherwise it becomes reset 0.

→ During subtraction (A - B), if A > B it becomes reset and if (A < B) it becomes set.

Carry flag is also called borrow flag.

Ex- 57 → 01010111

$$\begin{array}{r} + 96 \\ \hline \end{array}$$

$$\begin{array}{r} 10010110 \\ \hline 11101101 \end{array}$$

(ii)

1 1 1
(iii)

S = 1

Z = 0

AC = 0

P → 1

Cy = 0

short points → In each and every instruction
not all flag affected at same time

2) Among the 5 flag, AC flag is used internally for BCD Arithmetic operation.
The instruction does not includes any conditional jump instruction wait on the AC Flags.

X is the flag register unused flip-flop.
The value of D_1, D_2, D_3 bits should be taken as 0 in the program while use PSW instruction. program state word

Register Array

Temporary DR - It is also called as opend registers (8 bit).
It provides operands to the ALU.

TR → (w,z) : This register is not available for users. It is internally used by MP for the internal operation.

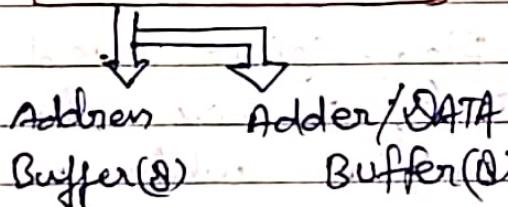
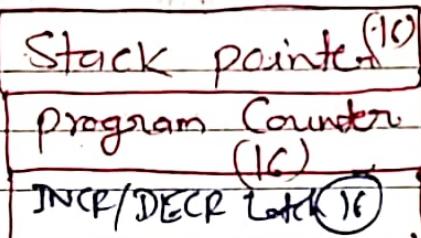
General purpose Register : 8085 MP

consists 6 types of register : 8 bit register GPR. That is B, C, D, E, H, L. These are available for users. 8 bit each.

→ GPR Put together is called scratch or memory BC, DE, HL → Hold data

(4) Special Purpose Register 8085 up

provide 2, 16 bit SPR. That is - PC and Stack pointer.



(a) Program Counter \rightarrow It is 16 bit register used to hold next memory address while the execution of the program.

(b) Stack pointer \rightarrow A stack is nothing but the portion of RAM.

\rightarrow It works on the LIFO concept.

\rightarrow Stack pointer maintains the address of the last byte that is entered into stack.

\rightarrow Each time when the data is loaded into stack, stack pointer gets decremented.

Timing And Control Units

\rightarrow Instruction Register and Decoder

\rightarrow IR - Hold the opcode of the instruction that is decoded and Instruction

Decoder \rightarrow The o/p of IR, connected to the Decoder :: The Decoder Decodes the Instructions and establishes the sequence of events.

Interrupt Control Unit

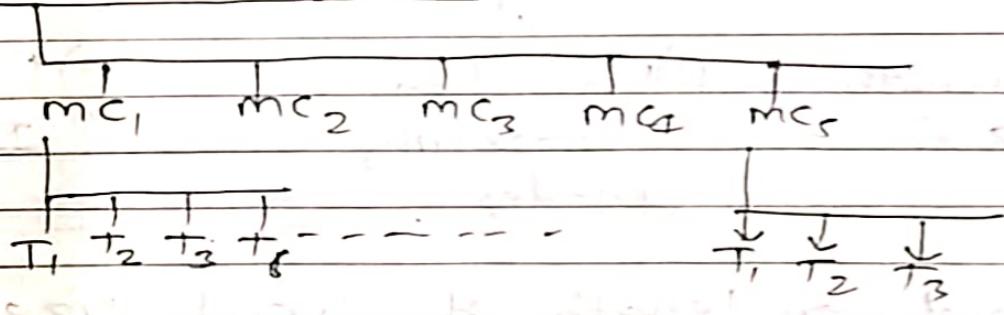
Instruction Set and Data format

Timing diagram related -

Instruction cycle \rightarrow Fetch cycle + Execution cycle
 (1 to 5 machine cycles) (opcode fetch)

Instruction cycle \rightarrow The CPU fetches one instruction from memory at a time and execute it - one instruction cycle make consists 1 to 5 machine cycles.

Instruction Cycle

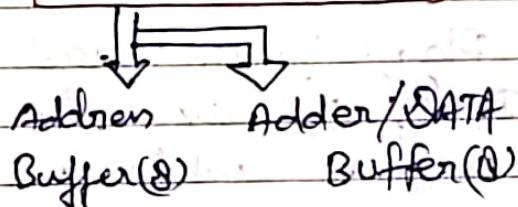
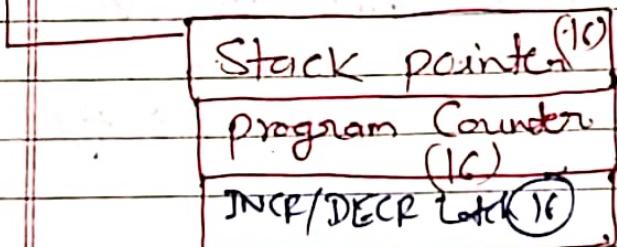


Machine Cycle \rightarrow Time required by the CPU to complete the operation of accessing memory or I/O device is called as MC.

\rightarrow Machine cycle consists 3 to GT state.

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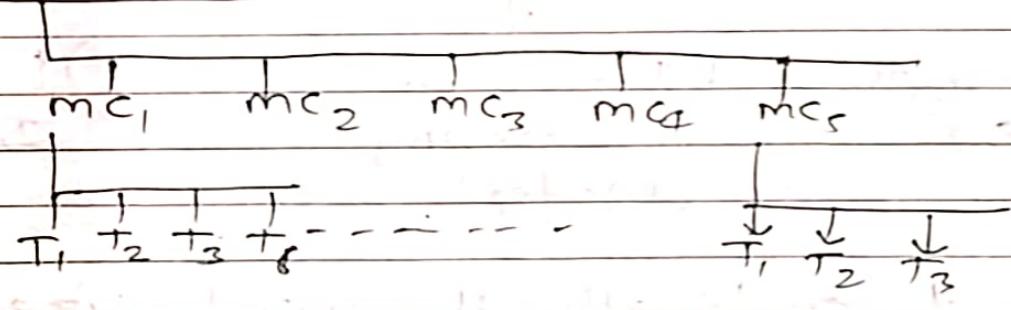
Instruction Set and Data format

Timing diagram omitted

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Instruction Cycle



Machine Cycle \rightarrow Time required by the CPU to complete the operation of accessing memory or I/O device is called as MC.

\Rightarrow Machine cycle consists 3 to GT state.

another words \Rightarrow It is nothing but simply read or write operation.

Imp: Different types of M.C. are:

- i) Opcode fetch MC \rightarrow required 1 to 6 T state
- (ii) Memory read (3T)
- (iii) Memory write (3T)
- (iv) I/O read (3T)
- (v) INTR Acknowledgement (3T)
- (vi) Bus Id (3T)

Note 1st Machine cycle in any instruction in opcode fetch cycle.

Classification of Instruction Set of 8085

Instruction Set

- A) Based on length of word size
- B) Based on Addressing modes
- C) Based on Operation Instruction

A) Based on length of word size -

- \rightarrow one byte length
- \rightarrow Two byte length
- \rightarrow Three byte length

- \rightarrow Register addressing mode
- \rightarrow Immediate " "
- \rightarrow Direct " "
- \rightarrow Indirect " "
- \rightarrow Implicit " "

I.S. → Instruction Set

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Based on Operation Mode.

Data transfer

AU operation

Logical operation

Branch control

Stack, I/O, And Machine control.

1 byte Instruction Sets In 1-byte instruction, the opcode and the operand of an instruction are represented in one byte. These instruction required single memory location.

func - Add the contents of AC to the contents of reg B

Mnemonic - ADD B

opcode - ADD

Operand - B

Hex code - 80H

Binary code - 1000,0000

2 byte - I.S. It uses 1 byte to specifies the operation (opcode) and 2nd byte specifies to the operation data these instruction required two successive memory location in the memory. 1st byte - opcode & 2nd byte - operand

3 byte - I.S. It 1st byte store opcode (operation to the perform, 2nd byte store lower order 8 bit of 16 bits data, and 3rd byte store higher order 8 bit or 16 bit store.

opcode

Low byte
data/address

High byte
data/Address

B(i) Register addressing Mode :- In this

addressing mode the source and destination are general purpose register.

Ex → MOD A, B → Move the content of B register to A register.

ii) Immediate Addressing Mode :- In this mode

the data is specified in the instruction itself.

Ex → MVI B, 3EH. - Move the data 3EH given in the instruction to B register.

(iii) Direct addressing Mode - In this mode 16

bit address of the operand is given within the instruction itself.

The address of the data is specified in the instruction directly.

Ex - LDA .1050H. - Load the data available in memory location 1050H in Accumulator.

(iv) Indirect addressing Mode :-

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