A Fast Transient LDO Based On Dual Loop FVF With High PSRR

Lei Wang[1], Wei Mao[2],Chundong Wu[1,3], Alan Chang[1] and Yong Lian[4]
[1]NXP Semiconductors Singapore Pte Ltd
[2]ECE Department, National University of Singapore
[3]School of Electronic and Electrical Engineering, Nanyang Technological University, Singapore
[4]School of Microelectronics, Shanghai Jiao Tong University
wleiece@gmail.com

***Abstract*—In this work, the design of a dual loop flipped voltage follower (FVF) based low-dropout regulator (LDO) to achieve fast transient response is proposed for all-digital phase locked loop (ADPLL) in the RFID application. With the help of an additional reference generation loop in FVF LDO and the cascaded structure, high power supply rejection ratio (PSRR) is achievable. This design is fabricated in GF 40nm CMOS technology. The FVF LDO core only occupies small area of 0.036 mm^2. This area also includes 80pF on chip capacitor. Without large off-chip capacitor, this LDO is suitable for system-on-chip (SoC) requirement. Post layout simulation shows that fast response of 45ns and high PSRR of -42dB through up to 10GHz frequency range.**

Keywords— flipped voltage follower (FVF); low-dropout regulator (LDO); fast transient response LDO; high PSRR LDO

I. INTRODUCTION

With the trends of green energy and system-on-chip (SoC), there is rapidly increasing demand for low-noise power-efficient low drop-out (LDO) regulator with single chip solution [1]. Fast response and high power supply rejection ratio (PSRR) are crucial requirements for LDO when it has fast switching load like phase locked loop (PLL) and delay locked loop (DLL) [2]. This paper describes a dual loop flipped voltage follower (FVF) based low-dropout regulator (LDO) for all-digital phase locked loop (ADPLL) which is used for very-high-bit-rate (VHBR) interface of 13.56 MHz PSK demodulation with phase range as large as 60^o. The whole system is used as a contactless smartcard [3] as shown in Fig. 1. The phase modulated signal from LA and LB is converted to square waves by the antenna buffer (amplitude limiting) without destroying the original phase information which is processed by ADPLL. This contactless smartcard is actually a passive RFID tag that is usually operated in harsh environments as the power is generated by rectifier from electromagnetic waves. Thus the supply is quite noisy and has a wide range of peak to peak variations up to 500mV. Therefore, high PSRR is required to ensure proper working of the system.

The crucial blocks in ADPLL include both a Time-to-Digital Converter (TDC) and a Digital Controlled Oscillator (DCO). The DCO is a low power design, so it does not consumes a lot of current and is insensitive to given voltage ripple. However, the delay line present in TDC is inverter based and the delay is very sensitive to VDD variations. Our simulation shows that10mV supply variation may cause TDC lose 0.4LSB (96ps is 1 LSB for this TDC). In order to have TDC maximum code variation due to the supply smaller than 1 LSB, the maximum transient ripple at the supply is 20mV which includes 5mV from supply input and 15mV TDC self-loading effect due to switching. This results in a large PSRR requirement of -40dB (from 500mV to 5mV). With maximally 60^o phase difference of the 13.56 MHz data rate, the longest pulse width is around 12ns with large peak current consumption of about 400μA. Thus the regulator also needs fast transient response ability. It has to recover the supply within 60ns to follow the TDC periodical switching. So the key requirement for LDO is fast transient and high PSRR at the same time. To achieve high PSRR, a feed-forward ripple cancellation path is adopted in [4] and [5], but larger than 4μF [4] and 6μF [5] load capacitor requirement makes them not suitable for SoC. [1] and [6] proposed external capacitor-less LDO but their settling time could be as large as 6μs [1] and 400ns [6]. Although [7] has output capacitor as small as 1pF and [8] could operate under large input peak-peak voltage range, their settling time is around 250ns [7] and 63μs [8]. To achieve less than -40dB PSRR and 60ns settling time at the same time without bulky external capacitor, this work proposed dual loop FVF LDO with cascaded structure.

The proposed FVF LDO system and circuit are shown in the following Section II. Post layout simulation results are shown in Section III, and the conclusion are provided in Section IV.

II. PROPOSED FVF LDO

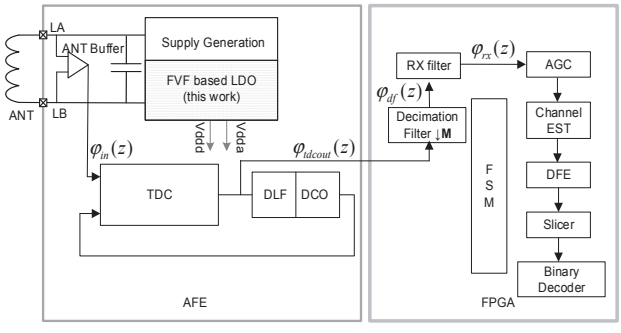

Fig. 1. LDO for ADPLL based PSK-demodulator smartcards.

A. Proposed FVF LDO System

In order to meet the given requirements, a cascaded LDO architecture has been adopted as shown in Fig. 2. Since a very high PSRR was required for the system, the idea was to reduce the supply variations across stages. The main advantage is that it helps to improve the overall line regulation of the system to achieve high PSRR across all frequencies without increasing the on-chip capacitance thus minimizing the required area. As shown in Fig. 2, the first stage, reduce the supply by a factor of 20dB, i.e. ~50mV from the initial supply variation of 0.5V. Both the first stage and the second stage are based on a FVF LDO. The output of the first stage is then used as the supply for the next stage which then gives only 5mV ripple. The second stage is also responsible to provide the fast transient currents in order to meet the TDC transient requirements. Considering the given current load specifications, the minimum output capacitance required is

$$C_{out} = \frac{I_{load\_max}\Delta t}{V_{ripple}} \quad (1)$$

where I_{load_max} is the peak load current of 400µA, and Δt is the width of the current pulse about 12ns. So $I_{load\_max}\Delta t$ is the total charge of the output current pulse, and it is about 4.8pC. With 20mV of total V_{ripple} requirement (including 15mV from self-loading effect), output capacitance C_{out} is about 240pF which is too large for on-chip implementation. Therefore, in order to maintain the voltage drop in required levels, the relatively large output capacitor is usually required, which is obviously not feasible for a SoC. So a lot of works use off chip capacitors. Our architecture adopts fully on chip 80pF output capacitor, because our circuit achieves a fast transient response by feedback in order to minimize the need of a large output capacitance. The detailed circuit is shown in the following Session II. B.

B. FVF LDO Circuit Implementation

The basic structure of FVF LDO is shown in Fig. 3. It is mainly composed of pass transistor M_P, control transistor M_C and a current source. M_P is to deliver large current from supply to the output load.

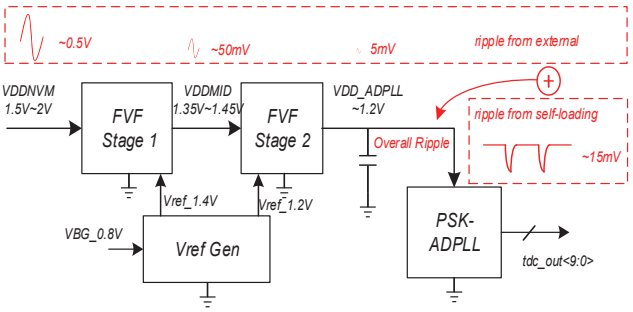

Fig. 2. The proposed FVF LDO system.

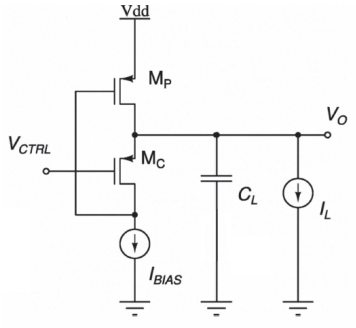

Fig. 3. The basic structure of FVF LDO.

The voltage at the source of M_C (V_o) follows the voltage at the gate of M_C (V_{CTRL}). It is defined as a 'flipped' structure since the bias current appears at the drain terminal of M_C instead of the source terminal, as that in simple source follower. As a voltage follower, the dc voltage at V_O can be expressed as

$$V_o = V_{CTRL} + V_{SG,Mc} \quad (2)$$

One major drawback of this technique is that it has minimum loading requirement [9]. If the loading is smaller than the minimum loading requirement, the gate voltage of M_P needs to increase to reduce its overdrive voltage. However, this will push M_C into triode region. In that case, the output voltage of the LDO will be altered.

The proposed dual loop FVF LDO is shown in Fig. 4. The pass transistor must be large enough to meet load current as well as drop-out voltage specification. The minimum channel length of the pass transistor is not used in this design, since it makes the transistor output impedance unacceptably low at high load current. Moreover the contribution of the pass transistor for improvement of the PSRR at high frequencies can be greatly affected if minimum channel length of the pass transistor is used. M3 is actually a common gate amplifier. Its input voltage is V_{out}, so the variance of V_{out} will generate an error voltage at node VA and then VG follows to feedback. This is indicated as “Loop 1” in Fig. 4. Low impedance node at the gate of the pass transistor VG allows the circuit to have high bandwidth and improved transient performance. PMOS M5 acts as a level shifter or source follower as shown in Fig. 4. By adding M5 in the feedback path from drain of M3 to M_{pass}, the minimum loading problem is alleviated because the DC operation of M_{pass} depends on M5 size and its bias current. Small changes at V_{out} can be sensed by transistor M3 and level shifted by M5 with a voltage of Vth.

The second loop “Loop 2” is used to generate the stable Vmir at the source of M4. As both transistors M3 and M4 are source followers, V_{out} is shifted one threshold level up forcing it to be equal to Vmir. This loop is majorly responsible for the DC gain of the system and thus good PSRR. The RC low pass filter between M4 and M3 is used to filter high frequency noise and get even better PSRR performance.

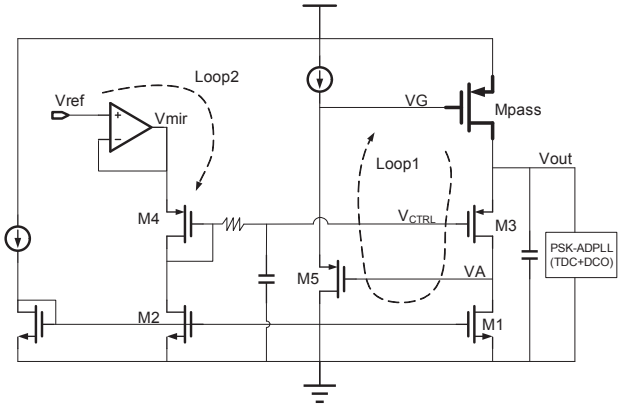

Fig. 4. The proposed dual loop FVF LDO.

III. Simulation Results

The layout floorplan is shown in Fig. 5. This FVF LDO is implemented on the same chip of the ADPLL. It occupies about 0.036mm^2 with most of the area is occupied by the on chip 80pF capacitors.

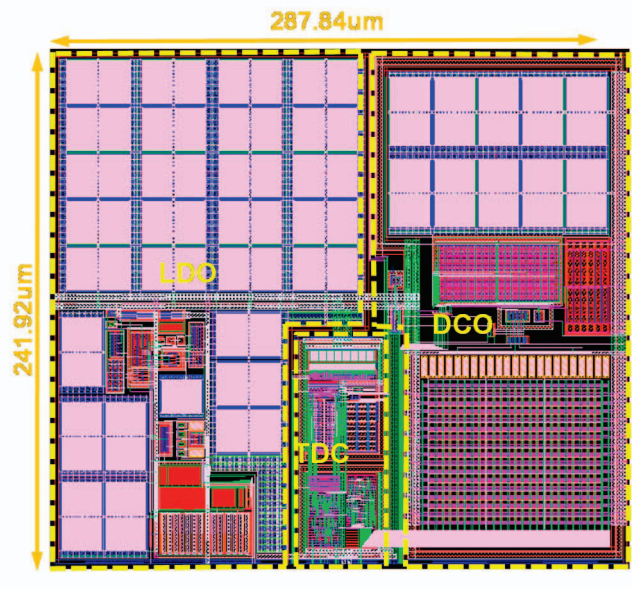

Fig. 5. The layout floorplan of the proposed FVF LDO.

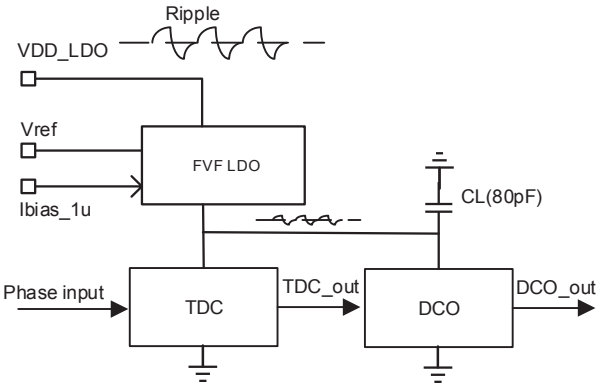

Fig. 6. The simulationn set-up for proposed FVF LDO.

To verify the proposed FVF LDO, it is simulated together with TDC and DCO which are critical blocks of the ADPLL as shown in Fig. 6. The LDO line regulation across 1.5 to 2 V supply range with different current loadings is shown in Fig. 7. Less than 1mV/V is achieved which indicates that our DC output variation is smaller than 0.5mV at 500mV input ripple. The load regulation of the LDO across 10 to 400uA current range with different supply voltages is shown in Fig. 8. The small variation 25mV/A is achieved. If the load current varies by 0 ~ 250uA, the load voltage almost has no changes. We also make the TDC switch at receiver operation frequency of 13.56MHz and simulate its recovery time as shown in Fig. 9. The simulation results show it could recover within 45ns which is much smaller than our specs of 60ns.

The PSRR simulation result is shown in Fig. 10. The first stage achieves around -20dB. With the help of second stage LDO and 80pF output capacitor, less than -40dB PSRR result is achieved through the whole frequency range up to 10GHz. We could find in Fig. 10 that the worst case happens at about 1.7MHz which is around 1/8 of the receiver center frequency. To investigate the supply variation at some important frequency, we inject the ripple with 500mV at frequency of interest. The LDO output ripples from supply and self-loading effect are shown in Table I.

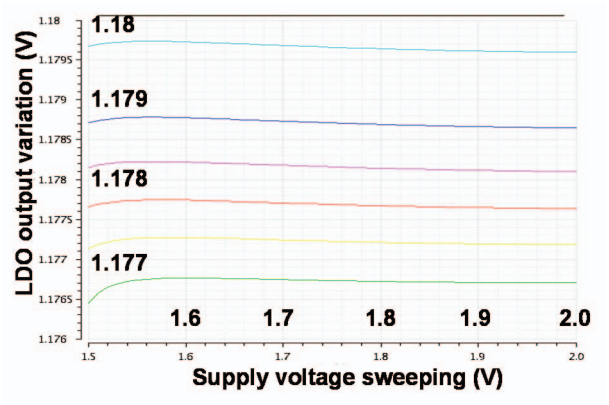

Fig. 7. The line regulation of the LDO with different current loadings across 1.5 to 2 V supply range.

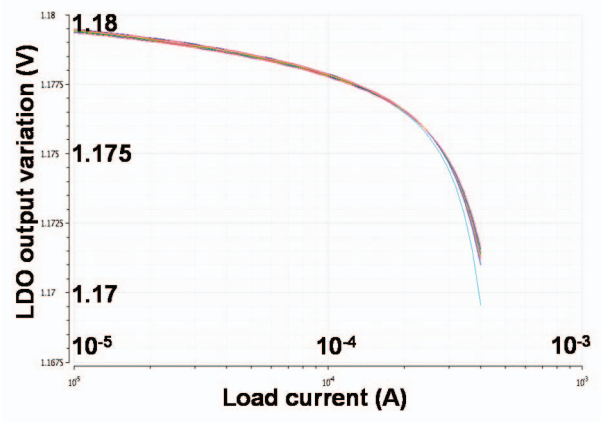

Fig. 8. The load regulation of the LDO with different supply voltages across 10 to 400uA current range.

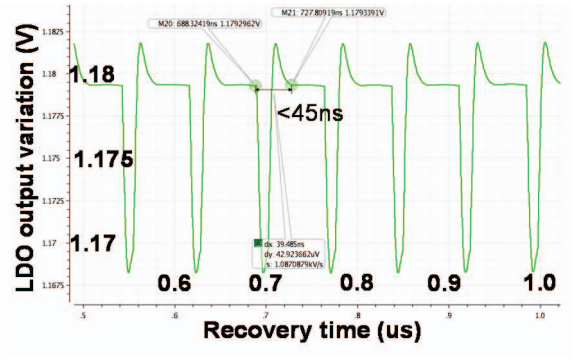

Fig. 9. The recovery time of LDO with TDC switching.

The worst case happens around fc/8 which matches the PSRR simulation result. Although large ripple of 500mV at fc/8 can barely happen in real application, we have to be sure that 21mV ripple still causes TDC phase shift less than 1 LSB or 0.5°. The results are shown on the last column of Table I which shows our specs can be satisfied. The performance summary and comparison table is shown in Table II from which we can find this work is the only one that achieves both good PSRR and fast transient response with large input variation and small on chip capacitor at the same time.

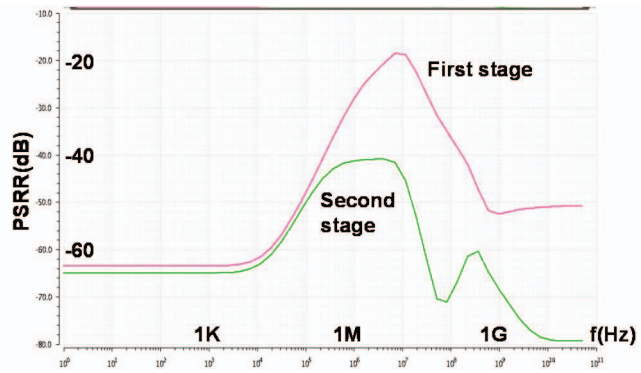

Fig. 10. The PSRR performance of the LDO.

TABLE I. TDC PHASE UNCERTAINTY UNDER RIPPLES OF DIFFERENT FREQUENCY

Frequency of ripple fc=13.56MHz	LDO input ripple (Vpp)	LDO output ripple (mV)		Phase Uncertainty (degrees)
		Due to input ripple	*Due to TDC Self-loading*	
fc/4	500mV	5	15	+/- 0.25
fc/8		6	15	+/- 0.25
fc/16		5	15	+/- 0.25
fc		3	15	+/- 0.25
2fc		2	15	+/- 0.25

TABLE II. LDO PERFORMANCE SUMARY AND COMPARISON TABLE

	[1] (measured)	[4] (measured)	[7] (simulated)	[8] (simulated)	This work (simulated)
Tech.	CMOS 0.18mm	CMOS 0.18mm	CMOS 0.18mm	CMOS 0.18mm	**CMOS 40nm**
Input Vpp	0.1V	0.1V	N.A	0.4V	**0.5V**
I_Q	55µA	50µA	34µA	15µA	**25µA**
Max I_{load}	50mA	25mA	0.5~ 250mA	1mA	**0.4mA**
Load cap	100pF	4µF (external)	1pF	2µF (external)	**80pF**
Area (mm^2)	0.14 (excluding load cap)	0.049	N.A	0.1	**0.036**
PSRR	-37dB @10MHz	-56dB @10MHz	N.A	>-18dB	**-43dB @10MHz**
Settling time (ns)	6000	600	250	>63000	**45**

IV. CONCLUSION

This work presents a design of the dual loop FVF LDO to achieve high PSRR and fast transient response for ADPLL in the RFID application. With only 80pF on chip output capacitor, this LDO core circuit only occupies small area of 0.036 mm^2, which makes it suitable for SoC requirement. Better than -42dB PSRR is achieved through out the frequency range with the help of an additional reference generation loop in FVF LDO and the cascaded structure. Post layout simulation also shows that fast response of 45ns. Thus this LDO can satisfy the stringent requirement of the ADPLL especially the TDC.

REFERENCES

[1] P. Chang-Joon, M. Onabajo, and J. Silva-Martinez, "External Capacitor-Less Low Drop-Out Regulator With 25 dB Superior Power Supply Rejection in the 0.4–4 MHz Range," IEEE Journal of Solid-State Circuits, vol.49, no.2, pp.486-501, Feb. 2014.

[2] L. Wang, L. Liu and H. Chen, "An Implementation of Fast-Locking and Wide-Range 11-bit Reversible SAR DLL", IEEE Trans. on Circuits and Systems II, Page(s): 421 – 425, 2010.

[3] Working group WG8 of ISO/IEC JTC1/SC17: 'Identification Cards', www.wg8.de.

[4] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sánchez-Sinencio, "High PSR low drop-out regulator with feed-forward ripple cancellation technique," IEEE J. Solid-State Circuits, vol. 45, no. 3, pp. 565–577, Mar. 2010.

[5] A. Amer and E. Sánchez-Sinencio, "A 140 mA 90 nm CMOS low dropout regulator with 56 dB power supply rejection at 10 MHz," IEEE Custom Integrated Circuits Conf. (CICC), Sep. 2010, pp. 1–4.

[6] E. N. Y. Ho and P. K. T. Mok, "Wide-loading-range fully integrated LDR with a power-supply ripple injection filter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 59, no. 6, pp. 356–360, Jun. 2012.

[7] C. Yen-Fu andT. Kea-Tiong, "A wireless power transmission subsystem with capacitor-less high PSRR LDO and thermal protection mechanism for artificial retina application," International Symposium on VLSI Design, Automation and Test (VLSI-DAT) , pp.1-4, 27-29 April 2015.

[8] H. Cheng-Han, D. Chung-Yen, and L. Shuenn-Yuh, "Power management with energy harvesting from a headphone jack," IEEE International Symposium on Circuits and Systems (ISCAS), pp.1989-1992, 1-5 June 2014.

[9] C. Hua, L. Ka Nang, "A fast-transient LDO based on buffered flipped voltage follower," International Conference of Electron Devices and Solid-State Circuits (EDSSC), pp.1-4, 15-17 Dec. 2010.