A 0.96–0.9-V Fully Integrated FVF LDO With Two-Stage Cross-Coupled Error Amplifier

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***Abstract*—This brief presents a fully integrated flipped-voltage-follower (FVF) based 0.96–0.9-V low-dropout regulator (LDO) with a high-gain two-stage cross-coupled error amplifier (XCEA). The proposed XCEA overcomes the constraint of intrinsic gain and helps achieve better power supply rejection (PSR) and load regulation. Besides, by setting power supplies of the pass transistor and EA separated and unequal, the efficient dropout increases and different parts of PSR could be measured individually. Fabricated in 28-nm bulk CMOS process, consuming 135-μA quiescent current and occupying active area of 0.0017 mm^2, the LDO features 27-MHz unity-gain bandwidth (UGB) at 20-mA load. The proposed LDO achieves 1.6 ns response time with 160-mV measured voltage undershoot for a 0-to-20-mA load transient current in 100 ps with C_L = 200 pF. Owing to the proposed high-gain XCEA, the overall PSR is as good as –38 dB at 10 kHz and –20 dB at 30 MHz.**

***Index Terms*—Cross-coupled error amplifier (XCEA), flipped voltage follower (FVF), low dropout regulator (LDO), super source follower (SSF).**

I. Introduction

FULLY integrated low-dropout regulators (LDOs) are attractive in very large-scale integrated (VLSI) circuits, based on the aspects of low design cost, small area occupation and fair power supply rejection (PSR). In high-speed wireline systems, as a common choice, analog LDOs are simple to implement and integrate. Compared to output-capacitorless analog LDOs [1], the ones with large on-chip capacitors are superior in PSR, stability and load capability, despite the indispensable large output capacitor considerably increasing the area cost, and extra power consumption required to push the internal pole to higher frequencies [2], [3]. Fig. 1 shows a typical working scenario that the LDO embedded in a single-ended (SE) high-speed transmitter (TX). The LDO loading large on-chip capacitor makes the SE TX robust against the undesired noise, which mainly comes from external power supplies, printed circuit board (PCB) and bonding wires.

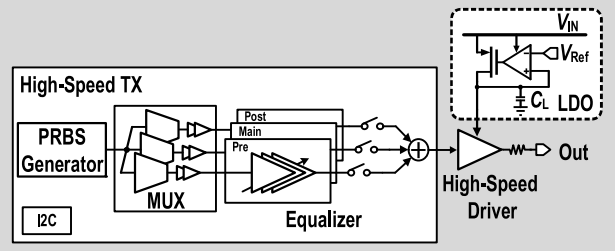

Fig. 1. Typical scenario of LDO working in a high-speed transmitter.

To realize better PSR and load/line regulations, the error amplifier (EA) is supposed to provide high DC gain. The cascode-structure-based EA was demonstrated to be able to provide about 50-dB gain in single stage [4]. However, given the relatively low supply voltage in advanced CMOS technologies, it is difficult to establish a single-stage high-gain EA by using the cascode structure. To cope with the awkwardness, the cross-coupled error amplifier (XCEA) was proposed previously. The loaded cross-coupled pair exhibits as negative resistance and partially neutralizes the equivalent resistance of the diode-connected PMOS. Nevertheless, the single-stage XCEA has a pair of differential outputs which could not be transferred to next stage simultaneously. Besides, it is insufficient to achieve enough high gain. In [5], one of the differential outputs was exploited to be an extra transient compensation loop. Yet the compensative loop functions marginally in the ultra-fast response condition and brings additional complexity into the circuitry.

The rest of this brief is organized as follows. Section II illustrates the conceptual diagram of the proposed design. Then, Section III presents the detailed circuit implementation of the proposed LDO and analyzes the gain boosting of the proposed XCEA. In Section IV, the measurement methods and results are provided. At last, the conclusion is drawn in Section V.

II. Concept of the Proposed Design

Fig. 2 shows the proposed LDO, employing a proposed two-stage high-gain XCEA and setting V_{EA} and V_{IN} to 0.9 V and 0.96 V, thereby enhancing effective dropout and aiding diverse loop PSR assessments. The fast loop and slow loop together constitute the main architecture. For the allocation of poles, by loading 200-pF capacitor at the output node, the pole p_O

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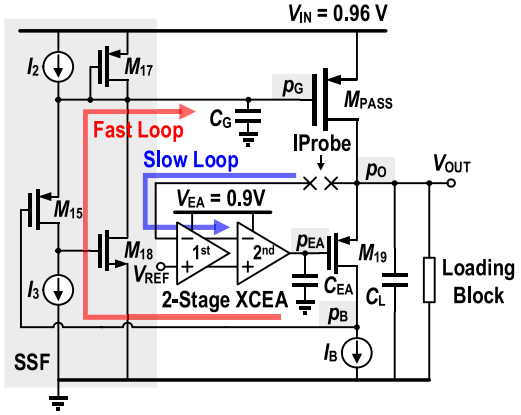

Fig. 2. Illustrative diagram of the proposed 60-mV dropout LDO and the stability simulation setup.

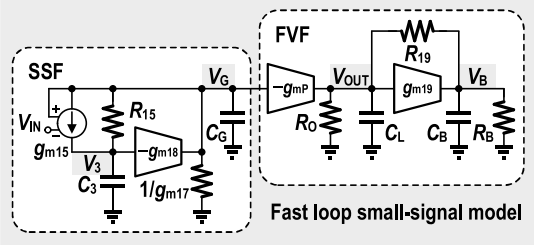

Fig. 3. Small-signal model of the fast loop which is composed of the SSF and FVF stages.

behaves dominantly in the whole circuit. To avoid p_G locating close to p_O, the super source follower (SSF) employing an extra common source stage is inserted between M_{19} and M_{PASS}. Thus, the effective impedance at M_{PASS} gate dramatically reduces and pushes the internal non-dominant pole p_G to GHz range, at a price of apportioning 40% of the quiescent current budget to the SSF. Moreover, to retain the capability of fast response, the transistor lengths of M_{15} and M_{18} are 30 nm to decrease realistic parasitic. In addition, to decrease the impact of p_B on the unity-gain bandwidth (UGB), the length of the bias transistors in the fast loop is chosen as 120 nm at the cost of partial current copy accuracy.

Fig. 3 shows the small-signal model of the fast loop. According to [4], the overall transfer function is derived as (1) which is shown at the bottom of the page, and A_{DC} is shown as

$$A_{DC} = \frac{-g_{mp}R_O R_B(1+g_{m19}R_{19})}{R_O+R_B+R_{19}+g_{m19}R_{19}R_O} \bullet \frac{g_{m15}R_{15}}{1+g_{m15}R_{15}}, \quad (2)$$

herein, g_{mp} and g_{m15-19} denote the transconductance of transistors M_{PASS} and M_{15-19}. R_O represents the output resistance at the V_{OUT} node. C_3, C_B and C_G are the capacitance on nodes V_3, V_B and V_G. R_{15-19} and R_B are the drain-source resistance of M_{15-19} and M_B.

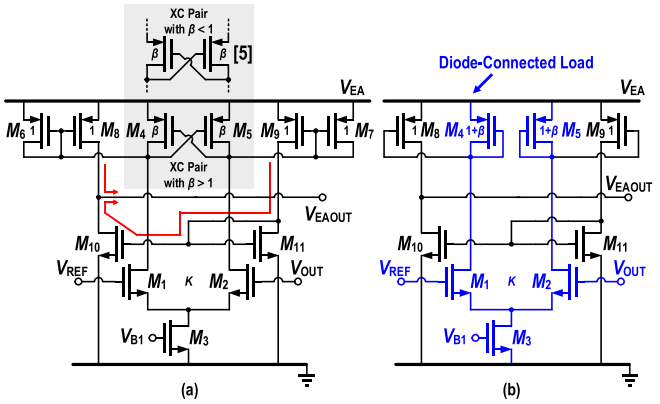

Fig. 4. The structures of (a) the proposed two-stage XCEA and (b) the two-stage EA with conventional diode-connected loaded amplifier.

This design casts off the intermediate set voltage generation stage and the XCEA output directly transfers to M_{19}. Subsequently, we disassemble the 7-pF bypass capacitor in [2] into two smaller capacitors C_{F1} and C_{F2}. For 200-fF C_{F1}, it filters noise of the XCEA output and guarantees the stability of the proposed LDO when connecting the slow and fast loops.

Meanwhile, C_{F2} is designed to be 4 pF and located at the gate of M_{13}, which also effectively filters the unwanted noise. Furthermore, we intentionally enlarge the static current in the FVF loop to accelerate the charging and discharging speed, which shortens the undershoot recovering time.

III. Implementation of the Proposed LDO

A. Proposed Two-Stage XCEA

As shown in Fig. 4 (a), the proposed XCEA could be decomposed into the first gain-boosting XCEA stage (M_1-M_7) and the second differential-to-single-ended (D2S) stage (M_8-M_{11}). To make a fair comparison, Fig. 4 (b) configures a two-stage EA with the first stage of the conventional diode-connected loaded amplifier. For the first stage, assume the size ratio between the transistor pairs (M_4, M_5) and (M_7, M_6) to be β. Compared to conventional diode-connected loaded error amplifier, whose gain is constrained by the transconductance of the transistors, under the same conditions, the XCEA could boost the gain by a factor of

$$\frac{A_v}{A_{v,conventional}} = \frac{[(1+\beta)g_{mp6,7}+g_{dsn1,2}]}{[(1-\beta)g_{mp6,7}+g_{dsn1,2}]}, \quad (3)$$

where $g_{mp6,7}$ and $g_{dsn1,2}$ denote the transconductance and conductance of the corresponding transistors, respectively [6]. In [5], to prevent a negative denominator, the value of β is charily chosen to be smaller than 1, which wastes most of the potential of XCEA gain boosting capability.

$$A_V = \frac{V_B}{V_{IN}} = \frac{A_{DC}(1+s\frac{C_3}{g_{m18}})}{(sR_OC_L+1)\bullet[s(R_O+g_{m19}R_OR_{19}+R_{19})||R_BC_B+1]\bullet[s^2\frac{C_GC_3}{g_{m15}g_{m18}}+s\frac{C_G+C_3+R_{15}C_3(g_{m15}+g_{m17})}{R_{15}g_{m15}g_{m18}}+(\frac{g_{m18}+g_{m17}}{R_{15}g_{m15}g_{m18}}+1)]} \quad (1)$$

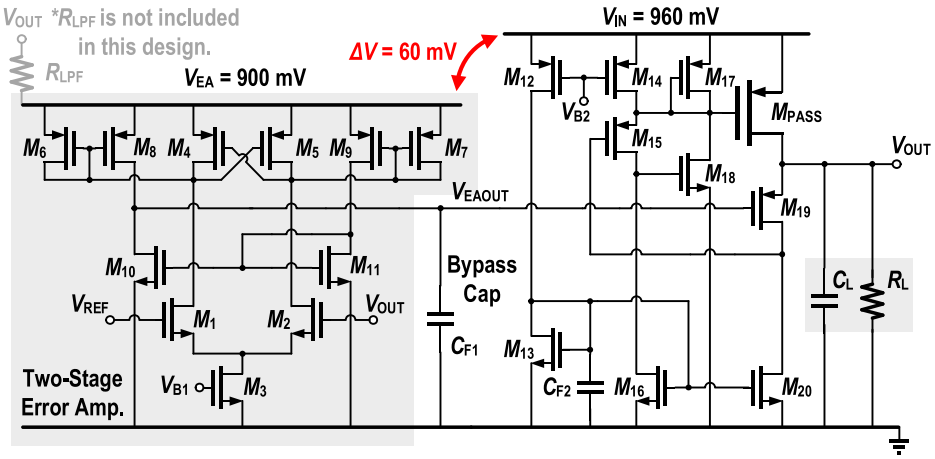

Fig. 5. The transistor-level schematic of the proposed LDO.

By contrast, in our design, we set β to be larger than 1 to achieve a higher gain. To explore the limitation of the maximum value of β, we start from the drain current expression of MOSFET working in the subthreshold region [7], which is given as

$$I_{\mathrm{D}} = \mu C_{\mathrm{d}} \frac{W}{L} V_{\mathrm{T}}^2 e^{\frac{V_{\mathrm{GS}}-V_{\mathrm{TH}}}{\zeta V_{\mathrm{T}}}} \left(1 - e^{\frac{-V_{\mathrm{DS}}}{V_{\mathrm{T}}}}\right). \tag{4}$$

Herein, μ is the carrier mobility and C_d represents the depletion region capacitance, $V_T = kT/q$ and $\zeta = 1 + C_d/C_{\mathrm{ox}}$.

Based on (4), the equations of g_{mn} and g_{dsn} and their relation can be calculated as

$$g_{\mathrm{mn}} = \frac{\partial I_{\mathrm{Dn}}}{\partial V_{\mathrm{GS}}} = \frac{\mu_{\mathrm{n}} C_{\mathrm{d}} V_{\mathrm{T}}}{\zeta} \bullet \frac{W}{L} e^{\frac{V_{\mathrm{GS}}-V_{\mathrm{TH}}}{\zeta V_{\mathrm{T}}}} \left(1 - e^{\frac{-V_{\mathrm{DS}}}{V_{\mathrm{T}}}}\right), \tag{5}$$

$$g_{\mathrm{dsn}} = \frac{\partial I_{\mathrm{Dn}}}{\partial V_{\mathrm{DS}}} = \mu_d C_{\mathrm{d}} V_{\mathrm{T}} \frac{W}{L} e^{\frac{V_{\mathrm{GS}}-V_{\mathrm{TH}}}{\zeta V_T}} e^{\frac{-V_{\mathrm{DS}}}{V_T}}, \tag{6}$$

$$g_{\mathrm{dsn}} = g_{\mathrm{mn}} \frac{1 + \frac{C_{\mathrm{d}}}{C_{\mathrm{ox}}}}{e^{\frac{V_{\mathrm{DS}}}{V_{\mathrm{T}}}} - 1}, \tag{7}$$

Therefore, we can convert the denominator into a more specific form, which is shown as

$$(1-\beta) g_{\mathrm{mp}} + g_{\mathrm{dsn}} = (1-\beta) g_{\mathrm{mp}} + \frac{\zeta \mathrm{K}}{e^{\frac{V_{\mathrm{DS}}}{V_{\mathrm{T}}}} - 1} g_{\mathrm{mn}}, \tag{8}$$

where K denotes the size ratio of M_1 and M_2 by normalization based on M_6 and M_7. In consideration of the whole circuit, K is chosen to be as large as 8 to not only provide high differential gain in stability, but also guarantee (8) to be positive. Additionally, β is chosen to be about 7.7 to decrease the denominator. Fig. 6 shows the simulated loop gain and phase margin of the proposed LDO at different loads, as well as the result with EA using conventional diode-connected load. The simulation results shows that the DC gain could be improved by 25 dB at 20 mA by using the proposed XCEA. It is worth mentioning that the negative capacitance generated by cross-coupled pair pushes p_{EA} to higher frequencies and thus extends the UGB. Therefore, the upper limit of β is also constrained by this respect to prevent the whole loop from falling into instability.

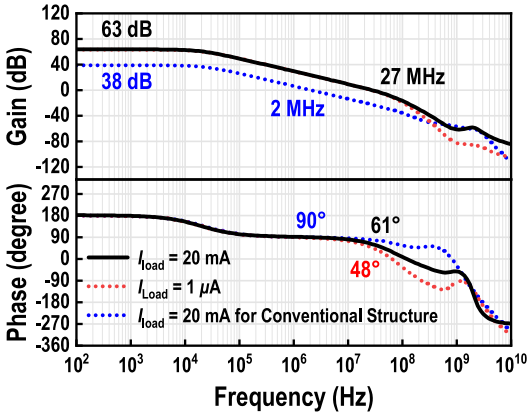

Fig. 6. Simulated loop gain and phase margin of different structures at different loads.

Furthermore, based on the single-stage XCEA, an extra D2S stage formed by M_8-M_{11} is added. This stage combines the former differential outputs together and transfers the single-ended output to M_{19}. Besides, it also provides extra gain. Since the XCEA works in the sub-threshold region and the extra amplification stage consumes little current, the impact on the current efficiency is negligible.

B. Separated Power Supplies

In our design, the power supplies V_{EA} and V_{IN} are separated on purpose, as shown in Fig. 5. V_{EA} is chosen as 0.9 V while V_{IN} is 0.96 V to create a 60-mV dropout between them. From the view of the superposition theorem, the effective dropout voltage is nearly enlarged to 120 mV, which alleviates the predicament of the large-size power transistor M_{PASS} working in. Besides, compared to the method adopting a lowpass filter composed of R_{LPF} and C_{L} to feedback the output to the EA, the power could be directly applied to the error amplifier instead of spending time charging C_{L}. As shown in Fig. 7(a), a higher R_{LPF} could lead to a more stable transient performance while deteriorate the recovering time of the undershoot.

In addition, the separated supplies could be convenient for investigating the PSR performances of different parts in LDO.

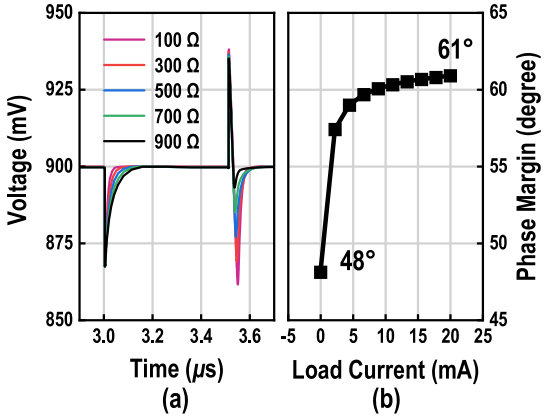

Fig. 7. (a) Simulated transient response versus different values of R_{LPF} and (b) simulated phase margin versus load current of the proposed LDO.

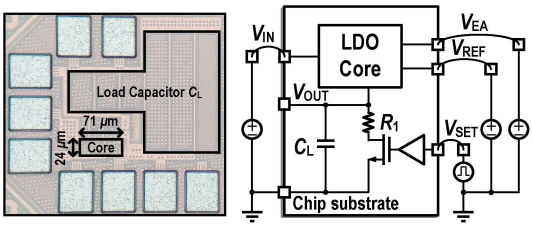

Fig. 8. The chip micrograph and the measurement setup.

As a common sense, the PSR could be calculated by

$$PSR = 20\log\frac{\Delta V_{\mathrm{Out}}}{\Delta V_{\mathrm{Supply}}}, \tag{9}$$

where ΔV_{Sup} and ΔV_{Outp} denote the voltage variations at power supplies and LDO output, respectively. Hence, by using superposition theorem, the relation between the overall PSR and separated ones can be approximately expressed as

$$PSR_{\mathrm{ALL}} = 20\left[\log\left(10^{\frac{PSR_{\mathrm{EA}}}{20}} + 10^{\frac{PSR_{\mathrm{IN}}}{20}}\right) - \log 2\right]. \tag{10}$$

Here, PSR_{EA} and PSR_{IN} represent the measured PSR by applying AC signals on V_{EA} and V_{IN}, respectively. Nevertheless, in LF domain, the PSR_{ALL} will be clamped by the PSR_{EA}, which is verified by simulation. This phenomenon will be reversed in ultra-high-frequency (UHF) domain.

Fig. 7(b) presents the simulated phase margin variation versus load current change. The worst case takes place at the least load and the phase margin is above 45°, which guarantees the loop stability.

IV. Experimental Results

The proposed LDO was fabricated in a 28-nm bulk CMOS. Fig. 8 shows the chip micrograph and illustrates the measurement setup. The active area of the proposed LDO occupies 0.0017 mm^2. The load capacitor is embedded within the core for validating the functionality of the chip as a fully integrated unit. Besides, the quiescent current is measured to be 135 μA.

A. Power Supply Rejection

Fig. 9 shows the measurement and calculated results of PSR up to 30 MHz at $I_{\mathrm{Load}} = 20$ mA. The blue and green lines represent the measured PSR_{IN} and PSR_{EA}, respectively.

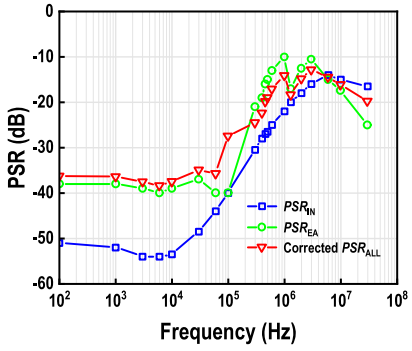

Fig. 9. Calculated PSR and comparison with separated loops.

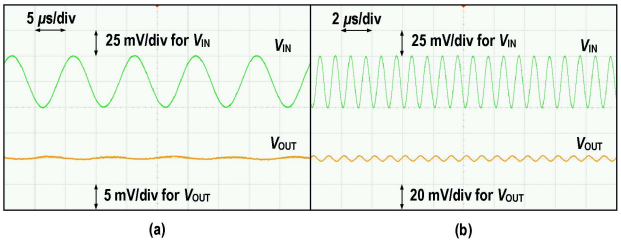

Fig. 10. Measured transient waveforms at full load for PSR_{IN} calculation at (a) 100 kHz and (b) 1 MHz.

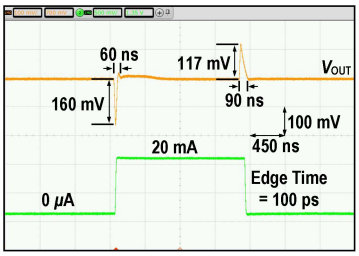

Fig. 11. Measured load-transient response.

For PSR_{IN}, it is lower than –50 dB at low frequencies and reaches a peak of –14 dB at 6 MHz. While PSR_{EA} keeps around –39 dB at low frequencies and shows superiority at high frequencies. The red line presents the calculated PSR_{ALL} after correction. The overall PSR is better than –37 dB at low frequencies. Due to the large 200-pF load capacitor, the PSR could maintain lower than –20 dB beyond 30 MHz.

Besides, Fig. 10 presents the measured transient waveform to demonstrate the ripple rejection capability in the aspect of time domain. Only the set of V_{IN} and V_{OUT} is given for illustration. The 50-mV sinusoidal ripples are imposed in frequencies of 100 kHz and 1 MHz to simulate the external disturbance. Through the LDO, the amplitudes are compressed as seen at V_{OUT} node.

B. Transient Response and Load Regulation

Fig. 11 depicts the measured transient response with an on-chip load block whose current changes from 0 μA to 20 mA within 100 ps. The measured undershoot and overshoot are 160 mV and 117 mV, which could be recovered both in less than 90 ns. The minor overshoot after the rising step, attributed to the unwanted package parasitic, can be disregarded due to its minimal amplitude.

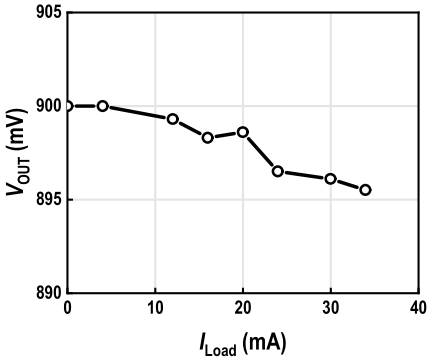

Fig. 12. Measured load regulation.

TABLE I
COMPARISON TABLE

	TCASI' 2015 [2]	TCASII' 2020 [6]	TPEL' 2021 [10]	JSSC' 2018 [11]	This work
Technology	65	28	65	65	28
Dropout (mV)	150	50	200	200	60
V_{IN}/ V_{OUT} (V)	1.15/1	0.9/0.85	1.2/1	1.2/1	0.96/0.9
I_Q (μA)	50	33	27-82	8-297.5	135
$I_{O(MAX)}$ (mA)	10	20	20	25	20*
$I_{O(MIN)}$ (μA)	0	0	5	0	0
C_L (pF)	140	30	300	240	200
PSR (dB/Hz)	-21/1M -15.5/1G	-30/100k -14/10M	-42/1M -25/10M	-52/1M -37/10M	-38/10k -20/30M
Eff. (%)	86.5	94.4	83	82.3	93.1
Load Reg. (mV/mA)	1.1	0.26	0.015	0.042	0.24
T_R/T_{Edge}(ns)	1.15/0.2	0.32/0.1	0.9/0.8	15/100	1.6/0.1
Area (mm²)	0.0234	0.0086	0.053	0.087	0.044
FoM_1 (mV)	1.48	0.29	1.94	191.45	1.08
FoM_2 (ns·V)	0.148	0.0783	0.0582	N/A	0.0648

*The supported maximum I_O = 40 mA.
$FoM_1 = K\,(\Delta V_{OUT} \cdot I_Q / \Delta I_{Load})$ [8], $FoM_2 = T_{Re} \cdot FoM_1$.

Fig. 12 shows the measured result of load regulation. Owing to the proposed XCEA providing high DC gain, the load regulation is as good as 0.24 mV/mA in a wide load current range of 0-34 mA.

A performance comparison with state-of-the-art works is summarized in Table I. With the implementation of the proposed high-gain XCEA, this brief achieves good load regulation in a wide load current range even under low dropout. Compared to previous fully integrated LDO works, the proposed LDO almost achieves PSR below –15 dB in a wide frequency range and –38 dB at low frequencies. The response time T_R is estimated according to [9]. For a fair comparison, the recovering time T_{Re} of undershoot is included to generate the FoM_2.

V. CONCLUSION

This brief has demonstrated a 60-mV dropout-voltage LDO in 28-nm bulk CMOS process, achieving fast response and high PSR. We propose a two-stage XCEA greatly improving gain and extending UGB, which achieves competitive PSR, better DC regulation and fast response. Besides, to overcome the constraint of low dropout voltage, as well as explore PSR performances in different loops intuitively, V_{EA} and V_{IN} are intentionally separated to be 0.9 V and 0.96 V. Furthermore, bypass and filter capacitors are utilized for stability and improving PSR. Loading 200-pF capacitance and occupying active area of 0.0017 mm^2, the proposed LDO features fast response, wide load range, and superior PSR with a power efficiency of 93.1%.

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