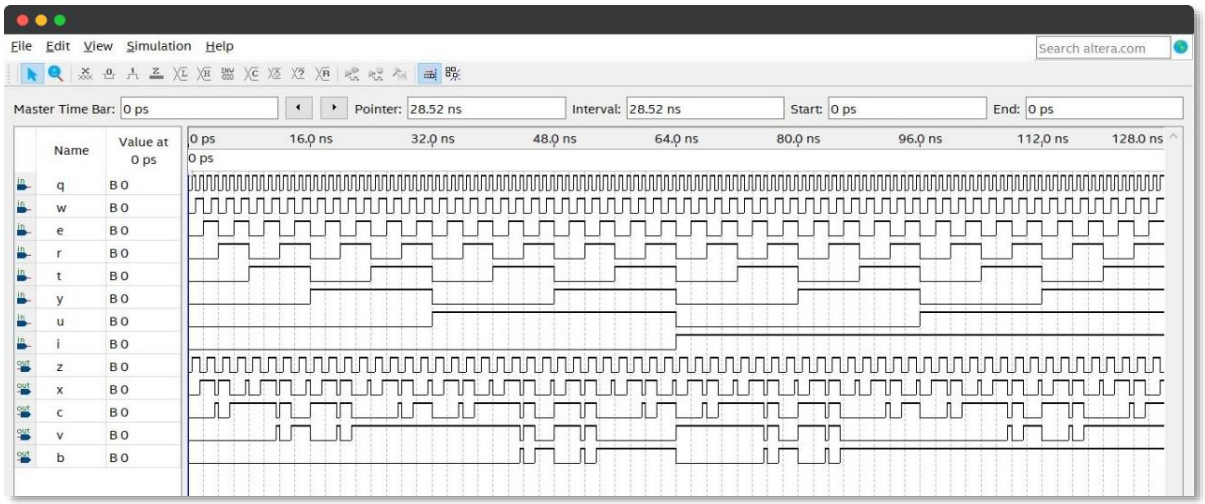
Lab Assignment 5

Question 1

Verilog Code

```
module ripple(q,w,e,r,t,y,u,i,z,x,c,v,b);
input q,w,e,r,t,y,u,i;
output z,x,c,v,b;
assign c0=0;
wire c1,c2,c3;
full_adder  ha1(
        .Data_in_A(q),
        .Data_in_B(w),
          .Data_in_C(c0),
        .Data_out_Sum(z),
        .Data_out_Carry(c1)
    );
full_adder  ha2(
        .Data_in_A(e),
        .Data_in_B(r),
          .Data_in_C(c1),
        .Data_out_Sum(x),
        .Data_out_Carry(c2)
    );
full_adder  ha3(
        .Data_in_A(t),
        .Data_in_B(y),
          .Data_in_C(c2),
        .Data_out_Sum(c),
        .Data_out_Carry(c3)
    );
full_adder  ha4(
        .Data_in_A(u),
        .Data_in_B(i),
          .Data_in_C(c3),
        .Data_out_Sum(v),
        .Data_out_Carry(b)
    );
endmodule
```

Quatrus Prime Waveform

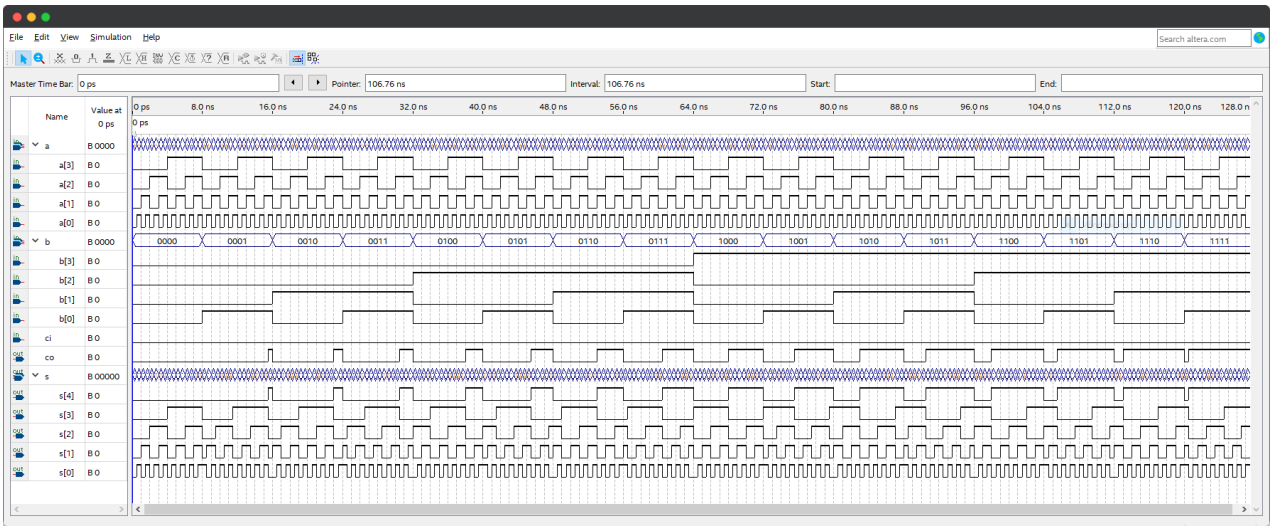


Question 2

Verilog Code

```verilog
module claa(a,b,ci,co,s);
 input [3:0]a,b;
 output [4:0]s;
 input ci;
 output co;
 wire [3:0]G,P,C;
 assign G = a&b;
 assign P = a^b;
 assign co=G[3]+ (P[3]&G[2]) + (P[3]&P[2]&G[1]) +  (P[3]&P[2]&P[1]&G[0]) + (P[3]&P[2]&P[1]&P[0]&ci);
 assign C[3]=G[2] + (P[2]&G[1]) + (P[2]&P[1]&G[0]) +  (P[2]&P[1]&P[0]&ci);
 assign C[2]=G[1] + (P[1]&G[0]) + (P[1]&P[0]&ci);
 assign C[1]=G[0] + (P[0]&ci);
 assign C[0]=ci;
 assign s = {co,P^C};
endmodule
```

Quatrus Prime Waveform



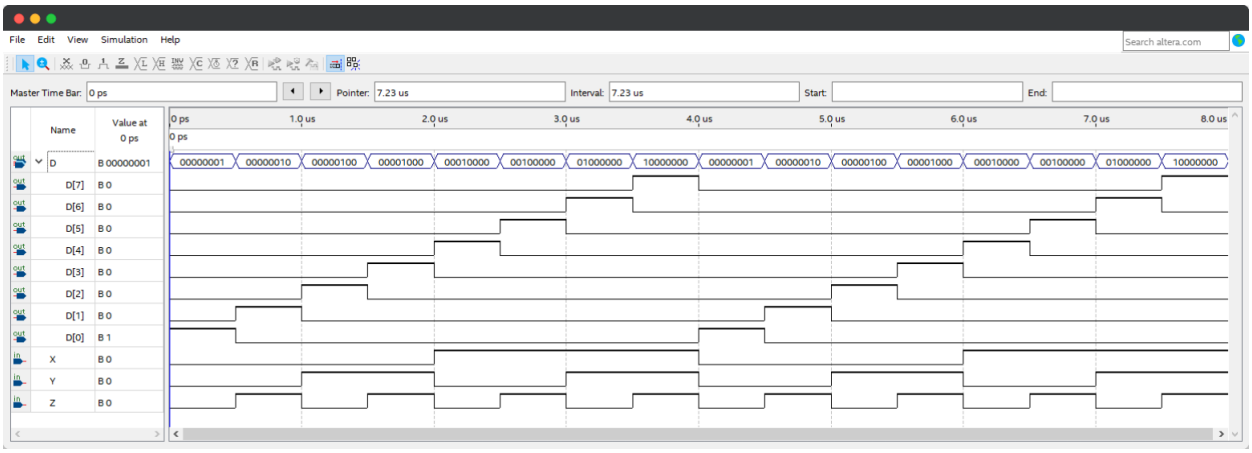
Question 3

Verilog Code

```verilog
module decoder(D,X,Y,Z);
  output [7:0] D;
  input X,Y,Z;
  assign D[0] = ~X & ~Y & ~Z;
  assign D[1] = ~X & ~Y & Z;
  assign D[2] = ~X & Y & ~Z;
  assign D[3] = ~X & Y & Z;
  assign D[4] =  X & ~Y & ~Z;
  assign D[5] =  X & ~Y & Z;
  assign D[6] =  X & Y & ~Z;
  assign D[7] =  X & Y & Z;
endmodule

```

Quatrus Prime Waveform



Question 4

Verilog Code

```verilog
module segment7(
     bcd,
     seg
    );

     input [3:0] bcd;
     output [6:0] seg;
     reg [6:0] seg;

    always @(bcd)
    begin
        case (bcd)
            0 : seg = 7'b0000001;
            1 : seg = 7'b1001111;
            2 : seg = 7'b0010010;
            3 : seg = 7'b0000110;
            4 : seg = 7'b1001100;
            5 : seg = 7'b0100100;
            6 : seg = 7'b0100000;
            7 : seg = 7'b0001111;
            8 : seg = 7'b0000000;
            9 : seg = 7'b0000100;
           default : seg = 7'b1111111;
        endcase
    end

endmodule
```

Quatrus Prime Waveform