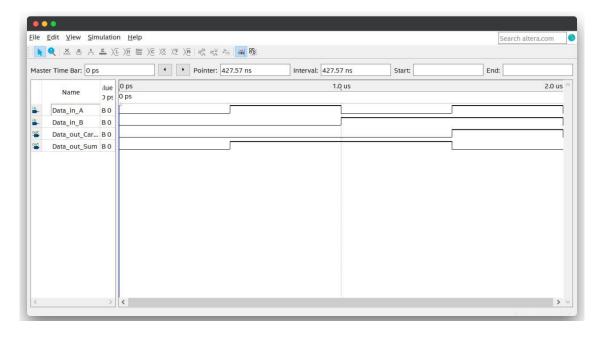
Lab Assignment 4

Question 1

Verilog Code

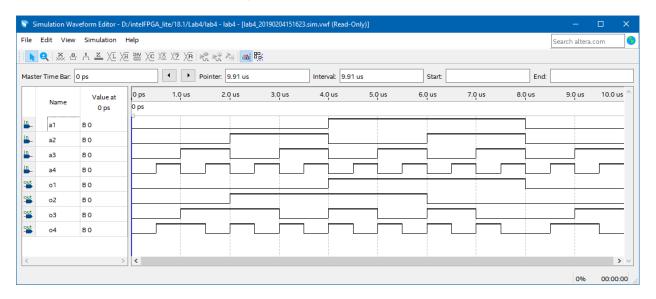
```
1 module half_adder(
2   output S,C,
3   input A,B);
4
5   xor(S,A,B);
6   and(C,A,B);
7
8 endmodule
9
```



Question 2

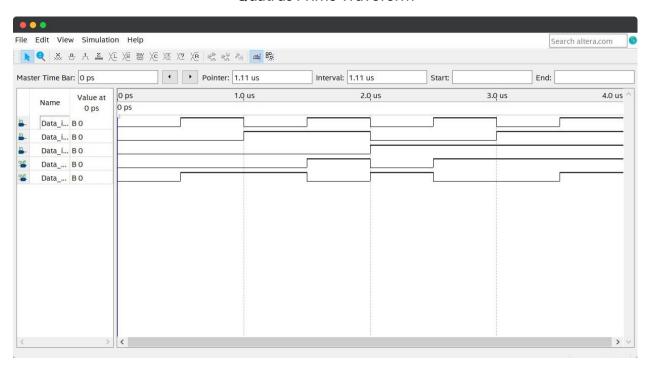
Verilog Code

```
1 module twos(a1, a2, a3, a4, o1, o2, o3, o4);
2
3    input a1, a2, a3, a4;
4    output o1, o2, o3, o4;
5    wire c1, c2, c3, c4;
6    assign c0 = 1;
7    half_adder hal(.a(~a1), .b(c0), .sum(o1), .carry(c1));
8    half_adder ha2(.a(~a2), .b(c1), .sum(o2), .carry(c2));
9    half_adder ha3(.a(~a3), .b(c2), .sum(o3), .carry(c3));
10    half_adder ha4(.a(~a4), .b(c3), .sum(o4), .carry(c4));
11
12 endmodule
13
```



Question 3

Verilog Code



Question 4

Verilog Code

