ECEN 5613 | **Embedded System Design** | **Fall 2022**

Lab #2 Signoff Sheet

You will need to obtain the signature of your instructor or TA on the following items in order to receive credit for your lab assignment. Signatures are due by **Friday, September 23, 2022 (Part 1 Elements) and Friday, September 30, 2022 (Part 2 Elements)**.

Print your name below, sign the honor code pledge, and then demonstrate your working hardware & firmware in order to obtain the necessary signatures.

Student Name: Anuja M

Honor Code Pledge: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. I have clearly acknowledged work that is not my own."

Student Signature: [signature]

Signoff Checklist

Part 1 Required Elements

- ☑ Schematic of acceptable quality, correct memory map, SPLD .PLD file
- ☑ Pins and signals labeled, decoupling capacitors, and two 28-pin wire wrap sockets present on board
- ☑ NVRAM (as EPROM substitute), decode logic, and LED functional
- ☑ Understands device programmer.
- ☑ Demonstrated ability to use logic analyzer to capture bus cycles and view fetches from NVRAM. Shows detailed knowledge of both state and timing modes. Captures latched address lines A[15:0], data lines D[7:0], ALE, /PSEN, and NVRAM chip select signal on the logic analyzer display.
- ☑ Shows and discusses logic analyzer screen captures:
- ☑ Assembly program and timer ISR functional:

[signature] 09/23/22

TA signature and date

Part 2 Required and Supplemental Elements

- ☑ AT89C51RC2, RS-232, and FLIP functional
- ☐ 74LS374 debug port functional
- ☐ Understands timing analysis, setup/hold/propagation
- ☑ ARM code build process, LED program, version control
- ☑ EFM8 functional, Lab 1 code ported successfully

Sakharade 09/30/22

TA signature and date

Instructor/TA Comments: ☐ ☐ ☐

FOR INSTRUCTOR USE ONLY **Part 1 Elements**	Not Applicable	Poor/Not Complete	Meets Requirements		Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☑		☐	☐
Hardware physical implementation	☐	☐	☐	✓	☐	☐
Part 1 Required Elements functionality	☐	☐	☐		☑	☐
Sign-off done without excessive retries		☐	☑	✓		
Student understanding and skills	☐	☐	☐		☐	☐
Overall Demo Quality (Part 1 Elements)	☐	☐	☐	✓	☐	☐

FOR INSTRUCTOR USE ONLY **Part 2 Elements**	Not Applicable	Poor/Not Complete	Meets Requirements		Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☐	✓	☐	☐
Hardware physical implementation	☐	☐	☐	✓	☐	☐
Part 2 Required Elements functionality	☑	☐	☐		☑	☐
Supplemental Elements functionality		☐	☑			
Sign-off done without excessive retries	☐	☐	☐		☑	☐
Student understanding and skills						
Overall Demo Quality (Part 2 Elements)	☐	☐	☐	✓	☐	☐

NOTE: This signoff sheet should be the top/first sheet of your submission.

E + I Logic analyzer shows correct results and program is functional.

[-] Schematic is missing some connections (SPLD - NVRAM, for example)

[+] Good use of the lab tools to validate the design.

[-] A bit more practice with the LA will work great for later signoffs.

Lab 2 Part 2 Signoff (09/30/22)

(+) Recommended part from part 1 completed.

Frequency = 0.3 Hz.

(+) ~~SPI~~ STM 32 Code

(+) LED blinks at correct frequency (TIM2 interrupt used)

(+) Blue, Green LEDs toggle ~~at 1sec period~~ with period of 1sec

switch turns of the toggling (Interrupt used).

(+) Version Control done using Github.

(+) EFM Code ported ~~as~~ successfully