ECEN 5613 **Lab #4 Signoff Sheet** **Fall 2022**

You will need to obtain the signature of your TA on the following items in order to receive credit for your lab assignment. Print your name below, sign the honor code pledge, and then demonstrate your working hardware & firmware in order to obtain the necessary signatures.

Student Name: Anohya.L

Honor Code Pledge: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. I have clearly acknowledged work that is not my own."

Student Signature: Anohya.L

Signoff Checklist

Part 1 Elements

- ☑ Pins and signals labeled and decoupling capacitors present on board
- ☑ C code for EEPROM functional, contents present after power cycle
- ☑ I²C diagram/timing analysis

Manas MD (11/16/22)

TA signature and date

Part 2 Elements

- ☑ LCD functional, C code for basic LCD routines functional
- ☑ LCD control signal timing meets specifications (logic analyzer trace/diagram, analysis)
- ☑ Elapsed time stop, restart, reset to "00:00.0":
- ☑ Good integration with previous code, all functions work, no irregularities

Manas MD (11/19/22)

Part 3 Required and Supplemental Elements

- ☑ LCD Hex/DDRAM/CGRAM dumps, custom LCD characters, fun logo
- ☐ SPI interface, logic analyzer trace, compare with I²C
- ☑ ARM code development, 2 new features, ISR (1 feature)
- ☐ PCF8574 I²C I/O Expander, input, output, ISR

Manas MD (11/19/22)

FOR TA/INSTRUCTOR USE ONLY
Part 1 Elements

	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☐	☑ ✓	☐
Hardware physical implementation	☐	☐	☐	☑ ✓	☐
Required Elements functionality	☐	☐	☑		☐
Sign-off done without excessive retries		☐	☐ ✓		
Student understanding and skills	☐	☐	☐	☐ ✓	☐
Overall Demo Quality (Part 1 elements)	☐	☐	☐	☐	☐

FOR TA/INSTRUCTOR USE ONLY
Part 2 Elements

	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☐	☑ ✓	☐
Hardware physical implementation	☐	☐	☐	☑ ✓	☐
Required Elements functionality	☐	☐	☑		☐
Sign-off done without excessive retries		☐	☐	✓	
Student understanding and skills	☐	☐	☐	✓	☐
Overall Demo Quality (Part 2 elements)	☐	☐	☐	☐	☐

FOR TA/INSTRUCTOR USE ONLY
Part 3 Elements

	Not Applicable	Below Expectation	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☐	☑ ✓	☐
Hardware physical implementation	☐	☐	☐	☑ ✓	☐
Required Elements functionality	☐	☐	☑		☐
Supplemental Elements functionality		☐	☐ ✓		
Sign-off done without excessive retries		☐	☐	☑ ✓	
Student understanding and skills	☐	☐	☐	☐ ✓	☐
Overall Demo Quality (Part 3 elements)	☐	☐	☐	☐	☐

TA/Instructor Comments ☐☐☐

Lab 4 Part 1 Signoff (11/16/22)

(+) Neat Schematic
(+) I2C read, write verified
(+) Hexdump verified.
(+) Reset Sequence Verified
(+) Power cycle & EEPROM values are retained.
(+) Timing analysis presented.

Lab 4 Part 2 Signoff (11/19/22)

(+) Neat Schematic
(+) LCD putstring, go to address, go to xy working
(+) All clock functions working fine.
(+) No skew observed. Very good clock implementation
(+) Good UI.
(-) UART missing characters due to frequent timer interrupts
(+) Timing analysis presented.

Lab 4 Part 3 Signoff (11/28/22)

(+) LCD custom dump presented. LCD logo, custom characters verified.
(+) SPI DAC functional but only on logic analyzer. SPI output not seen on Oscilloscope.
(+) STM32 features
→ WDT
~~RTC not working~~
→ RTC