Anuj Sarode

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Summary

Graduate student in Electrical and Electronics Engineering currently seeking internship opportunities to further develop skills in semiconductor device fabrication and advanced packaging technologies.

Education

Master of Science in Electrical and Electronics Engineering **GPA: 4.00/4.00**

Arizona State University, Arizona, United States *August 2025 - June 2027 (Expected)*

Relevant Coursework: CMOS and MEMS fabrication, Semiconductor Heterogenous Integration, Advance Semiconductor Packaging

Bachelor of Technology in Avionics **GPA: 7.71/10**

Indian Institute of Space Science and Technology, Thiruvananthapuram, India *June 2012 - May 2016*

Technical Skills

System Operation: Wafer Bonder, Flipchip Bonder, Wire bonder, Plasma Cleaning system, Parallel Gap welders, Pull Tester

Programming and engineering software: MATLAB, kLayout, PHP, MySQL, Python, HTML, SolidWorks, Silvaco, Advance Package Designer

Productivity Tools: Microsoft Word, PowerPoint, Excel, LaTeX

Professional Experience

Space Application Center, Indian Space Research Organization, India **July 2016 - July 2025**

Engineer; promoted to Scientist/Engineer "SE" ***July, 2024 - July 2025***

- Worked on developing and optimizing wafer bonding processes—metal–metal thermocompression, $LiNbO_3$-on-silicon (direct/adhesive), temporary BEOL bonding, and anodic sealing to support Wafer level packaging, photonics and MEMS applications at the Space Applications Center.
- Designed calibration wafer with fiducial using KLayout for wafer bonder camera and backlash calibration to improve process yield, saving significant time in procurement.
- Determined feasibility of the assembly process on Metal Matrix Composite (Silver-Diamond) to improve the thermal performance of high-power devices for future RF amplifier assembly.
- Developed flip-chip die attach process for Indium and SAC solder-based high-density chips for space qualified assembly.
- Conducted market analysis and authored RFPs ($\sim$ 300K) for photonic assembly equipment, and managed acquisition of cleanroom supplies ($\sim$\$80k) to ensure continuous lab operations.

Engineer; promoted to Scientist/Engineer "SD" ***July, 2020 - June, 2024***

- Implemented a silver sintering process to improve thermal dissipation in high-power amplifiers, replacing a gold-based method and reducing turnaround time by 40% and cost by 30%.
- Developed Au stud bonding process, including bumping using automated wire bonder, coining, and flip-chip bonding of bumped devices using flip-chip bonder for assembly of RF MMICs.
- Engineered a novel package design and hermetic sealing process using new materials, reducing turnaround time by $\sim$50% and process cost by $\sim$20%.
- Served as the key liaison with four external suppliers for outsourced micro-electronics assembly workload ($\sim$\$100,000 annual budget) from July 2020 to July 2025, ensuring schedule adherence and quality compliance.
- Establishment and maintenance of the auxiliary support systems, such as chiller, compressor and Nitrogen generator for advance packaging equipment.
- Identified and trained a team of three technicians for the daily operation of an automatic wire bonder-F&S 5600 and wafer bonder-AWB-04, achieving higher throughput by skill development of the technicians.

- Involved in Package Design Review, creation and approval of fabrication sequences for assembly of RF satellite subsystems.

Engineer; Scientist/Engineer "SC" ***July, 2016 - June, 2020***

- Led new process introduction for automated wire bonding on gold pads of GaAs and GaN chips by designing experiments, optimizing process parameters, and collaborating with QA, achieving 99% yield and 3× throughput compared to manual methods.
- Developed micro-assembly processes for Multi-Chip Modules on multi-layer radio frequency substrates for ISRO satellites.
- Received certification for ISRO-PAX-305, high reliability (based on MIL-STD-883) assembly from ISRO.

Leadership

- Led cross-functional team of 7 engineers from Aug 2022 to July 2025 on SAW device WLP project, managing schedules, budgets, and stakeholder communication; presented progress reports and financial tracking to review committees.
- Supervised 8-member technician team and served as liaison with project stakeholders from July 2020 to July 2025; resolved technical challenges, interpersonal conflicts, and ensured equipment readiness for space-qualified subsystem assembly for Chandrayaan-2 (Lunar Exploration Mission), Communication, and Remote Sensing payloads.
- Organized astronomy and astrophotography events through the outreach program of the Space Application Center to motivate school students for STEM education, astronomy, and astrophotography.
- Member of the technical committee for the special program for School Children called "Young Scientist Program" for the year 2025, sharing responsibility of managing a total of 51 students and technical programs.