AHBAPB Bridge Design

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INTRODUCTION

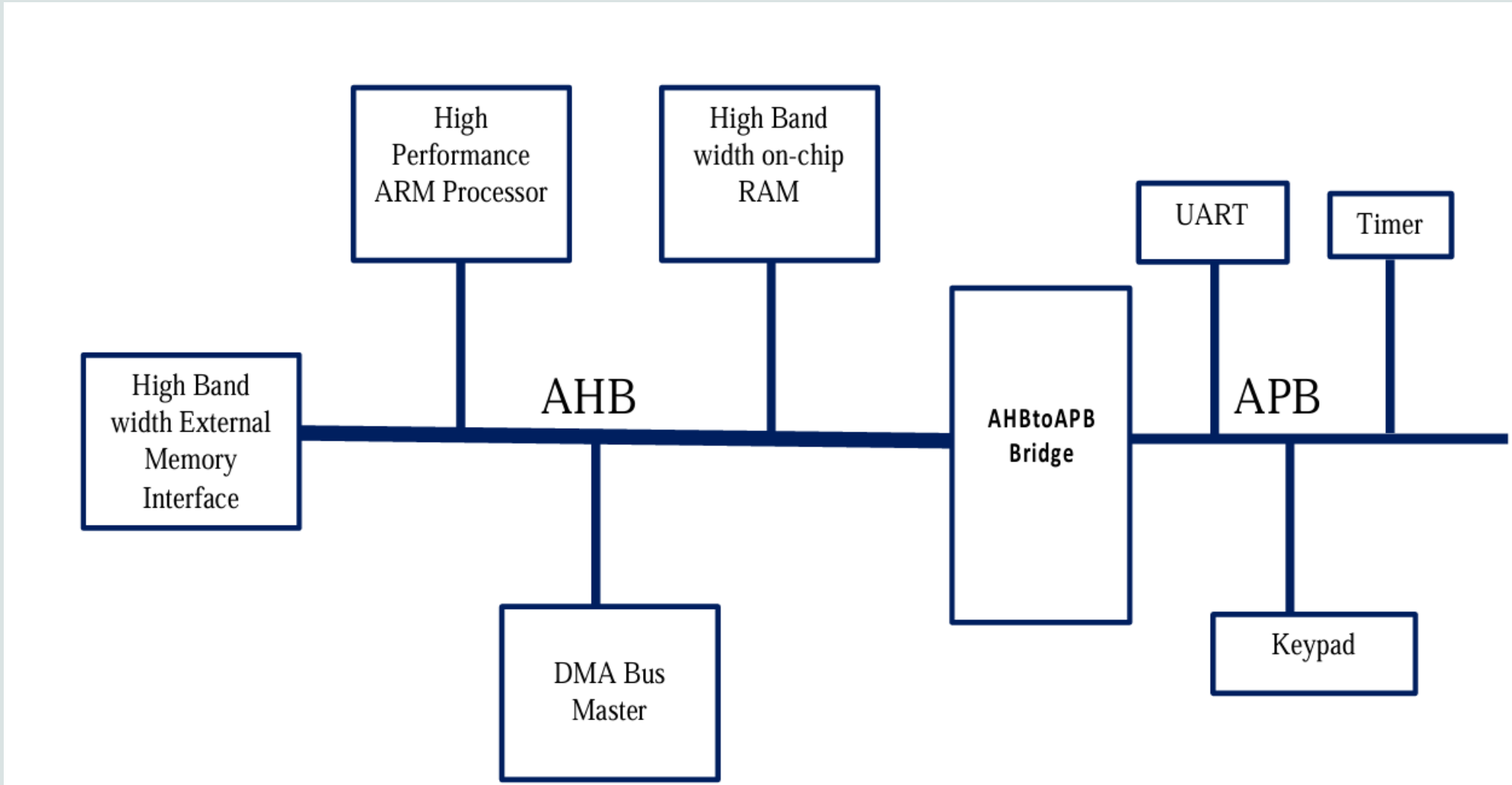
The ARM Advanced Microcontroller Bus Architecture (AMBA) is an open-standard, on-chip interconnect specification for the connection and management of functional blocks in system on-a-chip (SoC) designs. It facilitates the development of multi-processor designs with large numbers of controllers and components with a bus architecture. Today, AMBA is widely used on a range of ASIC and SoC parts including applications processors used in modern portable mobile devices like smartphones.

AMBA AHB is a bus interface suitable for high-performance synthesizable designs. It defines the interface between components, such as masters, interconnects, and slaves. AMBA AHB implements the features required for high-performance, high-clock frequency systems including:

- Burst transfers.
- Single clock-edge operation.
- Non-tristate implementation.
- Wide data bus configurations, 64, 128, 256, 512, and 1024 bits.

The most common AHB slaves are internal memory devices, external memory interfaces, high bandwidth peripherals, and a bridge to a narrower APB bus on which the lower bandwidth peripheral devices are located, as shown in the figure below. AHB is widely used on ARM7, ARM9 and ARM Cortex-M-based designs. A simple transaction on the AHB consists of an address phase and a subsequent data phase (without wait states: only two bus cycles).

The AMBA APB is designed for low bandwidth control accesses, for example, register interfaces on system peripherals such as Timers, UART, and GPIO. This bus has an address and data phase similar to AHB, but a much reduced, low-complexity signal list (for example no bursts). Furthermore, it is an interface designed for a low-frequency system with a low bit width (32 bits). It is optimized for minimal power consumption and reduced interface complexity.



Typical AMBA System

AHB Protocol

The AMBA AHB bus protocol is designed to be used with a central multiplexor interconnection scheme. Using this scheme all bus masters drive out the address and control signals indicating the transfer they wish to perform and the arbiter determines which master has its address and control signals routed to all of the slaves. A central decoder is also required to control the read data and response signal multiplexor, which selects the appropriate signals from the slave that is involved in the transfer.

Before an AMBA AHB transfer can commence the bus master must be granted access to the bus. This process is started by the master asserting a request signal to the arbiter. Then the arbiter indicates when the master will be granted use of the bus.

A granted bus master starts an AMBA AHB transfer by driving the address and control signals. These signals provide information on the address, direction and width of the transfer, as well as an indication if the transfer forms part of a burst. A write data bus is used to move data from the master to a slave, while a read data bus is used to move data from a slave to the master.

Every transfer consists of:

- an address and control cycle
- one or more cycles for the data.

The address cannot be extended and therefore all slaves must sample the address during this time. The data, however, can be extended using the HREADY signal. When LOW this signal causes wait states to be inserted into the transfer and allows extra time for the slave to provide or sample data.

APB Protocol

AMBA APB provides a low-cost interface that is optimized for minimal power consumption and reduced interface complexity. The APB interfaces to any peripherals that are low bandwidth and do not require the high performance of a pipelined bus interface. The APB has an unpipelined protocol.

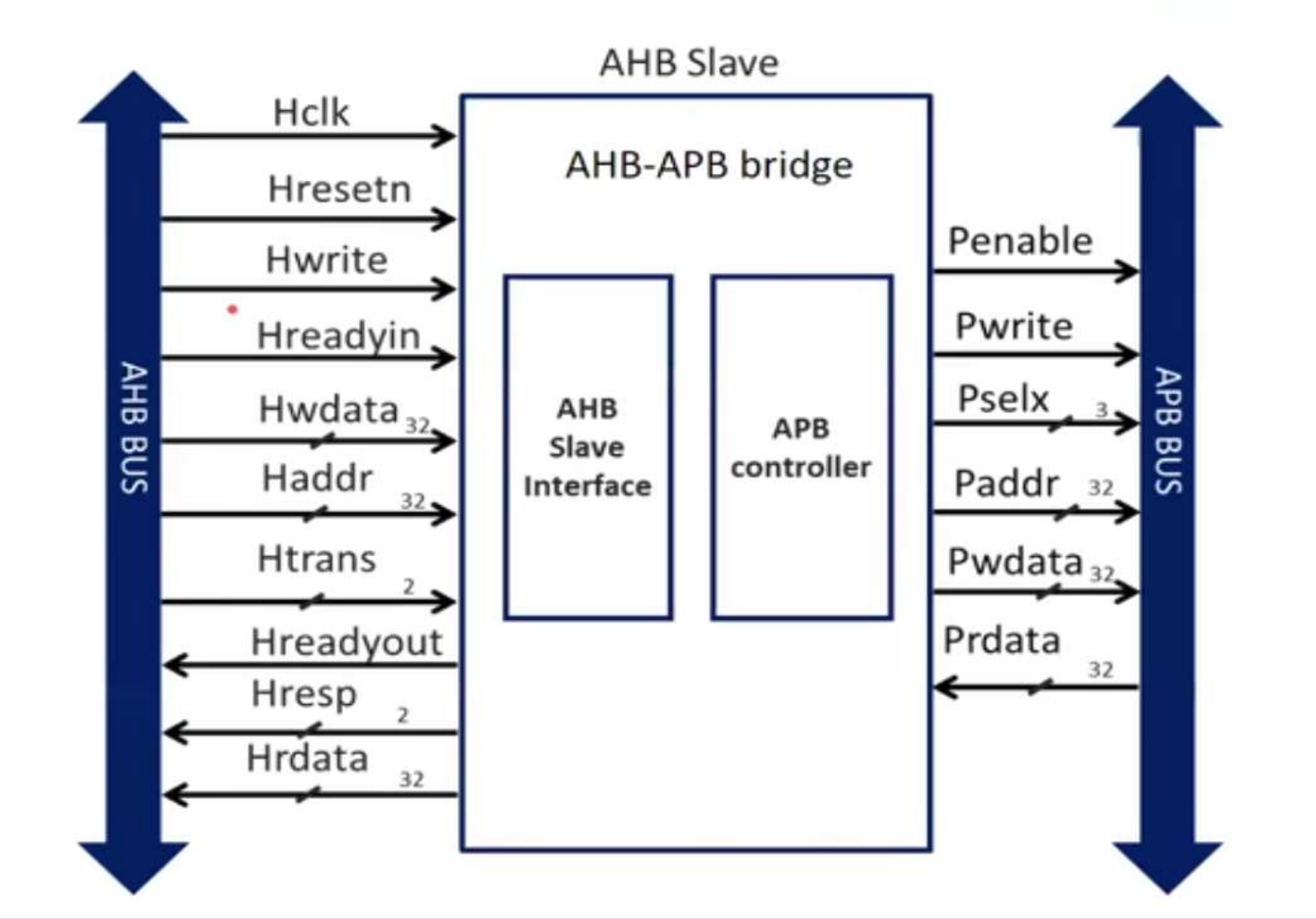
All signal transitions are only related to the rising edge of the clock to enable the integration of APB peripherals easily into any design flow. Every transfer takes two cycles in AMBA2, APB or more cycles in the later releases.

AHB to APB Bridge

The AHBtoAPB Bridge is an AHB slave, providing an interface between the high-speed AHB and the low-power APB. Read and write transfers on the AHB are converted into equivalent transfers on the APB. As the APB is not pipelined, then wait states are added during transfers to and from the APB when the AHB is required to wait for the APB.

The AHB to APB bridge translates signals and protocols from the AHB to the APB, allowing devices on the AHB to communicate with peripherals on the APB. Since the AHB operates at a higher speed with more complex operations (e.g., pipelining, burst transfers), and the APB is simpler and slower, the bridge handles the necessary conversions to maintain smooth communication.

Block Diagram



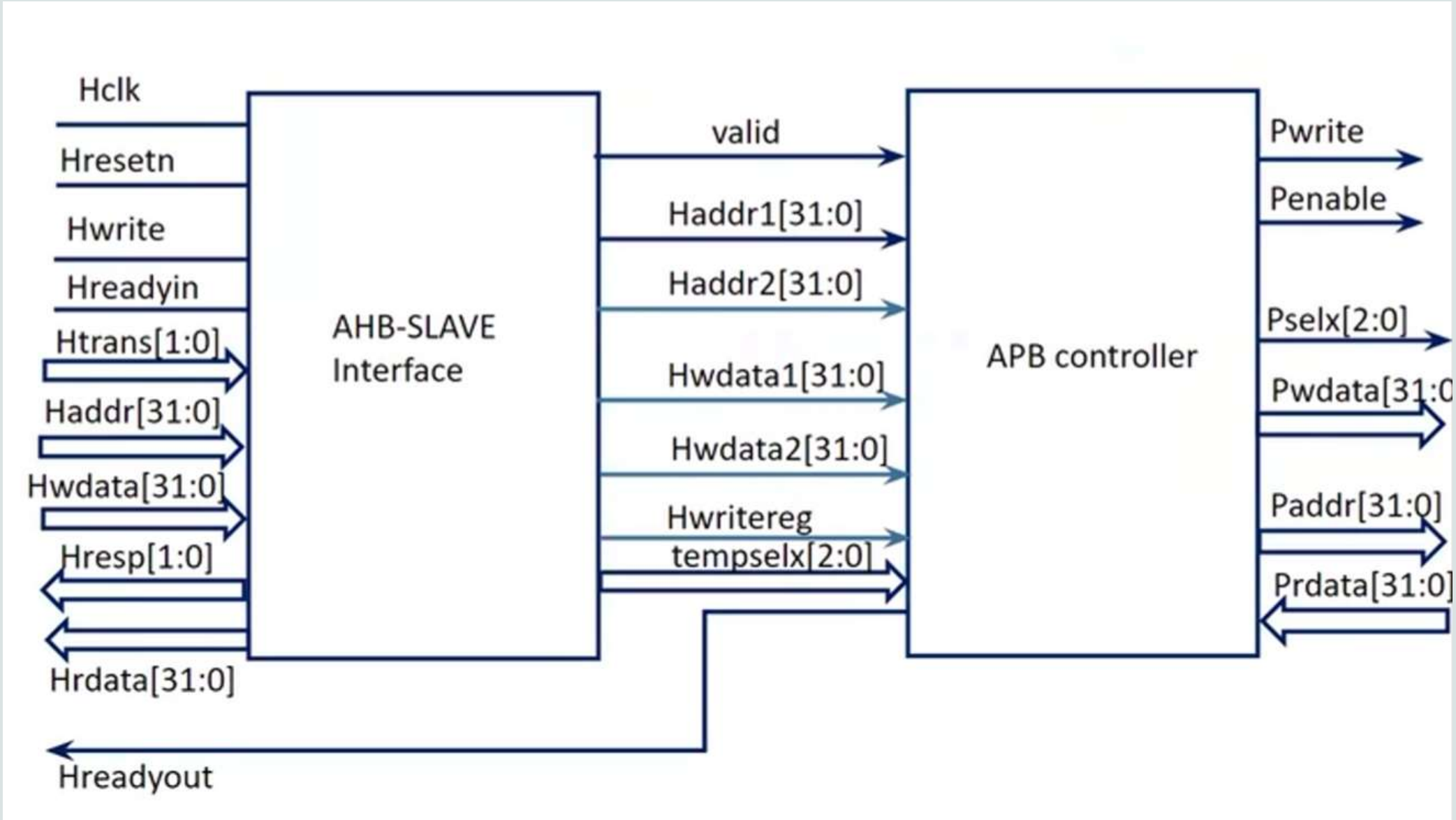
Specifications : AHB Signals

Signal Name	Description
HCLK	This clock times all bus transfers. All signal timings are related to the rising edge of HCLK.
HRESET	The bus reset signal is active LOW and is used to reset the system and the bus. This is the only active LOW signal.
HADDR	The 32-bit system address bus.
HTRANS	Indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.
HWRITE	When HIGH this signal indicates a write transfer and when LOW a read transfer.
HRDATA	The write data bus is used to transfer data from the master to the bus slaves during write operations. A minimum data bus width of 32 bits is recommended. However, this may easily be extended to allow for higher bandwidth operation.

Signal Name	**Description**
HRDATA	The read data bus is used to transfer data from bus slaves to the bus master during read operations. A minimum data bus width of 32 bits is recommended. However, this may easily be extended to allow for higher bandwidth operation.
HREADY	When HIGH the HREADY signal indicates that a transfer has finished on the bus. This signal may be driven LOW to extend a transfer. Note: Slaves on the bus require HREADY as both an input and an output signal.
HRESP	The transfer response provides additional information on the status of a transfer. Four different responses are provided, OKAY, ERROR, RETRY and SPLIT.

Specifications : APB Signals

Signal Name	Description
PENABLE	This strobe signal is used to time all accesses on the peripheral bus. The enable signal is used to indicate the second cycle of an APB transfer. The rising edge of PENABLE occurs in the middle of the APB transfer.
PADDR	This is the APB address bus, which may be up to 32-bits wide and is driven by the peripheral bus bridge unit.
PWRITE	When HIGH this signal indicates an APB write access and when LOW a read access.
PRDATA	The read data bus is driven by the selected slave during read cycles (when PWRITE is LOW). The read data bus can be up to 32-bits wide.
PWDATA	The write data bus is driven by the peripheral bus bridge unit during write cycles. The write data bus can be up to 32-bits wide.
PSELx	A signal from the secondary decoder, within the peripheral bus bridge unit, to each peripheral bus slave x. This signal indicates that the slave device is selected and a data transfer is required. There is a PSELx signal for each bus slave.


Hclk
Hresetn
Hwrite
Hreadyin
Htrans[1:0]
Haddr[31:0]
Hwdata[31:0]
Hresp[1:0]
Hrdata[31:0]
AHB-SLAVE
Interface
valid
Haddr1[31:0]
Haddr2[31:0]
Hwdata1[31:0]
Hwdata2[31:0]
Hwritereg
tempselx[2:0]
APB controller
Pwrite
Penable
Pselx[2:0]
Pwdata[31:0]
Paddr[31:0]
Prdata[31:0]
Hreadyout

Conclusion

The AHB to APB bridge is a vital component in VLSI and SoC designs, enabling efficient communication between high-speed and low-speed subsystems. Understanding this bridge involves grasping the intricacies of both the AHB and APB protocols, including how they differ in complexity, speed, and operation. By studying the AHB to APB bridge, one gains insight into protocol conversion, address decoding, and timing synchronization, all of which are crucial for optimizing system performance and power efficiency. This knowledge forms a foundational understanding of how complex digital systems integrate and interact, which is essential for anyone working in the field of VLSI design.