Board 2 Report: Switching noise with good and bad layout

Objective:

The objective of this report is to compare the effects of good and bad PCB layout practices on switching noise in a hex inverter circuit. By designing one circuit with a continuous return plane and properly placed decoupling capacitors, and another with a routed ground trace and distant decoupling capacitors, we aim to demonstrate how layout decisions impact signal integrity and electromagnetic interference.

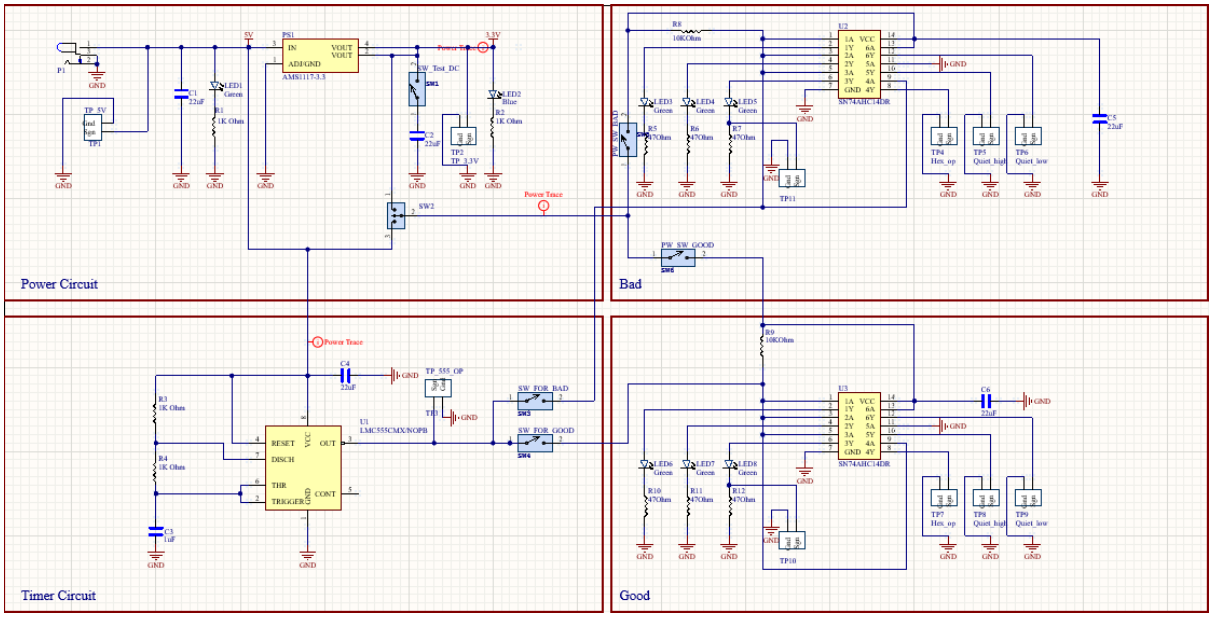
Bill of Materials:

	Item Details				
	Line #	Name	Description	Designator	Quantity
1		22uF	22uF ±10% 25V X5...	C1, C2, C4, C5, C6	5
2		1uF	MULTILAYER CERA...	C3	1
3		Green	Green 513~528nm...	LED1, LED3, LED4, L...	7
4		Blue	blue 1206 Light Em...	LED2	1
5		Power Jack	Power Barrel Connec...	P1	1
6		AMS1117-3.3	LOW DROPOUT RE...	PS1	1
7		1k	CHIP RESISTOR - SU...	R1, R2, R3, R4	4
8		47 Ohms	47Ω ±5% 0.25W ±2...	R5, R6, R7, R10, R11...	6
9		10k	10 kOhms ±5% 0.2...	R8, R9	2
10		SW_2Pin_100mil_Switch	2Pin Header	SW1, SW3, SW4, SW...	5
11		PREC003SAAN-RC	Connector Header T...	SW2	1
12		TP_5V	Test Point 300 mil ce...	TP1	1
13		10x Probe TP	Test Point 300 mil ce...	TP2, TP3, TP4, TP5,...	10
14		LMC555CMX/NOPB	555 Type, Timer/Osc...	U1	1
15		SN74AHC14DR	Inverter IC 6 Chann...	U2, U3	2

Altium Schematics:

The circuit consists of a power circuit, a timer circuit, and two hex inverter circuits one designed using best layout practices and the other intentionally designed with poor layout techniques.

Test points will help in measuring rise time, fall time, switching noise and signal integrity across both the good and bad layout designs.

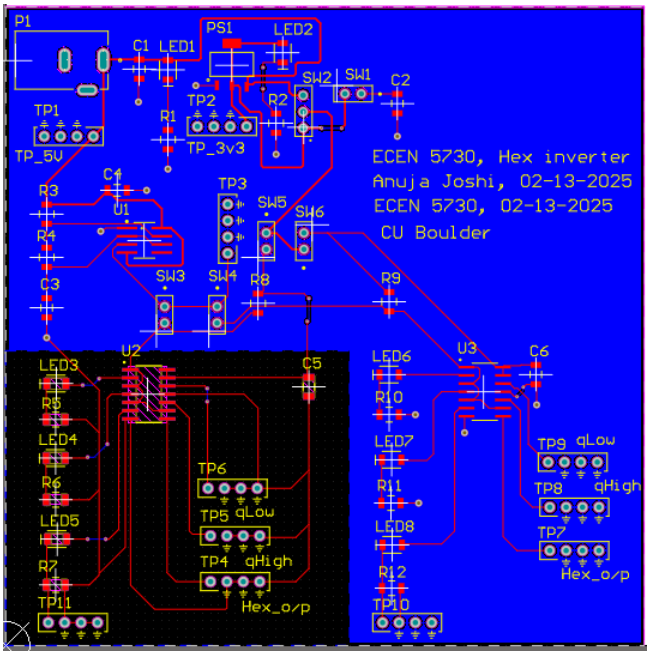


Board layout:

A critical design element in this project is the intentional layout differences:

The "good" layout features a continuous ground plane and decoupling capacitors placed close to the IC power pins to minimize switching noise.

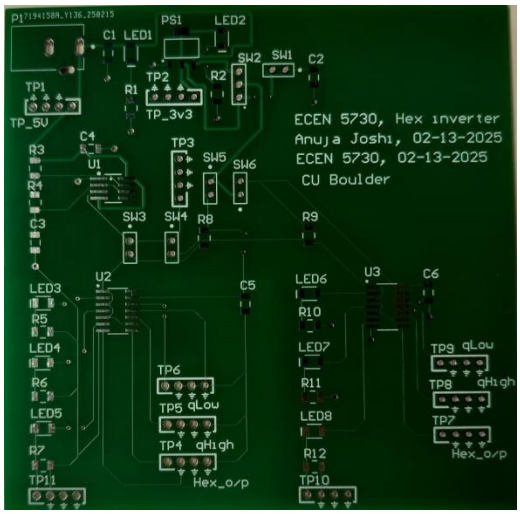
The "bad" layout lacks a ground plane, instead using a routed ground trace, and has its decoupling capacitor placed far from the IC, demonstrating the adverse effects of poor layout decisions.

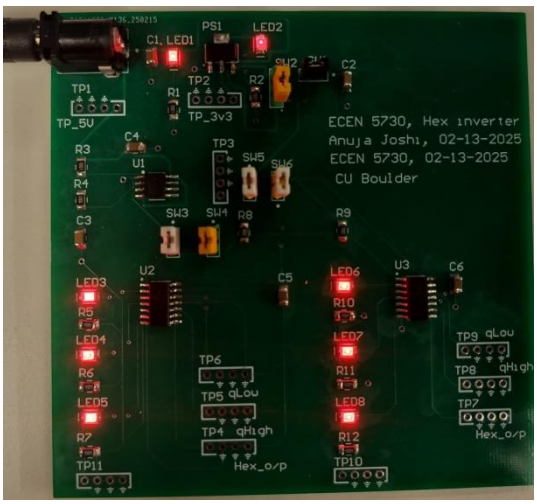


Board picture:

The images below showcase the PCB before assembly (left) and the fully assembled, powered-on board (right).

Switches are used to toggle between 3.3V and 5V for the hex inverters and to isolate either the good or bad circuit, ensuring only one is active at a time. This setup minimizes interference and allows for accurate measurement of switching noise and performance differences.





Working and Testing

The board functionality was verified step by step using designated test points to ensure correct operation and to analyze the impact of PCB layout choices. The following measurements were performed:

1. Verified 5V at TP1 to confirm the correct power supply input.
2. Checked 3.3V at TP2 after the LDO to ensure proper voltage conversion.
3. Measured 555 timer output at TP3

Bad Circuit Testing (Poor Layout Effects)

4. Measured Hex inverter output at TP4
5. Measured noise at Quiet High input (TP5)
6. Measured noise at Quiet Low input (TP6)

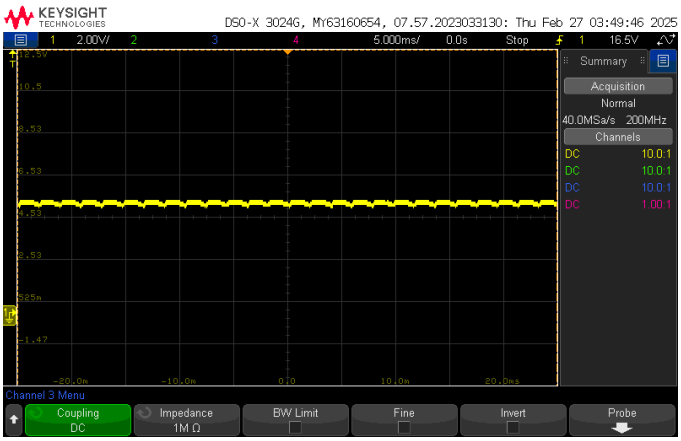
Good Circuit Testing (Optimized Layout Effects)

7. Measured Hex inverter output at TP7
8. Measured noise at Quiet High input (TP8)
9. Measured noise at Quiet Low input (TP9)

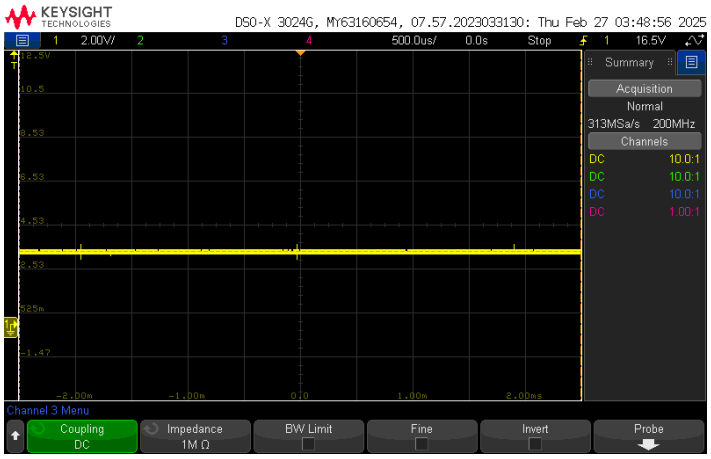
These tests provided a direct comparison between the good and bad PCB layouts, demonstrating how proper grounding, decoupling capacitor placement, and return paths impact switching noise and signal integrity.

Scope shots:

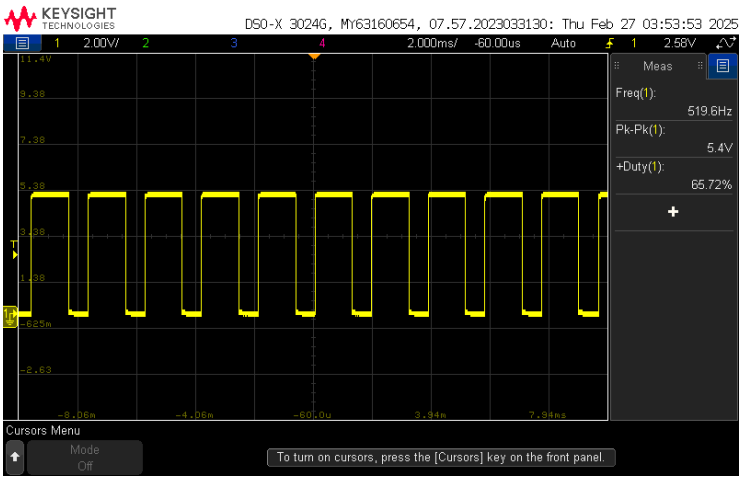
1. TP1: Power at TP1



2. TP2: LDO output 3.3V



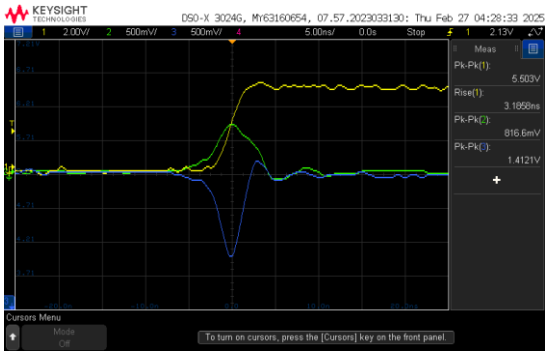
3. TP3: 555 output

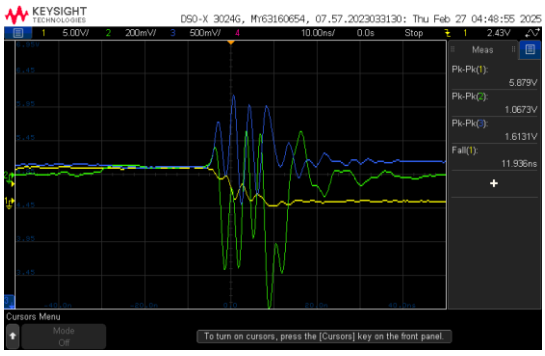


4. Bad Circuit(5V and 3.3V):

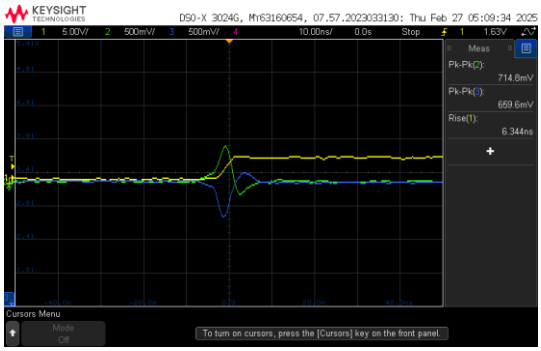
4.1 Rise time and fall time observations:

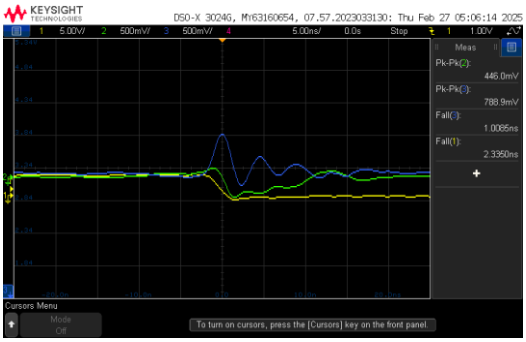
Observations for 5V:





Observations for 3.3V:





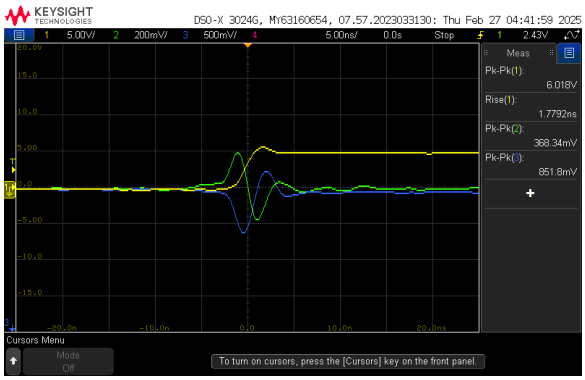
	Rise time	q_low	q_high
5V	3.1858ns	816.6mV	1.4121V
3.3V	6.344ns	714.8mV	659.6mV

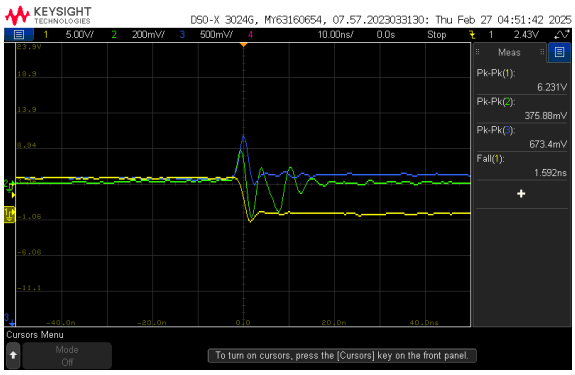
	Fall time	q_low	q_high
5V	11.936ns	1.0673V	1.6131V
3.3V	2.3350ns	446mV	788.9mV

5. Good Circuit(5V and 3.3V):

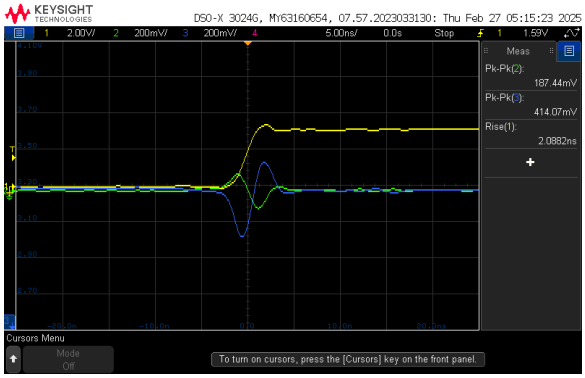
5.1 Rise time and fall time observations:

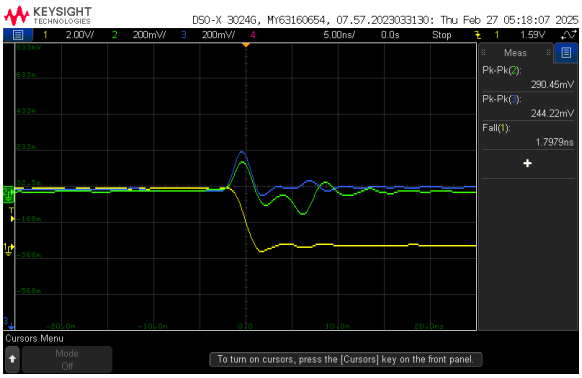
Observations for 5V:





Observations for 3.3V:





	Rise time	q_low	q_high
5V	1.7792ns	368.34mV	851.8mV
3.3V	2.0882ns	187.44mV	414.07mV

	Fall time	q_low	q_high
5V	1.592ns	375.88mV	673.4mV
3.3V	1.7979ns	290.45mV	244.22mV

Explanation:

	Bad Circuit Rise Time	Good Circuit Rise Time	Improvement in Good Circuit
5V	3.1858ns	1.7792mV	44.2%
3.3V	6.344ns	2.0882mV	67.1%

The good circuit shows a significantly faster rise time than the bad circuit for both 5V and 3.3V operations.

The slow rise time in the bad circuit is due to poor grounding and improper decoupling.

	Bad Circuit Fall Time	Good Circuit Fall Time	Improvement in Good Circuit
5V	11.936ns	1.592mV	86.6%
3.3V	2.3350ns	1.7979mV	22.9%

The good circuit significantly improves fall time, making transitions much faster.

Noise comparison:

- The good circuit significantly reduces noise on q_low and q_high signals, demonstrating better signal integrity.
- Noise is reduced by up to 73.8% on q_low and 69% on q_high, proving the effectiveness of proper PCB layout practices.
- The bad layout suffers from higher noise due to longer return paths, increased ground impedance, and improper decoupling capacitor placement.

What Did Not Work & Challenges Faced:

1. Incorrect Switch Placement Initially: The initial switch placement did not fully isolate the good and bad circuits as intended. After the CDR the switch positions were corrected to ensure complete isolation, allowing accurate comparisons between the two layouts.
2. Poor Labelling on PCB: The lack of clear labelling on the PCB made it difficult to identify test points, requiring frequent reference to the schematic. This reduced efficiency while taking measurements and will be improved in future designs with better silkscreen labelling.
3. Excessive Use of Cross under**:** The design incorporated multiple cross under, which is not a good PCB layout practice, as it can introduce additional inductance and signal integrity issues. In future designs, better component placement and optimized routing will be used to minimize the need for vias, improving overall board performance.

Conclusion:

This project successfully demonstrated the impact of PCB layout decisions on switching noise, signal integrity, and circuit performance**.** By comparing a well-designed layout with a poorly implemented one**,** we observed significant differences in rise time, fall time, and noise levels. The good layout**,** which incorporated a continuous ground plane and properly placed decoupling capacitors, resulted in faster transitions and significantly reduced noise, while the bad layout exhibited higher noise, slower transitions, and degraded signal integrity due to improper grounding and capacitor placement.

Key learnings:

1. Importance of Proper PCB Layout: A continuous ground plane and well-placed decoupling capacitors significantly reduce switching noise and improve signal integrity.

2. Effect of Poor Design Practices: Routing ground as a trace and placing decoupling capacitors far from ICs results in higher noise, slower transitions, and degraded performance.

3. Impact on Rise and Fall Times: The good layout improved rise time by up to 67% and fall time by up to 86%, proving that proper design minimizes parasitic effects.

4. Significance of Noise Reduction: The good circuit reduced noise levels by up to 73.8% at quiet high/low inputs, reinforcing the need for optimal layout strategies.

5. Switch Placement Matters: Properly positioning switches ensures complete circuit isolation, preventing interference and enabling accurate comparisons.

6. Labelling and Readability Improve Efficiency: Poor labelling on the PCB led to measurement inefficiencies, highlighting the importance of clear silkscreen markings for test points.

7. Minimizing Excessive Vias: Reducing unnecessary vias improves signal integrity and board reliability, emphasizing the need for better component placement in future designs.