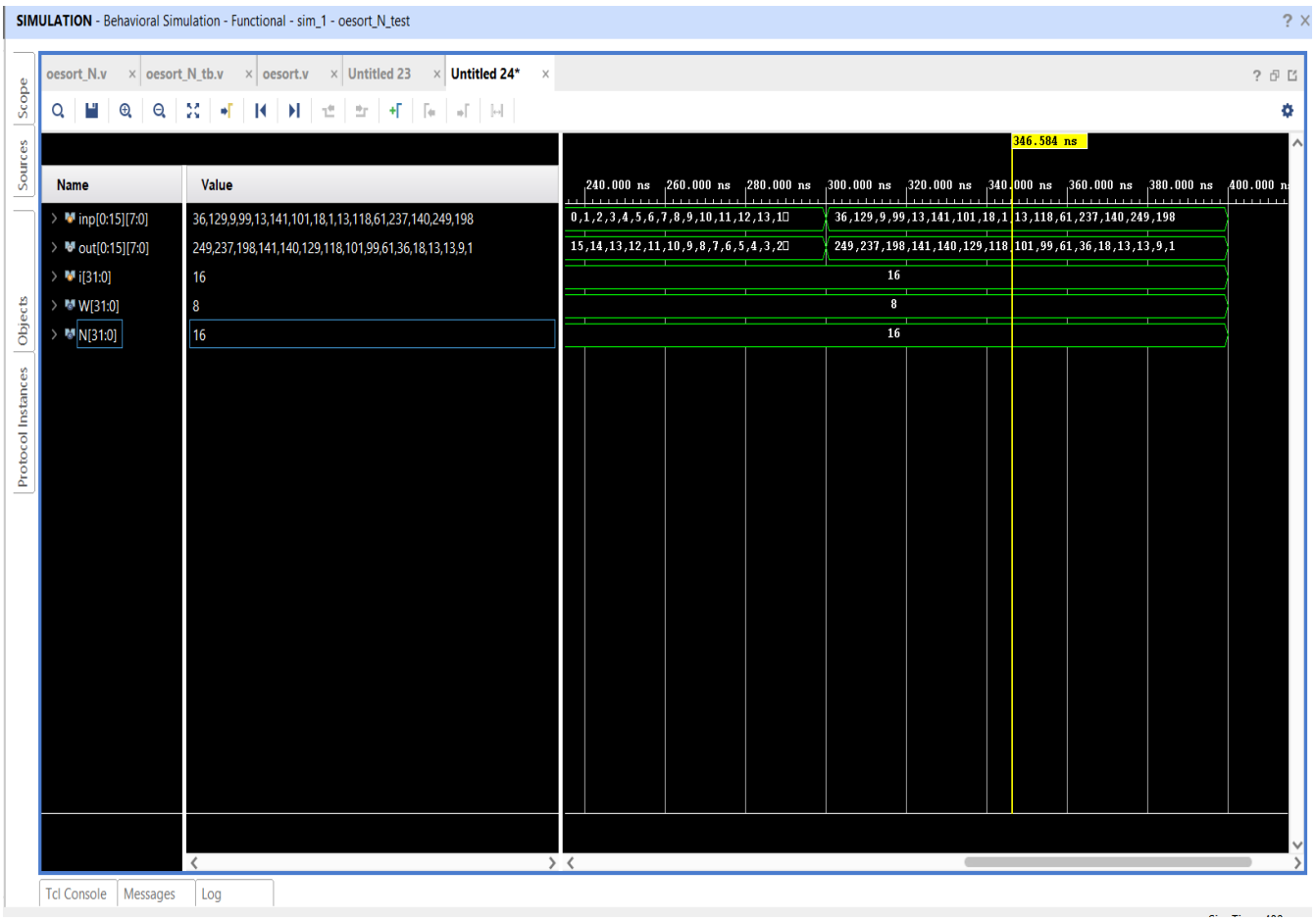
Report 1

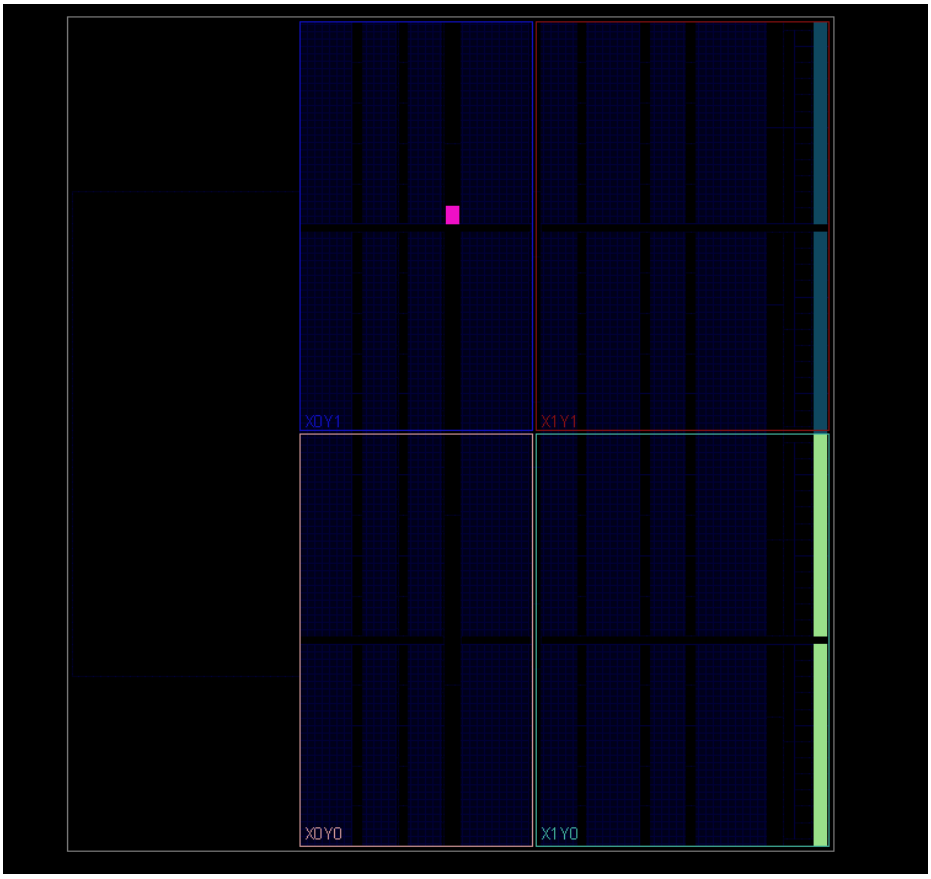
The link to my github account is https://github.com/anujp10/EE_599_aspatil_5704035814.git

1. For N = 16

Waveform



Schematic



Power

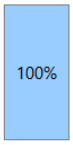
Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.09 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.0°C**
Thermal Margin:	74.0°C (6.2 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	High

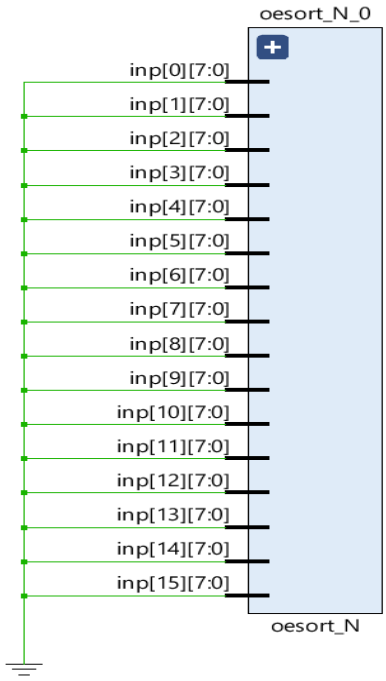
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power



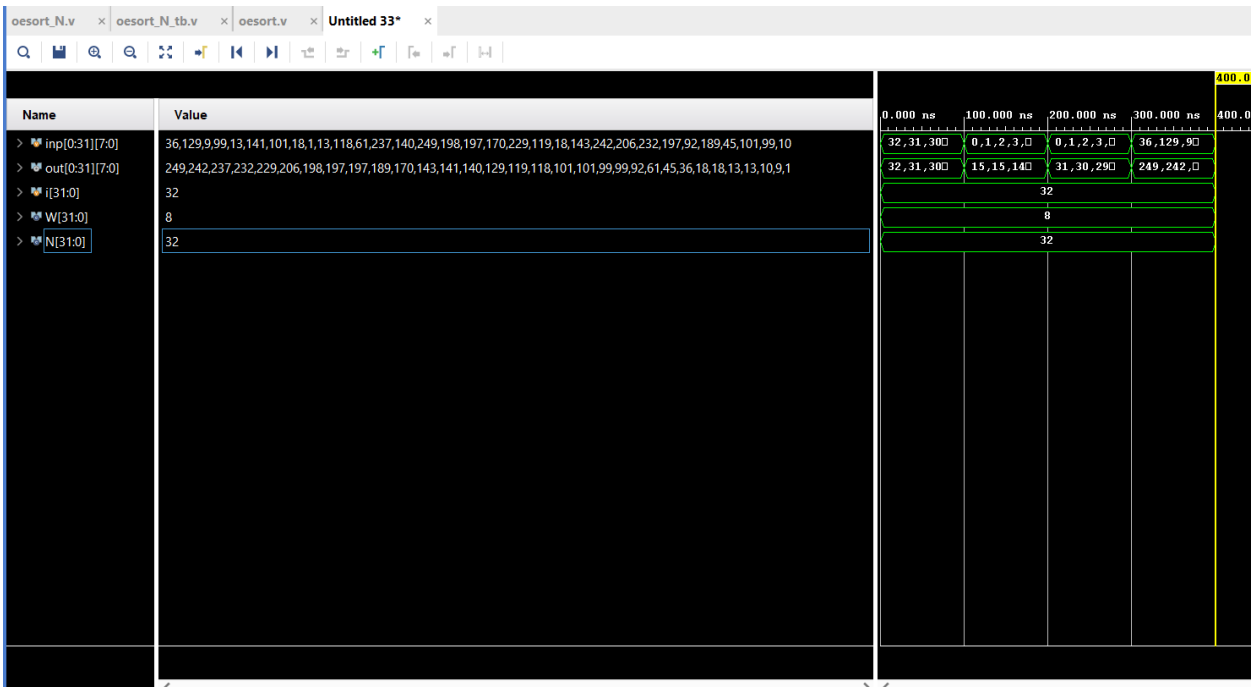
Dynamic:	0.000 W	(0%)
Device Static:	0.090 W	(100%)

Schematic

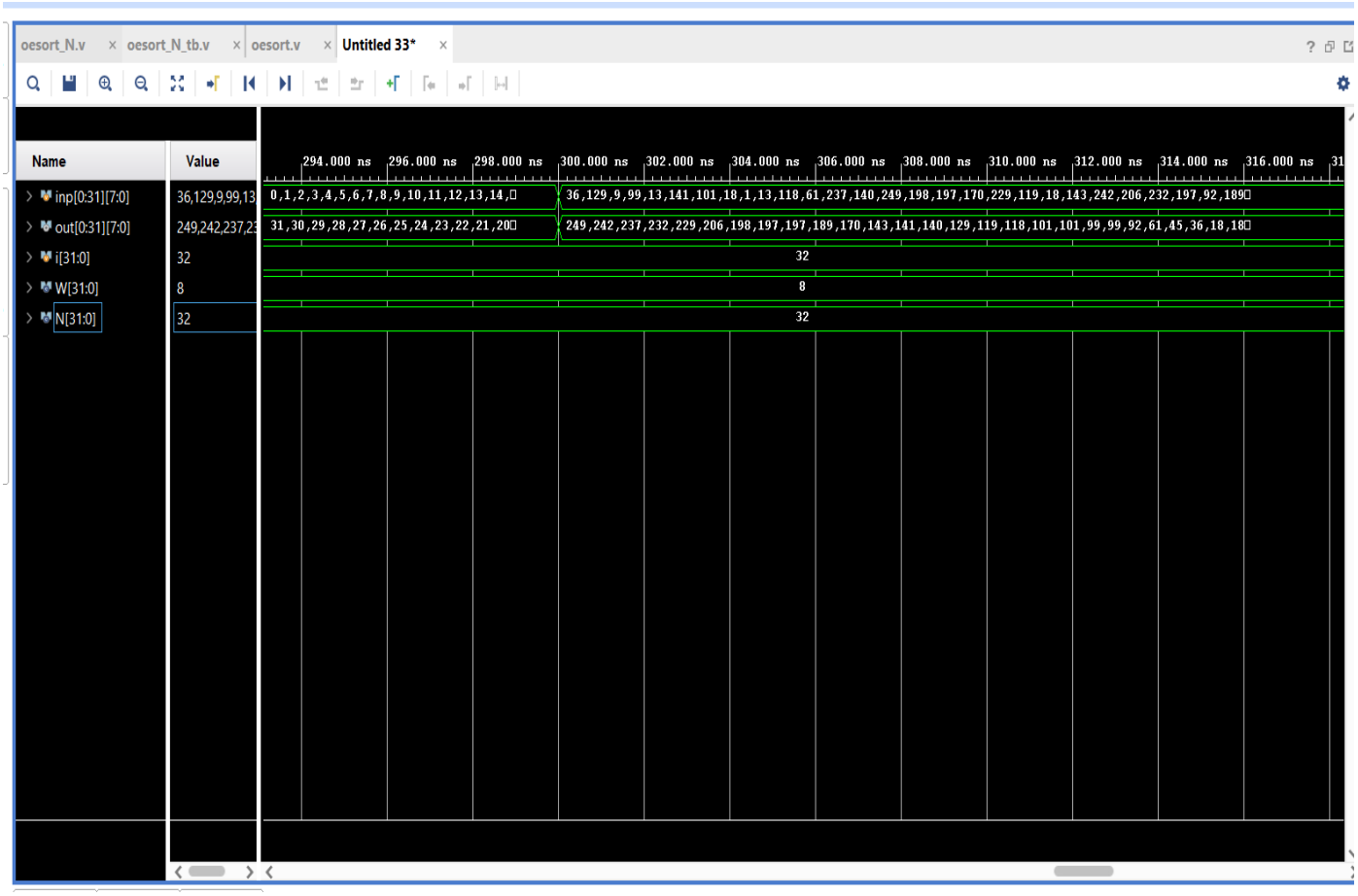


2. N = 32

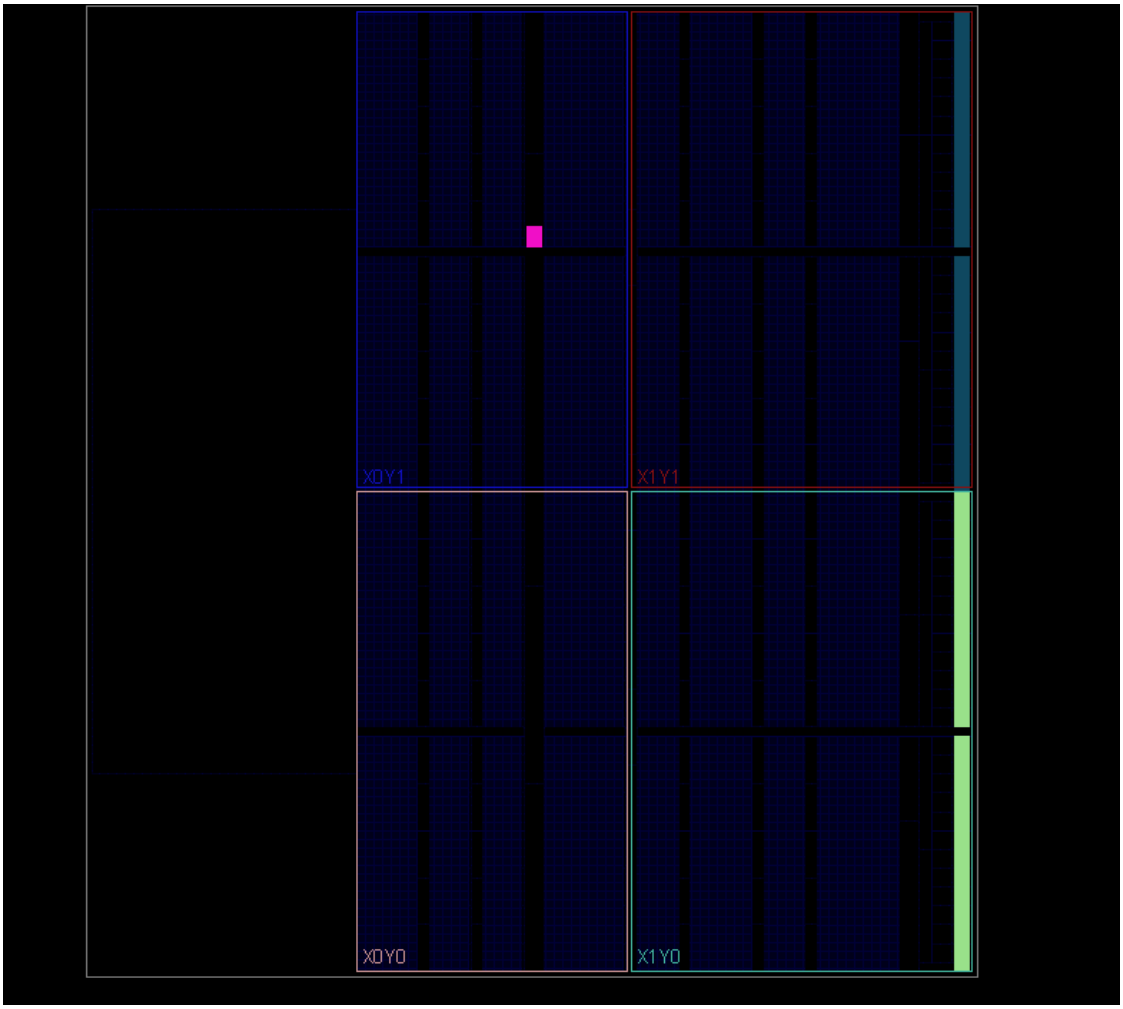
Waveform 1



Waveform 2



Schematic

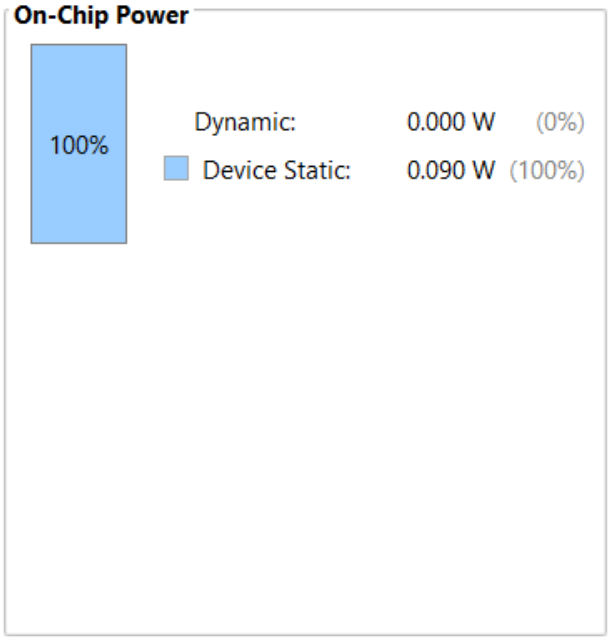

X0Y1
X1Y1
X0Y0
X1Y0

Power

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

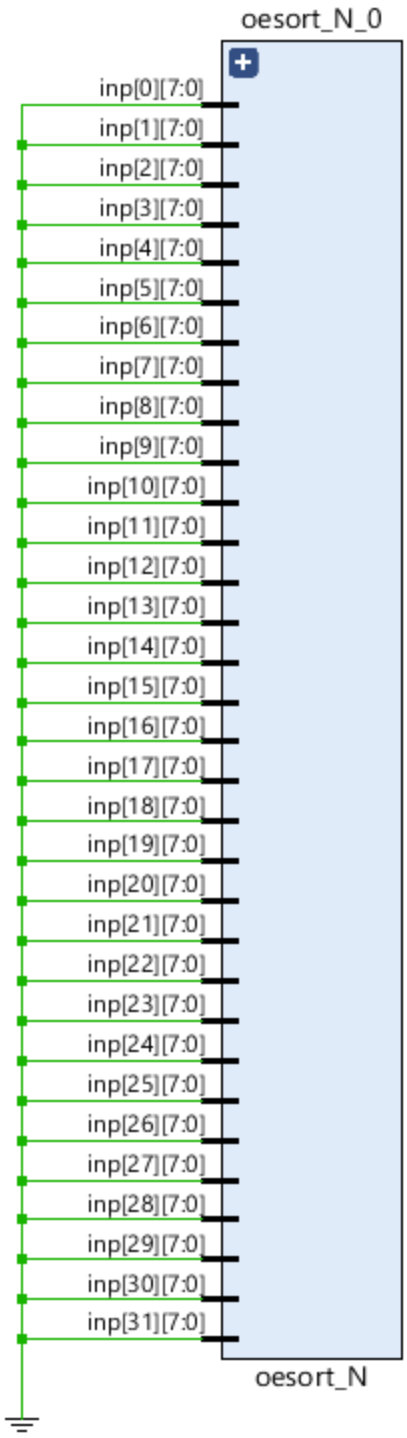
Total On-Chip Power:	**0.09 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.0°C**
Thermal Margin:	74.0°C (6.2 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	High

Launch Power Constraint Advisor to find and fix invalid switching activity



N = 64

Schematic

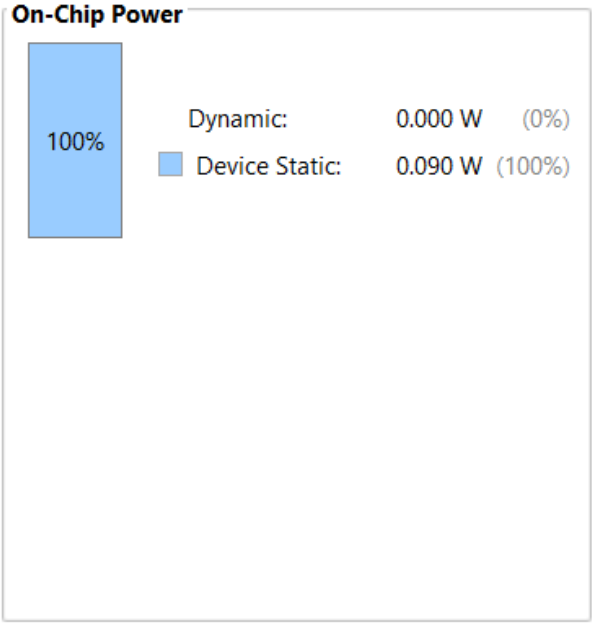

oesort_N_0
inp[0][7:0]
inp[1][7:0]
inp[2][7:0]
inp[3][7:0]
inp[4][7:0]
inp[5][7:0]
inp[6][7:0]
inp[7][7:0]
inp[8][7:0]
inp[9][7:0]
inp[10][7:0]
inp[11][7:0]
inp[12][7:0]
inp[13][7:0]
inp[14][7:0]
inp[15][7:0]
inp[16][7:0]
inp[17][7:0]
inp[18][7:0]
inp[19][7:0]
inp[20][7:0]
inp[21][7:0]
inp[22][7:0]
inp[23][7:0]
inp[24][7:0]
inp[25][7:0]
inp[26][7:0]
inp[27][7:0]
inp[28][7:0]
inp[29][7:0]
inp[30][7:0]
inp[31][7:0]
oesort_N

Power

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

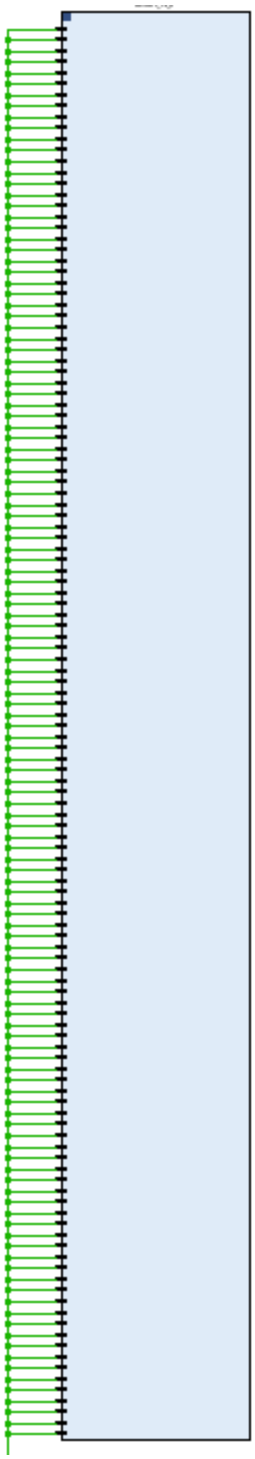
Total On-Chip Power:	**0.09 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.0°C**
Thermal Margin:	74.0°C (6.2 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	High

Launch Power Constraint Advisor to find and fix invalid switching activity



N = 128

Schematic



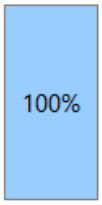
Power

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.09 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.0°C**
Thermal Margin:	74.0°C (6.2 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	High

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power



Dynamic:	0.000 W	(0%)
Device Static:	0.090 W	(100%)