Anuj Vaishnav

Addr.: 04.04.02, George Kenyon Hall, Manchester, M13 9PY;
Email: anuj.vaishnav@manchester.ac.uk; Mobile: +44 7436930733;
LinkedIn: uk.linkedin.com/in/anujvaishnav; Webpage: https://anujvaishnav.github.io/

Education

2017 – 2020 PhD Computer Science, University of Manchester, UK.

Research Topic: *Resource Elastic Management for FPGAs*.
Supervised by: *Dr. Dirk Koch* and *Dr. James Garside*

Research focus: Transparently scaling up and scaling out hardware accelerators within a node for maximising resource utilisation and performance. It would allow users to deploy their hardware accelerators described in OpenCL/C to the cloud or edge with ease and high-performance.

2014 – 2017 BEng (Hons) Computer System Engineering, University of Manchester, UK.

First-class degree with *85%* and specialisation in *System-on-Chip* and *Computer Architecture*.

- Final year project: Developed a library of high-performance hardware accelerators for security algorithms on vectorised FPGA interlays..
- Final year modules: Chip Multiprocessors, Implementing System-on-Chip Designs, Agile Software Engineering, Compilers, Cryptography and Network Security, and Documents on the Web.

Awards*:*

- ***President's Doctoral Scholar Award, University of Manchester – 2017-21***
  Given to the *top 3%* of research students across the university who demonstrate academic excellence and leadership potential.
- ***Runner Up for Outstanding Doctoral Paper in Computer Science, University of Manchester – 2017-18***
  Given to the *second-place winner* across the school for best research paper of the year, based on the external reviews, venue and acceptance rate. For "Live Migration for OpenCL FPGA Accelerators".
- ***Edwards Prize, University of Manchester – 2016-17***
  For the *highest distinction* in examinations, laboratories and projects relating to Computer Engineering courses *throughout the degree*.
- ***IBM Team Challenge Award, University of Manchester – 2015-16***
  For the consistent sterling performance of the *team* on all Software Engineering coursework.
- ***Kate Kneebone Acorn Bursary, University of Manchester – 2015-16***
  For a student with academic merit who has shown commitment, determination, enthusiasm, personal application and promise.
- ***Golden Anniversary Prizes, University of Manchester – 2014-15***
  For Excellence in first-year studies. Given to the *top 5* students of the year.

Research Experience

2019 Jun-Sept Multi-tenant FPGA Platform Designer, APT Group, University of Manchester, UK.

- Designed runtime system, library APIs and hardware accelerators in High-Level Synthesis.
- Responsible for project management, open-source release and a live demo at FPL 2019 conference.
- Supervised and mentored 2 summer interns during the platform development.

2015 July-Aug **Summer Research Assistant**, APT Group, University of Manchester, UK.

- Designed computer architecture based on Dataflow and Transport Triggered Arch.
- Built functional simulator of the resulting computer architecture in JAVA for experimentation.
- Wrote technical reports based on analysis of the design and existing research.

Experience

2018 Sept-Nov **Consulting Embedded Platform Engineer,** HTV GmbH / University of Manchester

- Delivered embedded platform with remote access for FPGA accelerators.
- Developed userspace drivers for cryptography accelerators (AES and Keccak/SHA3).
- Wrote tutorials and documentation for the platform handover.

2016 July-Sept **Hardware Intern – Design & Verification,** ARM

- Improved existing systems for better functional coverage checking.
- Integrated new AMBA features in verification test-benches.
- Created new regression work-flow for lint tool and its continuous integration.
- Reported and resolved bugs in work-flow and verification test-benches.

Selected Publications

- **A. Vaishnav**, et al., "*The FOS (FPGA Operating System) Demo*", 29th FPL, Barcelona, 2019.
- **A. Vaishnav,** K.D. Pham and D. Koch, "*Heterogeneous Resource-Elastic Scheduling for CPU+FPGA Architectures*", 10th HEART, 2019.
- **A. Vaishnav**, et. al, "*Live Migration for OpenCL FPGA Accelerators*", FPT, 2018. **(*Best Paper Nominee)**
- **A. Vaishnav**, K.D. Pham and D. Koch, "*A Survey on FPGA Virtualization*", 28th FPL Dublin, 2018.
- **A. Vaishnav**, et al., "*Resource Elastic Virtualization for FPGAs using OpenCL*", 28th FPL, Dublin, 2018.
- **A. Vaishnav,** J. R. G. Ordaz and D. Koch, "*A Security Library for FPGA Interlays*", 27th FPL, Ghent, 2017.

Full list available on Google Scholar: https://scholar.google.co.uk/citations?user=GIMybIcAAAAJ

Positions of responsibility

2017 – Present **Graduate Teaching Assistant,** University of Manchester
2018 Jan - Jun **Member of Organising Committee** for Postgraduate Summer Research Showcase (PSRS)
2015 – 2017 **Secretary for Manchester Ultimate Programming Society,** University of Manchester
2014 – 2016 **Board Member of School of Computer Science Committee,** University of Manchester
2014 – 2015 **Student Representative for School of Computer Science,** University of Manchester

Skills

Hardware: Verilog • Vivado • Vivado HLS • SDAccel/SDSoC • ISA simulation • Functional coverage • Verification test-bench • AMBA protocols
Embedded systems: C • ARM assembly • PetaLinux • Xilinx SDK • Userspace drivers
Object-oriented lang.: Java • Python • Ruby • Matlab
Website development: HTML + CSS • SQL • XSL
OS & other software: OpenCL • Bash • Tcsh • JUnit Testing • GNU/Linux • Windows • Gitlab • SVN