# EE671: VLSI Design Assignment 1 CMOS Inverter Design using Sky130 PDK

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### Introduction

In this assignment, a CMOS inverter is designed and simulated using the SkyWater 130nm (Sky130A) PDK in NGSpice. The design objective is to obtain a minimum-size inverter with equal rise and fall times, and then extract its static and dynamic characteristics. The inverter is loaded with another identical inverter to capture realistic behavior.

## Q1: Minimum Size CMOS Inverter (INVX1)

### Design Parameters

The minimum channel length  $(L_{min})$  is fixed at  $0.15 \,\mu\text{m}$ . NMOS width is restricted to  $0.42 \,\mu\text{m}$ , while PMOS width is chosen to balance rise and fall times.

Inverter Design Parameter	Value
PMOS Width (μm)	1.26
PMOS Length $(\mu m)$	0.15
NMOS Width $(\mu m)$	0.42
NMOS Length $(\mu m)$	0.15

### **Dynamic Characteristics**

The input was a rail-to-rail pulse with rise/fall time of 20 ps. The inverter was loaded with another INVX1. The measured rise time, fall time, and propagation delay are:

• Rise time  $(t_r)$ : Defined as the time taken for the output voltage to rise from 20% to 80% of  $V_{DD}$ .

$$t_r = t_{80\% \ V_{DD}} - t_{20\% \ V_{DD}}$$

• Fall time  $(t_f)$ : Defined as the time taken for the output voltage to fall from 80% to 20% of  $V_{DD}$ .

$$t_f = t_{80\% \ V_{DD}} - t_{20\% \ V_{DD}}$$

• Propagation delay  $(t_p)$ : Calculated as the average of low-to-high and high-to-low propagation delays:

$$t_p = \frac{t_{PHL} + t_{PLH}}{2}$$

where

$$t_{PHL} = t_{50\% \ V_{in, \ rising}} - t_{50\% \ V_{out, \ falling}}, \quad t_{PLH} = t_{50\% \ V_{in, \ falling}} - t_{50\% \ V_{out, \ rising}}$$

$$t_{PHL} = 22.8 \text{ ps}, \quad t_{PLH} = 17.4 \text{ ps}$$

Final  $t_p = 20.1 \text{ ps}$ 

Value
18.5
18.5 20.1

```
Q1a.cir
                                                    × Q1b.cir
                                                                                                              Q2a.cir
*Vout and Vin with time for INVX1 is loaded with INVX1
.lib ~/.local/share/pdk/sky130A/libs.tech/ngspice/sky130.lib.spice tt
.param Lmin = 0.15
.param wp = 1.26
.param wn = 0.42
.param ap = 2*wp*Lmin
.param pp = 2*(wp + 2*Lmin)
.param an = 2*wn*Lmin
.param pn = 2*(wn+ 2*Lmin)
* The voltage sources:
Vdd vdd gnd DC 1.8
Vi in gnd pulse(0 1.8 0p 20p 10p 1n 2n)
Xnot1 in vdd gnd p not1
Xnot2 p vdd gnd out not1
.subckt not1 a vdd vss z
.subck note: a vdd vdd sky13<u>0</u> fd_pr__pfet_01v8 l=0.15 w={wp} as={ap} ad={ap} ps={pp} pd={pp} xm02 z a vss vss sky13<u>0</u> fd_pr__nfet_01v8 l=0.15 w={wn} as={an} ad={an} ps={pn} pd={pn}
.ends
* Simulation command:
tran 1ps 10ns
.measure tran tr TRIG v(p) VAL=0.36 RISE=2 TARG v(p) VAL=1.44 RISE=2
.measure tran tf TRIG v(p) VAL=1.44 FALL=2 TARG v(p) VAL=0.36 FALL=2
.measure tran tph1 TRIG v(in) VAL=0.9 RISE=2 TARG v(p) VAL=0.9 FALL=2
.measure tran tph1 TRIG v(in) VAL=0.9 FALL=2 TARG v(p) VAL=0.9 RISE=2
wrdata /mnt/c/Users/anujy/IITB_COURSES/7th_SEMESTER_AUGUST_2025/EE671/Assignment_1/Q1a|.txt in p
plot in p
```

Figure 1: Code snippet for Dynamic Characteristics INVX1

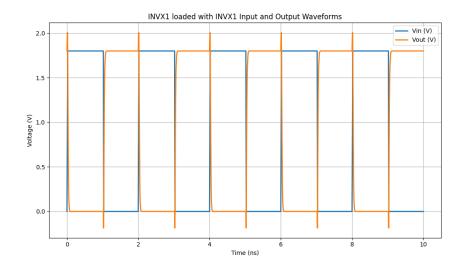


Figure 2: Inversion of the input signal by INVX1.

Figure 3: Dynamic Transfer Characteristic of INVX1.

#### **Static Characteristics**

Using a DC sweep on the input, the Voltage Transfer Characteristic (VTC) was obtained and parameters were extracted:

• Switching Threshold  $(V_M)$ : The input voltage at which  $V_{in} = V_{out}$ .

$$V_M = V_{in}$$

Measured value: 0.89 V

• Noise Margins: The noise margins are calculated using:

$$N_{ML} = V_{IL} - V_{OL}, \quad N_{MH} = V_{OH} - V_{IH}$$

where  $V_{OL} \approx 0$  and  $V_{OH} \approx V_{DD}$ .

–  $V_{IL}$ : Maximum input voltage recognized as logic '0', obtained from the VTC where  $\frac{dV_{out}}{dV_{in}} = -1$  (lower transition point). Measured  $V_{IL} = 0.77$  V

–  $V_{IH}$ : Minimum input voltage recognized as logic '1', obtained from the VTC where  $\frac{dV_{out}}{dV_{in}}=-1$  (upper transition point). Measured  $V_{IH}=1.01~{\rm V}$ 

Static Characteristic	Value
$V_{IH}$ (V)	1.01
$V_{IL}$ (V)	0.77
$N_{MH}$ (V)	0.79
$N_{ML}$ (V)	0.77
Switching Voltage $V_M$ (V)	0.89

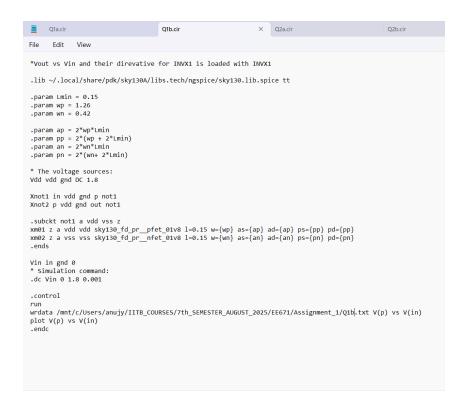


Figure 4: Code snippet for Static Characteristics INVX1

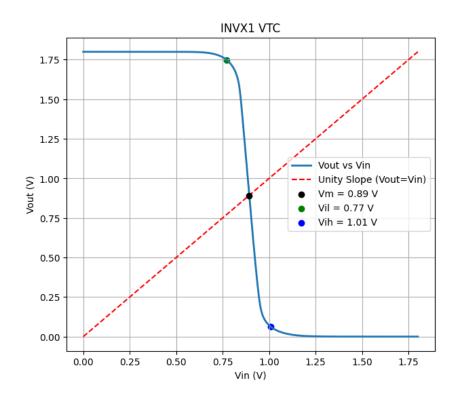


Figure 5: Static Transfer Characteristic of INVX1 with unity slope line and extracted parameters.

# Q2: Strength-2 Inverter (INVX2)

The transistor widths were doubled to obtain INVX2. The inverter was loaded with INVX1 and the same set of measurements were repeated.

#### Design Parameters

Inverter Design Parameter	Value
PMOS Width (μm)	2.58
PMOS Length $(\mu m)$	0.15
NMOS Width $(\mu m)$	0.84
NMOS Length $(\mu m)$	0.15

### **Dynamic Characteristics**

These are the dynamic characteristics calculated with the target of making the rise time equal to the fall time

Dynamic Characteristic	Value
Rise time, $t_r$ (ps)	17.3
Fall time, $t_f$ (ps)	17.3
Propagation delay, $t_p$ (ps)	15.3

Figure 6: Code snippet for Dynamic Characteristics INVX2

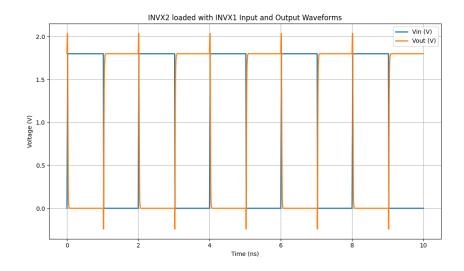


Figure 7: Inversion of the input signal by INVX2

Figure 8: Dynamic Transfer Characteristic of INVX2

#### Static Characteristics

Using a DC sweep on the input, the Voltage Transfer Characteristics was obtained and parameters extracted:

Static Characteristic	Value
	1.00
$V_{IH}$ (V)	1.02
$V_{IL}$ (V)	0.77
$N_{MH}$ (V)	0.78
$N_{ML}$ (V)	0.77
Switching Voltage $V_M$ (V)	0.90

```
File Edit View

.param ap1 = 2*wp1*Lmin1
.param pp1 = 2*(wp1 + 2*Lmin1)
.param pp1 = 2*(wp1 + 2*Lmin1)
.param pp1 = 2*(wp2 + 2*Lmin1)
.param ap1 = 2*wp1*Lmin2
.param ap2 = 2*wp2*Lmin2
.param pp2 = 2*(wp2 + 2*Lmin2)

* The voltage sources:
Vdd vdd gnd Dc 1.8

Xnot1 in vdd gnd p not2
Xnot2 p vdd gnd out not1

.subckt not1 a vdd vss z
xm01 z a vdd vdd sky130_fd_pr__pfet_01v8 l={Lmin1} w=(wp1) as={ap1} ad={ap1} ps={pp1} pd={pp1}
xm02 z a vss vss sky130_fd_pr__nfet_01v8 l={Lmin1} w=(wn1) as={an1} ad={an1} ps={pn1} pd={pn1}
.ends

.subckt not2 a vdd vss z
xm03 z a vdd vdd sky130_fd_pr__pfet_01v8 l={Lmin2} w=(wp2) as={ap2} ad={ap2} ps={pp2} pd={pp2}
xm03 z a vdd vdd sky130_fd_pr__nfet_01v8 l={Lmin2} w=(wp2) as={ap2} ad={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={Lmin2} w=(wp2) as={ap2} ad={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={Lmin2} w=(wp2) as={ap2} ad={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={Lmin2} w=(wp2) as={ap2} ad={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={Lmin2} w=(wp2) as={ap2} ad={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={Lmin2} w=(wp2) as={ap2} ad={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={Lmin2} w=(wp2) as={ap2} ad={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={Lmin2} w=(wp2) as={ap2} ad={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={Lmin2} w={wp2} as={ap2} ad={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={Lmin2} w={wp2} as={ap2} ad={ap2} ad={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={Lmin2} w={wp2} as={ap2} ad={ap2} ad={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={Lmin2} w={wp2} as={ap2} ad={ap2} ad={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={ap2} ps={pp2} pd={pp2}
xm04 z a vss vss sky130_fd_pr__nfet_01v8 l={ap2} ps={pp2} pd={pp2}
x
```

Figure 9: Code snippet for Static Characteristics INVX2

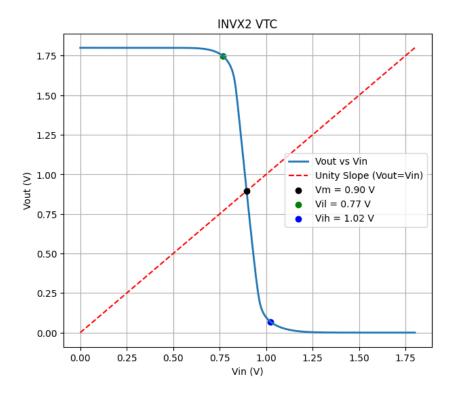


Figure 10: Static Transfer Characteristic of INVX2 with unity slope line and extracted parameters.

# Results and Comparison

Parameter	INVX1	INVX2
$t_r \text{ (ps)}$	18.5	17.3
$t_f$ (ps)	18.5	17.3
$t_p$ (ps)	20.1	15.3
$V_M$ (V)	0.89	0.90
$N_{MH}$ (V)	0.79	0.78
$N_{ML}$ (V)	0.77	0.77

### Observation

INVX2 shows improved drive strength compared to INVX1, leading to reduced rise/fall times and propagation delay. The switching voltage  $V_M$  remains approximately unchanged, but dynamic performance improves.